VIRUTUAL INSTRUMENTATION BASED HARMONIC ANALYSIS AND PERFORMANCE MONITORING OF THREE- PHASE INDUCTION MOTOR DRIVE

By

LAKSHMI PRABA. A

Reg. No. 71203415007

KUMARAGURU COLLEGE OF TECHNOLOGY
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A PROJECT REPORT

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In partial fulfillment of the requirements
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CHENNAI 600 025

AUTOMATIC CALIBRATION BENCH FOR BIMETALLIC RELAYS

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Submitted by

J.JEYAMANI (71203415006)

in partial fulfillment for the award of the degree

of

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Under the guidance of

Mrs. SHARMILA DEVE Lecturer

KUMARAGURU COLLEGE OF TECHNOLOGY,COIMBATORE

ANNA UNIVERSITY:CHENNAI-600 025

JUNE 2005

Bonafide Certificate

Certified that this project entitled "**AUTOMATIC CALIBRATION BENCH FOR BIMETALLIC RELAYS**" is the bonafide work on **J.Jeyamani** who carried out the research under my supervision.Certfied further, that to the best of my knowledge the work reported hearing does not form part of any other project report or dissertion on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

6/6/05
Project Guide

6/6 K.T. VARA
Head of the Department Prof

The candidate with University registration number **71203415006** was examined by us in the project viva voce exam held on 23.06.2005

K.Subramanian
Internal Examiner

23/06/0
External Examiner
(DR S.Shbha Rani)

SALZER ELECTRONICS LTD. salzer
Samichettipalayam, Coimbatore - 641 047, India.

May 31, 2005

CERTIFICATE

This is to certify that **Ms.J.JEYAMANI, M.E - (Power Electronics and Drives)** IInd Year student of **KUMARAGURU COLLEGE OF TECHNOLOGY, COIMBATORE,** has sucessfully completed her Project work entitled **" AUTOMATIC CALIBRATION BENCH FOR BIMETALLIC RELAYS ",** as a part of her course, in our Company from **JULY 2004 to MAY 2005.**

She has evinced keen interest in absorbing the nature, concept and functions of our Organisation and her conduct and character were **good** during the period.

For SALZER ELECTRONICS LIMITED,

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**DIRECTOR (CORPORATE AFFAIRS) &
COMPANY SECRETARY.**

NQA ISO 9001 REGISTERED COMPANY
ANSI-RAB QMS ACCREDITED
Phone : 2692531 Fax : + + 91 422 2692170 Grams : SALZER
E-mail : salzersales@satyam.net.in
E-mail : salzer@vsnl.com

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ABSTRACT

Quality control is very important in every organization, especially for a manufacturing firm. The quality of a product decides its values life and ensures its competitiveness in the market. The bimetallic relays manufactured by M/S Salzer Electronics Ltd are meant for protecting the machineries from abnormal currents and hence it is very much important that they function properly. Manual testing currently used is a time consuming inaccurate process.

In this project an automatic calibration bench is devised that determines the operating time for the bimetallic relays for various current levels. We have automated the process by using a PIC micro controller 16F877 and thereby we have increased the speed of the testing, simultaneously improving the accuracy of the measurements. This facilitates a drastic improvement in the productivity of the testing and calibration section of the starters and increase the overall productivity.

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CHAPTER 1

1.INTRODUCTION

The project Automatic calibration Bench for Bimetallic Relays is an advanced process of automation technology used with the introduction of various micro controller aspects of our future industry. The important aspect of the project is automation of the calibration process, which improves rate of production and accuracy of testing. Since the error rate is minimal this can be widely used in developing industries that wish to nourish it with high levels of international standards.

The bimetallic relays manufactured by M/S Salzer Electronics Ltd is a single phase switch that is capable of isolating the equipment it controls whenever fault occurs in it. This tripping is done with the help of a bimetallic strip in the relays and hence the name bimetallic relays. Proper thickness and tension in which these strips are held are the important parameters to be considered while manufacturing and assembling them in a relay. It thus becomes essential that they should be tested for their functionality. At Salzer Electronics the time of testing of one strip takes nearly 15 minutes, but this is not a fair value as this leads to reduction in relay manufacturing and assembly. Thus the quantity of starters going out of the company becomes less in number. The use of micro controller caters the need of the company by increasing the number of relays being tested to four instead of one. A brief overview of the testing and the bimetal characteristics has been given below.

1.1. Bimetallic Strip:

A bimetallic strip is nothing but two different metals joint together by spot welding. When the temperature of the bimetallic strip increases the metals expand. But due to the difference in the elongation of the two metals the strip tends to bend. This Bending is used to open the switch in a bimetallic relay.

Bimetallic relays have an inverse time relay operation, that is the time taken to open the relay varies inversely as the current flowing through the relay as shown in Fig.1.1.

0 The bending of the bimetallic strip is controlled by the tension in the strip. Greater the tension greater the resistance to bend lesser the bend for a given value of current and hence slower will be the responsive time. Hence by adjusting the tension we can fix the responsive time to our need.

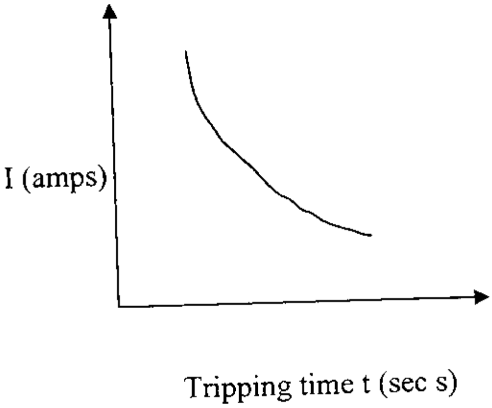


Fig.1.1.Inverse time relay operation

1.2. Description of thermostatic bimetal and its function:

It is well known that different metals expand to different extents when heated. When the temperature is reduced this expansion is reversed.

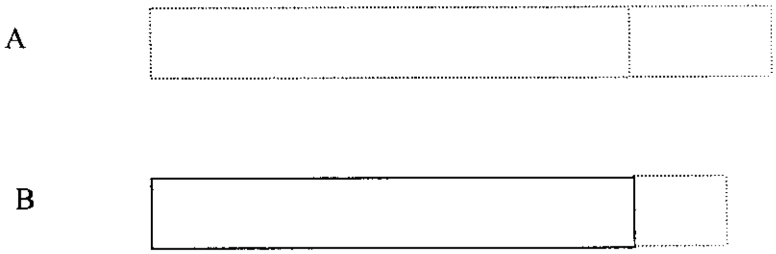


Fig 1.2.Strips of different metals before and after heating

Fig 1.2 shows two strips of different metals before and after heating. The area enclosed by the dotted lines indicates the elongation after heating. Strip A should elongate more than strip B.

When the two metal strips bonded together the strip A is partly prevented from expanding by the strip B when heated. A considerable force is thereby developed which causes the welded strips to bend. In absence of external forces the bimetal will take the shape of an arc. The deformation of the assembly is greater than the elongation of the individual strips. The bimetal will also bend in the direction of the width. This cross curvature and explains why the bimetal deflection also depends upon the bimetal width.

A bimetal is also called thermostatic bimetal since its function results from the effect of heat. Instead of the metal strips mentioned above the different alloys can be chosen. Two alloys with greatly differing coefficients of thermal expansion are normally selected. Of the two metal layers, which are permanently joined together, the side that develops the largest thermal expansion is known as the active component. It generally consists of an alloy containing nickel, iron manganese or chrome in different amounts. The side with the lower degree of expansion is known as the passive component for which Invar is often chosen which is an iron-nickel alloy containing 36% nickel. The relation of the thickness of the layers of the two components can vary for different grades. Within one bimetal type however the relationship is always the same.

Some bimetal types have a layer of nickel or copper between the two layers mentioned in order to reduce the electrical resistivity and to increase the thermal conductivity.

1.3 The manufacture of thermostatic bimetals:

The components of thermostatic bimetal are melted in high frequency furnaces. Samples are taken from each melt for checking the analysis and determining the resistivity and expansion properties. On the basis of these laboratory tests the components are selected so that the finished bimetal products have uniform properties according to the quality specification.

The two components are bonded together by means of cold bonding. Special measures are taken to ensure that the joint is completely free from defects. The quality of the bonded joints is checked by microscopic and mechanical tests.

The bonded material is rolled in different cold rolling mills where the thickness is maintained within close tolerances. Between the various rolling processes the bimetal strips are heat treated in annealing furnaces in a controlled atmosphere. The sequence of annealing and rolling affects the properties of the bimetal.

During the final manufacturing process the cold rolled strips are provided with the respective quality designation marks and the edges are slit and debarred. Marking is normally done on the active component which is situated on the convex side of the heated thermostatic bimetal strip.

1.4.Measuring the deflection:

Bimetals are usually measured in the DIN measuring device. The test strips are heated in a silicon oil bath the temperature of the oil being kept uniform by thermostatic control. Measurement is normally done in the temperature range prescribed by DIN 1715. Before measurement the test strips are stress relieved by means of a stabilizing heat treatment process. If a bimetal is thinner than 0.25mm the angular rotation of a standard spiral coil is measured.

1.5.Tensile strength, yield point and hardness:

As standard thermostatic bimetals have a tensile strength of 600 to 800Nmm2 and yield point lies between 400 and 500 Nmm2.Tensile strength yield point and hardness depend on the degree of cold rolling reduction.

Thermostatic bimetals can be supplied with a higher degree of hardness, which means considerably improved elasticity properties. It must be recognized however that if the hardness is increased a decreased maximum operating temperature should be taken into account. As a standard the cold rolling reduction is 20%.

The thermostatic bimetals can also be supplied in a softer state in cases where the requirements for ductility are particularly high. However due to the softer state the bending load capacity is reduced. The cold rolling reduction must be at least 7%.

1.6.Modulus of elasticity:

The values indicated for the modulus of elasticity have been measured at room temperature in accordance with DIN 50151. It is difficult to judge to what extent this property changes with temperature. The stiffness at increased temperature is influenced not only by the modulus of elasticity but also by deformations of the thermostatic bimetal part, which can appear for instance as cross curvature.

In order not to complicate the calculation of bimetal elements we refrain from considering the modulus of elasticity as a temperature dependant material constant. When making calculations the value of modulus of elasticity at room temperature can also be used for temperatures within the normal range of application. The error resulting from this simplification is usually insignificant.

1.7.Choice of suitable bimetal type:

When choosing a bimetal type for a particular application the following factors should be considered:

1.Temperature of operation and deflection
2.Mechanical stress
3.Electrical resistivity and thermal conductivity
4.Corrosion resistance
5. Machine ability
6.Price

1.7.1.Temperature of operation and deflection:

The bimetal volume required for a desired performance decrease with increasing specific deflection. It should be recognized that the specific deflection of a bimetal type the smaller is its linearity range and the lower its highest permissible temperature.

Thermally active bimetal types are principally used in cases where large deflection is required by a moderate temperature change of a small active length. These bimetal types do not withstand high mechanical strain and should not be heated to a temperature much higher than 250 degree Celsius.

1.7.2.Mechanical stress:

The bimetal is often in a state of mechanical stress by the action of an external force. When thermostatic bimetal elements are overstressed a permanent deformation occurs. Different types of bimetals differ with regard to maximum permissible bending stress and its dependence on temperature. The same applies to modulus of elasticity. The maximum permissible bending stress as a function of the temperature is indicated.

In many thermostats operating as temperature limiters the thermostatic bimetal strip is under restraint by an adjusting screw in such a way that the contacts do not open until a temperature has been reached and thus a force developed which corresponds to the restraint. If this type of thermostat is exposed to very low temperatures a permanent deformation of the bimetal may occur. Thermostats for higher temperatures should be designed so that the thermostatic bimetal element is without stress at ambient temperature. The influence of hardness on the maximum permissible increases of temperature in cases where the thermostatic bimetal is completely restrained from motion.

1.7.3.Electrical resistivity and thermal conductivity:

A thermostatic bimetal with high electrical resistivity always has a low thermal conductivity. Conversely if the electrical resistivity is low the thermal conductivity is always good. When the bimetal is heated mainly by conduction in its length direction a high thermal conductivity causes a rapid reaction. Bimetal parts, which are heated indirectly by a heating coil, should preferably have a low thermal conductivity as otherwise great losses occur due to conduction. This would result in unnecessary heating of the fixing point and require a high power of the heating coil.

The bimetal part is often included in the electric circuit, if in such a case any heating due to the electric current is undesirable the type of bimetal used should have a low electrical resistivity .It is often necessary to obtain the heating of the bimetal by the passage of an electric current. The current is normally fixed and thus the internal resistance of the bimetal can be calculated in relation to this amperage. The higher the passing current the smaller should be the electrical resistivity of the bimetal.

1.7.4.Corrosion resistance and protection:

The corrosion resistance of most of thermostatic bimetals is incomparably better than that of iron. The bimetals can often operate without particular protection. The condition of the surface of the bimetal is of great importance where the bimetal is subject to corrosion attacks. In such case the identification marking is often applied by means of a printing ink instead of etching. Electrolytic polishing of fabricated bimetal parts presents an advantageous improvement of the corrosion resistance.

For operation in humid atmospheres galvanizing or cadmium plating is suitable. In water copper plating is preferable. The thermal deflection is normally not affected by the surface treatment and only in the case of thicker layers can a diminution occurs. Chromium plating and nickel-plating result in a hard surface and are to be preferred in the case of high operating temperatures. It should be noted however that the true protection provided by nickel plating is often doubtful as the nickel coating is porous and can easily be damaged.

1.7.5.Machineability:

Viewpoints regarding processing can also be of importance for the choice of bimetal type welding being an example. Differences between the various bimetal types as regards punching bending and threading can generally be overcome by changing the degree of cold rolling since this affects the hardness.

1.8.Applications:

The function of a thermostatic bimetal strip is caused by an alteration in temperature. Therefore the bimetal is used in most cases for transformation of a temperature change into movement and/or force. Electric energy can also be used for release of function in cases where the thermostatic bimetal is electrically heated. Conversely a movement and force can be converted into an electrical effect for instance in a liquid level gauge.

This means that there is wide range of use for thermostatic bimetal within the fields of measuring regulating and safety techniques. Since bimetal is a simple and reliable element technical development continuously opens new possibilities for utilizing its function. Some important applications for thermostatic bimetal are as follows:

1.9.Temperature indication:

Temperature indication as in thermometers for air, steam or liquids and indication of other characteristics. For example indication of electrical current voltage or power indication of gas or pressure level of fluid or velocity of flow and quantity of circulating gas.

1.10.Control:

Control as in thermostats in heating, cooling, cooking, baking applications for control of room temperature in living rooms and industrial plants for step less control of electrical power for the control of cooling water circulation or ventilation as guide plates and valve control of circulating air gases and exhaust gases and for temperature control in water mixing valves steam traps and liquid outlets for use in current and voltage regulators in brightness regulators for twilight switches etc. Time limiting and control as in toasters cigar lighters fluorescent lamp and staircase lighting switches.

1.11.Safety function:

Safety function as overload protection of electric motors transformers and wiring over heating protection in the windings of electric machines and transformers in gas safety pilot elements as thermal cutouts against non-permittable heating in devices and in fire alarms.Temperature compensation in measuring devices and control units as for compensation of fluctuating room temperature.

1.12.Different methods of heating bimetal:

1.Heat transmission by conduction where the bimetal is in direct contact with the source of heat or the medium to be controlled.

2.Heat transmission by radiation or convection.

3.Heat developed by passage of electric current where the bimetal itself serves as resistance and thus as the source of heat.

4.Indirect electric heating by means of a heating element made of ribbon or strip.

The function of bimetal can be utilized to produce a force a movement or a combination of both. By using stacks of bimetal strips a relatively great force is obtained by a large movement. Parts of heating elements or shunts can be inserted between the bimetal layers. The main disadvantages are the friction between adjacent layers and risk of corrosion.

1.13.Fabricating thermostatic bimetal parts:

1.13.1:Stamping and cutting:

A thermostatic bimetal is made up of two different alloys which also differ with regard to hardness. In order to obtain an appropriate function of the fabricated bimetal part care should be taken to ensure that there is no burr left out from stamping and cutting operations. This means that stamping and cutting tools must be very accurate and the play should be the smallest possible. The bimetal strip must be fed in so that the cutting tool is first applied to the harder component. When calculating the cutting pressure a shearing strength of 600 N-mm2 can be assumed.

It is an advantage to cut the bimetal element longitudinally from the strip. However for economical reason bimetal strips are often stamped across the direction of rolling. In such a case a decrease in deflection of 1 to 2%must be considered.

1.13.2.Bending:

Sharp bends should be avoided as far as possible since this may cause cracks to develop in the outer layer. No general rules can be given as to how bending should be carried out since several factors play a part. In this connection the degree of cold rolling or hardness is of important significance. The harder a bimetal strip is the better are the elastic properties. At the same time it is also considerably more brittle. Bending across the direction of rolling offers less difficulty than bending along the direction of rolling. The stress of bimetal strips differs according to the shape of the bending.

A bimetal strip with normal degree of cold rolling should not be bent across the direction of rolling with a radius less than the strip thickness. If the bending is done along the rolling direction the bending radius should not be less than 1.5 to 2 times the strip thickness.

1.13.3.Coiling:

When manufacturing spiral and helical coils for thermometers and other applications the normal resilience properties of bimetal type chosen should be considered. Spiral coils of strips with small cross sectional are can be coiled without the use of inserts provided that the strip has the correct degree of hardness (cold rolling).When using strips of heavier sizes it is recommended to employ an insert during cooling in order to obtain uniform pitch. Coils with the small distance between the turns should preferably be wound with the active component on the inside. In such a case coil operates on the opening and there is no risk of contact between the adjacent turns. Such a contact would restrain the angular deflection and should be avoided. If coils operate on closing have a sufficient pitch this problem does not occur.

1.13.4.Stress-relieving(Ageing):

During the manufacture of bimetal parts certain stresses occur which affect their function. For this reason an stress relieving operation is recommended. This is especially important when the shape of a bent bimetal part is complicated. A proper heat treatment process(ageing)will not change the physical properties, the strength or the hardness of the bimetal element. Such a process will assist in maintaining a uniform function and will not result in any alteration of the initial values. One stress relieving treatment followed by slow cooling is generally sufficient. The temperature should be at least 50 degree Celsius above the maximum temperature of operation.

The duration of the stress relieving treatment should amount to 2 to 3 hours. The lower the temperature of stress relieving, the longer the duration of the treatment should be. Ageing is seldom performed at temperatures below200 degree Celsius as the duration of the treatment would be too long. During the stress relieving treatment a deformation of the bimetal element can occur. This deformation which is especially apparent as far as bent parts are concerned, can usually be taken into account during the manufacture of the bimetal part.

The heat treatment temperature during the second and the third ageing stages should be somewhat lower than during the first one. A protective atmosphere is not necessary for this stress relieving treatment, although it is recommended if the bimetal part is to be welded, brazed or surface-treated after heat treatment. If stress relieving is carried out in normal atmospheric air, a dark surface will be formed which causes a higher emissive, thereby improving the heat exchange with the surroundings.

1.13.5.Mounting:

Uniformly and accuracy in mounting bimetal parts are necessary in order to ensure perfect function and consistency of the zero point position. Spot welding, lasers welding riveting and screwing are normally recommended. Brazing requires such a high temperature that the bimetal softens and new internal stresses occur during cooling.

1.14.Spot welding:

Stamped parts should be carefully degreased so that a good contact is obtained with the welding electrode during spot welding. In mass production of bimetal parts and devices the surface condition is often impaired to a varying extent by different treatment and processes. In order to obtain a good spot welded joint, it may therefore be advisable to apply a thin coating of tin or brass to the bimetal. To ensure a defined current flow and good heat distribution during spot welding a small projection can be stamped into the bimetal element at a point where an increase in temperature is required.

1.15.Importance of relay testing:

The bimetallic relays manufactured through the above mentioned processes will have its own deviation from ideal working condition. This is because of the minute variations in the size of the strip and slight differences in the tension in the strip. These variations are inevitable and will be present in any practical device. Our system helps in adjusting the time setting of the relay after it has been tested to compensate for these variations.

Basically it becomes essentially important to obtain the accuracy of operating time because of the following common conditions wherein which the relays are used.

1.Electrical apparatus may be damaged if they are made to carry the fault currents for a long time.

2.A failure on the system leads to a great reduction in the system voltage. If the faculty section is not disconnected quickly then the low voltage created by the fault may shutdown consumers motors and generators and the system may become unstable.

The high speed relay system decreases the possibility of one type of fault into the other more several type.

1.16.Organization of the report:

The second chapter gives an overall view of the system. It gives the past, current and future scenario in the testing of the bimetallic relays. It also gives the block diagram for the whole setup and a brief description of each block. It also has details of the system design i.e. it shows how the components are mounted and connected.

The third chapter gives a complete description of what was given in the second chapter. It gives the circuit details of each and every part of the system individually and explains their working.

The fourth chapter gives the details about the operating procedure for the calibration bench and the algorithm flowchart and program for which the micro controller was programmed. Since the programming is through embedded C the program code is in C.

The fifth chapter is an overall conclusion. It gives the advantage of the current method over the traditional method the possibilities for further improvement.

CHAPTER2

DESIGN AND FABRICATION

This project is for finding the tripping time for a relay for a given value of current. There are various modules taking part in the operation of the whole process. These processes have been coordinated by the use of a micro controller. Employing a micro controller to do the duty of sensing the tripping of each relay noting the time of each tripping and giving control signals to each bypass relay so as to close the path has enhanced the project.

2.1.Basic Block Diagram

The principal requirement being the operating time of the bimetallic strips under unbalanced conditions the system is divided into several modules according to the need. They are

- ☐ Power supply modules
- ☐ Controllable constant current source that uses IGBT
- ☐ Sensing module comprising of comparators
- ☐ Bypass circuit implemented by 24V,250 relays
- ☐ Control circuit that uses a micro controller

These modules are represented as a block in Fig.2.1.

The three phase AC supply is stepped down and rectified into a DC voltage through a step down transformer and rectifier. The DC supply is given to a controllable constant current source which will provide constant current to the relays under test. It is necessary as we have to maintain the test conditions constant even if the load on circuit changes.

The sensing circuit will sense the tripping of a relay and sends an appropriate signal to the micro controller. The bypass relays are used to maintain the continuity of the circuit and are controlled by the signals it receives from the controller whenever a relay opens. The micro controller controls the overall activity of the system and also displays the tripping time through the LCD display. The input signals of start, bypass, increment, decrement, clear are given through push button switches mounted on the front panel and four sensing circuit inputs gives an indication of the tripping of a relay.

The following could be explained briefly from the given block diagram. The entire assembly is depicted clearly in the representation which has a micro controller specially programmed for the testing. Special study has been made to program the micro controller that will be used for testing process. Since this project deals with high level automation ,high level periphery interface controllers are involved with various control circuits

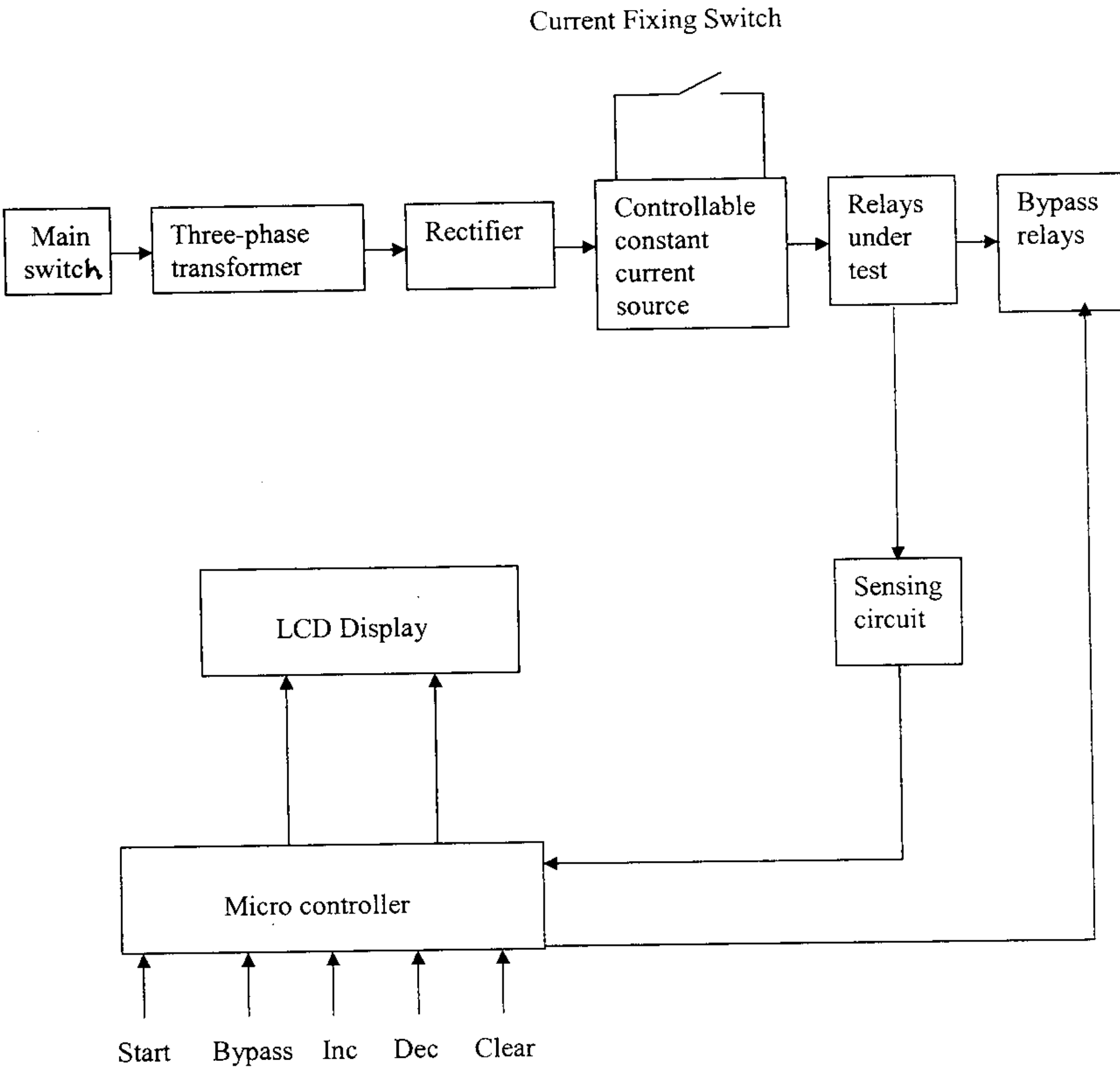


Fig.2.1.Basic Block Diagram

2.2.System Design:

For simplifying the operation and wiring the whole assembly is divided into three parts

- Bottom Module
- Top Module
- Front Panel

2.2.1.Bottom Module:

The bottom module has the supply which consists of the contactor three phase star delta transformers three phase diode bridge rectifier and the constant current source components(IGBT, PCB. resistance, ammeter shunt, etc)which are mounted as a separate unit.

2.2.2.Top Module:

The top module has control components and high power components. The high power components consist of the bypass relays, current setting relay, start stop relay and tapings for the relays to be tested. The control components consist of the sensing circuit micro controller circuits and the interfacing circuits .It also has power supplies necessary for the sensing circuits the controller circuits and the bypass relays.

2.2.3.Front panel:

The front panel consists of the LCD display for displaying the time ammeter which indicates the current through the relays push button switches which control the operation and the data that is to be displayed on the LCD and a rotary switch to control the main contactor.

2.3.Power Supply Modules:

There are 3 power supply modules required. They are

- Power supply for Micro controller and relays
- Power supply for sensing circuit
- Power supply for starters

2.3.1.Power supply for Micro controller and Relays:

The power supply modules needs to supply voltages of 5V and 12V to micro controller circuit and the bypass relay circuit respectively. The supply of 230V AC is stepped down to 12V and then rectified and filtered. This voltage is given to the relays and also to a 5V voltage regulator. The regulated voltage is then given to the micro controller unit.

2.3.2.Power supply for sensing circuit:

Another supply requisite is for the sensing module, which needs a voltage of 6V.The 230V AC supply is stepped down to 18V and then given to a rectifier and filter and then regulated to 6V that are given to the comparator LM324. LM324is a single chip containing four comparator in it. The sensing circuit is provided with four different sets of power supplies, one each for a bimetallic relay.

2.3.3.Power supply for starters:

The starters to be tested need a current of 70A and voltage of 14V.The supply is taken by stepping down three phase 415Vto 14V and then rectifying it to DC using a three phase bridge rectifier.

2.4.Past,Present,and Future of Bimetallic Testing:

Initially the bimetallic strips were tested manually by passing the rated current and noting the tripping time manually. It required a person to be present near the test bench always. This method could test only one strip at a time and the number of circuit breakers that came out after testing was less in number(Around 20 circuit breakers per day). It also led to human fatigue and poor testing efficiency. These difficulties were overcome by initiating the testing process to be carried out electronically as discussed below.

The method currently used employs a system based on the principle of bimetallic testing. The work aimed at determining the tripping time of 5 bimetallic strips each rated for 70A connected in series. The work was carried out with the following modules viz., controllable constant current source, a sensing module, time display unit, a SCR current bypass segment and a delay timer unit.

- It is important to have a controllable constant current source because relays under test have varying drop when SCRs connected in parallel. When a particular relay trips it is not desirable to have a change in value of current.

- Sensing of relay opening is done by the sensing circuit which sends a stop signal to the display unit and gives a gate trigger to the SCR connected in parallel to the relay.

- Display unit displays the tripping time for various relays.
- The constant current source used a set of 7 transistors to get the rated current of 50A.

2.4.1.THE PROPOSED CHANGES:

- The bypass circuit is replaced by relay.
- A new module the control circuit which is a micro controller based circuit keeping track of the time display and the tripping of various CBs replaces the timer and display modules in the older system. This module synchronizes the various modules.
- The display has been changed to LCD display.
- There is only one display and a keypad is provided for viewing the tripping time of the next relay or previous relay.
- The constant current source uses a singular power IGBT in place of 7 transistors.

CHAPTER 3

CIRCUIT DESCRIPTION

This chapter gives an in depth view of the various blocks which were explained in the previous chapter.

3.1.Main Switch:

This is used for cutting off the supply to the whole system after completion of the test so that the system is isolated while the next batch of relays is connected.

3.2.Transformer and Rectifier:

This consists of a three phase 415V/14Vstep down transformer and a three phase diode bridge rectifier. It is used for stepping down and rectifying the 415V AC voltage in order to reduce the power consumption during the testing process.

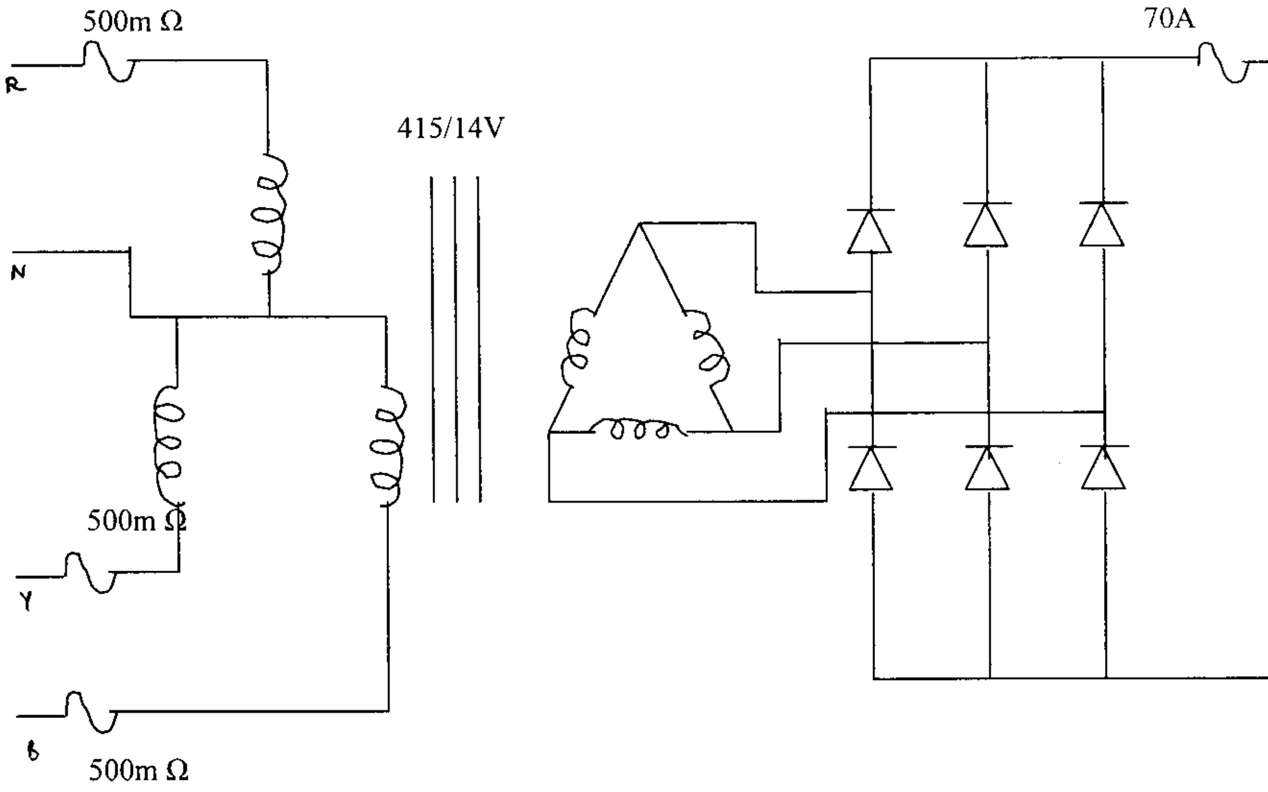


FIG 3.1.TRANSFORMER AND RECTIFIER

The heating of the bimetal strip is dependant upon the I2r losses in the strip, which will be the same for a DC current of I amperes and an AC current I amperes(r.m.s).Hence a low voltage DC supply is used as a source which causes no change in heating of the strip.

Instead of using traditional EI core type transformers toroidal transformers are used. Toroidal transformers have the following features:

1.Compact size
2.Flexibility in dimensions
3.More efficient.

4.Magnetically quieter

5.Acoustically quieter.

6.Improved thermal performance

7.Easy mounting.

3.3.Controllable constant current source

There will be variation in the supply voltage and load on the system especially when a switch opens and a bypass relay is closed in its place. This will lead to variations in the current through the circuit leading to erroneous readings. Hence we use a constant current source to feed the relays. Since the setup will be used for different ratings we need a controllable constant current source that can make the output current a constant at any desired value.

The DC supply represents the three phase star delta step down transformer and rectifier unit. The 7810 regulator supplies a constant 10V supply to the op-amp and the reference potentiometer. The feedback to the op-amp is given through the 700 ohms resistance. The current through the relays is controlled by IGBT(BSM 100 GB 60 DLC 03430)which is in series with the supply. The base current to the IGBT is supplied by the op-amp.

The voltage drop across the 8.1.milli ohms resistance is feedback to the op-amp and whenever there is a change in the load current the op-amp output is varied till the original conditions are regained.

The op-amp is supplied with a variable reference voltage through the potentiometer to make this a controllable constant current source. By adjusting the value of the reference voltage we can control the op-amps output and hence the current which is to be maintained constant is also controlled. The circuit for the constant current source is as follows:

CONSTANT CURRENT SOURCE

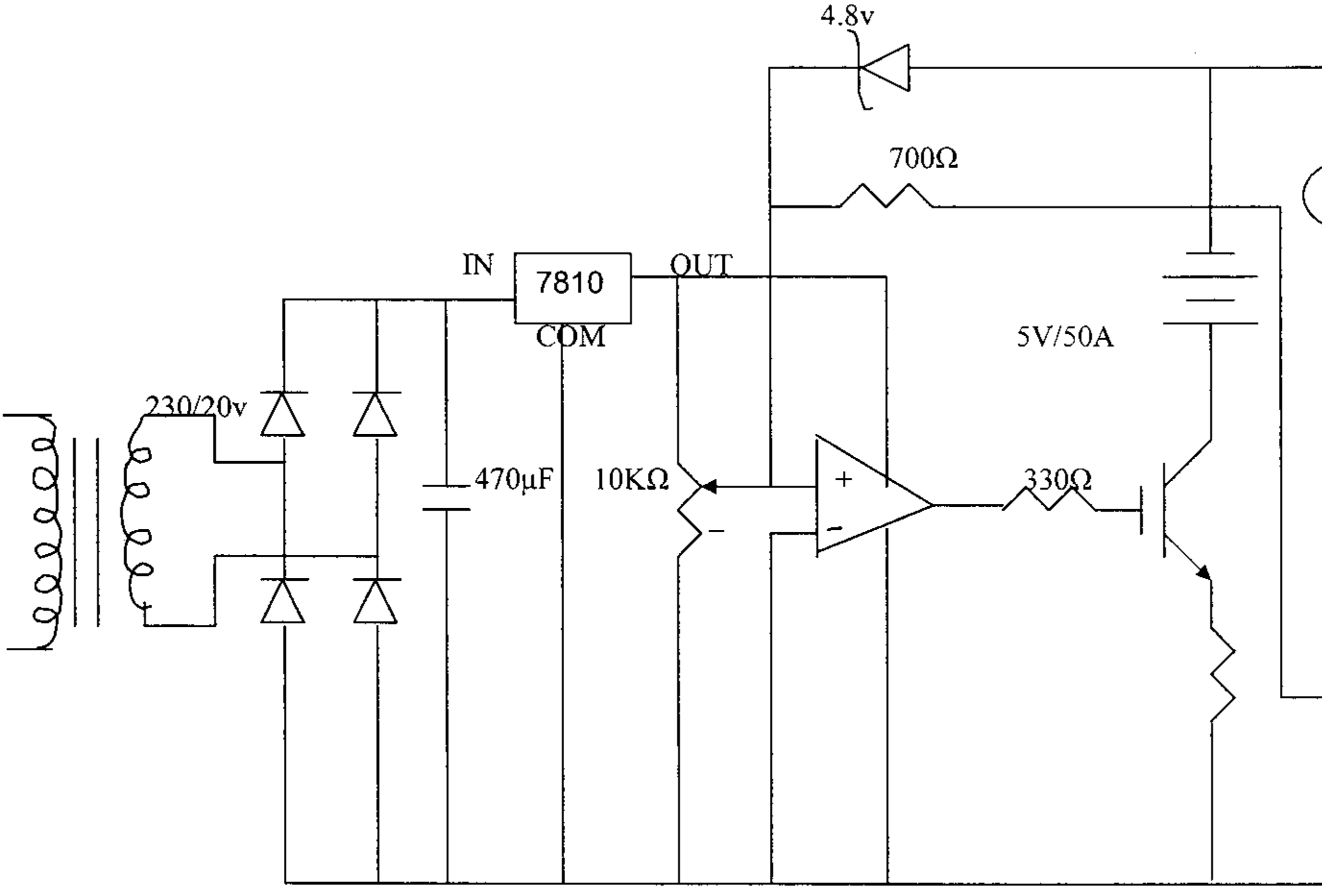


Fig 3.2.Controllable Constant Current Source

3.4.Test relays and Bypass relays:

Four relays are connected in series so that the same current flows through all relays and they are tested simultaneously.

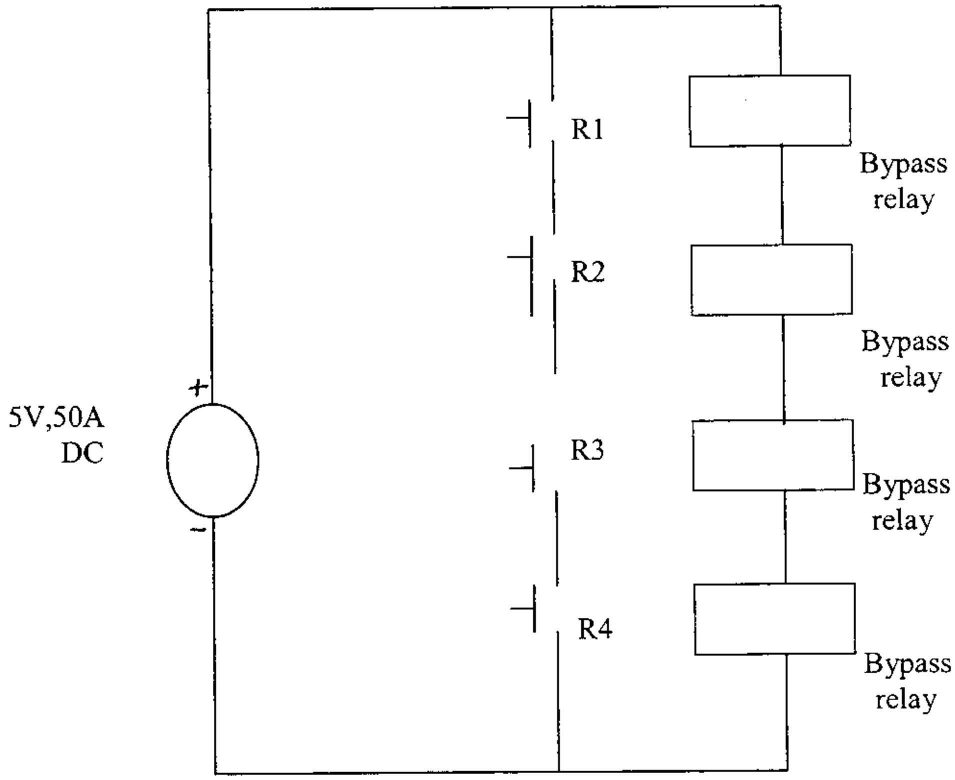


Fig.3.3.Test relays and Bypass relays

In such a situation when a relay is tripped it will open the circuit and hence to maintain continuity of the circuit we provide four bypass relays. They are closed whenever a parallel relay trips thereby maintaining the closed circuit.

A current setting relay and an start/stop relay is provided parallel to the relays and series with the relays respectively. A bypass relay is provided on the front panel controls the current setting relay. The start/stop relay is controlled by the micro controller.

3.5.Sensing circuit:

Sensing circuit being the integral part of the project helps in detecting the opening of relay contacts and it is provided to indicate to the micro controller that relay has tripped and an appropriate action has to be taken

The sensing circuit consists of a resistor parallel to the relay When the relay is closed the current flows through the relay and voltage drop is only the drop across the relay, which are only volts. When relay is opened current flows through the resistor and voltage is dropped across the resistor. This is given to the non- inverting terminal of an op-amp comparator, the inverting terminal of which is connected to a voltage of approximately 0.5v. Hence when a relay is closed, output of the op-amp is 0V and when a relay is tripped output of op-amp is approximately 6v.

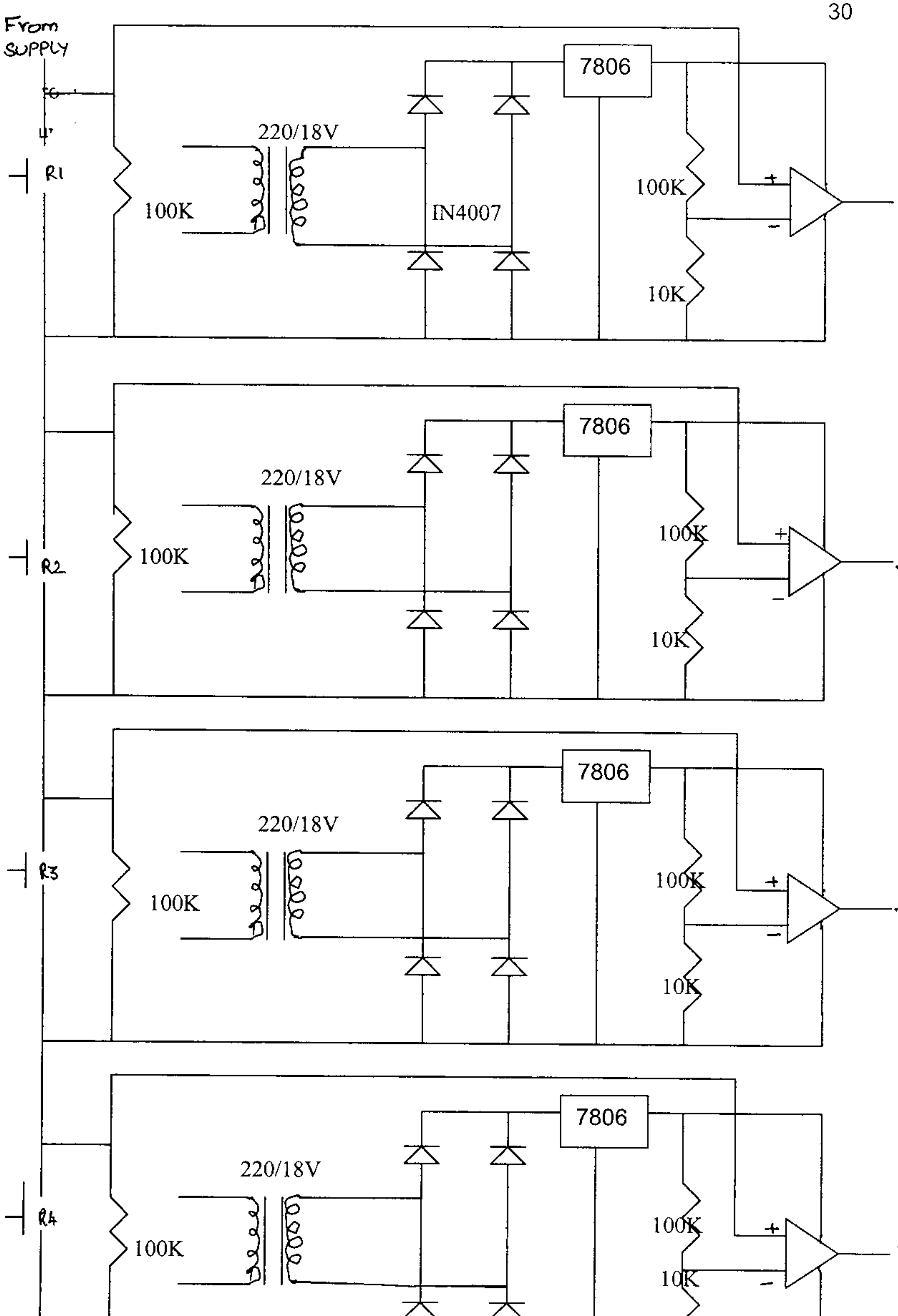
3.5.1.Selection of reference voltage:

The reason for selecting 0.5V as the reference is that when the relay is closed the voltage drop across the relay is only 0.039V. Hence the reference should necessarily be greater than this voltage. On the other hand taking the extreme condition of all the relays tripping simultaneously the net voltage occurring across each resistor is the supply voltage divided by the number of relays.(5/4=1.25). The reference voltage should hence be within 0.04 to 1.25. a value of 0.5V is hence selected.

3.5.2.Working:

The sensing circuit operates on the principle of voltage comparator. The functional part of the circuit is the LM 324 comparator. The comparator is used in its open loop configuration. The input to the circuit is a voltage that is developed across a resistance connected in parallel with each relay. Whenever the relay is conducting no current flows through the resistance as the current takes the least resistant path. But once a relay trips the circuit opens and the current now starts to flow through the resistance causing a voltage drop to occur across it. The four relays each have a resistance of 100 ohms connected in parallel. The voltage developed across the resistor is given to the positive terminal of the op-amp and the negative terminal is given to a reference voltage of 0.5V.

The saturation voltage given is 6V and the inputs may be full 5V when only one relay opens or may be a minimum of 1.25V when all the relays trip simultaneously as discussed above. The output is 4.8V that is coupled to the micro controller.


From
SUPPLY
FG
4'
R1
100K
220/18V
IN4007
7806
100K
10K
+
−
R2
100K
220/18V
7806
100K
10K
+
−
R3
100K
220/18V
7806
100K
10K
+
−
R4
100K
220/18V
7806
100K
10K
+
−

3.6.Micro controller:

The micro controller controls the overall activity of the system. The output of the sensing circuit is given to the micro controller through an interfacing circuit for reasons mentioned above. The micro controller also receives inputs start, stop, increment, decrement ,clear from push button switches for controlling the operation. The start button starts the testing process, the stop button is a manual interruption in case of faulty relays.

The increment and decrement buttons are used to control the display on the LCD. The clear button clears the memory in which the tripping time of the previous batch relays are stored.

The micro controller sends output to the bypass relays through an interfacing circuit. The interface consists of an isolator which drives a 12V relay through a BC547 transistor. The 12V relay in turn controls the coil of the bypass relays.

3.7.Liquid Crystal Display:

The liquid crystal display is used to display the tripping time for the relays. By default it displays the tripping time of the first relay. Whenever the increment or decrement buttons are pressed the corresponding time is displayed. All data for the LCD comes from the micro controller and when a relay does not trip the time is indicated as zero.

3.7.1.Introduction:

Liquid Crystal Displays(LCDs)have materials which combine the properties of both liquids and crystals. Rather than having a melting point they have a temperature range within which molecules are almost as mobile as they would be in a liquid, but are grouped together in an ordered form similar to a crystal.

A LCD consists of two glass panels with the liquid crystal material sand witched in between them. The inner surface of the glass plates are coated with transparent electrodes which define the character, symbols or patterns to be displayed polymeric layers are present in between the electrodes and the liquid crystal which makes the liquid crystal molecules to maintain a defined orientation angle. One each polarisers are pasted outside the two glass panels. These polarisers would rotate the light rays passing through them to a definite angle in a particular direction. When the LCD is in the off state the two polarisers and the liquid crystal rotate light rays such that the light rays come out of the LCD without any orientation and hence the LCD appears transparent.

When sufficient voltage is applied to the electrodes the liquid crystal molecules would be aligned in a specific direction. The LCDs are light weight with only a few millimeters thickness. Since the LCDs consume less power electronic circuits and can be powered for long durations. The LCD's don't generate light and so light is needed to read the display. By using backlighting reading is possible in the dark. The LCD's have long life and a wide operating temperature range.

Changing the display size or the layout size is relatively simple which makes the LCD's more customer's friendly. The LCD's used exclusively in watches calculators and measuring instruments are the simple seven segment displays having a limited amount of numeric data. The recent advances in technology have resulted in better legibility more information displaying capability and a wider temperature range. These have resulted in the LCD's being extensively used in telecommunications and entertainment electronics. The LCD's have been started replacing the cathode ray tubes used for the display of text and graphics and also in small TV applications.

3.7.2.Power supply:

The power supply should be of +5V with maximum allowable transients of 10mv to achieve a suitable contrast for the display, the voltage (VL)at pin 3 should be adjusted properly.

A module should not be inserted or removed from a live circuit. The ground terminal of the power supply must be isolated properly so that no voltage is induced in it. The module should be isolated from the other circuits so that stray voltages are not induced which could cause a flickering display.

3.7.3.Hardware:

Develop a uniquely decoded 'e' strobe pulse, active high to accompany each module transaction. Address or control lines can be assigned to drive the RS and R/W inputs. Utilize the Host's extended timing mode if available when transacting with the module. Use instructions which prolong the read and write or other appropriate data strobes so as to realize the interface timing requirements. If a parallel port is used to drive the RS,R/W and e control lines setting the 'E' bit simultaneously with RS and R/W would violate the modules setup time. Separate instruction should be used to achieve proper interfacing timing requirements.

CHAPTER 4

4.SOFTWARE PROGRAMMING

4.1.System Operation:

All the modules are assembled together by giving necessary interface connections. Referring to all the modules the operation can be briefed as follows. Initially the supply is turned off and the relays that are to be tested are connected to the test bench. The supply is switched on using the rotary contactor. Now the supply reaches the step down transformer where the voltage is reduced and the three phase diode bridge rectifier rectifies this reduced voltage.

The bypass relay is switched on to turn on the current setting relay and the current setting potentiometer is adjusted till the required current is obtained and after that the constant current is set in. When the current setting relay opens and start/stop relay closes it allows this high current to flow through the bimetallic relays under test.

When the operation starts the timer of micro controller starts counting the time. When any one of the relays trips then the corresponding time of the tripped device is stored. A bypass path is provided for the current flow to the next relay with the help of the bypass circuit. Giving a stop signal to the start/stop relay when there is a fault in any of the relays can stop the operation. Then the time of each trip can be noted down from the LCD display using the increment and decrement switches.

After the testing of one set of batch is over the operation can be continued for the next set of relays. The clear switch is used to clear the contents of the timer and make it ready to get new set of time. Hardware reset is also provided so as to avoid any trouble while operating.

4.2.Algorithm:

Step1:Assign the registers to be used.

Step2:Initialize the registers.

Step3:Initialize the LCD.

Step4:Display the first device data.

Step5:If increment is pressed display next data if available.

Step6:If decrement is pressed display previous data if available.

Step7:If clear is pressed clear the memory.

Step8:If start button is pressed turn on the ON-OFF relay and start timer.

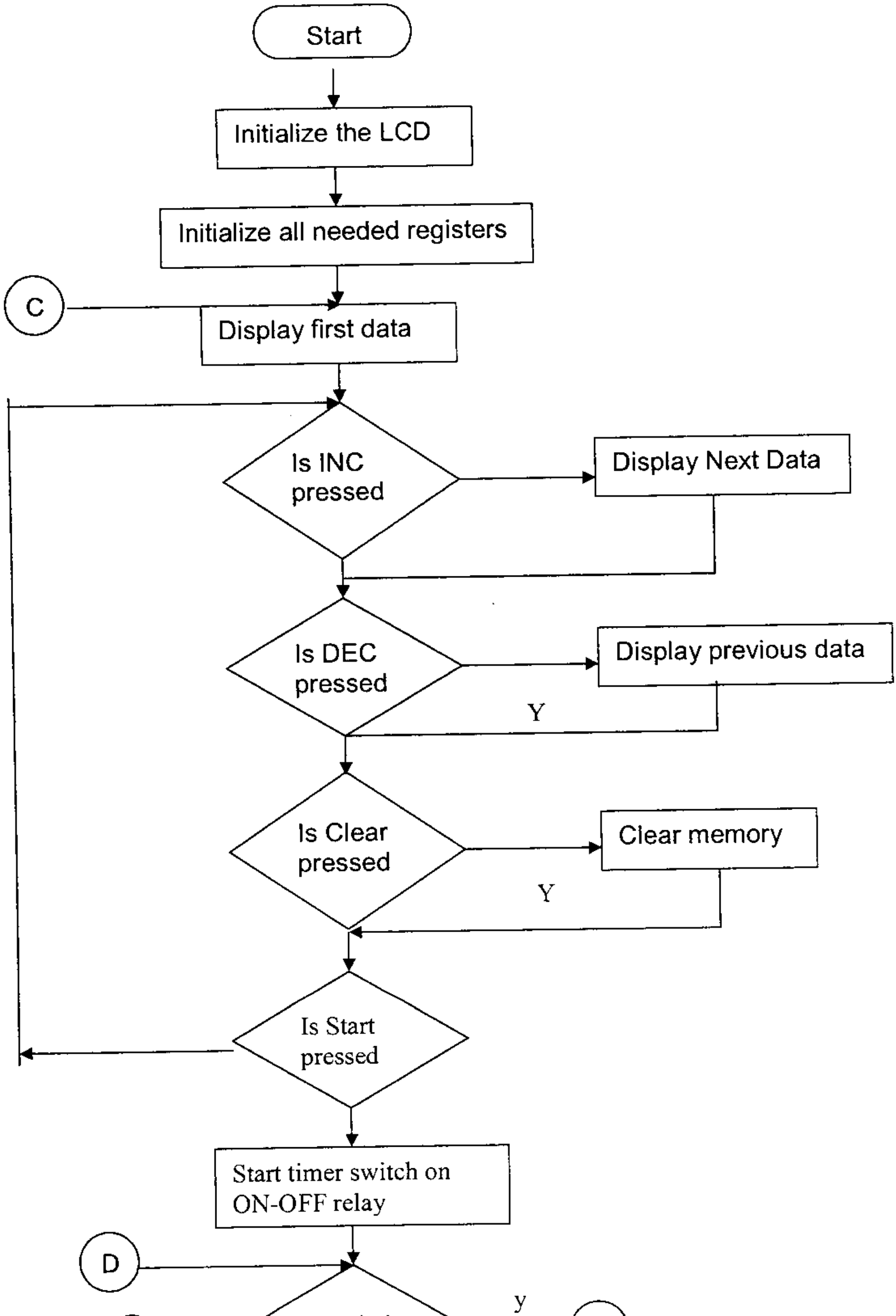
Step9:If relay trips store timer in memory and turn on appropriate bypass relay.

Step10:If all four relays are tripped stop timer turn off ON-OFF relay and display first data.

Step11:If stop button is pressed stop timer turn off ON-OFF relay and display first data.

Step12:Repeat from step5.

4.3 FLOWCHART



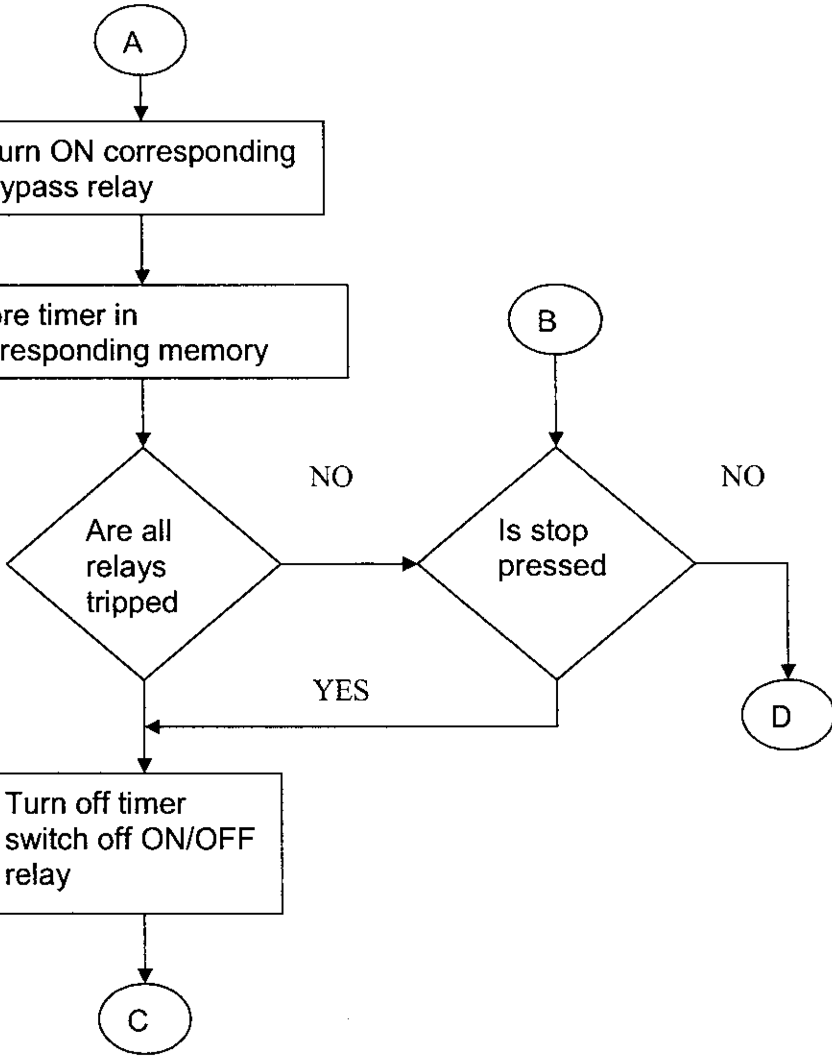


Fig 4.1.Flowchart

4.4 CONTROL CIRCUIT

4.4.1. Micro controller :

The micro controller used is PICI6F877. It is a RISC processor programmed in 'C'. It is programmed to receive the signals from the sensing circuit and to actuate the corresponding relay to drive the bypass circuit. The input and output have to be isolated from the power circuits to prevent noise from entering the C. This is effected by using an optic isolator MCT2E and relays. Once a switch trips the C also notes the time of tripping of the corresponding switch. The time is kept track by the timer module in the C. The C module is a low power module needing a power supply of only 5V. The LCD display also needs a power supply of 5V. The pull down resistors AJ102 and AJ103 are used to ground the floating load. The connections to the C chip is depicted in Fig 4.2.

4.4.2. Inputs To Micro Controller :

The inputs to the Micro Controller are basically the keypad inputs viz. start, stop increment, decrement, clear memory and load set the input from the sensing circuit as shown in the Fig 4.2.

The bypass relay turns on a current setting relay that aids setting of the required load current. Initially when the current is being adjusted the current should to flow through the relays because it will cause heating of the bimetal strip even before the start of test. Hence the entire test set-up is bypassed using a current setting relay using this bypass switch. The load current is then set and the bypass relay is turned off and the start switch is pressed which causes the current to flow through the relays under test. In case of emergencies or for faulty relays using stop switch, which stops the current flow to the relays, can terminate the testing. After the testing is over the increment and decrement switches, can terminate the testing. After the testing is over the increment and decrement switches are used to note down the tripping time of the bimetals. The clear key helps to clear the tripping time details in the memory.

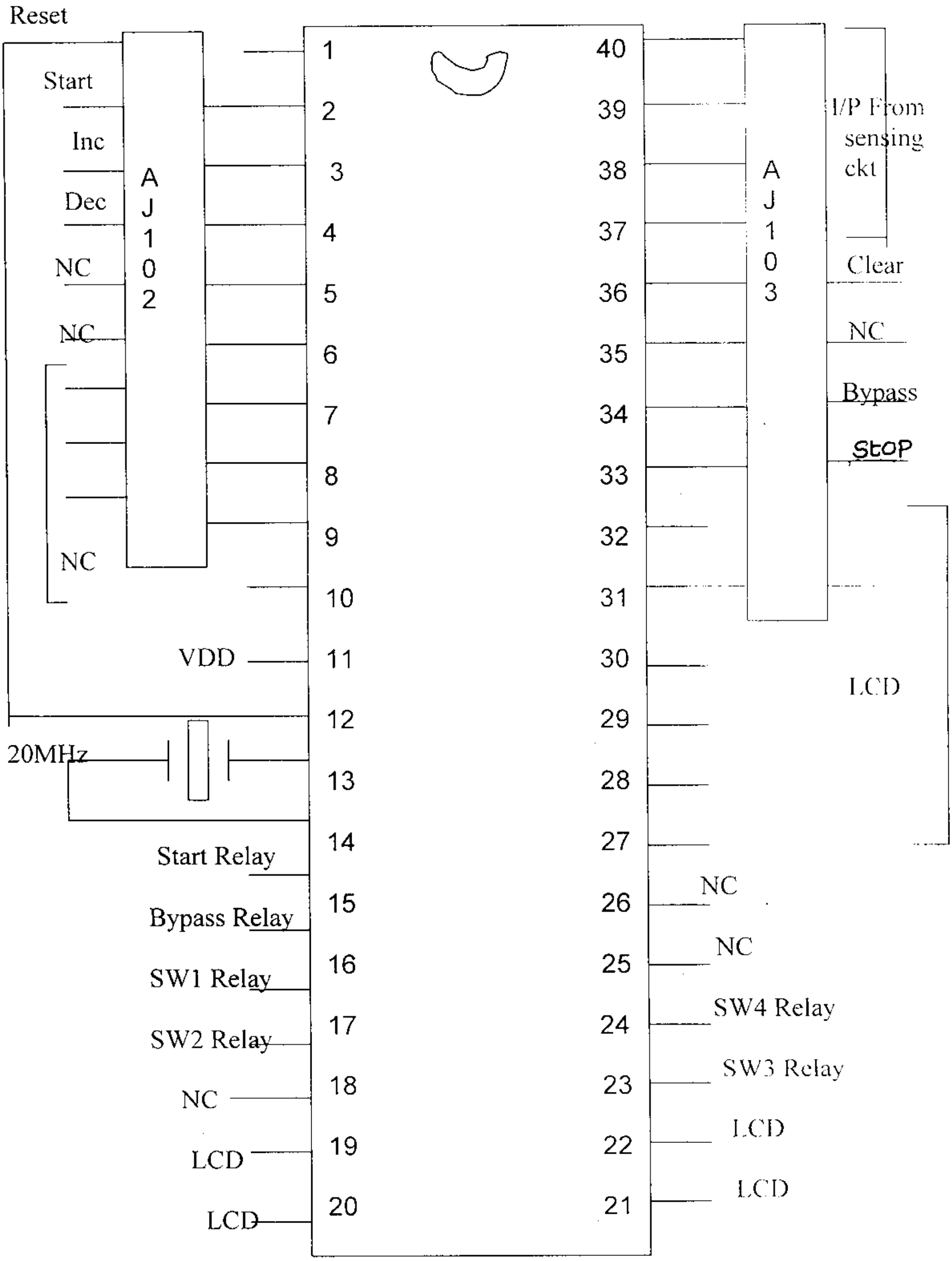


Fig4.2.MICROCONTROLLER CONNECTIONS

The other set of inputs from the sensing circuit that sense the tripping of the relays cause the Micro Controller to turn ON the corresponding bypass relays and also to record the tripping time of the corresponding relays. This input is given through a relay interfacing circuit.

The output of the op-amp in the sensing circuit is given to the base of an SL100 switching transistor. The relay coil is supplied with a 6V regulator IC7806 provided in the sensing circuit. When a relay trips the transistor is turned on and energizes the relay coil and thereby sending a high to the micro controller to indicate the tripping of a relay.

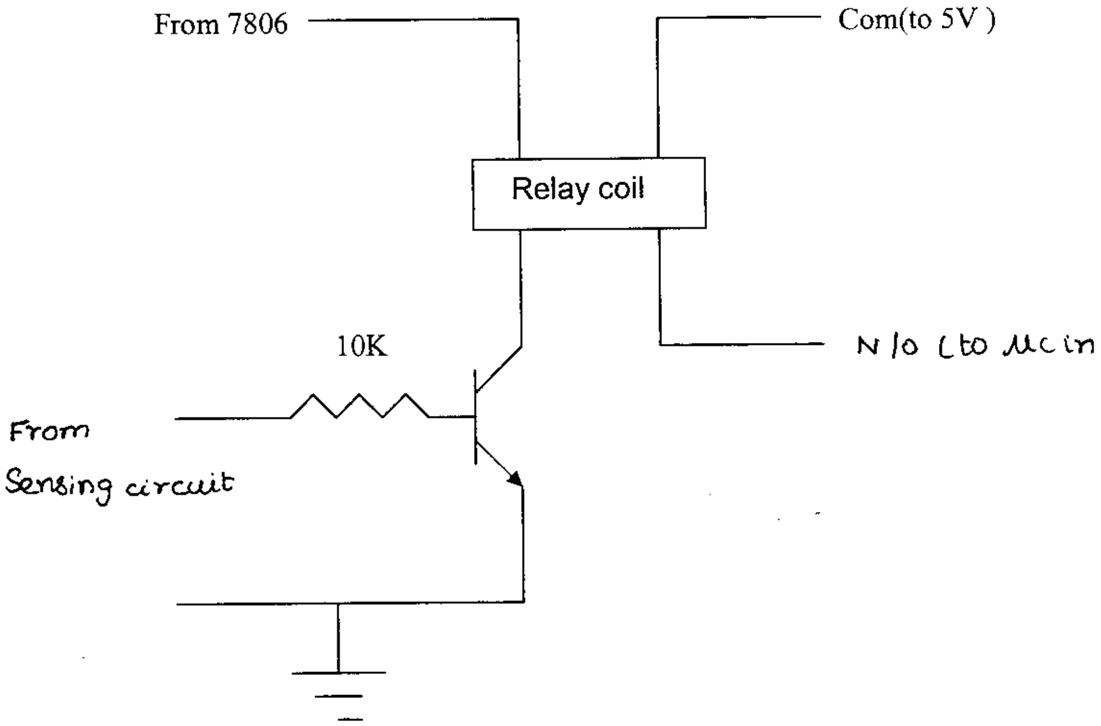


fig.4.3. Inputs to Micro Controller

4.4.3. Output From the Controller :

The outputs are signals to actuate the relays that are usually sent through an opto isolator circuit and to the display unit, which is a LCD display unit. The controller has to ,in all actuate six relays among which four are for the switch bypass and the other two are each a start/stop and current setting relay. The LCD unit was described in the previous chapter. The purpose of MCT2E opto isolator is to isolate the low power circuits from high power circuits.

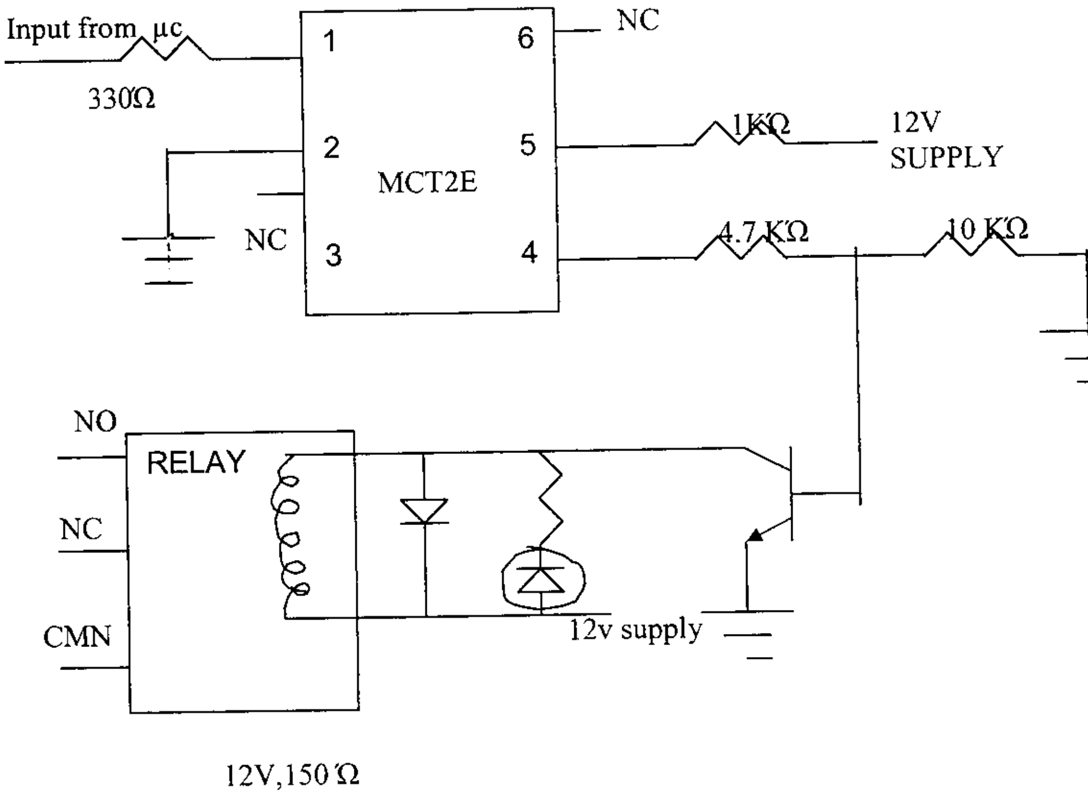


Fig 4.4.Relay circuit

4.5. Opto Isolators:

The proper isolation between input and output becomes very important in several of the digital and analog applications. The traditional methods of isolation involve the use of devices such as capacitor, relays, transformers and opto couplers. Of these the Optocoupler provide an ideal combination of speed, OC response, high common mode noise for both analog and digital applications in industrial, medical and military products. Examples are logic isolations, line receivers, sensing circuits, power supply feed back, high voltage current monitoring, telephone, lines patient monitoring equipment, adaptive control, audio and video amplifiers, triggering of thyristors, and so on.

Optocoupler consists of an LED emitter and a photo sensor of transistor or diode type. The one utilizes a phototransistor is limited in it improves the speed upto a hundred times that of a phototransistor coupler by reducing the base-collector capacitance. All high speed optocoupler employs this as principle of operation.

CHAPTER 5

5. TEST RESULTS AND CONCLUSION

5.1. Simulations :

Before the final testing the assembly was tested with low value of currents to check for the proper functioning of the various modules. The switches were manually turned On and OFF to simulate the tripping of a relay. Since the current was very low there was no chance for the relay to trip and hence the experiment was performed under full fledged manual control. Whenever a switch was turned OFF manually, the tripping time was recorded and cross-checked with a stop watch. When all the four switches under test were turned OFF, the supply to the relays was cut off. When the stop button was pressed before the completion of the test, the supply was cut off to the relays.

5.2. Specifications of Relays under Test :

Our project setup is designed to vary the current from 0-70A, with 14V DC supply. So any bimetallic strip rated between this rating can be tested and calibrated.

The strip manufactured and tested had the following specifications.

Grade : 145R17
Current : 12A.
Bimetal contact resistance : 0.194 ohms at 11A.
Length of contact : 60 x 10 mm.
Area of contact : 6.5 mm.
Switch résistance : 3.58 m at 11A.
Voltage drop at one relay : 0.0394V

5.3. Calibration Table for Bimetallic Strips :

Four relays, the specification for which was given in the previous section were tested for a current of 24A and the results are depicted in table 5.1

RELAYS	RATING	APPLIED CURRENT (A)	ACTUAL OPERATING TIME (S)	TIME DISPLAYED (S)
1	12	24	45	46
2	12	24	45	48
3	12	24	45	45
4	12	24	45	47

5.4.Future Scope :

The number of switches tested can be increased further by slight modifications in the sensing circuit and the control circuit. This number is restricted by the number of ports available in the controller. The testing can be improved further by considering the following features;

- ❑ A personal computer can be used instead of a micro controller so that a wide range of tests can be performed.
- ❑ Various tests like Routine test, type test can be performed to facilitate the study of other important factors that affect the performance of the switch.
- ❑ Considering the Network facilities it is possible to obtain latest information and developments regarding the switches that are under test.
- ❑ With the help of network monitoring using high-tech personal computers the process of troubleshooting can be done easily.
- ❑ Combining the above features along with robotics the process time will be reduced further.

- Complete automation is possible through robotics with no manual interruption from the production till calibration.
- Usage of two-dimensional robots instead of three-dimensional robots will make the system affordable for even small firms.
- Considering the economical conditions the two-dimensional robots are involved only in certain firms and further research is made in this testing.

5.5. Conclusion:

An industry producing quality products, if wants to place its market to international standards needs its product manufactured to be approved quality. Testing and calibrating are the two important aspects to satisfy the quality expected. Our project forming the integral unit of testing OF SALZER ELECTRONICS, a leading international Electronics company in Coimbatore, works out efficiently to the desired expectation.

Since testing and calibration takes place four switches at a time, it increases the production speed of the starters. Moreover the range of current control being 0-70A, it becomes an another confident approach permitting the bimetallic switches to be tested under varying current input conditions.

The system can be undergone with further expansion to carry out testing of bimetallic strips more than 4 units if the sensing and bypass arrangements are slightly altered. Modules can also be made so as to adjust the initial tension of the bimetallic strip.

PROGRAMMING IN C LANGUAGE:

```
# include <pic.h>
# include <stdio.h>
unsigned char tab - 1 []
unsigned char car,num,temp;
unsigned int delay;
bit flag;

void 1cs init();
void out (unsigned char);
void nop (void);
void display(void);
void dly (void);

unsigned char device _m_1, device_m_2,device_m_3, device_m_4, minute, device, timer count,
device _s_1,device_s_2,device_s_3,device_s_4, second;
bit bypass;
void Hardware _Initialization(void)
main()
{
 Hardware Initialization ();
sprintf(tab _1,"Device 1 % 02d:%02d S " , minute, second);
display();
while ( 1 )
{..
        If ( RC 2 && RC3 && RC4 && RC5)
        {
                RC0=RC2=RC3=RC4=RC5=0;
                TMR1ON=0;
```

```
}
if(RB3&&!TMR1ON)//Clear Button
{
PORT C=0;
device_m_1=device_m_2=device_m_3=device_m_4=0;
device_s_1=device_s_2=device_s_3=device_s_4=0;
}
if(RA0)
{
PORT C=0;
RC0=1;
device=1;
minute=second=0;
TMR1ON=1;
}
RC1=RB1;
if(TMR1ON)
{
relay(device)
{
case1:
{
sprintf( tab_1,"Device 1%02d:%02d S", minute, second);
break;
}
case2:
{

sprintf( tab_1,"Device 2%02d:%02d S", minute, second);
break;
}
```

```
case3:
{
sprintf( tab_1,"Device 3%02d:%02d S", minute, second);
break;
}
case4:
{
sprintf( tab_1,"Device 4%02d:%02d S", minute, second);
break;
}
default:
{
break;
}
 }
 else
 {
 if(RA1)
 {
 relay(device)
{
case1:
{
sprintf(tab_1,"Device1 %02d:%02dS",
device_m_1,device_s_1);
break;
}
case2:
{
sprintf(tab_1,"Device2 %02d:%02dS",
device_m_2,device_s_2);
```

```
break;
}
case3:
{
sprintf(tab_1,"Device3 %02d:%02dS",
device_m_3,device_s_3);
break;
}
case4:
{
sprintf(tab_1,"Device4 %02d:%02dS",
device_m_4,device_s_4);
break;
}
default:
{
sprintf(tab_1,"Device1 %02d:%02dS",
device_m_1,device_s_1);
break;
}
}
      display();
      if(device !=4)
      {
                 device++;
      }
      for(delay=0;delay<=30000;delay++);
      for(delay=0;delay<=30000;delay++);
      while(RA1);
      for(delay=0;delay<=30000;delay++);
      for(delay=0;delay<=30000;delay++);
```

```
            }
            if(RA2)
            {
             relay(device)
             {
             case1:
             {
             sprintf(tab_1,"Device1 %02d:%02dS",
             device_m_1,device_s_1);
             break;
        }

                    case2:
                         {
                                 sprintf(tab_1,"Device2 %02d:%02dS",
device_m_2,device_s_2);
                                 break;
                          }

                     case3:
                          {
                                  sprintf(tab_1,"Device3 %02d:%02dS",
 device_m_3,device_s_3);
                                  break;
                           }


                      case4:
                           {
                                   sprintf(tab_1,"Device4 %02d:%02dS",
  device m 4,device s 4);
```

```
                                                break;
                                        }
                                        default:

                                        {
                                                sprintf(tab_1,"Device1 %02d:%02dS",
device_m_1,device_s_1);
                                                device=1;
                                                break;
                                        }

                                }

                                    display();
                                    if(device !=0)
                                    {
                                            device--;
                                    }
                                    for(delay=0;delay<=30000;delay++);
                                    for(delay=0;delay<=30000;delay++);
                                    while(RA2);
                                    for(delay=0;delay<=30000;delay++);
                                    for(delay=0;delay<=30000;delay++);

                                }

                        }

                                }

                        }
```

```
void iterrupt isr(void)
{
GIE=0
        if(RBIF)
        {
                if(RB7)
                {
                        RC2=1;
                        device_m_1=minute;
                        device_s_1=second;
                        device=2;
                }

                if(RB6)
                {
                        RC3=1;
                        device_m_2=minute;
                        device_s_2=second;
                        device=3;
                }

                if(RB5)
                {
                        RC4=1;
                        device_m_3=minute;
                        device_s_3=second;
                        device=4;
                }

                if(RB4)
                {
```

```
                RC5=1;
                device_m_4=minute;
                device_s_4=second;
                device=1;
            }

            for(delay=0;delay<=30000;delay++);
            for(delay=0;delay<=30000;delay++);
            RBIF=0;

        }
        if(TMR1IF)
        {
            TMR1H=0X0B;
            TMR1L=0XDB;
            if(timer _count=10)
            {
             timer _count=0;
             if(second=59)
             {
                    second=0;
                    minute++;
             }
             else
             {
                    second++;
             }

          }
          else
          {
```

```
                        timer_count++;
                    }
                    TMR1IF=0;


            }
            if(INTF)
            {
                TMR1ON=0;
                RC0=0;
                INTF=0;


            }
            GIE=1;
}
void Hardware_Initialisation(void)
{


            TRISA=0XFF;
            TRISB=0XFF;
            TRISC=0X80;

            GIE=1;
            PEIE=1;

/* PORTB Change Interrupt */
            RBPU=1;
            RBIE=1;
            RBIF=0;

/* Timer 1 Setup-100ms */
```

```
                TMR1IF=0;
                TMR1IE=1;
                T1CON=0XF4;
                lcd_init();
}
void lcd_init()
{
                while(delay<5000)
                        delay++;
                delay=0;
                out(car=0x30);
                while(delay<1000)
                delay++;
                delay=0;
                out(car=0x30);
                while(delay<100)
                        delay++;
                delay=0;
                out(car=0x30);
                nop();
                out(car=0x21);
                nop();
                out(car=0x0c);
                nop();
                out(car=0x06);
                nop();
                out(car=0x01);
                nop();
                //out(car=0x02);
  }
```

```
void out(unsigned char)
{
            PORTD=0;
            TRISD=0XF1;
            RD1=0;
            RD2=1;
            nop();
            RD3=1;
            nop();
            while(RD7);
            PORTD=0;
            TRISD=0X01;
            temp=car&0xf0;
            PORTD=temp;
            if(flag)
                  RD1=1;
            nop();
            RD3=1;
            nop();
            RD3=0;
            temp=car;
            temp=temp<<4;
            temp=temp&0xF0;
            PORTD=temp;
            if(flag)
                  RD1=1;
            nop();
            RD3=1;
            nop();
            RD3=0;
            RD2=0;
```

```
                flag=0;
                return;
}
void nop(void)
{
#asm
NOP
NOP
NOP
#endasm
return;
}

void display(void)
{
                flag=0;
                out(car=0x80);
                num=0;
                while(num<8)
                {
                       flag=1;
                       delay=0;
                       while(delay<500)
                              delay++;
                       out(car=tab_1[num]);
                       num++;
                }
                flag=0;
                       out(car=0xc0);
                       while(num<16)
                        {
```

```
                flag=1;
                delay=0;
                while(delay<500)
                        delay++;
                out(car=tab_1[num]);
                num++;
        }
        flag=0;
        return;

}
```

COMPANY PROFILE

SALZER ELECTRONICS LIMITED

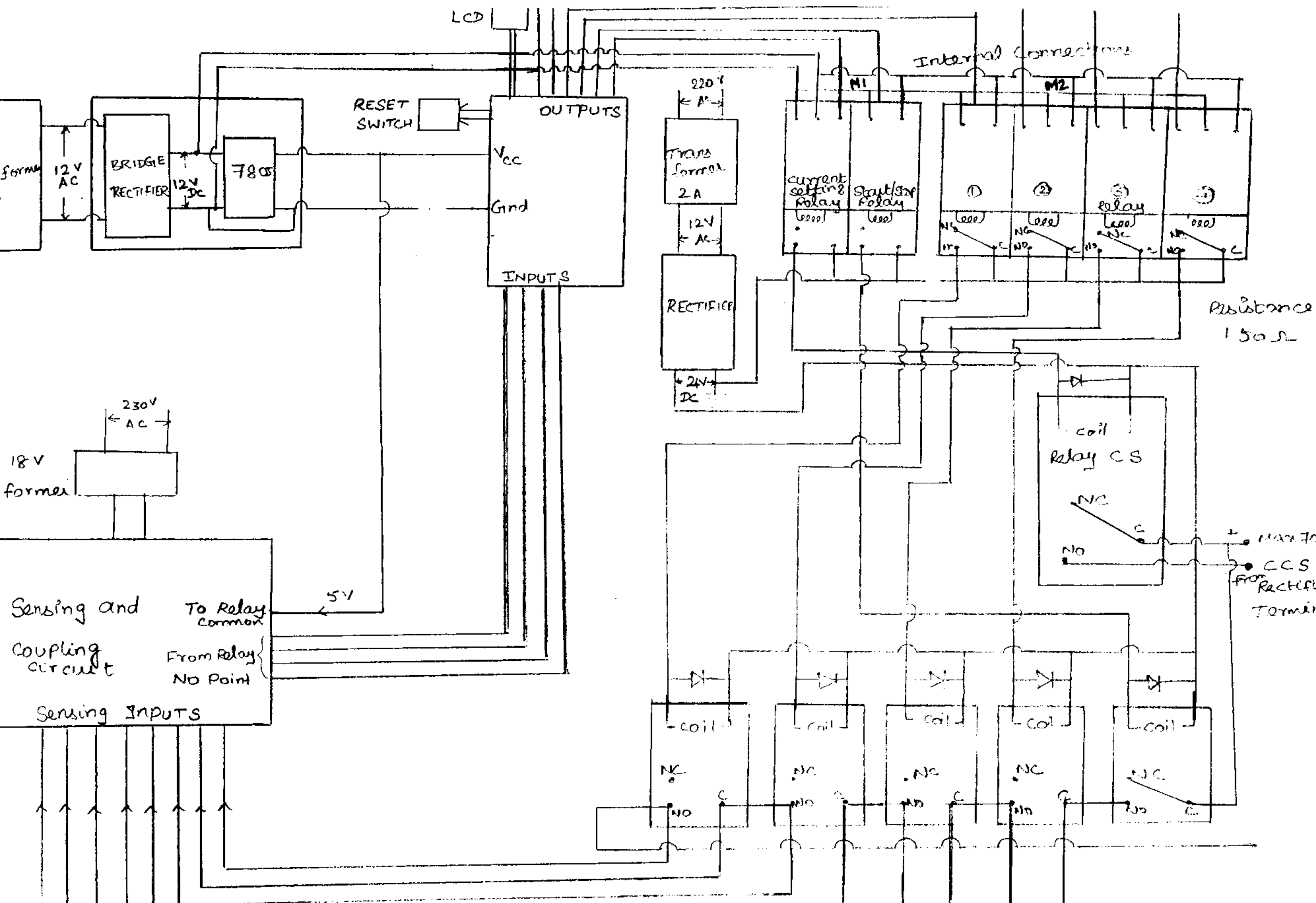
Salzer Electronics Limited was established in 1985 to design and manufacture world class Cam operated Rotary Switches in Technical Collaboration with M/S.Salzer Schaltgerate Fabric, Germany. The company has a consistent track record for the last five years in profit making and declaring dividends.

The prestigious ISO 9002:1994 Certification based on the recommendation by KPMG of U.S.A. was obtained for manufacture and supply of Cam operated Rotary switches in 6 to 400 Amps range. The company has a strong R&D facility with the full fledged laboratory to upgrade the products and set new market trends.

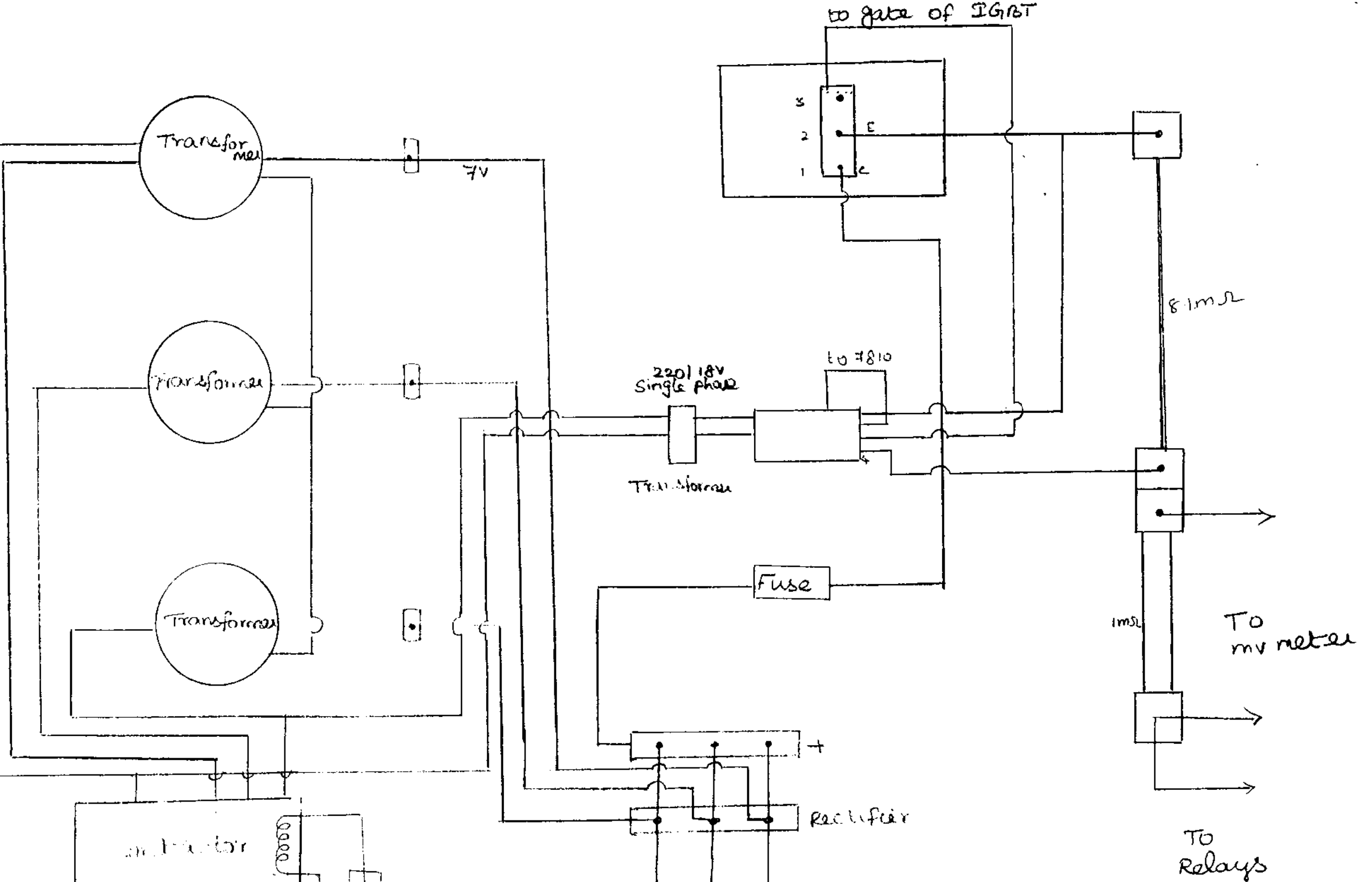
M/S/. Larsen & Toubro Limited , the Indian Industrial Giant Engineering has been marketing Salver switches throughout India since 1993.

Distinctions:

- Formed in 1985,we have a 12 year track record of success.
- 7 factories with international connections.
- International product approvals like csa ,ul, vde & ce.
- Worldwide availability of our products.
- Full fledged R&D facilities.
- ISO 9000 series accreditation for all factories are at various levels.
- Self sufficient captive tool room .


LCD
Internal Connections
M1
M2
RESET SWITCH
OUTPUTS
Vcc
Gnd
INPUTS
former
12 V AC
BRIDGE RECTIFIER
12V DC
7805
220V AC
Trans former
2 A
12V AC
RECTIFIER
24V DC
current setting Relay
Start/stop Relay
①
②
③ Relay
④
NC
NO
C
Resistance 150 Ω
coil
Relay CS
NC
C
NO
+ Max To
CCS
From Rectifier Terminal
230V AC
18 V former
5V
Sensing and Coupling circuit
To Relay common
From Relay NO Point
Sensing Inputs
coil
NC
NO
C

Power supply with Constant current Source Layout



APPENDIX 2

PIC MICRO CONTROLLER

DATA SHEET

MICROCHIP

PIC16F87X

28/40-Pin 8-Bit CMOS FLASH Microcontrollers

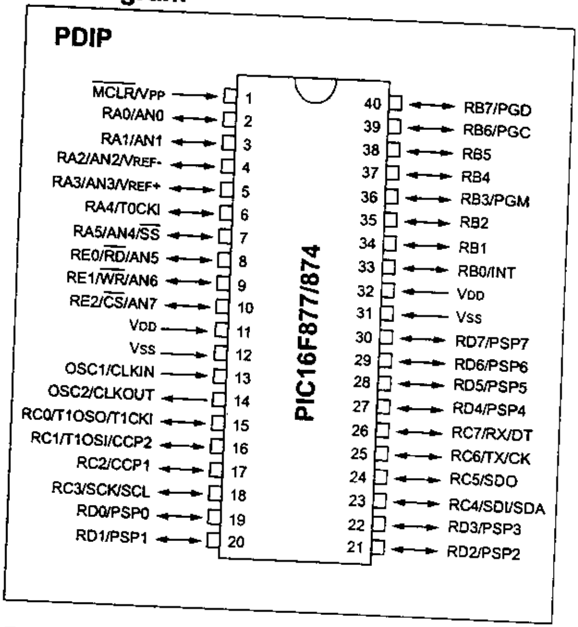
Devices Included in this Data Sheet:

- PIC16F873
- PIC16F874
- PIC16F876
- PIC16F877

Microcontroller Core Features:

- High performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Up to 8K x 14 words of FLASH Program Memory,
  Up to 368 x 8 bytes of Data Memory (RAM)
  Up to 256 x 8 bytes of EEPROM Data Memory
- Pinout compatible to the PIC16C73B/74B/76/77
- Interrupt capability (up to 14 sources)
- Eight level deep hardware stack
- Direct, indirect and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low power, high speed CMOS FLASH/EEPROM technology
- Fully static design
- In-Circuit Serial Programming™ (ICSP) via two pins
- Single 5V In-Circuit Serial Programming capability
- In-Circuit Debugging via two pins
- Processor read/write access to program memory
- Wide operating voltage range: 2.0V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial, Industrial and Extended temperature ranges
- Low-power consumption:
  - < 0.6 mA typical @ 3V, 4 MHz
  - 20 µA typical @ 3V, 32 kHz
  - < 1 µA typical standby current

Pin Diagram

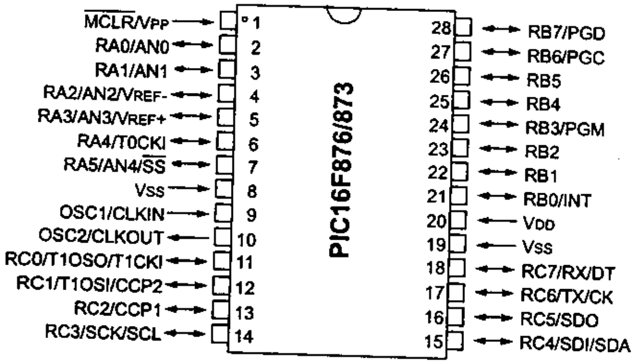


Peripheral Features:

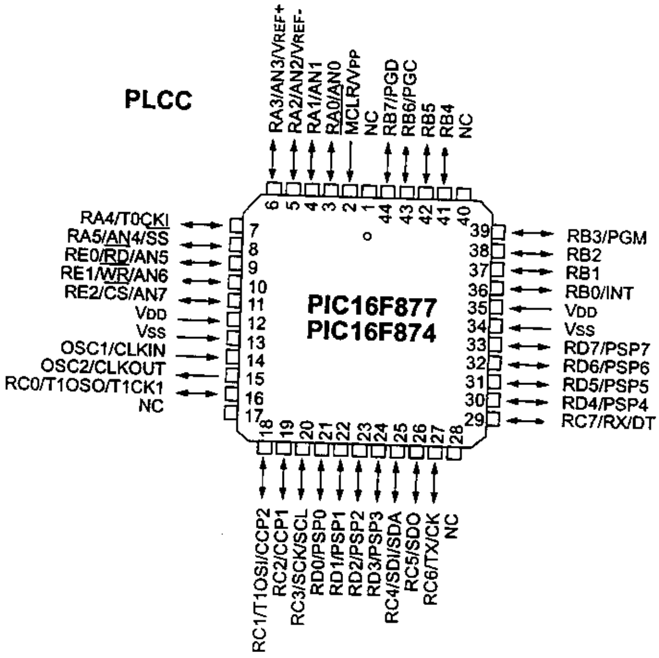
- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during SLEEP via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
  - Capture is 16-bit, max. resolution is 12.5 ns
  - Compare is 16-bit, max. resolution is 200 ns
  - PWM max. resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI™ (Master mode) and I^{2}C™ (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) 8-bits wide, with external $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

Pin Diagrams

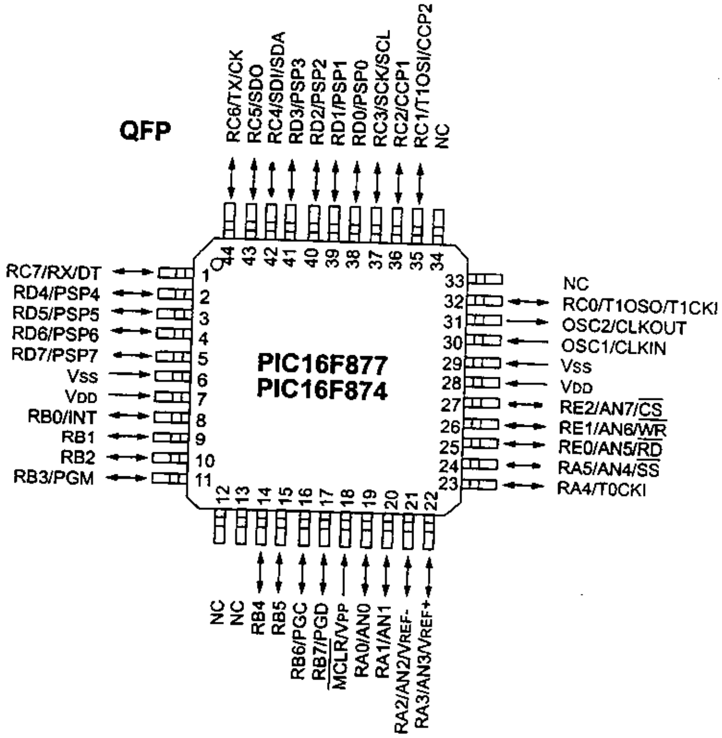
PDIP, SOIC



PLCC



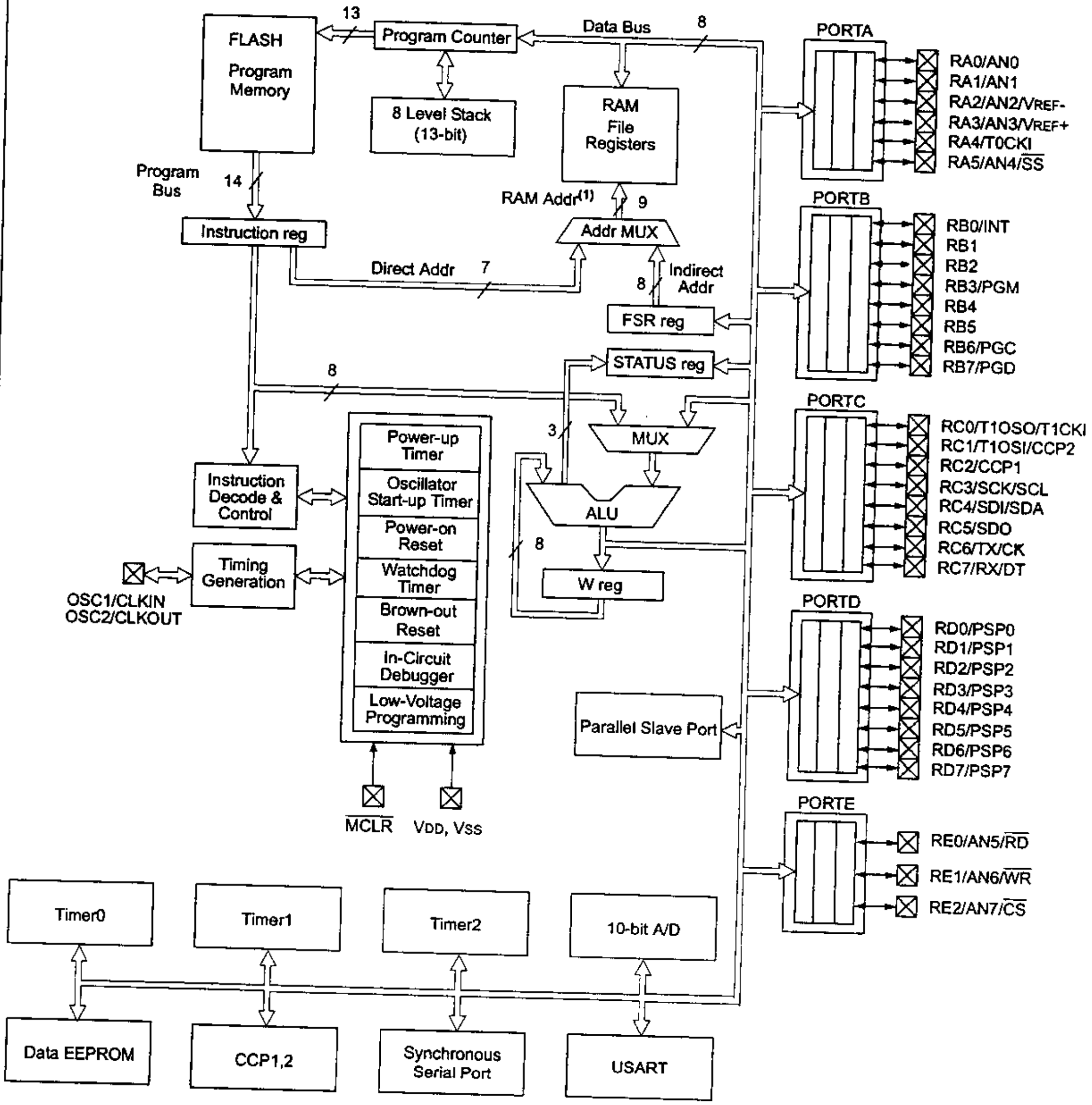
QFP



Key Features PICmicro™ Mid-Range Reference Manual (DS33023)	**PIC16F873**	**PIC16F874**	**PIC16F876**	**PIC16F877**
Operating Frequency	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz
RESETS (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
FLASH Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
EEPROM Data Memory	128	128	256	256
Interrupts	13	14	13	14
I/O Ports	Ports A,B,C	Ports A,B,C,D,E	Ports A,B,C	Ports A,B,C,D,E
Timers	3	3	3	3
Capture/Compare/PWM Modules	2	2	2	2
Serial Communications	MSSP, USART	MSSP, USART	MSSP, USART	MSSP, USART
Parallel Communications	—	PSP	—	PSP
10-bit Analog-to-Digital Module	5 input channels	8 input channels	5 input channels	8 input channels
Instruction Set	35 instructions	35 instructions	35 instructions	35 instructions

FIGURE 1-2: PIC16F874 AND PIC16F877 BLOCK DIAGRAM

Device	Program FLASH	Data Memory	Data EEPROM
PIC16F874	4K	192 Bytes	128 Bytes
PIC16F877	8K	368 Bytes	256 Bytes



Note 1: Higher order bits are from the STATUS register.

TABLE 1-2: PIC16F874 AND PIC16F877 PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	I	ST/CMOS(4)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{\text{MCLR}}$/VPP	1	2	18	I/P	ST	Master Clear (Reset) input or programming voltage input. This pin is an active low RESET to the device.
						PORTA is a bi-directional I/O port.
RA0/AN0	2	3	19	I/O	TTL	RA0 can also be analog input0.
RA1/AN1	3	4	20	I/O	TTL	RA1 can also be analog input1.
RA2/AN2/VREF-	4	5	21	I/O	TTL	RA2 can also be analog input2 or negative analog reference voltage.
RA3/AN3/VREF+	5	6	22	I/O	TTL	RA3 can also be analog input3 or positive analog reference voltage.
RA4/T0CKI	6	7	23	I/O	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/$\overline{\text{SS}}$/AN4	7	8	24	I/O	TTL	RA5 can also be analog input4 or the slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST(1)	RB0 can also be the external interrupt pin.
RB1	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3/PGM	36	39	11	I/O	TTL	RB3 can also be the low voltage programming input.
RB4	37	41	14	I/O	TTL	Interrupt-on-change pin.
RB5	38	42	15	I/O	TTL	Interrupt-on-change pin.
RB6/PGC	39	43	16	I/O	TTL/ST(2)	Interrupt-on-change pin or In-Circuit Debugger pin. Serial programming clock.
RB7/PGD	40	44	17	I/O	TTL/ST(2)	Interrupt-on-change pin or In-Circuit Debugger pin. Serial programming data.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

4: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

TABLE 1-2: PIC16F874 AND PIC16F877 PINOUT DESCRIPTION (CONTINUED)

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
						PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	15	16	32	I/O	ST	RC0 can also be the Timer1 oscillator output or a Timer1 clock input.
RC1/T1OSI/CCP2	16	18	35	I/O	ST	RC1 can also be the Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output.
RC2/CCP1	17	19	36	I/O	ST	RC2 can also be the Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3 can also be the synchronous serial clock input/output for both SPI and I^{2}C modes.
RC4/SDI/SDA	23	25	42	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^{2}C mode).
RC5/SDO	24	26	43	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK	25	27	44	I/O	ST	RC6 can also be the USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	26	29	1	I/O	ST	RC7 can also be the USART Asynchronous Receive or Synchronous Data.
						PORTD is a bi-directional I/O port or parallel slave port when interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	I/O	ST/TTL(3)	
RD1/PSP1	20	22	39	I/O	ST/TTL(3)	
RD2/PSP2	21	23	40	I/O	ST/TTL(3)	
RD3/PSP3	22	24	41	I/O	ST/TTL(3)	
RD4/PSP4	27	30	2	I/O	ST/TTL(3)	
RD5/PSP5	28	31	3	I/O	ST/TTL(3)	
RD6/PSP6	29	32	4	I/O	ST/TTL(3)	
RD7/PSP7	30	33	5	I/O	ST/TTL(3)	
						PORTE is a bi-directional I/O port.
RE0/$\overline{\text{RD}}$/AN5	8	9	25	I/O	ST/TTL(3)	RE0 can also be read control for the parallel slave port, or analog input5.
RE1/$\overline{\text{WR}}$/AN6	9	10	26	I/O	ST/TTL(3)	RE1 can also be write control for the parallel slave port, or analog input6.
RE2/$\overline{\text{CS}}$/AN7	10	11	27	I/O	ST/TTL(3)	RE2 can also be select control for the parallel slave port, or analog input7.
VSS	12,31	13,34	6,29	P	—	Ground reference for logic and I/O pins.
VDD	11,32	12,35	7,28	P	—	Positive supply for logic and I/O pins.
NC	—	1,17,28, 40	12,13, 33,34		—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

4: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 2-1.

The Special Function Registers can be classified into two sets: core (CPU) and peripheral. Those registers associated with the core functions are described in detail in this section. Those related to the operation of the peripheral features are described in detail in the peripheral features section.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:
Bank 0											
00h(3)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	27
01h	TMR0	Timer0 Module Register								xxxx xxxx	47
02h(3)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	26
03h(3)	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	18
04h(3)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	27
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--0x 0000	29
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	31
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	33
08h(4)	PORTD	PORTD Data Latch when written: PORTD pins when read								xxxx xxxx	35
09h(4)	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	36
0Ah(1,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	26
0Bh(3)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	20
0Ch	PIR1	PSPIF(3)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	22
0Dh	PIR2	—	(5)	—	EEIF	BCLIF	—	—	CCP2IF	-r-0 0--0	24
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	52
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	52
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	51
11h	TMR2	Timer2 Module Register								0000 0000	55
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	55
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	70, 73
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	67
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								xxxx xxxx	57
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								xxxx xxxx	57
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	58
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	96
19h	TXREG	USART Transmit Data Register								0000 0000	99
1Ah	RCREG	USART Receive Data Register								0000 0000	101
1Bh	CCPR2L	Capture/Compare/PWM Register2 (LSB)								xxxx xxxx	57
1Ch	CCPR2H	Capture/Compare/PWM Register2 (MSB)								xxxx xxxx	57
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	58
1Eh	ADRESH	A/D Result Register High Byte								xxxx xxxx	116
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON	0000 00-0	111

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

2: Bits PSPIE and PSPIF are reserved on PIC16F873/876 devices; always maintain these bits clear.

3: These registers can be addressed from any bank.

4: PORTD, PORTE, TRISD, and TRISE are not physically implemented on PIC16F873/876 devices; read as '0'.

5: PIR2<6> and PIE2<6> are reserved on these devices; always maintain these bits clear.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:
Bank 1											
80h[3]	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	27
81h	OPTION_REG	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	19
82h[3]	PCL	Program Counter (PC) Least Significant Byte								0000 0000	26
83h[3]	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	18
84h[3]	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	27
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	29
86h	TRISB	PORTB Data Direction Register								1111 1111	31
87h	TRISC	PORTC Data Direction Register								1111 1111	33
88h[4]	TRISD	PORTD Data Direction Register								1111 1111	35
89h[4]	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111	37
8Ah[1,3]	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	26
8Bh[3]	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	20
8Ch	PIE1	PSPIE[2]	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	21
8Dh	PIE2	—	(5)	—	EEIE	BCLIE	—	—	CCP2IE	-r-0 0--0	23
8Eh	PCON	—	—	—	—	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	---- --qq	25
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	68
92h	PR2	Timer2 Period Register								1111 1111	55
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	73, 74
94h	SSPSTAT	SMP	CKE	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	UA	BF	0000 0000	66
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	95
99h	SPBRG	Baud Rate Generator Register								0000 0000	97
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	ADRESL	A/D Result Register Low Byte								xxxx xxxx	116
9Fh	ADCON1	ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0	0--- 0000	112

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

2: Bits PSPIE and PSPIF are reserved on PIC16F873/876 devices; always maintain these bits clear.

3: These registers can be addressed from any bank.

4: PORTD, PORTE, TRISD, and TRISE are not physically implemented on PIC16F873/876 devices; read as '0'.

5: PIR2<6> and PIE2<6> are reserved on these devices; always maintain these bits clear.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:
Bank 2											
100h(3)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	27
101h	TMR0	Timer0 Module Register								xxxx xxxx	47
102h(3)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	26
103h(3)	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	18
104h(3)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	27
105h	—	Unimplemented								—	—
106h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	31
107h	—	Unimplemented								—	—
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah(1,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	26
10Bh(3)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	20
10Ch	EEDATA	EEPROM Data Register Low Byte								xxxx xxxx	41
10Dh	EEADR	EEPROM Address Register Low Byte								xxxx xxxx	41
10Eh	EEDATH	—	—	EEPROM Data Register High Byte						xxxx xxxx	41
10Fh	EEADRH	—	—	—	EEPROM Address Register High Byte					xxxx xxxx	41
Bank 3											
180h(3)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	27
181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	19
182h(3)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	26
183h(3)	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	18
184h(3)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	27
185h	—	Unimplemented								—	—
186h	TRISB	PORTB Data Direction Register								1111 1111	31
187h	—	Unimplemented								—	—
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah(1,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	26
18Bh(3)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	20
18Ch	EECON1	EEPGD	—	—	—	WRERR	WREN	WR	RD	x--- x000	41, 42
18Dh	EECON2	EEPROM Control Register2 (not a physical register)								---- ----	41
18Eh	—	Reserved maintain clear								0000 0000	—
18Fh	—	Reserved maintain clear								0000 0000	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

2: Bits PSPIE and PSPIF are reserved on PIC16F873/876 devices; always maintain these bits clear.

3: These registers can be addressed from any bank.

4: PORTD, PORTE, TRISD, and TRISE are not physically implemented on PIC16F873/876 devices; read as '0'.

5: PIR2<6> and PIE2<6> are reserved on these devices; always maintain these bits clear.

2.2.2.1 STATUS Register

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are not writable, therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions not affecting any status bits, see the "Instruction Set Summary."

Note: The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

REGISTER 2-1: STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C
bit 7							bit 0

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
`1` = Bank 2, 3 (100h - 1FFh)
`0` = Bank 0, 1 (00h - FFh)

bit 6-5 **RP1:RP0**: Register Bank Select bits (used for direct addressing)
`11` = Bank 3 (180h - 1FFh)
`10` = Bank 2 (100h - 17Fh)
`01` = Bank 1 (80h - FFh)
`00` = Bank 0 (00h - 7Fh)
Each bank is 128 bytes

bit 4 **$\overline{\text{TO}}$**: Time-out bit
`1` = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
`0` = A WDT time-out occurred

bit 3 **$\overline{\text{PD}}$**: Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2 **Z**: Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC**: Digit carry/$\overline{\text{borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
(for $\overline{\text{borrow}}$, the polarity is reversed)
`1` = A carry-out from the 4th low order bit of the result occurred
`0` = No carry-out from the 4th low order bit of the result

bit 0 **C**: Carry/$\overline{\text{borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
`1` = A carry-out from the Most Significant bit of the result occurred
`0` = No carry-out from the Most Significant bit of the result occurred

Note: For $\overline{\text{borrow}}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high, or low order bit of the source register.

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR
'1' = Bit is set
'0' = Bit is cleared
x = Bit is unknown

2.2.2.2 OPTION_REG Register

The OPTION_REG Register is a readable and writable register, which contains various control bits to configure the TMR0 prescaler/WDT postscaler (single assignable register known also as the prescaler), the External INT Interrupt, TMR0 and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

REGISTER 2-2: OPTION_REG REGISTER (ADDRESS 81h, 181h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7 **$\overline{\text{RBPU}}$:** PORTB Pull-up Enable bit
`1` = PORTB pull-ups are disabled
`0` = PORTB pull-ups are enabled by individual port latch values

bit 6 **INTEDG**: Interrupt Edge Select bit
`1` = Interrupt on rising edge of RB0/INT pin
`0` = Interrupt on falling edge of RB0/INT pin

bit 5 **T0CS**: TMR0 Clock Source Select bit
`1` = Transition on RA4/T0CKI pin
`0` = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE**: TMR0 Source Edge Select bit
`1` = Increment on high-to-low transition on RA4/T0CKI pin
`0` = Increment on low-to-high transition on RA4/T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit
`1` = Prescaler is assigned to the WDT
`0` = Prescaler is assigned to the Timer0 module

bit 2-0 **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
`000`	1 : 2	1 : 1
`001`	1 : 4	1 : 2
`010`	1 : 8	1 : 4
`011`	1 : 16	1 : 8
`100`	1 : 32	1 : 16
`101`	1 : 64	1 : 32
`110`	1 : 128	1 : 64
`111`	1 : 256	1 : 128

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Note: When using low voltage ICSP programming (LVP) and the pull-ups on PORTB are enabled, bit 3 in the TRISB register must be cleared to disable the pull-up on RB3 and ensure the proper operation of the device

2.2.2.3 INTCON Register

The INTCON Register is a readable and writable register, which contains various enable and flag bits for the TMR0 register overflow, RB Port change and External RB0/INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit 7							bit 0

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE**: Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE**: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4 **INTE**: RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3 **RBIE**: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2 **T0IF**: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INTF**: RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0 **RBIF**: RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state; a mismatch condition will continue to set the bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared (must be cleared in software).
0 = None of the RB7:RB4 pins have changed state

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

2.2.2.4 PIE1 Register

The PIE1 register contains the individual enable bits for the peripheral interrupts.

Note:	Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

REGISTER 2-4: PIE1 REGISTER (ADDRESS 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIE[1]	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

bit 7 **PSPIE[1]**: Parallel Slave Port Read/Write Interrupt Enable bit
1 = Enables the PSP read/write interrupt
0 = Disables the PSP read/write interrupt

bit 6 **ADIE**: A/D Converter Interrupt Enable bit
1 = Enables the A/D converter interrupt
0 = Disables the A/D converter interrupt

bit 5 **RCIE**: USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt

bit 4 **TXIE**: USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 3 **SSPIE**: Synchronous Serial Port Interrupt Enable bit
1 = Enables the SSP interrupt
0 = Disables the SSP interrupt

bit 2 **CCP1IE**: CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1 **TMR2IE**: TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

bit 0 **TMR1IE**: TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

Note 1: PSPIE is reserved on PIC16F873/876 devices; always maintain this bit clear.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.2.2.5 PIR1 Register

The PIR1 register contains the individual flag bits for the peripheral interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt bits are clear prior to enabling an interrupt.

REGISTER 2-5: PIR1 REGISTER (ADDRESS 0Ch)

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF[(1)]	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

bit 7 **PSPIF[(1)]**: Parallel Slave Port Read/Write Interrupt Flag bit
1 = A read or a write operation has taken place (must be cleared in software)
0 = No read or write has occurred

bit 6 **ADIF**: A/D Converter Interrupt Flag bit
1 = An A/D conversion completed
0 = The A/D conversion is not complete

bit 5 **RCIF**: USART Receive Interrupt Flag bit
1 = The USART receive buffer is full
0 = The USART receive buffer is empty

bit 4 **TXIF**: USART Transmit Interrupt Flag bit
1 = The USART transmit buffer is empty
0 = The USART transmit buffer is full

bit 3 **SSPIF**: Synchronous Serial Port (SSP) Interrupt Flag
1 = The SSP interrupt condition has occurred, and must be cleared in software before returning from the Interrupt Service Routine. The conditions that will set this bit are:

- SPI
  - A transmission/reception has taken place.
- I²C Slave
  - A transmission/reception has taken place.
- I²C Master
  - A transmission/reception has taken place.
  - The initiated START condition was completed by the SSP module.
  - The initiated STOP condition was completed by the SSP module.
  - The initiated Restart condition was completed by the SSP module.
  - The initiated Acknowledge condition was completed by the SSP module.
  - A START condition occurred while the SSP module was idle (Multi-Master system).
  - A STOP condition occurred while the SSP module was idle (Multi-Master system).

0 = No SSP interrupt condition has occurred.

bit 2 **CCP1IF**: CCP1 Interrupt Flag bit
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM mode:
Unused in this mode

bit 1 **TMR2IF**: TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

bit 0 **TMR1IF**: TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

Note 1: PSPIF is reserved on PIC16F873/876 devices; always maintain this bit clear.

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR
'1' = Bit is set
'0' = Bit is cleared
x = Bit is unknown

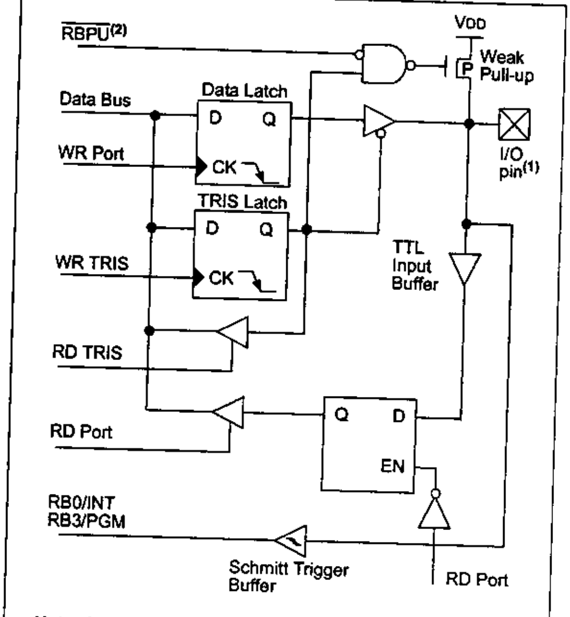
3.2 PORTB and the TRISB Register

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

Three pins of PORTB are multiplexed with the Low Voltage Programming function: RB3/PGM, RB6/PGC and RB7/PGD. The alternate functions of these pins are described in the Special Features Section.

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

FIGURE 3-3: BLOCK DIAGRAM OF RB3:RB0 PINS



Note 1: I/O pins have diode protection to VDD and VSS.

2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit (OPTION_REG<7>).

Four of the PORTB pins, RB7:RB4, have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.

b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

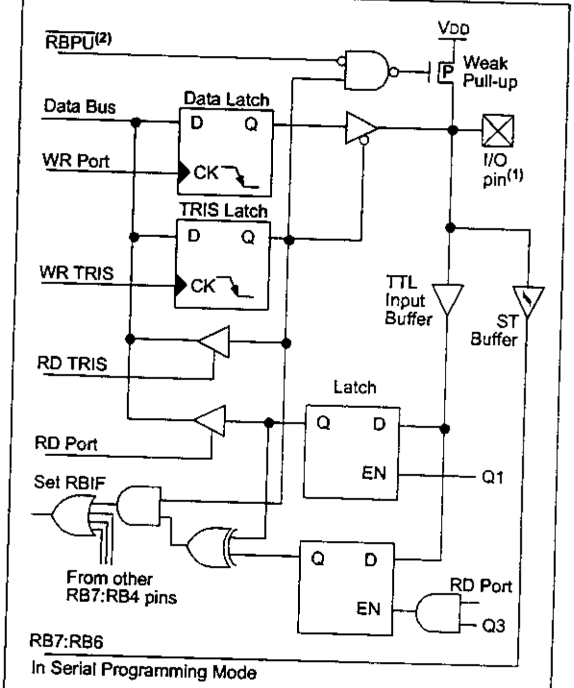
The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

This interrupt-on-mismatch feature, together with software configureable pull-ups on these four pins, allow easy interface to a keypad and make it possible for wake-up on key depression. Refer to the Embedded Control Handbook, *"Implementing Wake-up on Key Strokes"* (AN552).

RB0/INT is an external interrupt input pin and is configured using the INTEDG bit (OPTION_REG<6>).

RB0/INT is discussed in detail in Section 12.10.1.

FIGURE 3-4: BLOCK DIAGRAM OF RB7:RB4 PINS



Note 1: I/O pins have diode protection to VDD and VSS.

2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit (OPTION_REG<7>).

TABLE 3-3: PORTB FUNCTIONS

Name	Bit#	Buffer	Function
RB0/INT	bit0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3/PGM(3)	bit3	TTL	Input/output pin or programming pin in LVP mode. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6/PGC	bit6	TTL/ST(2)	Input/output pin (with interrupt-on-change) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming clock.
RB7/PGD	bit7	TTL/ST(2)	Input/output pin (with interrupt-on-change) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: Low Voltage ICSP Programming (LVP) is enabled by default, which disables the RB3 I/O function. LVP must be disabled to enable RB3 as an I/O pin and allow maximum compatibility to the other 28-pin and 40-pin mid-range devices.

TABLE 3-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	`xxxx xxxx`	`uuuu uuuu`
86h, 186h	TRISB	PORTB Data Direction Register								`1111 1111`	`1111 1111`
81h, 181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	`1111 1111`	`1111 1111`

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

3.3 PORTC and the TRISC Register

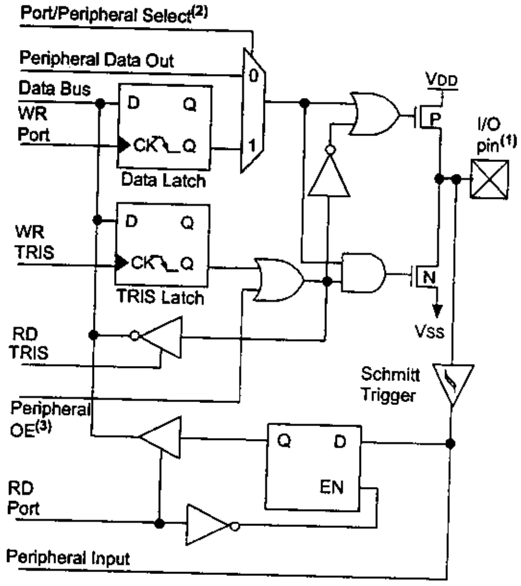
PORTC is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISC. Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin).

PORTC is multiplexed with several peripheral functions (Table 3-5). PORTC pins have Schmitt Trigger input buffers.

When the I^{2}C module is enabled, the PORTC<4:3> pins can be configured with normal I^{2}C levels, or with SMBus levels by using the CKE bit (SSPSTAT<6>).

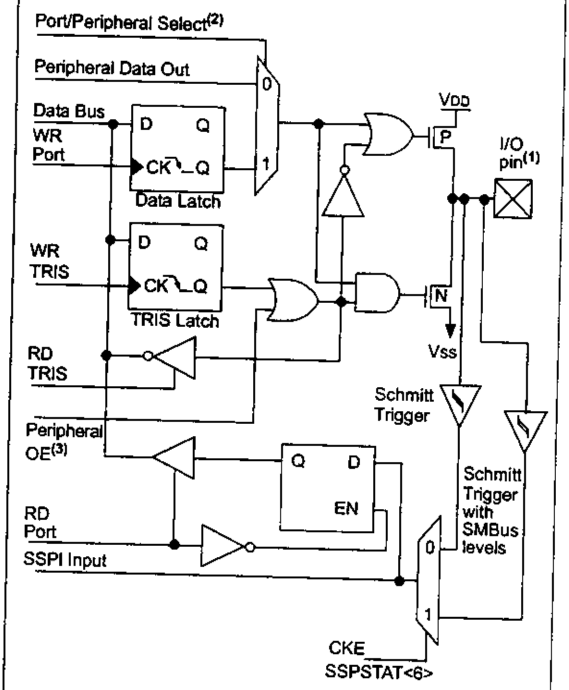
When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (`BSF`, `BCF`, `XORWF`) with TRISC as destination, should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

FIGURE 3-5: PORTC BLOCK DIAGRAM (PERIPHERAL OUTPUT OVERRIDE) RC<2:0>, RC<7:5>



Note 1: I/O pins have diode protection to VDD and Vss.
2: Port/Peripheral select signal selects between port data and peripheral output.
3: Peripheral OE (output enable) is only activated if peripheral select is active.

FIGURE 3-6: PORTC BLOCK DIAGRAM (PERIPHERAL OUTPUT OVERRIDE) RC<4:3>



Note 1: I/O pins have diode protection to VDD and Vss.
2: Port/Peripheral select signal selects between port data and peripheral output.
3: Peripheral OE (output enable) is only activated if peripheral select is active.

TABLE 3-5: PORTC FUNCTIONS

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input.
RC1/T1OSI/CCP2	bit1	ST	Input/output port pin or Timer1 oscillator input or Capture2 input/ Compare2 output/PWM2 output.
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/ PWM1 output.
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I^2C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	bit5	ST	Input/output port pin or Synchronous Serial Port data output.
RC6/TX/CK	bit6	ST	Input/output port pin or USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	bit7	ST	Input/output port pin or USART Asynchronous Receive or Synchronous Data.

Legend: ST = Schmitt Trigger input

TABLE 3-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	`xxxx xxxx`	`uuuu uuuu`
87h	TRISC	PORTC Data Direction Register								`1111 1111`	`1111 1111`

Legend: x = unknown, u = unchanged

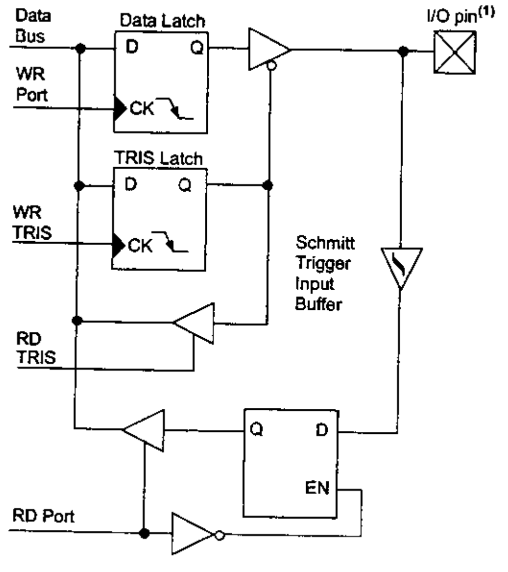
3.4 PORTD and TRISD Registers

PORTD and TRISD are not implemented on the PIC16F873 or PIC16F876.

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configureable as an input or output.

PORTD can be configured as an 8-bit wide microprocessor port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

FIGURE 3-7: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)



Note 1: I/O pins have protection diodes to VDD and VSS.

TABLE 3-7: PORTD FUNCTIONS

Name	Bit#	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL(1)	Input/output port pin or parallel slave port bit0.
RD1/PSP1	bit1	ST/TTL(1)	Input/output port pin or parallel slave port bit1.
RD2/PSP2	bit2	ST/TTL(1)	Input/output port pin or parallel slave port bit2.
RD3/PSP3	bit3	ST/TTL(1)	Input/output port pin or parallel slave port bit3.
RD4/PSP4	bit4	ST/TTL(1)	Input/output port pin or parallel slave port bit4.
RD5/PSP5	bit5	ST/TTL(1)	Input/output port pin or parallel slave port bit5.
RD6/PSP6	bit6	ST/TTL(1)	Input/output port pin or parallel slave port bit6.
RD7/PSP7	bit7	ST/TTL(1)	Input/output port pin or parallel slave port bit7.

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port mode.

TABLE 3-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
08h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
88h	TRISD	PORTD Data Direction Register								1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTD.

3.5 PORTE and TRISE Register

PORTE and TRISE are not implemented on the PIC16F873 or PIC16F876.

PORTE has three pins (RE0/$\overline{\text{RD}}$/AN5, RE1/$\overline{\text{WR}}$/AN6, and RE2/$\overline{\text{CS}}$/AN7) which are individually configureable as inputs or outputs. These pins have Schmitt Trigger input buffers.

The PORTE pins become the I/O control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make certain that the TRISE<2:0> bits are set, and that the pins are configured as digital inputs. Also ensure that ADCON1 is configured for digital I/O. In this mode, the input buffers are TTL.

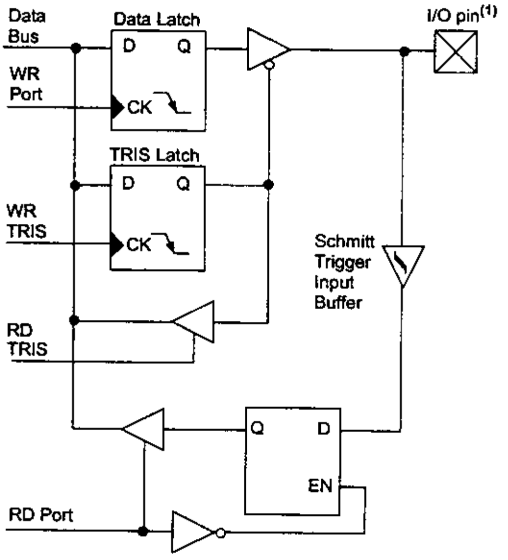
Register 3-1 shows the TRISE register, which also controls the parallel slave port operation.

PORTE pins are multiplexed with analog inputs. When selected for analog input, these pins will read as '0's.

TRISE controls the direction of the RE pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.

Note: On a Power-on Reset, these pins are configured as analog inputs, and read as '0'.

FIGURE 3-8: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)



Note 1: I/O pins have protection diodes to VDD and VSS.

TABLE 3-9: PORTE FUNCTIONS

Name	Bit#	Buffer Type	Function
RE0/$\overline{\text{RD}}$/AN5	bit0	ST/TTL(1)	I/O port pin or read control input in Parallel Slave Port mode or analog input: $\overline{\text{RD}}$ 1 = Idle 0 = Read operation. Contents of PORTD register are output to PORTD I/O pins (if chip selected)
RE1/$\overline{\text{WR}}$/AN6	bit1	ST/TTL(1)	I/O port pin or write control input in Parallel Slave Port mode or analog input: $\overline{\text{WR}}$ 1 = Idle 0 = Write operation. Value of PORTD I/O pins is latched into PORTD register (if chip selected)
RE2/$\overline{\text{CS}}$/AN7	bit2	ST/TTL(1)	I/O port pin or chip select control input in Parallel Slave Port mode or analog input: $\overline{\text{CS}}$ 1 = Device is not selected 0 = Device is selected

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port mode.

TABLE 3-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
09h	PORTE	—	—	—	—	—	RE2	RE1	RE0	`---- -xxx`	`---- -uuu`
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			`0000 -111`	`0000 -111`
9Fh	ADCON1	ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0	`--0- 0000`	`--0- 0000`

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTE.

REGISTER 3-1: TRISE REGISTER (ADDRESS 89h)

R-0	R-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
IBF	OBF	IBOV	PSPMODE	—	Bit2	Bit1	Bit0
bit 7							bit 0

Parallel Slave Port Status/Control Bits:

bit 7 **IBF:** Input Buffer Full Status bit

1 = A word has been received and is waiting to be read by the CPU
0 = No word has been received

bit 6 **OBF:** Output Buffer Full Status bit

1 = The output buffer still holds a previously written word
0 = The output buffer has been read

bit 5 **IBOV:** Input Buffer Overflow Detect bit (in Microprocessor mode)

1 = A write occurred when a previously input word has not been read (must be cleared in software)
0 = No overflow occurred

bit 4 **PSPMODE:** Parallel Slave Port Mode Select bit

1 = PORTD functions in Parallel Slave Port mode
0 = PORTD functions in general purpose I/O mode

bit 3 **Unimplemented:** Read as '0'

PORTE Data Direction Bits:

bit 2 **Bit2:** Direction Control bit for pin RE2/$\overline{\text{CS}}$/AN7

1 = Input
0 = Output

bit 1 **Bit1:** Direction Control bit for pin RE1/$\overline{\text{WR}}$/AN6

1 = Input
0 = Output

bit 0 **Bit0:** Direction Control bit for pin RE0/$\overline{\text{RD}}$/AN5

1 = Input
0 = Output

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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APPENDIX 1

CIRCUIT LAY-OUT