



**AUTOMATIC POWER FACTOR CORRECTION CONTROLLER
FOR INDUSTRIAL MACHINES**

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COIMBATORE**

A PROJECT REPORT
Submitted to the

**FACULTY OF ELECTRICAL & ELECTRONICS
ENGINEERING**

*In partial fulfillment of the requirements
for the award of the degree*

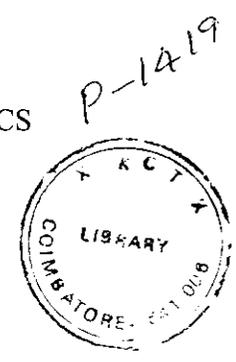
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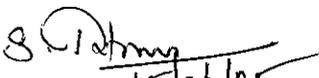
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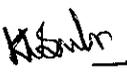
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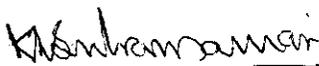
BONAFIDE CERTIFICATE

Certified that this project report titled **AUTOMATIC POWERFACTOR CORRECTION CONTROLLER FOR INDUSTRIAL MACHINES** is the bonafide work of **Mr. J.SATISH BABU** who carried out the research under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other project report or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.


 PROJECT GUIDE


 HEAD OF THE DEPARTMENT

The Candidate with University Register No: 71203415019 was examined by us in the project Viva-Voce examination held on 22.06.2008


 INTERNAL EXAMINER


 EXTERNAL EXAMINER



LAKSHMI ELECTRICAL CONTROL SYSTEMS LIMITED

2-5-2005

TO WHOMSOEVER IT MAY CONCERN

This is to certify that Mr. J. Sathish Babu, Roll No. 71203415014, Final Year M.E. (Power Electronics and Drives) student of Kumaraguru College of Technology, Coimbatore has done a project on "Automatic Powerfactor Correction Controller for Industrial machines" in our organisation.

We found his performance and conduct highly commendable.

For LAKSHMI ELECTRICAL CONTROL SYSTEMS LIMITED


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Manager-HRD

ABSTRACT

Pure sinusoidal voltage curves do not occur in distribution networks. Because neither generator is able to generate them nor a transformer able to transmit them in a linear manner because of its magnetic rating. Normally in industries power factor is low due to inductive nature of the load which takes lagging power factor. Operating plant in low power factor causes loss of revenue directly because of high electricity bills and indirectly by reducing the efficiency and capacity of the plant which in turn affects the productivity of the equipment it serves. In order to improve power factor some devices taking leading current like static capacitors, synchronous condensers, phase advancers should be connected in parallel with the load.

In this project improvement of power factor is automatically done by using a RISC processor such as the PIC16F877 for controlling the capacitor banks by means of contactors in order to achieve powerfactor close to unity along with the display of various parameters and with optional features such as the second target power factor selection.

ACKNOWLEDGEMENT

First and foremost, I would like to extend my heart-felt gratitude and thanks to our beloved Principal of **Kumaraguru College of Technology, Dr.K.K.PADMANABHAN** for his unclenching support while doing the project.

I wish to record my heartfelt thanks to our H.O.D **Prof. REGUPATHY SUBRAMANIAM** for his valuable guidance and persistent encouragement extended by him throughout the execution of the project work.

I am indeed thankful to the organization of **LAKSHMI ELECTRICAL CONTROL SYSTEMS Ltd**, Arasur, Coimbatore for granting us permission to do our project in their centre and for providing all the facilities. A special motto of thanks goes to our external guide **Mr.V.SHANKAR**, R & D Engineer, LECS Ltd, Coimbatore who took pains in guiding me towards the successful completion of this project.

Heart of my project is my project guide **Mr.S.TITUS M.E.**, Lecturer, Department of Electrical and Electronics Engineering, for his continuous guidance, motivation and the much needed technical support extended for me to complete the project.

I am also indebted to **Dr. T.M.KAMESWARAN**, our Project Co-ordinator **Mrs. R. MAHALAKSHMI M.E.**, our class Advisor **Mrs. N. KALAIARASI M.E.**, for the helping hand they extended during trying periods while doing the project.

COMPANY PROFILE

The company LAKSHMI ELECTRICAL CONTROL SYSTEMS, Coimbatore, a public limited company more popularly recognized as LECS was set up in the year 1981. LECS is a part of 1000 crore LMW group which is the third largest manufacturers of textile machinery in the world. LMW group is known for its quality of products and fine engineering practices

The manufacturing products of LECS are switchgears, control panels for textile machines, plastic components, CNC systems, DOL starters, star-delta starters, motor panels, contactors, limit switches and relays.

- **Achievements**

High productivity and profit based on re-engineering concepts.

Any type of panel boards can be designed.

ISO 9001/ 9002 accreditation

10% of low voltage switchgears are marketed in India.

- **Quality Policy**

LECS provides value and satisfaction to the customer specifications and requirements, baked by optimum after sales and services. This is achieved through a systematic training , development, and excellent motivation of the employees. To this end the company has established and is maintaining quality systems on documented policy.

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LIST OF ABBREVIATIONS AND SYMBOLS

AC	-	Alternating Current
DC	-	Direct Current
F	-	Frequency
V	-	Voltage
I	-	Current
P	-	Real Power
Q	-	Reactive power
S	-	Apparent power
W	-	Watt
VAR	-	Volt Ampere Reactive
VA	-	Volt Ampere
HP	-	Horse Power
Pf	-	Power Factor
APFC	-	Automatic Power Factor Correction
APFCC	-	Automatic Power Factor Correction Controller
PCC	-	Point of Common Coupling
MCCB	-	Maximum Current Circuit Breaker
MCB	-	Miniature Circuit Breaker
ZCD	-	Zero Crossing Detector
PT	-	Potential Transformer
CT	-	Current Transformer
EMF	-	Electro Magnetic Flux
PIC	-	Peripheral Interface Controller
RISC	-	Reduced Instruction Set Computer
ADC	-	Analog to Digital Converter
RAM	-	Random Access Memory
PROM	-	Programmable Read Only Memory

ROM	-	Read Only Memory
EEPROM	-	Electrically Erasable Programmable Read Only Memory
IC	-	Integrated Circuits
LCD	-	Liquid Crystal Display
EOC	-	End Of Conversion
SOC	-	Start Of Conversion
FIFO	-	First In First Out
LIFO	-	Last In First Out
Φ	-	Power factor angle
Φ_1	-	Target power factor
Φ_2	-	Existing power factor

CHAPTER 1

1.1 INTRODUCTION

Normally the electrical energy is almost exclusively generated, transmitted and distributed in the form of alternating current. Most of the loads (e.g., induction motor arc lamps) are inductive in nature and hence have lagging power factor. The low power factor is highly undesirable as it causes an increase in current, resulting in additional losses of power in all the elements of power system from power station generator down to the utilization devices. In order to ensure most favorable stand point, it is important to have power factor as close to unity as possible. The automatic power factor correction controllers for power factor correction in low-voltage systems measure the actual power factor and connect or disconnect capacitors to achieve a certain desired value $\cos\Phi$. The single-phase measuring system detects the active and reactive component of the network. From this it calculates the phase shift between the fundamentals of current and voltage and compares this to the set target power factor. If there are deviations of the power factor, capacitor stages are switched in or out by the controller and this process is done with the help of a RISC processor such as the PIC 16F877 controller through contactors. The relay will automatically select from its memory the most appropriate capacitor step size to meet the required load demand. Here the second target power factor is also considered in case if the power is from auxiliary sources such as the generators.

1.2 OUTLINE OF THE PROJECT

Chapter 1: Gives a general introduction about the need for power factor correction.

Chapter 2: It deals with the various parameters associated with power factor correction and the methods to achieve it.

Chapter 3: It deals with the technical design aspects and hardware configurations of the automatic power factor correction controller.

Chapter 4: Here how phase detection is carried out using digital phase detection is well explained.

Chapter 5: It contains the simulation results and test reports performed with APFC Controller.

Chapter 6: It contains the special features of the PIC 16F877 controller and the algorithms needed for software coding.

Chapter 7: Conclusion and scope for future work.

CHAPTER: 2

GENERAL CONCEPTS

2.1. POWER FACTOR

- Power factor is also defined as the ratio of real power to the apparent power.

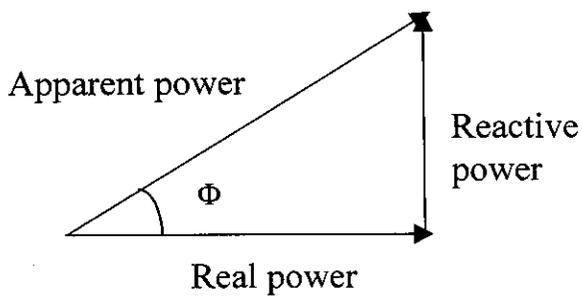


Figure 2.1 Power triangle

- Power Factor (PF) is defined as the cosine of the angle between the voltage and the current.

$$\text{Cos } \Phi = \text{Real power} / \text{Apparent power}$$

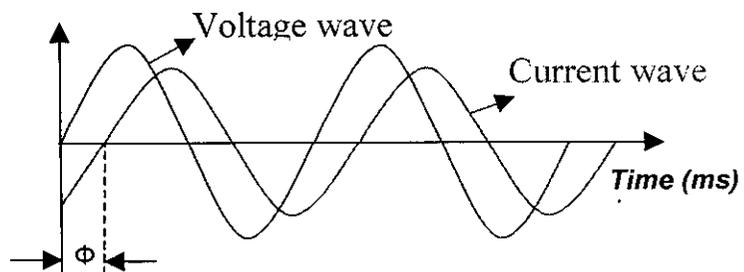


Fig (ii): Measurement of phase angle

$$\text{Power factor} = \text{cos}\Phi$$

2.2. COMPONENTS OF POWER

2.2.1 Active power

The amount of input power converted into output power is termed active power and generally indicated by P in watts (W) and defined by the following formula:

$$P = \sqrt{3}VI\cos\Phi \text{ [W]}$$

The entire input power, e.g. apparent power should be converted into useful output power stated as active power, e.g. the real motor output.

2.2.2 Reactive power

Electrical machines work on the principle of conversion of electromagnetic energy (e.g. electric motors, transformers). Part of the input energy is consumed to create and maintain the magnetic field. Inductive consumers shift the angle between voltage and current (to a value > 0). Power created by portions of V and I waveforms having opposite directions (+ and -) is called reactive power. This part of the energy (magnetic reversal energy), defined as reactive power Q in volt ampere reactive [var], cannot be converted into active power and is returned to the electrical supply network during changes in the magnetic field. But the same amount of energy will be consumed by the network again and required for the next change in the magnetic field.

$$Q = \sqrt{3}VI\sin\Phi \text{ [var]}$$

2.2.3 Apparent power

In principle, applications of electrical equipment are based on conversion of electrical energy into some other form of energy. The electrical

power drawn by equipment from the source is termed as apparent power, indicated by S in volt ampere [VA], and consists of active and reactive power,

$$S = \sqrt{3}VI \quad [\text{VA}]$$

2.3. NEED TO CONTROL THE POWER FACTOR

Consider the following general power equation in an electrical circuit at the constant voltage (5V) and the constant power (10kW). Assume the power factor is unity in the first case and is 0.5 in the second case.

$$P = V I \cos\Phi$$

$$10 = 5 * 2 * 1 \text{ (case 1, when power factor is unity)}$$

$$10 = 5 * 4 * 0.5 \text{ (case 2, when power factor is only 0.5)}$$

It is evident that when the power factor reduced from 1 to 0.5, the current in the system doubles for the same power and the voltage (In all systems the real power remains the same depending on the work to be done and the voltage at which this power is transmitted also remains the same). Increase in current results in large kVA rating of the equipments, greater current size, large copper loss and poor voltage regulation. Since the maximum value of power factor ($\cos\Phi$) can assume is 1, it is clear that any power factor other than unity power factor results in an increase in the current in the system. This is true irrespective of the fact whether the current is leading or lagging (i.e. capacitive or inductive or export or import of reactive power).

2.3.1 Penalty charges

Power consumption charges:

1 – 1500 units = Rs. 4.00/unit

1501 & > = Rs 4.70/unit

Fixed charge bi monthly = Rs. 60.00

Tax = 5%

For 1 kW = Rs. 80.00 (minimum)

2.3.1.1 Penalty

The consumers must pay penalty for operating the equipment in poor power factor ranges specified by the suppliers:

POWER FACTOR	% OF CONSUMPTION CHARGE
0.84	1.0
0.83	2.0
0.82	3.0
0.81	4.0
0.80	5.0
0.79	6.0
0.78	7.0

Table 1.1 Power factor - % of consumption charge

- When power factor is below 0.85 lag and up to 0.77 lag 1% of current consumption charges for every reduction of 0.01 in power factor.
- When the power factor is below 0.75 lag, the charges are 1.5% of consumption charges.

2.3.1.2. Rebate

Industrial consumers have an added advantage when they operate the equipments in high power factor.

POWER FACTOR	% REBATE FROM CONSUMPTION CHARGES
0.93	1.5
0.95	2.5
0.97	3.5
0.98	4.0
0.99	4.5
1.00	5.0

Table 1.2 Power factor - % Rebate

- When power factor exceeds 0.90 lag, a rebate of 0.5% of the current consumption charges for every increase in 0.01 power factor is allowed.

2.4. CAUSES FOR LOW POWER FACTOR

When the power factor is low there will be large current drawn from the mains. This large current due to low PF results in the following drawbacks,

1. Higher energy consumption and high cost.
2. Large KVA rating of equipment.
3. Increased conductor size.
4. Increased copper loss.
5. Poor voltage regulation.
6. Reduced handling capacity of the power system.

2.4.1. Large KVA rating of equipment

The electrical machines are always rated in kVA.

$$\text{kVA} = \text{kW} / \cos \phi$$

It is clear that kVA rating of the equipment is inversely proportional to PF. If the PF is poor the kVA rating will be high. Therefore at low PF, the kVA rating of the equipment has to be increased, making the equipment large and expensive.

2.4.2. Increased conductor size

To transmit or distribute a fixed amount of power at constant voltage, the conductor will have to carry more current at low PF. This leads to large size of the conductor.

2.4.3. Increased copper loss

Since copper loss is proportional to the square of the current, which is inversely proportional to the PF, copper loss is very high for poor PF. This results in poor efficiency of the system.

2.4.4. Poor voltage regulation

If the PF is lagging, the load voltage will be very low and for leading PF the load voltage will be very high. This causes the increase in the percentage of voltage regulation. Generally the load voltage must be maintained between 95% and 105% of the rated voltage.

2.4.5. Reduced handling capacity of the power system

The lagging PF reduces the handling capacity of all the elements of the system, because the reactive component of current prevents the full utilization of installed capacity.

2.5. REACTIVE POWER COMPENSATION

Most of the industries have inductive load, to develop magnetic field in that load some power (reactive power) is needed to produce flux. This reactive power is supplied from the capacitor banks which are connected in parallel with the mains. To calculate the required capacitor reactive power (Q_c) in volt ampere reactive [var], the following formula is used:

$$Q_c = P (\tan\Phi_1 - \tan\Phi_2) \quad [\text{var}]$$

A capacitor of Q_c kvar will compensate the inductive Q and compensate to $\cos\Phi = 1$. It is not common practice to aim for $\cos\Phi = 1$ by installation of capacitors since it may result in overcompensation due to load changes and

response time of the controller. Generally public utilities or power companies specify a value ($\cos\Phi_2$) to which the existing power factor ($\cos\Phi_1$) should be corrected.

The rational use of electrical energy calls for the economical generation, transmission and distribution with little loss. That means restricting all factors in electrical networks that cause losses. One of these factors is lagging reactive power. Consumers in industrial and public electrical networks are primarily of an ohmic- inductive nature.

The purpose of systems for power correction in networks is to compensate the generated lagging reactive power by leading reactive power at defined nodes. In this way impermissibly high voltage drops and additional ohmic losses are also avoided. The necessary leading power is produced by capacitors parallel to the supply network, as close as possible to the inductive consumer.

2.6. METHODS OF IMPROVING POWER FACTOR

Power factor can be improved by the following methods.

2.6.1 By using static capacitors

Capacitors are connected in parallel with the supply mains and take leading current from the mains, which neutralizes reactive lagging component of the load current. The value of the total capacitance required for improving the power factor to unity for given power P in the circuit is at the frequency f , and voltage V is determined as follows,

$$\text{Reactive power to be compensated, } Q_c = P (\tan\phi_1 - \tan\phi_2)$$

If the capacitors are star connected in each stages,

$$\text{Capacitance required, } C = Q_c / (V^2\omega)$$

$$\text{Total Capacitance required} = 3 * C$$

If the capacitors are delta connected in each stages,

$$\text{Capacitance required, } C = Q_c / (3 * V^2 \omega)$$

$$\text{Total Capacitance required} = 3 * C$$

2.6.2 By using synchronous condensers

To achieve easy control of power factor, synchronous condensers are used. Synchronous condenser is a synchronous motor working at over excitation and drawing current from the supply mains at leading power factor. By adjusting the excitation to the field of synchronous motor, the amount of reactive power supplied by the synchronous motor to the supply mains is controlled.

Rotary amplifiers are used to obtain the stable operation even in the case of sudden changes in the system. It is noted that the synchronous condenser has an inherently sinusoidal waveform and the harmonics in the voltage do not exist.

2.6.3 By using the phase advancers

The low power factor of the induction motor is only due to the exciting current required by the stator winding. If this existing current is provided by some other means then the power factor of the induction motor can be improved. The phase advancer is introduced here to serve this purpose. This is an AC exciter. The phase advancer is attached with the rotor of the induction motor. it provides the exciting current to the rotor circuit at the slip frequency. By providing more ampere turns than the required, the induction motor can be brought to work in leading side also as synchronous motor.

The draw back of this system is that this can be applied only for motors with the rating more than 200 HP.

In our project we have used the capacitor bank for the improvement of power factor.

There are two types of methods by using capacitor bank as follows:

- Individual compensation
- Group compensation

2.7 Advantages and disadvantages of the individual and group compensation:

PARAMETER	INDIVIDUAL COMPENSATION SCHEME (on primary secondary and tertiary winding of transformer)	GROUP COMPENSATION SCHEME (at service connection of sub station)
Total size of compensation required	High. As each system has to be provided the full requirement	Low. As there is an averaging effect the total size required is low.
Cost	High. Due to higher size as well as large number of individual controllers (N times fixed cost)	Low. As total compensation required is lower than the sum of requirement for individual system.
Possibility of over compensation.	High. Due to higher size of compensation required. It can be taken care by special controllers and protection schemes.	None. As total compensation required is lower than the sum of requirement for individual system.
Possibility of over excitation and damage to system.	High. As main currents are not sensed and the size of compensation required is high.	None. As the size is small and the main currents are sensed.
Compensation for transformer magnetizing current.	Not possible. As the compensation is on secondary side of the transformer.	Possible. As the compensation is at the point of common coupling (PCC).
Operational ease	Low. Higher maintenance. Costs a large number of systems to be maintained.	High. Lower maintenance costs as a very few systems to be maintained.



CHAPTER 3

3. TECHNICAL DESIGN

3.1. AUTOMATIC POWER FACTOR CORRECTION PANEL

BLOCK DIAGRAM

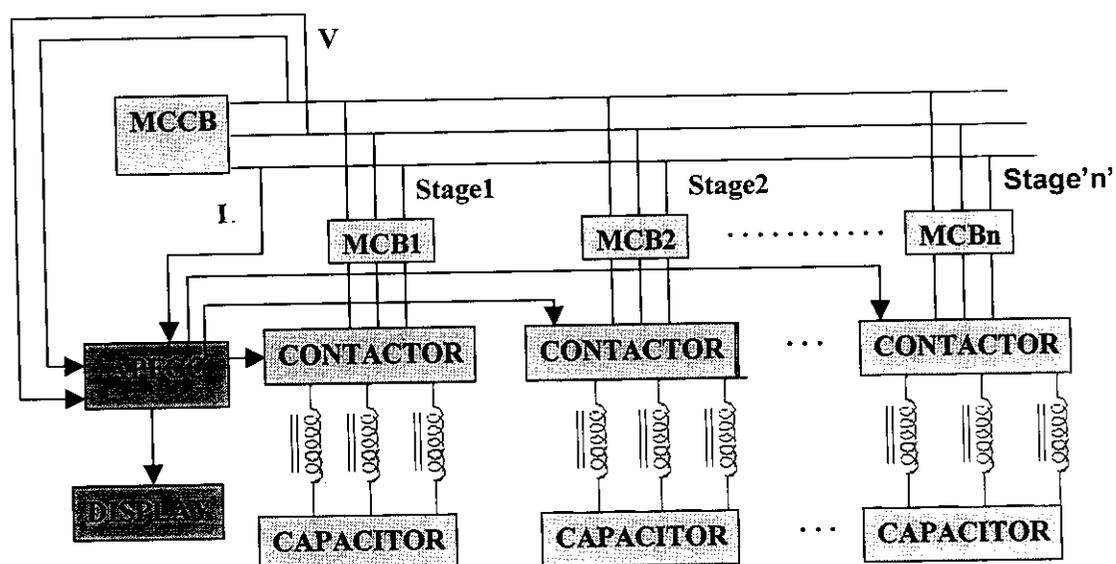


Figure 3.1 Automatic Power factor Correction panel

This diagram shows the components present in the panel. Our part in this panel design is to develop APFCC and the display part.

3.1.1. PROTECTION

In Automatic power factor correction panels, dual protection is provided

- MCCB
- Individual stage MCB's

3.1.1.1. MCCB

Incoming circuit breaker is selected with the tripping characteristics for the individual capacitor circuit as well as multiband parallel switching characteristics.

3.1.1.2. MCB

MCB which has tuned tripping characteristics which ensures the inrush current of the capacitors.

3.1.2. Power Factor Correction Capacitor

Power factor correction capacitors produce the necessary leading reactive power to compensate the lagging reactive power. PFC capacitors should be capable of withstanding high inrush current caused by switching operations. If Capacitors are connected in parallel, i.e. as banks, the inrush currents will increase because the charging current comes from the grid as well as from capacitors connected in parallel is switched on.

3.1.3 Capacitor contactor

Contactors are electromechanical switching elements used to switch capacitors or reactors and capacitors are standard and detuned PFC systems. The switching operations can be performed by mechanical contacts or an electronic switch (semiconductor or the transistors). An electronic switch is preferable if fast switching is required for a sensitive load .

The type of contactor used is 'TYPE – CA3 - _K' for frequent switching of capacitor banks connected in parallel .It is of compact size and can be used to switch ON and OFF a wide range capacitor banks of range 5,10, 15, 20, 25 KVAR .

3.1.3.1 Features of Capacitor contactor

- Controlled switching of capacitors.
- High electrical and mechanical life.
- Ideal for switching a number of capacitors in parallel without derating.

3.1.3.2 Advantages

- Inrush current produced by providing damping resistors results in reduced rating of fuses/ cables and avoid welding during starting.
- Energy in the capacitor discharged through damping resistors results in increased switching frequency of contactors / capacitors.
- Less space required compared to normal contactors.
- Captive screws for easy wiring and reduces installation time.
- Suitable for systems with a number of capacitor banks in parallel (APFC).

3.1.3.3 SCHEMATIC DIAGRAM OF TYPE – CA3 – K CONTACTOR

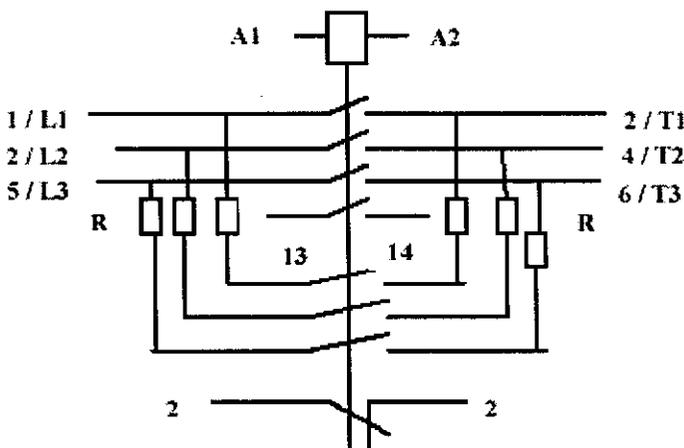


Figure 3.2 TYPE – CA3 – K CONTACTOR

3.1.4 Reactor

Power distribution networks are increasingly subjected to harmonic pollution from modern power electronic devices, so called non-linear loads, e.g. drives, capacitors

connected in the PFC circuit especially if the capacitors operate at resonant frequency. The series connection of reactor and capacitor to detune the series resonant frequency (the capacitor is resonant frequency) helps to prevent capacitor damage. Detuned capacitor banks also help to reduce the harmonic distortion level and clean the network.

3.2 BLOCK DIAGRAM OF APFCC

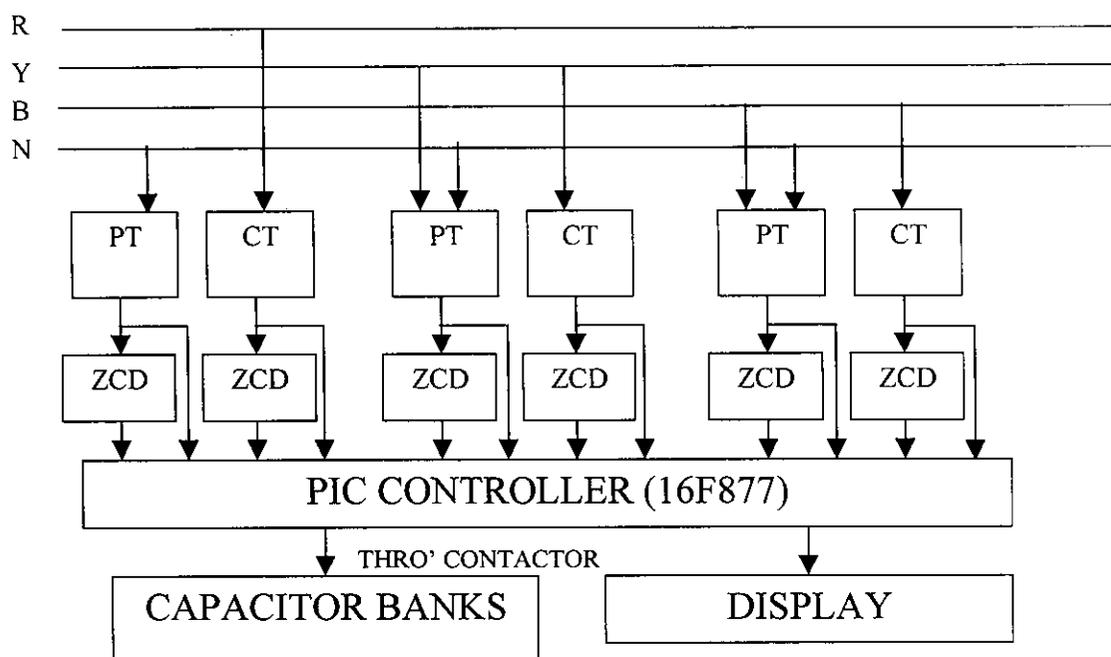


Figure 3.3 Block diagram of APFCC

The block diagram of automatic power factor correction controller block diagram is shown ,

Here the voltage and current from the each phases are measured by using PT and CT. This measured sinusoidal voltage is then converted to square wave using ZCD. This ZCD output is then given to the PIC microcontroller (one phase is given directly to microcontroller and the other two phases is given through the A/D converter). The programming is done in the microcontroller for correcting the power factor and the signal is given to the contactor to switch ON or OFF the capacitor.

3.3 POWER SUPPLY

3.3.1 +5V POWER SUPPLY:

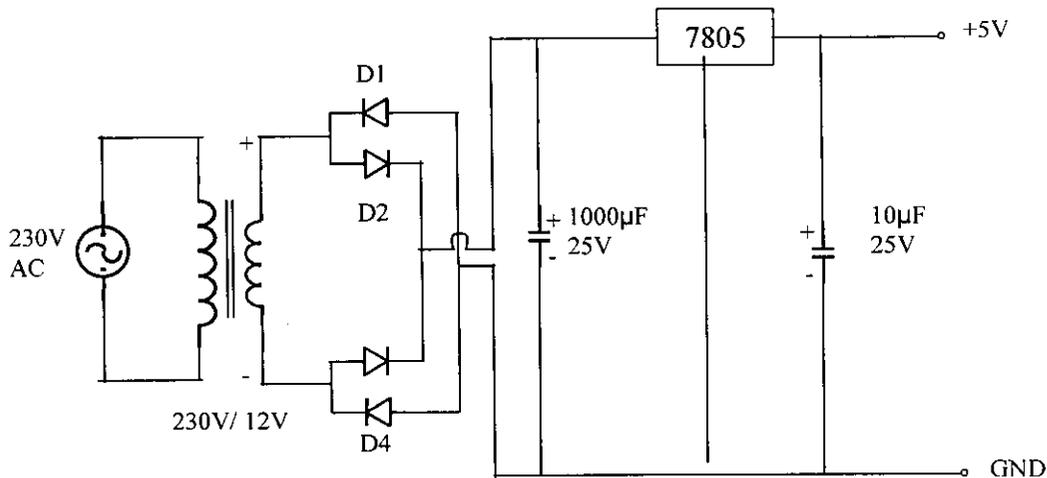


Figure3.4 +5V Regulated power supply

The output of the transformer being 12V is given to the bridge rectifier. This converts the AC input power to DC. The DC obtained has ripple content in them, so in order to smooth out the ripples the filters are employed here. The smoothed power needs to be regulated, so we employ a positive regulator (7805). The regulated power needs to be smoothed if there is any ripple. The filter is again employed, because the smallest of ripples can affect the working of the Digital circuitry used. So we get an output of +5 V from the power supply module. This is used throughout the project for biasing the various chips and circuits.

3.3.2 -5V POWER SUPPLY

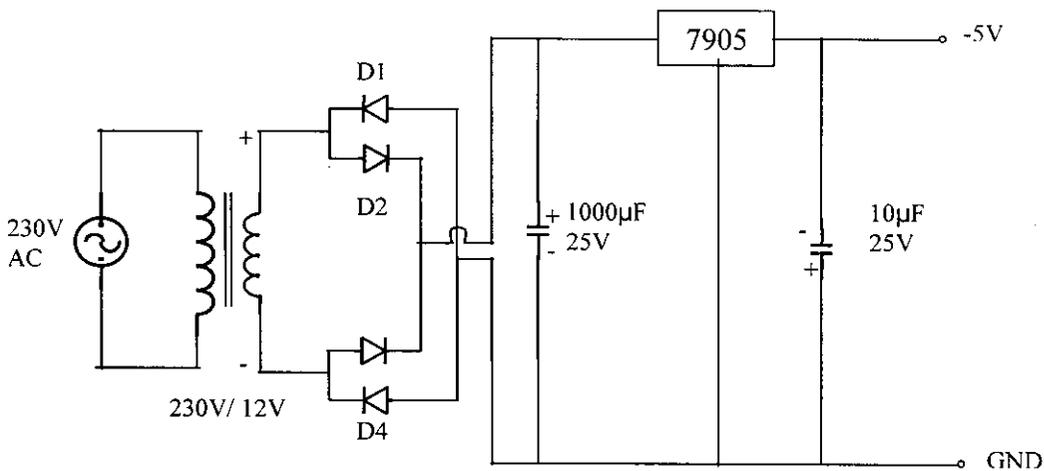


Figure 3.5 -5V Regulated power supply

The output of the transformer being 12V is given to the bridge rectifier. This converts the AC input power to DC. The DC obtained has ripple content in them, so in order to smooth out the ripples the filters are employed here. The smoothed power needs to be regulated, so we employ a negative regulator (7905). The regulated power needs to be smoothed if there is any ripple. The filter is again employed, because the smallest of ripples can affect the working of the Digital circuitry used. So we get an output of -5V from the power supply module. This is used throughout the project for biasing the various chips and circuits.

3.4 GENERATION OF SQUARE WAVE

3.4.1 FROM SINUSOIDAL VOLTAGE WAVE:

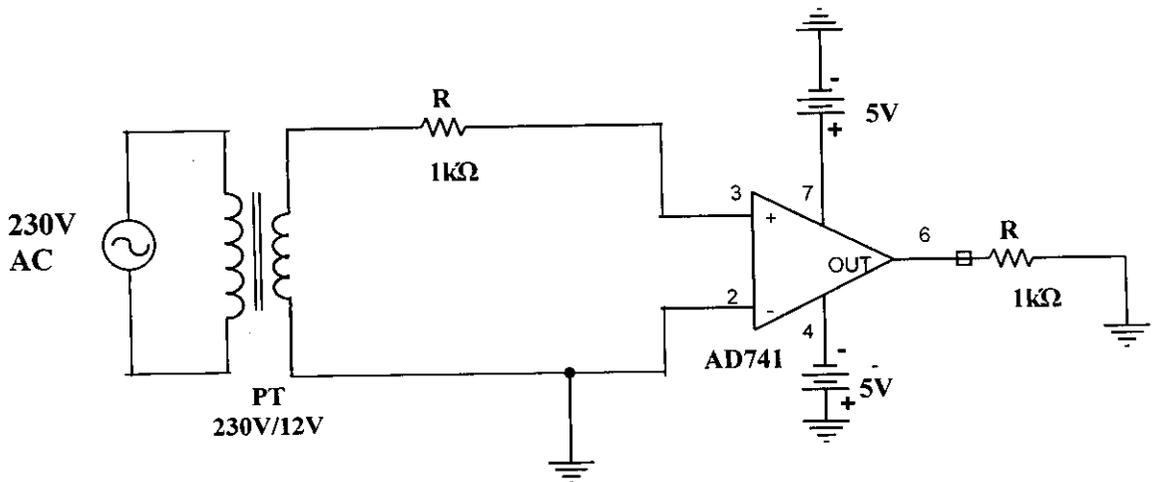


Figure 3.6 Generation of square wave from sinusoidal voltage

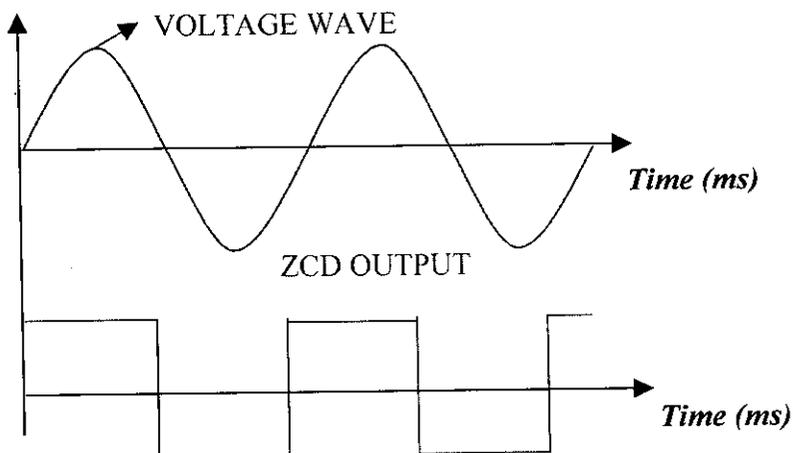


Figure3.7 Input-Output waveforms for voltage

This circuit shows the production of square wave output from the sine wave. The 230V is stepped down to 12V using PT, the ZCD is developed using the operational amplifier (IC 741). The operation of the ZCD and PT is shown below:

3.4.1.1 Operation of potential transformer

When the primary winding of the PT is energized by the main supply “(phase) voltage alternating flux is set up in the core of the transformer. This flux links with the secondary winding and EMF is induced in the secondary winding according to the Faraday’s law of electromagnetic induction. Since the number of turns is less than that of primary winding the EMF in the secondary is stepped down.

3.4.1.2 Zero crossing detector

Zero crossing detector can be constructed by using operational amplifiers (IC 741).they are non-inverting comparators (with inverting input grounded). When the given input voltage is greater than 0V (ideally) then the output will be at $+V_{sat}$. If the input voltage is less than 0V (ideally) then the output will be at $-V_{sat}$.

This generates the square wave, which is then given to the microcontroller for calculation.

3.4.2 FROM SINUSOIDAL CURRENT WAVE

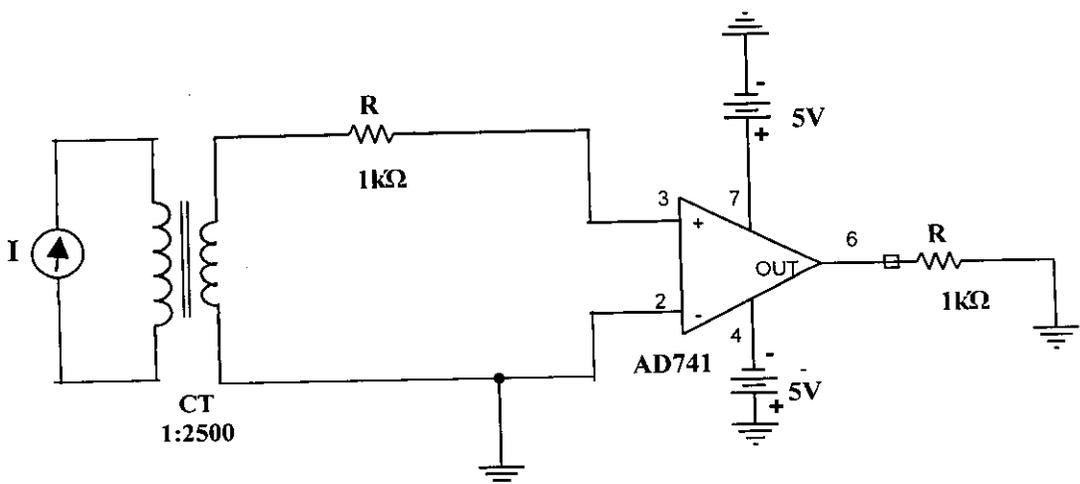


Figure 3.8 Generation of square wave from sinusoidal current

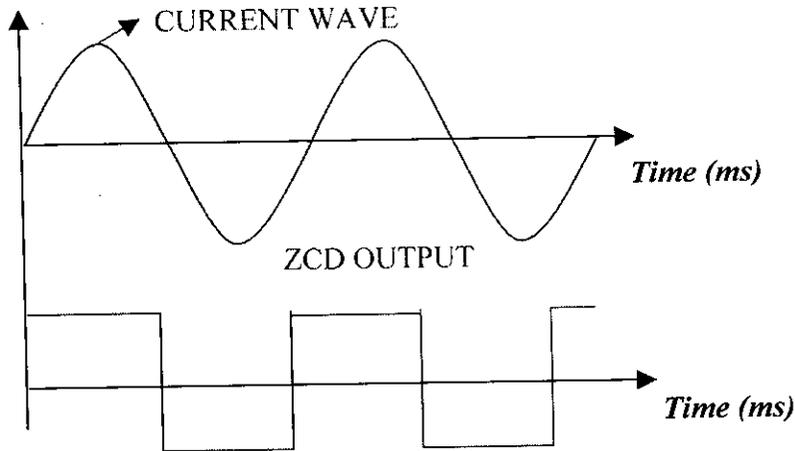


Figure 3.9 Input – Output Waveforms for current

This circuit shows the production of square wave output from the sine wave. The stepped down CT is used to reduce the current, the ZCD is developed using the operational amplifier (IC 741). The operation of the ZCD and CT is shown below:

3.4.2.1 Operation of current transformer (CT)

The toroidal type current transformer uses the line conductor as the primary winding. The winding over the toroidal core acts as secondary winding. The secondary winding cuts the flux produced by the current flow through the line conductor and hence EMF is induced in the secondary winding. Here the primary is only a single conductor and the secondary is having more number of turns.

$$I_1 N_1 = I_2 N_2$$

$$\text{Therefore, } I_2 = I_1 N_1 / N_2$$

Hence the current through the secondary winding will be less. i.e., the current is stepped down. It is noted that the CT secondary is always (while working) kept close through a very low resistance. During the normal operation the flux set up by the current through the secondary winding opposes the flux set up by the current through the

primary winding. Hence the resultant flux will be very less and hence EMF induced in the secondary winding will be less. If the secondary of CT is opened when it is in service the secondary current becomes zero and hence no flux is produced by secondary winding.

Hence the resultant flux will be high and hence the induced EMF will be very high. For example let us take the case of CT used in this project. Here the current is stepped down to $1/2500^{\text{th}}$ of the primary current (load current) and hence the voltage during open circuit will be 2500 times the supply voltage. i.e., $2500 * 230\text{V} = 575000\text{V}$ this emf is very dangerous to the insulation provided in the CT. Hence the CT gets damaged when its secondary winding is open circuited. To avoid this care must be taken not to open the secondary winding of the CT while it is in service.

3.4.2.1 Zero crossing detector

Zero crossing detector can be constructed by using operational amplifiers (IC 741). They are non-inverting comparators (with inverting input grounded). When the given input voltage is greater than 0V (ideally) then the output will be at $+V_{\text{sat}}$. If the input voltage is less than 0V (ideally) then the output will be at $-V_{\text{sat}}$.

This generates the square wave, which is then given to the microcontroller for calculating the width of the pulses, which in turn gives the phase angle in radians.

3.5. OVERALL CIRCUIT

3.5.1 DESCRIPTION

The voltage and current are step down using the PT and CT. The step down values are given to the analog inputs of PIC16F877, for the measurement of voltage and current. The step down voltage and current are converted to square wave through ZCD. The ZCD output from the R phase is given to the port E of PIC 16F877 for the measurement of power factor angle and frequency. The ZCD output of other two phases (Y & B) are given to interval timer of 8254, this timer gives the time period for the measurement of power factor angle and frequency. The calculation is made in the PIC controller, the calculated values are fed in to the latch 74LS373 for interfacing the

various input and output to and from the controller. The 74LS244 is a buffer for temporarily storing the results of the ADC. The manual and automatic modes are selected using the mode selection switches which are placed at the front side of the APFC panel. The changeover of power supply between the mains and the auxiliary power is by means of an autoswitch. The various parameters that are displayed are selected by means of using the toggle keys that are placed on the apfc panel. The LCD is a two line display segment with 2*14 characters display. The contrast of the LCD can be varied by connecting a +5v potentiometer across the +5v terminal and the Gnd pins of the LCD display. The PIC 16F877 controller is solely selected for this purpose it directly accepts the analog inputs through the port A without any conversion. Since the controller has two 8 bit timers and one 16 bit timer, the two 8 bit timers are used to calculate the time interval of the R phase and Y phase and for the B phase it is done with the help of an 8254 programmable interval timer or counter in the mode 2, the rate generator mode.

OVERALL CIRCUIT DIAGRAM OF THE PROJECT

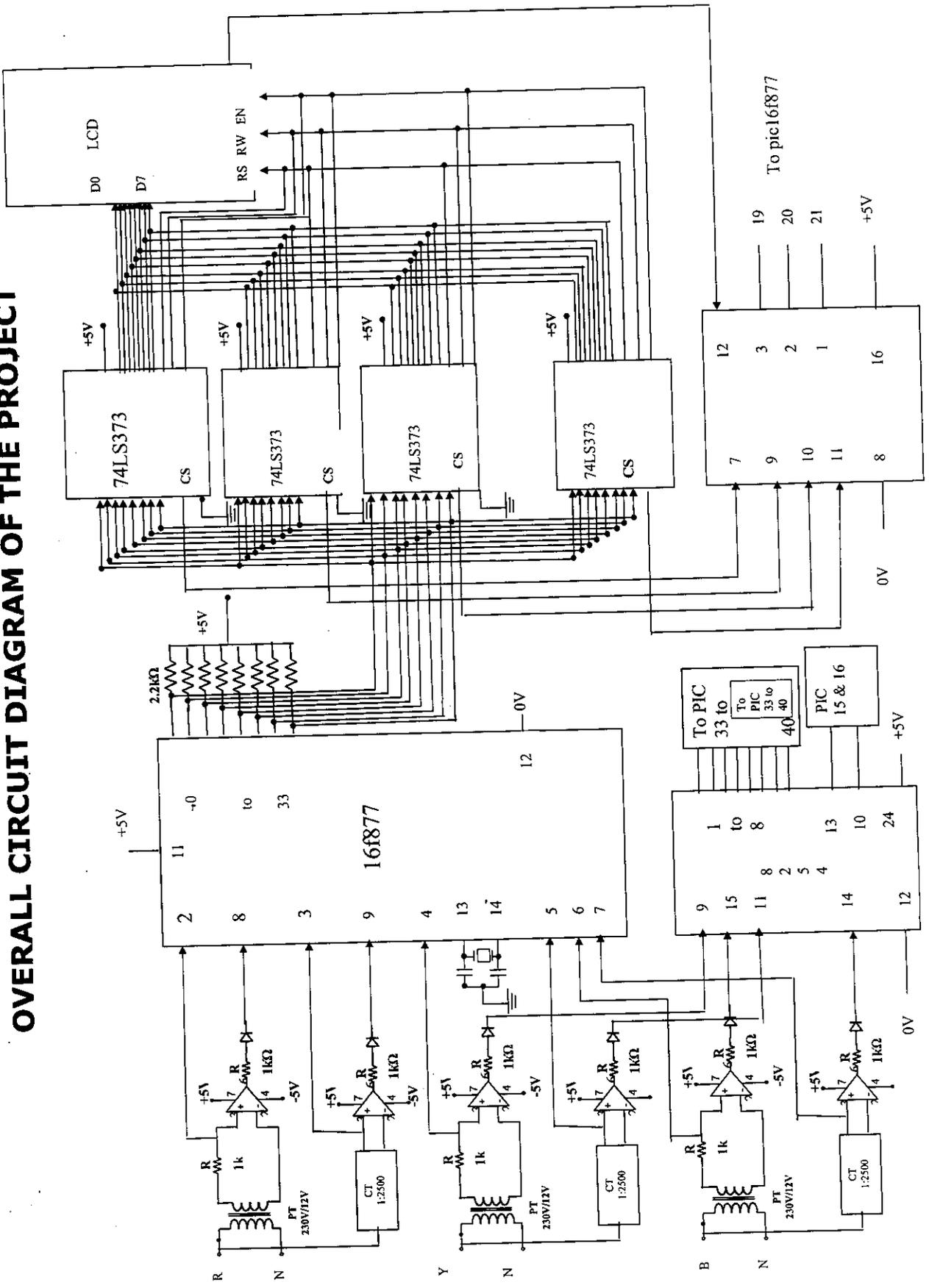


Fig: (xiii) overall circuit diagram of APFCC

CHAPTER 4

DIGITAL PHASE DETECTION

4.1 GENERATION OF PHASE ANGLE PULSES

To allow accurate control of the current waveform, the phase of the utility voltage need to be measured with considerable accuracy. This problem is simplified by prior knowledge of the wave shape and the Indian standard is a sinusoidal with a frequency of 50Hz. Practically speaking however, the digital controller will have to deduce phase given sequence of unsigned numbers obtained from the on-board analog to digital controller. To fully understand how the numbers are interpreted, one must know what happens to the utility before it is sampled. The first step in the phase detection is what is known as signal conditioning.

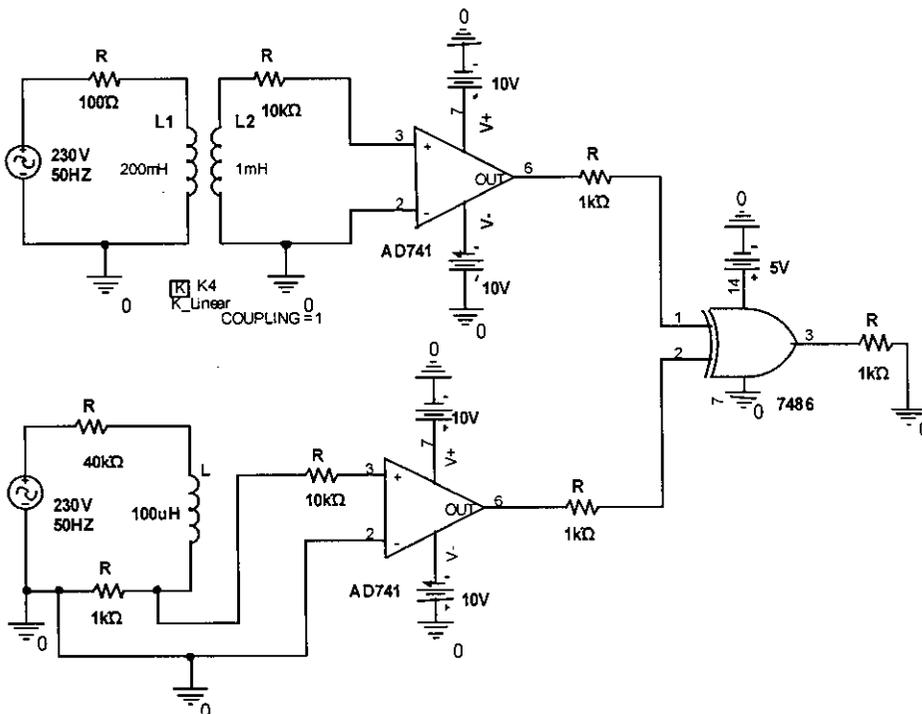


Figure 4.1 Digital Phase detection

Large bipolar voltages present on the utility grid are scaled down and dc biased to a form, the processor hardware can measure. Voltages present on the power utility grid in the most extreme form range from -690v to +690v. This is altered to a voltage between +3.3v and 0v with a virtual ground at 1.65v. On the PIC 16F877, this range in voltage is sampled and the result is a 10 bit unsigned number.

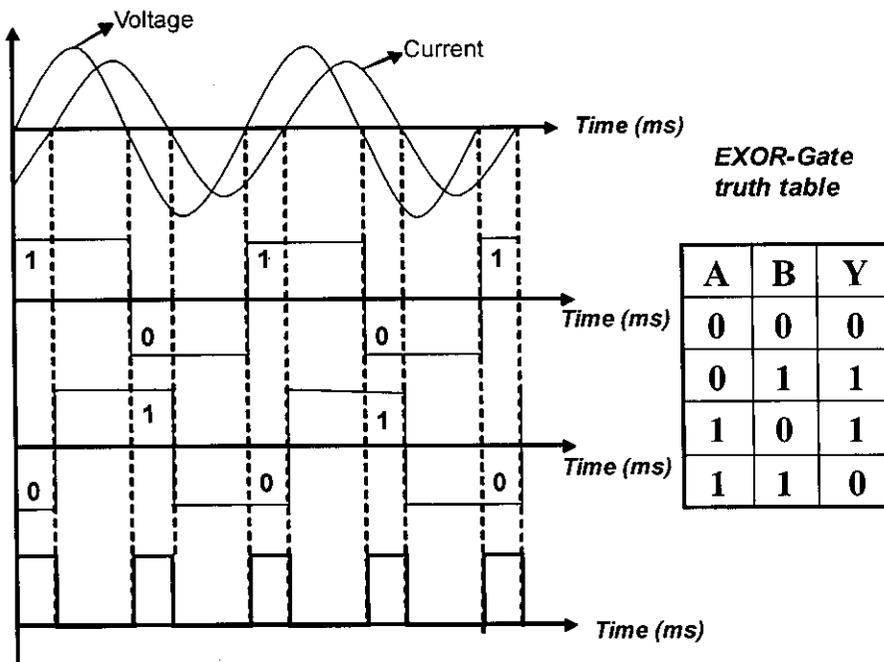


Figure 4.2 Generation of phase angle pulses.

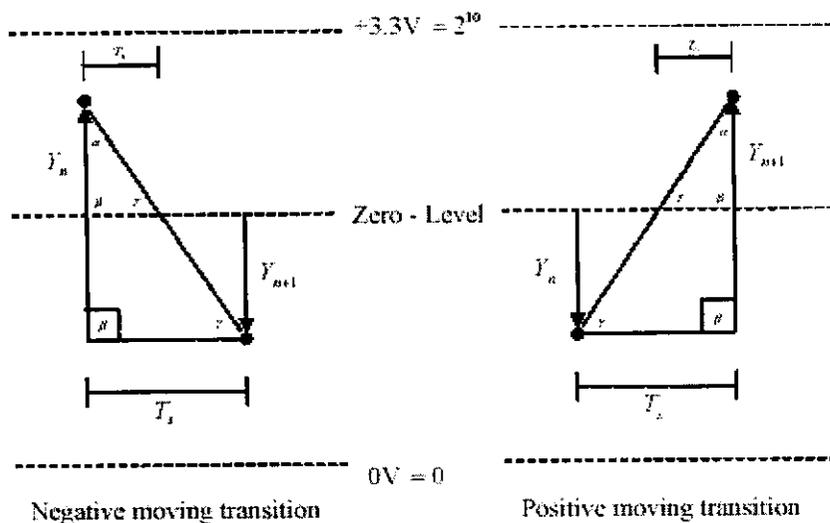


Figure 4.3 Negative & Positive moving transition

Note the two triangles formed between the two samples are similar, which means the corresponding angles in each triangle are equal. Also, for any two similar triangles,

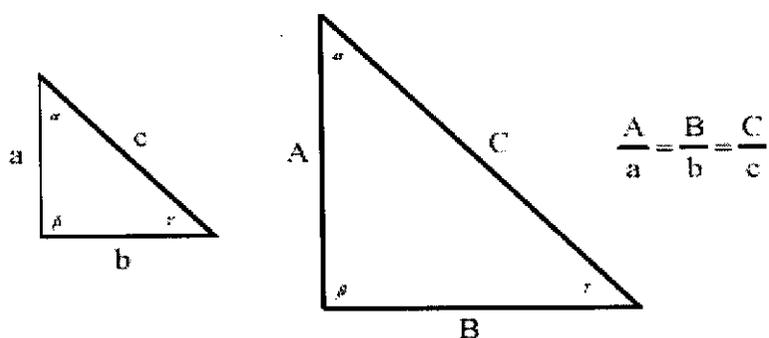


Figure 4.4 Phase Triangles

Using this theory, a simple linear interpolation will be used to deduce an accurate zero-crossing time for the sine-wave [11]. Using the similar triangles rule in relation to the above two sampling situations.

$$\frac{T_x}{T_0} = \frac{Y_{n-1} - Y_n}{Y_{n-1} - (\text{ZeroLevel})} \rightarrow T_0 = \frac{T_x [Y_{n-1} - (\text{ZeroLevel})]}{Y_{n-1} - Y_n} \quad (4.1)$$

Thus, for a negative moving transition,

$$\phi = \pi + \frac{T_x - T_0}{(1/f_{grid})} * 2\pi \quad (4.2)$$

$$\frac{T_x}{T_0} = \frac{Y_n - Y_{n-1}}{Y_n - (\text{ZeroLevel})} \rightarrow T_0 = \frac{T_x [Y_n - (\text{ZeroLevel})]}{Y_n - Y_{n-1}} \quad (4.3)$$

Thus, for a positive moving transition,

$$\phi = \frac{T_0}{(1/f_{grid})} * 2\pi \quad (4.4)$$

The phase of the utility voltage for the rest of the cycle can simply be predicted by adding on the known sampling time during each update. Next, an implementation of the phase detection algorithm will be tested using ORCAD PSPICE SIMULATION.

4.2 PRELIMINARY CALCULATIONS

SETTING THE NUMBER OF CAPACITOR STAGES

Let us now consider the following example and decide the number of capacitor stages.

Given parameters:

Induction motor: 220kw

Network (line delta): 440 v ac , 3 phase.

Frequency: 50 hz

Power factor:

Current power factor: 0.7 (lag)

Target power factor: 0.9 (lag)

Calculation:

Capacitor ratings for star and delta connection

Current power factor :0.7	Target power factor : 0.9
$\cos\phi_1=0.7$	$\cos\phi_2=0.9$
$\phi_1=45.57$ degrees	$\phi_2=25.84$ degrees
$\tan\phi_1=1.02$	$\tan\phi_2=0.48$

$$\begin{aligned}
 \text{Reactive power to be compensated: } Q_c &= p (\tan\phi_1 - \tan\phi_2) \\
 &= 220 \times 1000 * (1.02 - 0.48) \\
 &= 118800 \text{ var} \\
 Q_c &= 118.8 \text{ kvar.}
 \end{aligned}$$

Hence a total of 118.8 kvar of reactive power is to be compensated to achieve the required target power factor of 0.9.

Case1 Star connection:

$$\text{Capacitance voltage} = 440/\sqrt{3} = 254 \text{ v}$$

$$\begin{aligned}
 \text{Capacitance in a star connection} &= \frac{Q_c}{V^2 * \omega} \\
 &= \frac{118.8 * 1000}{440 * 440 * 2 * 3.14} \\
 &= 1954 \mu \text{ f/ line(phase).}
 \end{aligned}$$

$$\begin{aligned}
 \text{Total capacitance in a star connection} &= 3 * 1954 \\
 &= 5862 \mu \text{ f.}
 \end{aligned}$$

Case2 Delta connection:

$$\begin{aligned} \text{Capacitance in a delta connection} &= \frac{Q_c}{3 * V^2 * \omega} \\ &= \frac{118.8 * 1000}{3 * 440 * 440 * 2 * 3.14 * 50} \\ &= 651 \mu \text{ f / line (phase)}. \end{aligned}$$

$$\begin{aligned} \text{Total capacitance in a delta connection} &= 3 * 651 \\ &= 1953 \mu \text{ f} \end{aligned}$$

let the 118.8 KVAR of reactive power is compensated in five stages to achieve the target power factor of 0.9.

To achieve 5 stages of switching 118.8 KVAR is divided into

$$118.8 \text{ KVAR} = (25 \text{ kvar} * 4) + (18.8 \text{ kvar} * 1)$$

when using EPCOS capacitor from siemens,

$$\begin{aligned} \text{the total effective capacitance per phase is } & \} = (4 * 3 * 137) + (1 * 3 * 103) \\ & = 1953 \mu \text{ f / phase.} \end{aligned}$$

Hence from the above results , the total effective capacitance per phase in star connection is thrice the total effective capacitance in a delta connection. Hence most of the power factor correction capacitors are usually star connected internally.

CHAPTER 5

SIMULATION RESULTS AND TEST REPORTS

5.1 SIMULATION RESULTS

An implementation of the phase detection algorithm is tested in **ORCAD PSPICE SIMULATION Software**. The system used in this simulation looks like:

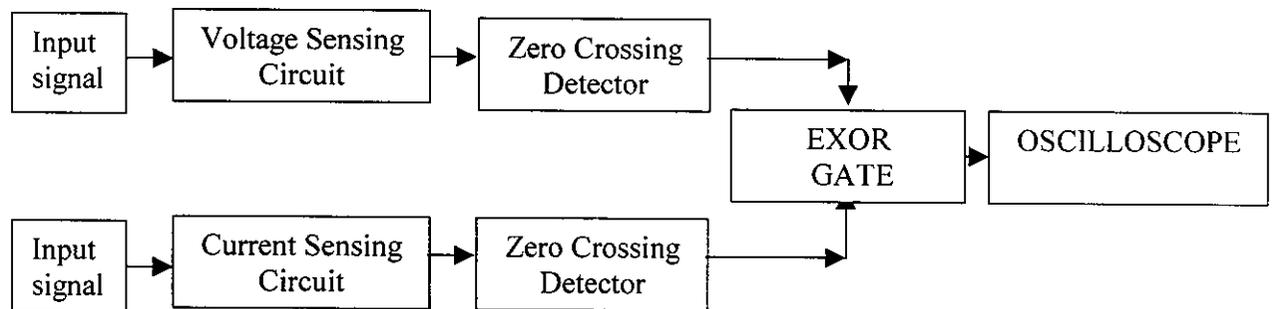


Figure 5.1 Phase detect simulation model

The type of simulation performed here is a ‘fixed-step’ simulation. Because the sine wave block in the **ORCAD PSPICE SIMULATION** will produce samples at a constant rate. It will accept samples one at a time and output the phase angle pulses to the scope.

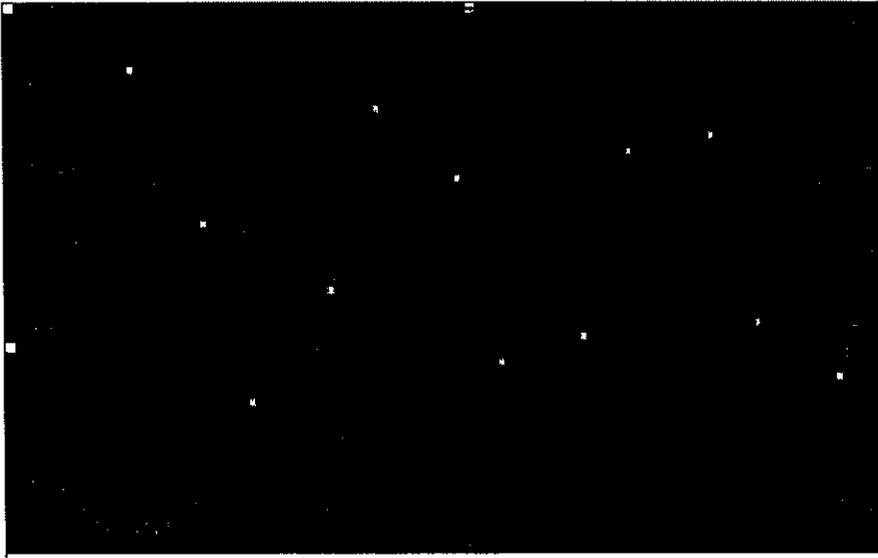


Figure 5.2 Input signal



Figure 5.3 ZCD output of voltage waveform

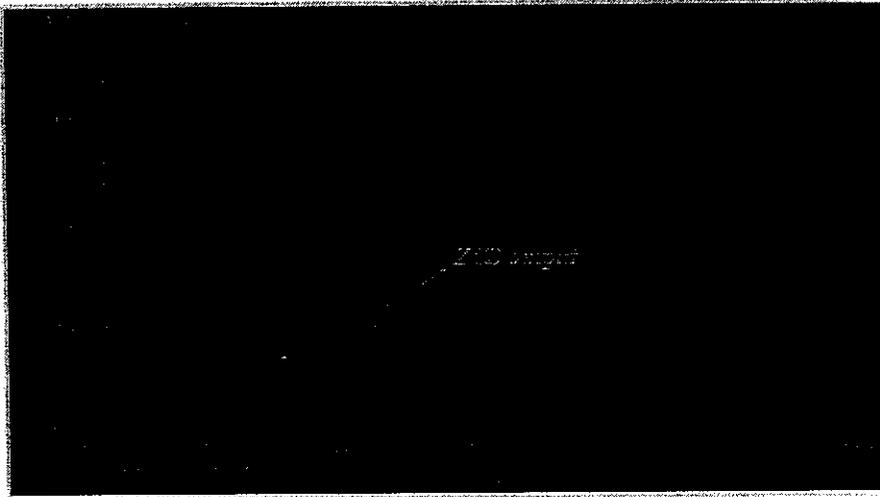


Figure 5.4 ZCD output of current waveform

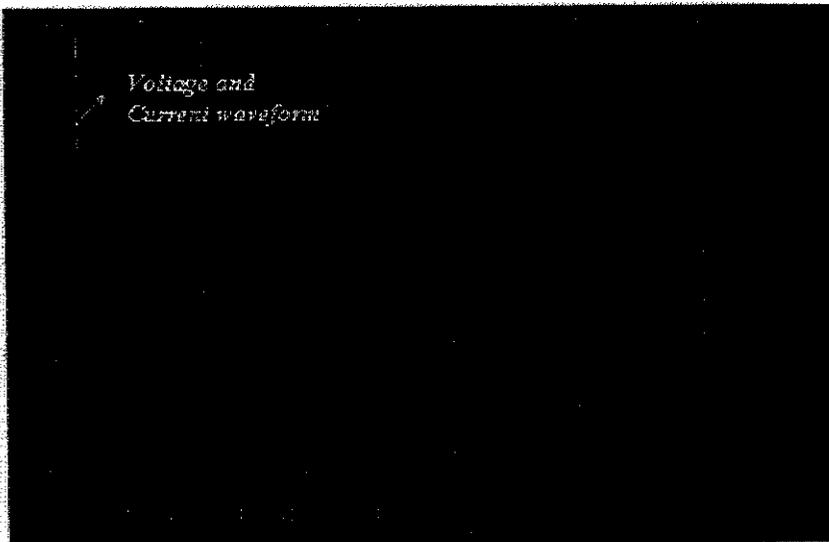


Figure 5.5 Current and Voltage are in phases

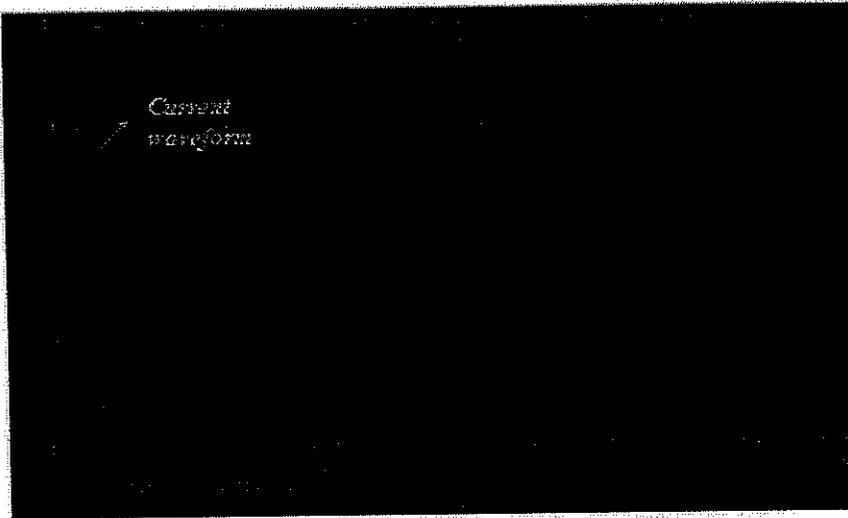


Figure 5.6 Current lags Voltage by 30°

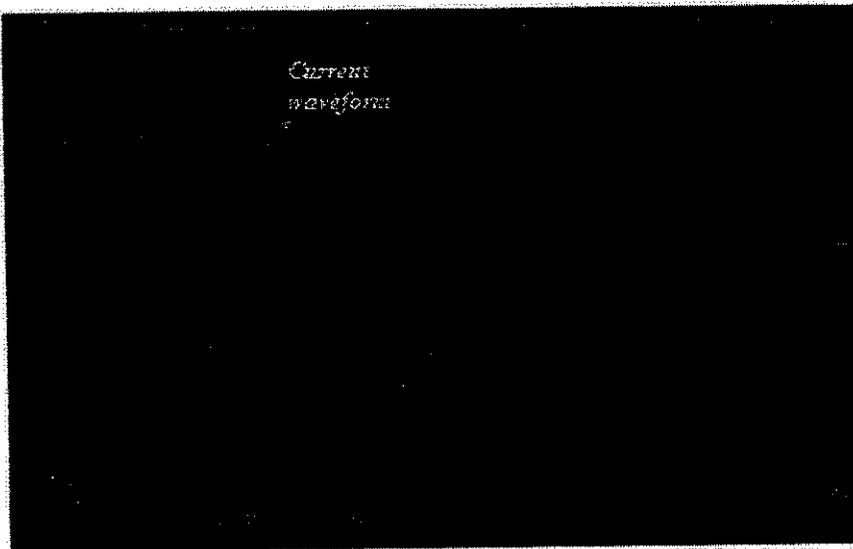


Figure 5.7 Current lags Voltage by 60°

The results of the simulation shown above clearly show the algorithm is effective. The code for phase angle detection using PIC16F877 is listed in Appendix A

5.2 TEST REPORTS

Typical casestudy in "LAKSHMI ELECTRICAL CONTROL SYSTEMS"
COIMBATORE ON 21/04/2005 USING TOSHIBA POWER SPECTRUM
ANALYSER.

5.2.1 Before Installation of APFC Controller

MAIN	INST.	CIRCUIT1	2005/04/21 15:05:35
U1	251.39 V	I1	0.0923kA
U2	251.29 V	I2	0.0831kA
U3	252.09 V	I3	0.0870kA
Uave	251.59 V	Iave	0.0875kA
		I4	0.0000kA
P1	20.02kW	Q	32.64kvar
P2	17.76kW	S	66.01kVA
P3	19.59kW	PF	0.8692
P	57.38kW	f	49.489 Hz
WP+	0.000kWh		0:00:00
			U 600V × 1.00 I 500A × 2.00 I4 500A × 2.00 WIRING 3P4W4I CIRCUIT x1 PLL U1 50Hz INTVL. 1min
SCREEN		AVERAGE	HOLD

Table 5.1 Load Parameter

5.2.2 After Installation of APFC Controller

MAIN	INST.	CIRCUIT1	2005-04/21 17:36:06
U1	232.94 V	I1 0.3274kA	U 600V x 1.00
U2	232.33 V	I2 0.2571kA	I 500A x 2.00
U3	232.11 V	I3 0.3106kA	I4 500A x 2.00
Uave	232.46 V	Iave 0.2984kA	WIRING 3P4W4I
P1	75.47kW	Q 31.19kvar	CIRCUIT x1
P2	58.72kW	S 208.11kVA	PLL U1 50Hz
P3	71.57kW	PF -0.9887	INTVL. 1min
P	205.76kW	f 49.857 Hz	
WP+	0.000kWh	0:00:00	
SCREEN	AVERAGE	HOLD	

Table 5.4 Load Parameter

LIST	CIRCUIT1	2005-04/21 17:39:53
I3	[A] [x] [deg]	I3 ORD 01 U 600V x 1.00
1	0.3465k 100.00 121.58	0.3465kA I 500A x 2.00
2	0.0041k 1.17 -172.05	100.00 % I4 500A x 2.00
3	0.0043k 1.24 -173.15	TOTAL WIRING 3P4W4I
4	0.0011k 0.331 -175.15	0.3466kA CIRCUIT x1
5	0.0011k 0.333 -175.06	THD-F 1.98 %
6	0.0017k 0.330 -175.03	f 49.925 Hz
7	0.0007k 0.200 -175.03	INTVL. 5sec
8	0.0001k 0.03 -100.43	
9	0.0004k 0.03 -115.93	
10	0.0004k 0.11 -57.00	
11	0.0001k 0.03 -56.01	
12	0.0001k 0.03 -29.11	
13	0.0002k 0.05 -104.31	
14	0.0000k 0.02 -35.77	
15	0.0000k 0.01 -111.42	
16	0.0000k 0.00 -148.87	
17	0.0000k 0.01 -48.26	
18	0.0000k 0.00 -87.16	
19	0.0000k 0.01 -43.12	
20	0.0000k 0.00 -34.23	
SCREEN	CH	ORDER HOLD

Table 5.5 Harmonic Spectrum

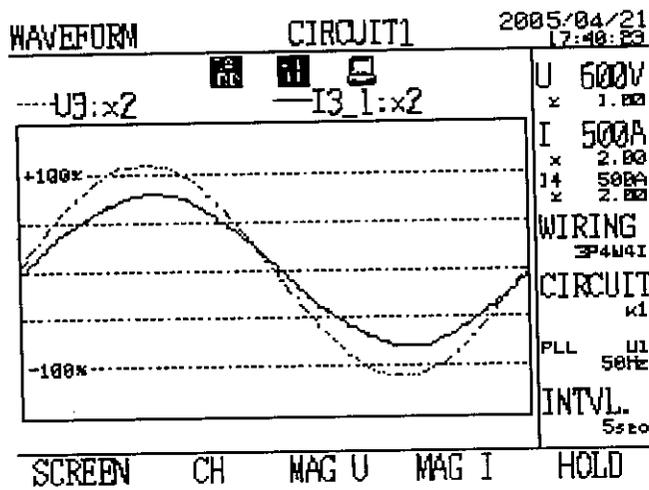


Figure 5.9 Voltage and Current Waveform

From the above figures it may be inferred that after the installation of APFC controller, the load voltage has been reduced from **251.39 volts** down to **232.94 volts**; and the total harmonic distortion factor has been reduced from **31.53%** down to **1.98%**. From the figure it can also be seen that the voltage and current waveforms has achieved a more steady path from being a distorted one.

CHAPTER 6

SOFTWARE DETAILS

6.1 FEATURES OF PIC MICROCONTROLLER

The PIC stands for “Peripheral Interface Controller”. This is a low cost, low power, high-speed RISC Microcontroller used in many embedded control system applications. Most instructions are executed in a single instruction cycle, making it one of the fastest low-cost microcontrollers on the market. The PIC micro devices are grouped by the size of their instruction word. The PIC is a complete embedded controller with Program Memory, RAM, Timers, and inbuilt peripherals like ADC, PWM, USART, IIC, SPI, LCD drivers, with features like brown out, interrupts, low power consumption, software code protection and operating from DC to 33 MHz (device specific). The clock that makes the PIC tick can be from an internal RC in some devices, an external RC combination, crystal or a resonator. Memory varieties available for PIC are EPROM, ROM, FLASH and OTP.

6.2 MICROCONTROLLER CORE FEATURES

- High-performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input DC - 200 ns instruction cycle
- Up to 8K x 14 words of FLASH Program Memory,
- Up to 368 x 8 bytes of Data Memory (RAM)
- Up to 256 x 8 bytes of EEPROM data memory
- Pin out compatible to the PIC16C73B/74B/76/77/77A
- Interrupt capability (up to 14 sources)
- Eight level deep hardware stack

- Direct, indirect and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS FLASH/EEPROM technology
- Fully static design
- In-Circuit Serial Programming (ICSP) via two pins
- Single 5V In-Circuit Serial Programming capability
- In-Circuit Debugging via two pins
- Processor read/write access to program memory
- Wide operating voltage range: 2.0V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial and Industrial temperature ranges
- Low-power consumption:
 - < 2 mA typical @ 5V, 4 MHz
 - 20 mA typical @ 3V, 32 kHz
 - < 1 mA typical standby current

6.3. PERIPHERAL FEATURES

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
 - Capture is 16-bit, maximum resolution is 12.5 ns
 - Compare is 16-bit, maximum resolution is 200 ns

- PWM maximum resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI (Master Mode) and IIC (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls

6.4. ALGORITHM

Step 1: The controller starts its action only after 'zero voltage release time' when the power supply is 'ON'.

Step 2: Read the potential transformer (PT) ratio

A (primary voltage)/C (secondary voltage) given by the designer.

Step 3: Read the value after transformer as V_{RN} , V_{YN} and V_{BN} from the port.

Step 4: Calculate actual values of V_{RN} , V_{YN} and V_{BN} by using the

$$\text{formulas, } V_{RN}(\text{actual}) = (A/C) * V_{RN}$$

$$V_{YN}(\text{actual}) = (A/C) * V_{YN}$$

$$V_{BN}(\text{actual}) = (A/C) * V_{BN}$$

and store the results and display it.

Step 5: Calculate line voltage by using the formula,

$$V_{RY} = \sqrt{3} V_{RN}(\text{actual})$$

$$V_{YB} = \sqrt{3} V_{YN}(\text{actual})$$

$$V_{BR} = \sqrt{3} V_{BN}(\text{actual})$$

and store the results and display it .

Step 6: Read the current transformer (CT) ratio

X (primary current)/Z (secondary current) given by the designer.

Step 7: Read the value after transformer as I_{RN} , I_{YN} and I_{BN} from the port.

Step 8: Calculate actual value of I_{RN} , I_{YN} and I_{BN} by using the

$$\text{formulas, } I_{RN}(\text{actual}) = (X/Z) * I_{RN}$$

$$I_{YN}(\text{actual}) = (X/Z) * I_{YN}$$

$$I_{BN}(\text{actual}) = (X/Z) * I_{BN}$$

and store the results and display it.

Step 9: Get the V_{RN} , V_{YN} and V_{BN} (after ZCD) from the port.

Step 10: Frequency measurement: Start the timer when 'Rising edge' of voltage occurs and stop it when 'Falling edge' occurs at each phase.

Step 11: Read the value of each timer as $T_R(\text{supply})$, $T_Y(\text{supply})$ and $T_B(\text{supply})$ and store the result.

Step 12: Calculate each line frequency by using the formula,

$$F_R(\text{supply}) = 1/[2 * T_R(\text{supply})]$$

$$F_Y(\text{supply}) = 1/[2 * T_Y(\text{supply})]$$

$$F_B(\text{supply}) = 1/[2 * T_B(\text{supply})]$$

and store the result and display it.

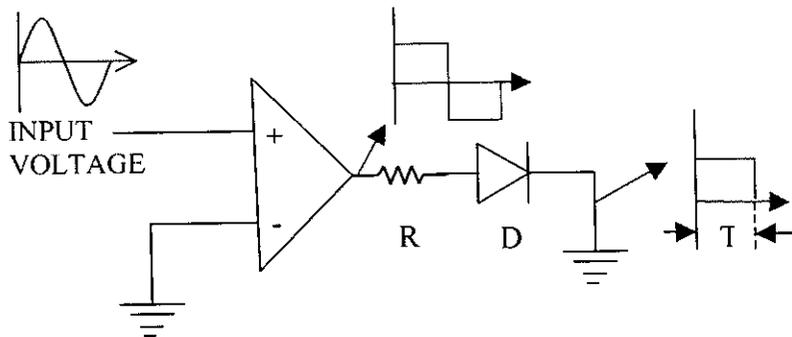


Figure 6.1 Frequency measurement

The frequency of each phase is calculated by measuring the pulse width of the ZCD output. When rising edge occurs the timer starts and the timer stops while the falling edge of the square pulse is reached. This timer value gives the time period of the pulse and inverse of twice the time period gives the frequency.

Step 13: Get the V_{RN} , V_{YN} and V_{BN} (after ZCD) from the port.

Step 14: Get the I_{RN} , I_{YN} and I_{BN} (after ZCD) from the port.

Step 15: Phase angle measurement: Start timer with the 'Rising edge' of the voltage and stop timer when the 'Rising edge' of the current occurs at each phase.

Step 16: Read the timer value as $T_{ON}(R)$, $T_{ON}(Y)$ and $T_{ON}(B)$ and store the result.

Step 17: Calculate phase angle from each line by using the formula

$$\Phi_R = \{T_{ON}(R) / [1/F_R (\text{supply})]\} * 360$$

$$\Phi_Y = \{T_{ON}(Y) / [1/F_Y (\text{supply})]\} * 360$$

$$\Phi_B = \{T_{ON}(B) / [1/F_B (\text{supply})]\} * 360$$

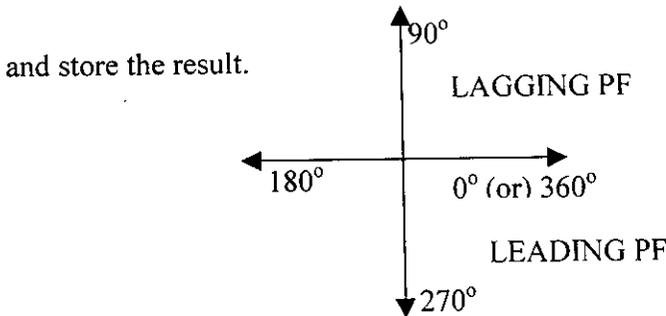


Figure 6.2 Four quadrant

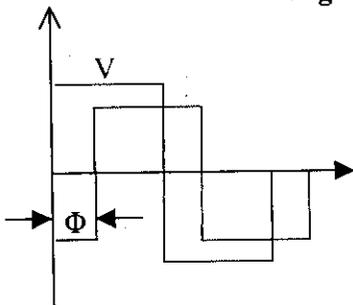


Figure 6.3 Lagging PF angle measurement

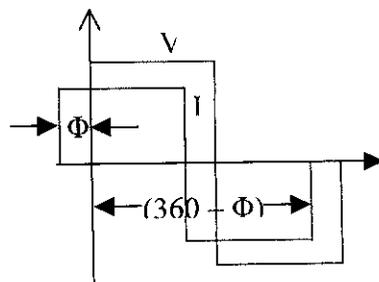


Figure 6.4 Leading PF angle measurement

$$\cos(270 + \Phi) = \cos\Phi$$

In case of lagging power factor, the angle is measured directly by starting the timer when the rising edge of the voltage occurs and it stops while the rising edge of current occurs. But in case of leading power factor the angle cannot be measured directly, that is the timer will measure the angle as $360^\circ - \Phi$ (i.e. greater than 270°).

Then the power factor angle is calculated as $\Phi = 360 - (360^\circ - \Phi)$.

Step 18: Calculate average PF angle, $\Phi = (\Phi_R + \Phi_Y + \Phi_B)/3$.

Step 19: If Φ lies between 0° and 90° , then display 'lag' or '-'

Step 20: If Φ lies between 270° and 360° , then display 'lead' or '+'

Step 21: Calculate PF of each phase by taking cosine of each angle as shown, $\cos\Phi_R$, $\cos\Phi_Y$ and $\cos\Phi_B$.

Step 22: Calculate $\cos\Phi = (\cos\Phi_R + \cos\Phi_Y + \cos\Phi_B)/3$ and display it.

Step 23: Get the number of capacitor stages. Enable the number of capacitor stages requested by the user.

Step 24: Check weather the selected mode is automatic (1) or manual(0).

Step 25: If it is automatic go to step 27.

Step 26: If it is manual go to step 36.

Step 27: Check weather the current is positive or negative.

Step 28: If the current is negative, get the 'lock OUT time' and check Existing PF = Second target PF after 'lock OUT time'.

If YES go to step 36, else go to step 30.

Step 29: If the current is positive check

Existing PF = Target PF

If YES, go to step 36, else continue.

Step 30: Calculate the reactive power needed to compensate by using the formula, $Q_c = P (\tan \Phi_1 - \tan \Phi_2)$

Step 31: Then calculate the total capacitance needed to achieve the compensation by using the formula,

In star connection, $C = 3 * [Q_c / (V^2 * \omega)]$

In delta connection, $C = 3 * [Q_c / (3 * V^2 * \omega)]$

Step 32: Check weather the capacitor needed to compensate is available.

If NO, give alarm signal.

Step 33: Get the value of 'Switch IN and Switch OUT time' and store it.

Step 34: Check weather the power factor is lead or lags. If the PF is lag switch ON the capacitor bank one by one for every 'Switch IN time' by FIFO method until it gets compensated.

- Check for the change in PF after every stages if there is no change then give the alarm signal.

Step 35: If the power factor is lead switch OFF the capacitor banks one by one for every 'Switch OUT time' by LIFO method .

- Check for the change in PF after every stages if there is no change then give the alarm signal.

Step 36: Calculate real power in each line by using the formula,

$$P_R = V_{RN}(\text{line}) * I_R(\text{actual}) * \cos\Phi$$

$$P_Y = V_{YN}(\text{line}) * I_Y(\text{actual}) * \cos\Phi$$

$$P_B = V_{BN}(\text{line}) * I_B(\text{actual}) * \cos\Phi$$

$$P = P_R + P_Y + P_B$$

and store the result and display it.

Step 37: Calculate reactive power in each line by using the formula,

$$Q_R = V_{RN}(\text{line}) * I_R(\text{actual}) * \sin\Phi$$

$$Q_Y = V_{YN}(\text{line}) * I_Y(\text{actual}) * \sin\Phi$$

$$Q_B = V_{BN}(\text{line}) * I_B(\text{actual}) * \sin\Phi$$

$$Q = Q_R + Q_Y + Q_B$$

and store the result and display it.

Step 38: Calculate apperant power in each line by using the formula,

$$S_R = V_{RN}(\text{line}) * I_R(\text{actual})$$

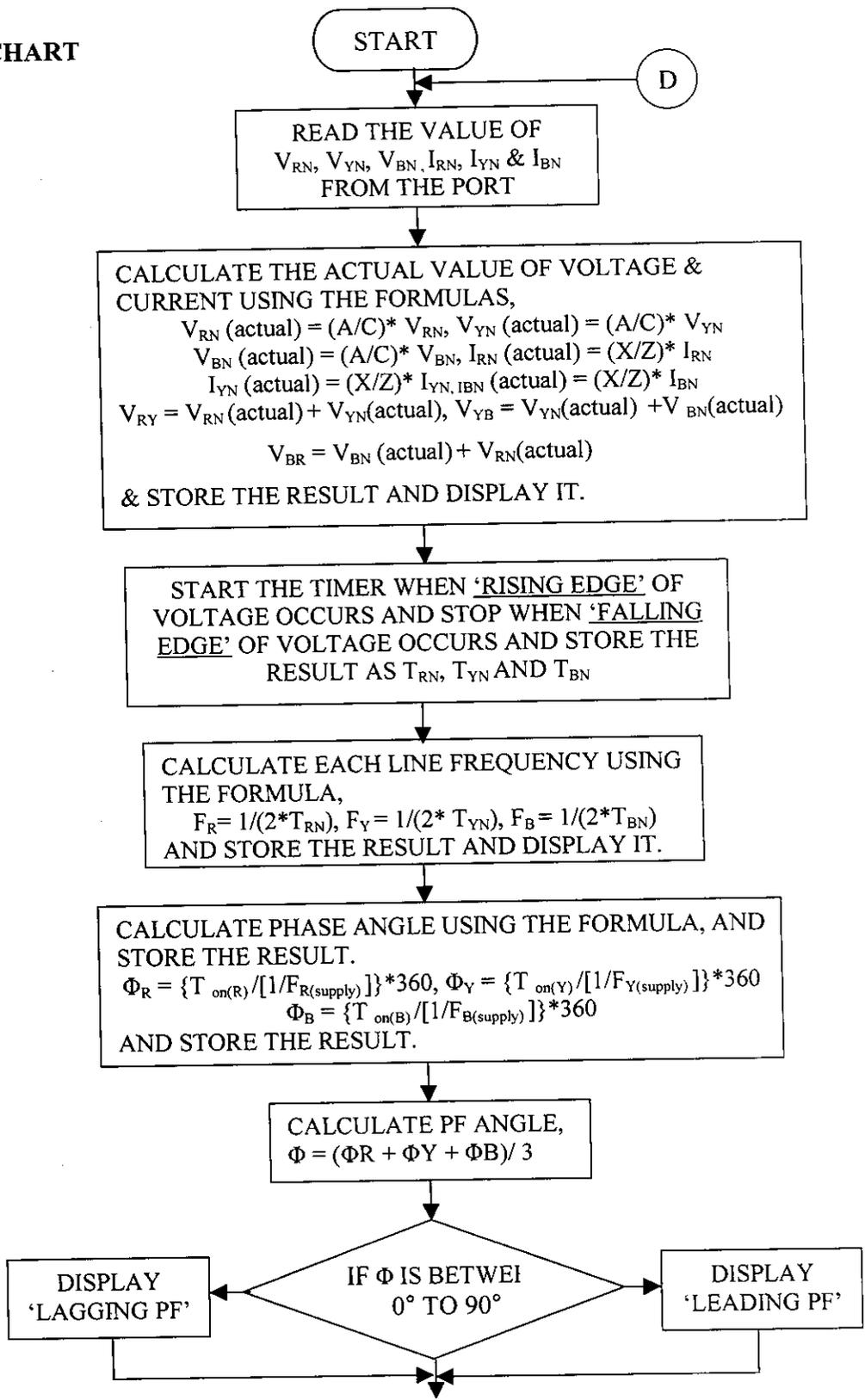
$$S_Y = V_{YN}(\text{line}) * I_Y(\text{actual})$$

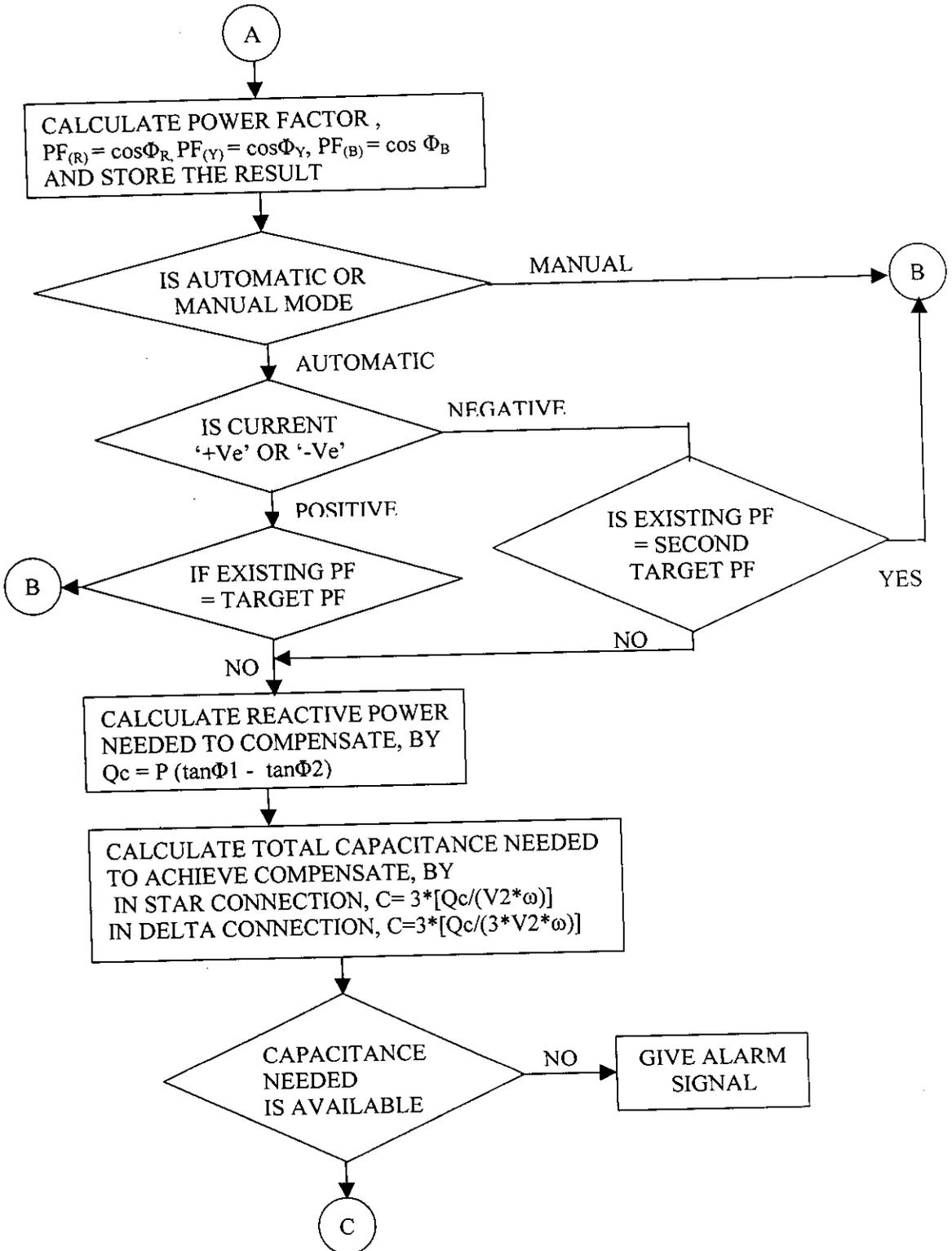
$$S_B = V_{BN}(\text{line}) * I_B(\text{actual})$$

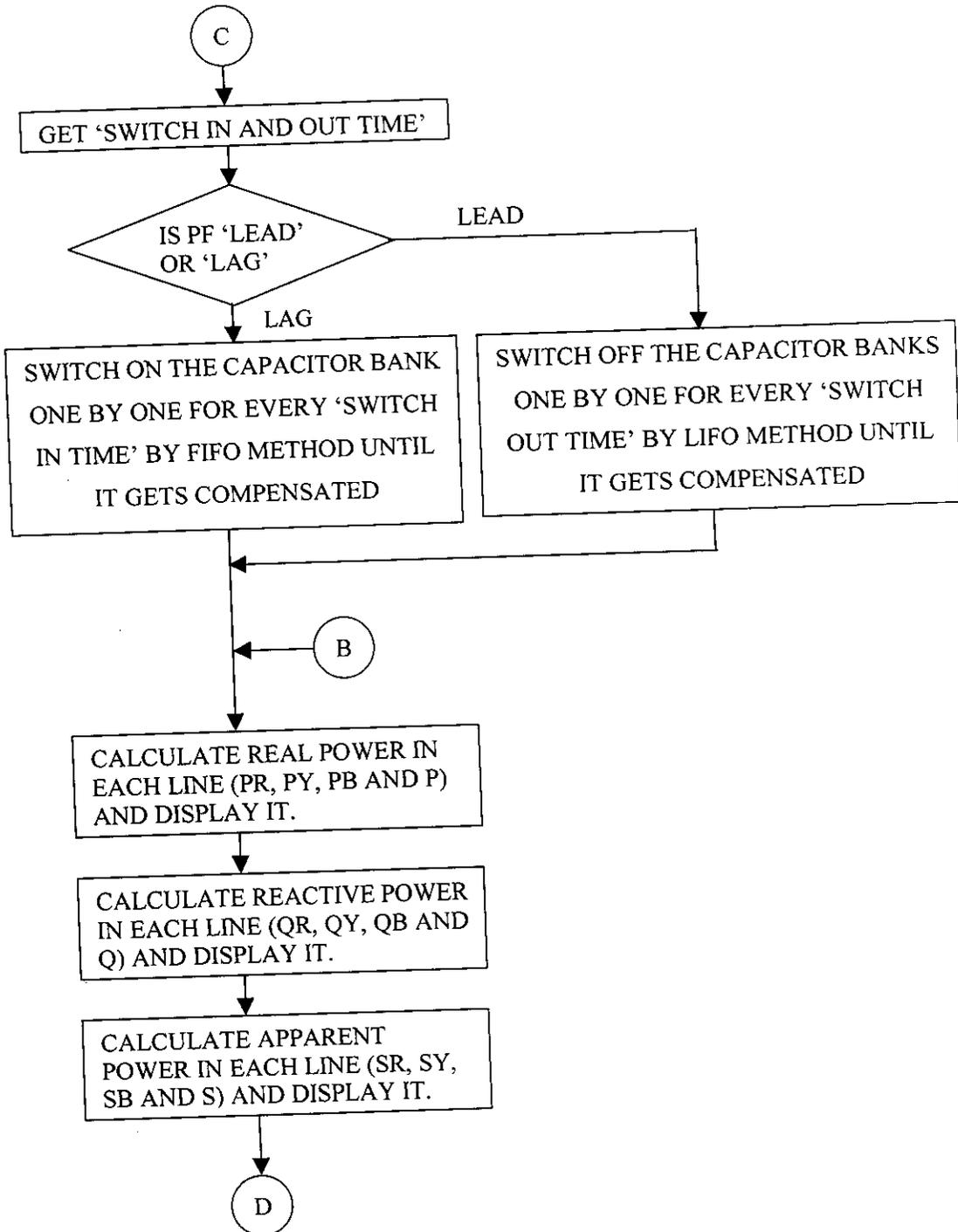
$$S = S_R + S_Y + S_B$$

and store the result and display it.

6.5 FLOWCHART







CHAPTER 7

CONCLUSION

At the outset of the automatic power factor correction controller, it was envisaged that the PIC 16F877 would be capable of handling practically any of the computational requirements made of it within the required time frames.

The Automatic power factor correction controller has been designed and tested and its operation is found to be satisfactory. With the adoption of PIC 16F877 controller to control the power factor in an APFC panel, new generation of power factor correction technology is developed with high performance and capability to save a considerable amount of energy. The power factor without APFC compensation is found to be 0.707 and after the inclusion of the APFC controller in the panel it improved to 0.967. As a result a net energy saving of 27% is obtained. Obviously, the control technique in combination with slow phase detection was the cause of most problems. The measured speed of the phase interpolation was around $300 \mu\text{s}$, when the minimum switching times for even a wide tolerance practical situation was at most $100 \mu\text{s}$. One useful aspect that did surface in testing was the look-up table implementation. It was able to calculate a sin function at excellent accuracy within $2\mu\text{s}$. Future work on this device using other control implementations should be able to use this code with confidence in its speed and accuracy.

The advantage of this controller over other controllers is that, the power factor is controlled dynamically.

1. Time delay for the disconnection of capacitor bank is inbuilt.
2. Errors in human reading can be avoided.

APPENDIX 1

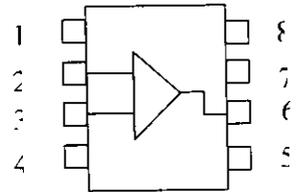
DESCRIPTION OF ICs USED

AD 741 (Operational Amplifier)

Pin Details

- | | |
|------------------|------------------|
| 1. OFFSET NULL | 2. INV INPUT |
| 3. NON-INV INPUT | 4. - Vcc |
| 5. OFFSET NULL | 6. OUTPUT |
| 7. + Vcc | 8. NO CONNECTION |

IC 741



Characteristics:

Supply voltage: $\pm 22V$

Supply current: 1.7mA

Input offset voltage: 20mV

Input offset current: 20nA

Input bias current: 80nA

Input resistance: $2M\Omega$

Input capacitance: 1.4pF

Input voltage: $\pm 13V$

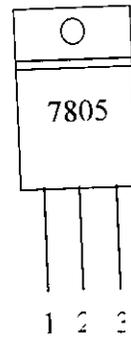
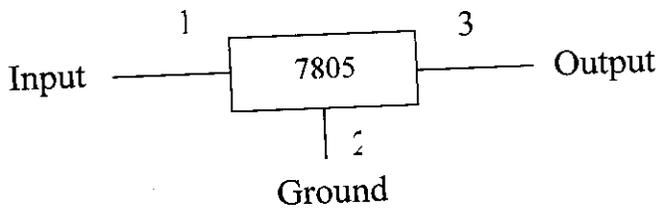
Power consumption: 50mW

Slew Rate: $0.5V/\mu\text{sec}$.

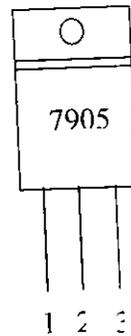
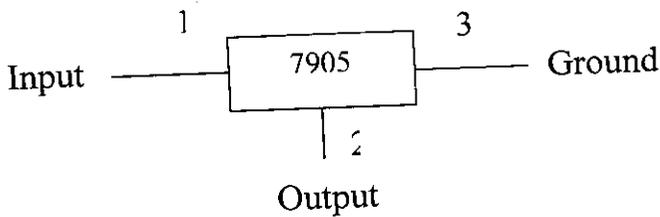
Operating Temperature Range: -55°C to 125°C

VOLTAGE REGULATOR

Positive voltage regulator(7805):



Negative voltage regulator(7905):



Characteristics:

Output voltage: $\pm 5V$

Line Regulation: 100mV

Quiescent current: 8mA

Output Noise Voltage: 40 μ V

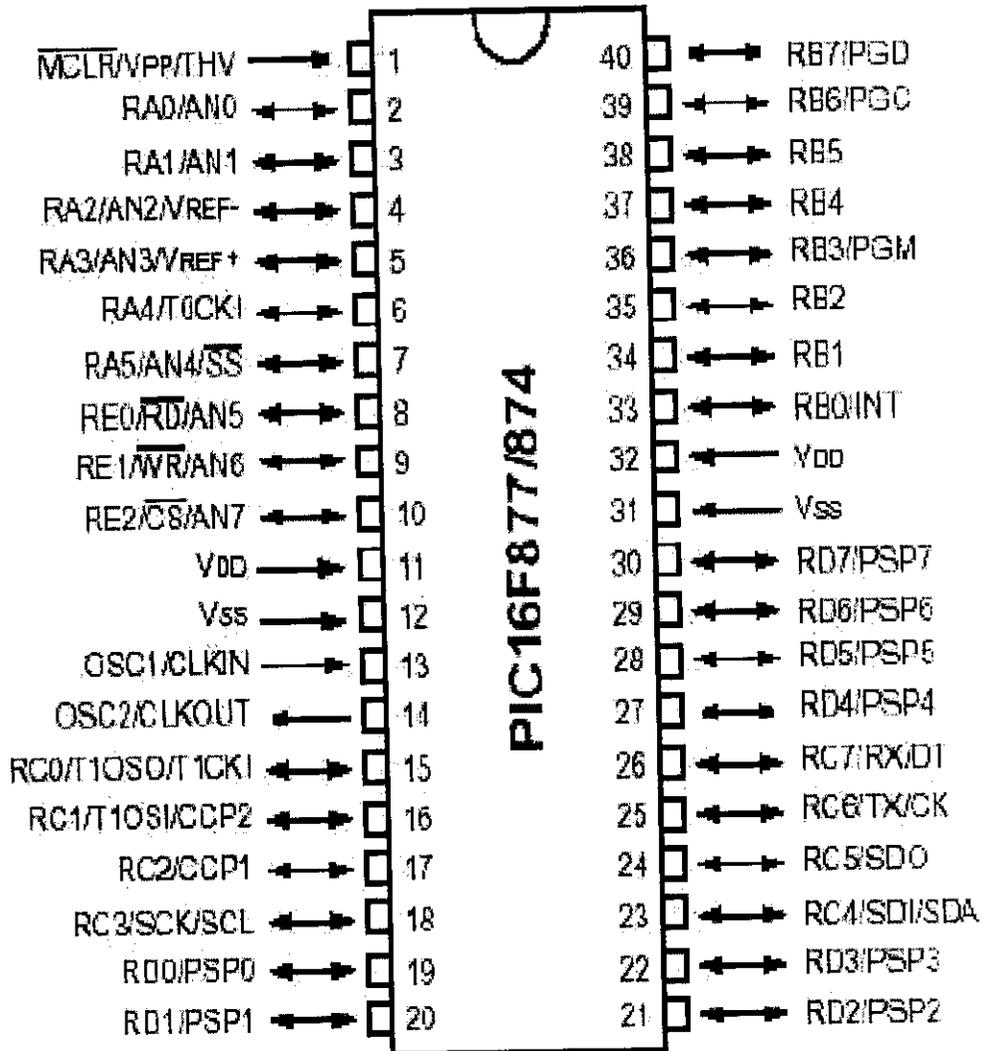
Output Resistance: 17m Ω

Short Circuit Current: 750mA

Peak Output Current: 2.2A

Average Temperature coefficient of output voltage: 1.1mV/°C.

PINDIAGRAM OF PIC 16F877



PIN DIAGRAM OF 8254 (INTERVAL TIMER)

(In the circuit it is used as external timer)

Pin 8-1: (D0- D7)- Data bus 8 bit.

Pin 9: Clock 0

Pin 10: Out 0

Pin 11: gate 0

Pin 12: ground

Pin 13: out 1

Pin 14: gate 1

Pin 15: clock 1

Pin 16: gate 2

Pin 17: out 2

Pin 18: clock 2

Pin 19: counter select (A0)

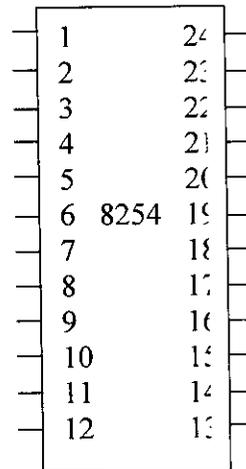
Pin 20: counter select (A1)

Pin 21: chip select (CS)

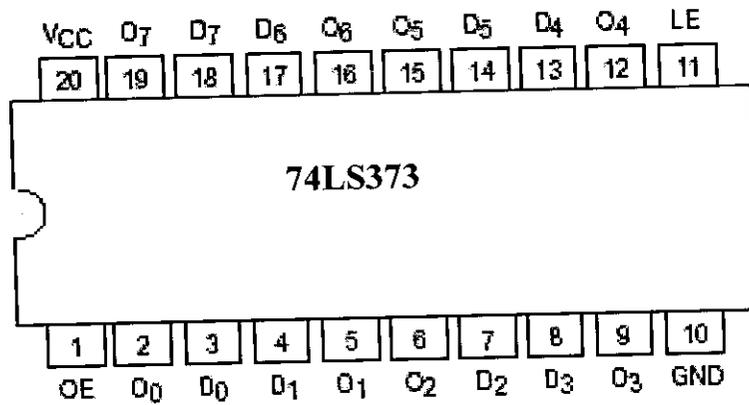
Pin 22: read counter (RD)

Pin 23: write command or data(WR)

Pin 26: supply (+Vcc)



PIN DIAGRAM OF 74LS373



D0–D7 - Data Inputs

LE - Latch Enable (Active High) Input

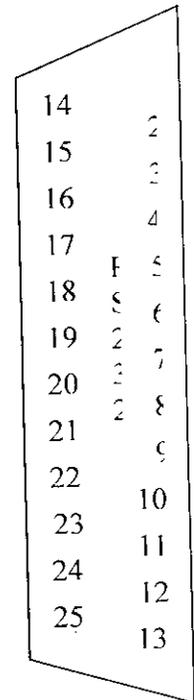
CP - Clock (Active High Going Edge) Input

OE - Output Enable (Active Low) Input

O0–O7 - Outputs

PIN DIAGRAM OF RS232

1. Protective ground
2. Transmitted data (TXD) – DCE
3. Received data (RXD) - DTE
4. Request to send (RTS) – DCE
5. Clear to send (CTS) – DTE
6. Data set ready (DSR) – DTE
7. Signal ground
8. Received line signal detector
9. (Reserved for dataset testing)
10. (Reserved for dataset testing)
11. Unassigned
12. Sec. Rec'd line signal detector
13. Sec. Clear to send
14. Secondary transmitted data
15. Transmission signal element timing (DCE source)
16. Secondary received data
17. Receiver signal element timing (DCE source)
18. Unassigned
19. Secondary request send
20. DCE - data terminal ready (DTR)
21. Signal quality detector
22. Ring indicator
23. Data signal rate selector (DCE/DTE)
24. Transmit signal element timing (DTE)
25. Unassigned



APPENDIX 2

CONTROL WORDS FOR 16F877

TIMER

Timer0 control register:

RPTU(1)	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0
---------	--------	------	------	-----	-----	-----	-----

bit 7 RPTU(1): Weak Pull-up Enable bit

1 = Weak Pull-ups are disabled

0 = Weak Pull-ups are by individual port latch values

bit 6 INTEDG: Interrupt Edge Select bit

1 = Interrupt on rising edge of INT pin

0 = Interrupt on falling edge of INT pin

bit 5 TOCS: TMR0 Clock Source Select bit

1 = Transition on TOCK1 pin

0 = Internal instruction cycle clock (CLKOUT)

bit 4 TOSE: TMR0 Source Edge Select bit

1 = Increment on high-to-low transition on TOCK1 pin

0 = Increment on low-to-high transition on TOCK1 pin

bit 3 PSA: Prescaler Assignment bit

1 = Prescaler is assigned to the WDT

0 = Prescaler is assigned to the Timer0 module

bit 2 0 Prescaler Rate Select bit

Timer1 control register

-	-	TICKPS1	TICKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON
---	---	---------	---------	---------	--------	--------	--------

bit 7:6 Unimplemented (Read as 0)

bit 5:4 TICKPS1:TICKPS0:Timer1 Input Clock Prescale Select bit

bit 3 T1OSCEN: Timer1 Oscillator Enable bit

1 = Oscillator is enabled

0 = oscillator is shut off. The oscillator inverter and feedback resistor are tuned off to eliminate power drain.

bit 2 T1SYNC:Timer1 External Clock Input Synchronization Select bit

When TMR1CS = 1:1 = Do not synchronize external clock input

0 = Synchronize external clock input

When TMR1CS = 0:This bit is ignored.Timer1 uses the internal clock.

bit 1 TMR1CS:Timer1 Clock Source Select bit

1 = External clock from pin T1OSO/T1CKI (on the rising edge)

0 = Internal clock (FOSC/4)

bit 0 TMR1ON:Timer1 On bit

1 = Enables Timer1

0 = Stops Timer1

A/D Converter

Control Register for ADCON0

ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	-	ADON
-------	-------	------	------	------	---------	---	------

bit 7-6:ADCS1:ADCS0:A/D Conversion Clock Select bit

0 0 = FOSC/2

0 1 = FOSC/8

1 0 = FOSC/32

1 1 = FRC (clock derived from an RC oscillator)

bit 5-3 CHS2:CHS0: Analog Channel Select bit

0 0 0 = Channel0 (RA0/AN0)

0 0 1 = Channel1 (RA1/AN1)

0 1 0 = Channel2 (RA2/AN2)

0 1 1 = Channel3 (RA3/AN3)

1 0 0 = Channel4 (RA5/AN4)

1 0 1 = Channel5 (RE0/AN5)

1 1 0 = Channel6(RE1/AN6)

1 1 1 = Channel7(RE2/AN7)

bit2: GO/DONE: A/D Conversion Status Bit

if ADON = 1

1= A/D conversion in progress (setting this bit starts the A/D conversion)

0= A/D conversion not in progress (The bit is automatically cleared by hardware

when the A/D conversion is complete)

bit1: Unimplemented: Read as '0'.

bit0: ADON: A/D On bit

1= A/D converter module is operating.

0= A/D converting module is shut off and consumes no operating current.

Note1: these channels are not available on the 28-pin devices.

Control Register for ADCON1

REGISTER -2: ADCON1 REGISTER (ADDRESS 9Fh)

ADFM	-	-	-	PCFG3	PCFG2	PGFC1	PCFG0
------	---	---	---	-------	-------	-------	-------

bit7: ADFM: A/D result format select

1= right justified. 6 most significant bits of ADRESH are read as '0'.

0= left justified 6 least significant bits of ADRESL are read as '0'.

bit 6-4: unimplemented (Read as '0')

bit 3-0: PCFG3; PCFG0: A/D port configuration control bits.

Control Register for 8254

SC1	SC0	RW1	RW0	M2	M1	M0	BCD
-----	-----	-----	-----	----	----	----	-----

bit 7:6 0:0 = Counter0

0:1 = Counter1

1:0 = Counter2

1:1 = Read back command

bit 5:4 0:0 = Counter Latch command

0:1 = Read only LSB

1:0 = Read only MSB

1:1 = Read LSB first and MSB second

bit 3:2:1 0:0:0 = mode0

0:0:1 = mode1

X:1:0 = mode2

X:1:1 = mode3

1:0:0 = mode4

1:0:1 = mode5

bit 0 BCD: 0 = Counts hexadecimal to binary

1 = Counts BCD to decimal

Control Resister for LCD

Function Set

0	0	1	DL	N	F	X	X
---	---	---	----	---	---	---	---

bit 4 DL: Display select

1 = 8 bits

0 = 4 bits

bit 3 N: Number of lines

1 = 2 lines

0 = Single line

bit 2 F: Font size select

1 = 5*10 dots

0 = 5*8 dots

Display OFF

0	0	0	0	1	D	C	B
---	---	---	---	---	---	---	---

bit 2 D: Display Select

1 = Display ON

0 = Display OFF

bit 1 C: Curser Select

1 = Curser move on

0 = Curser move off

bit 0 B: Blinking (Only one character blinks at a time)

1 = Blinking

0 = No Blinking

Display Clear:

0	0	0	0	0	0	0	1
---	---	---	---	---	---	---	---

Always to clear display control word is 01h.

Entry mode set

0	0	0	0	0	1	I/D	S
---	---	---	---	---	---	-----	---

bit 1 I/D: Increment/Decrement select

1 = Increment

0 = Decrement

bit 0 S: Shift select

1 = Shift

0 = No Shift

Display ON

0	0	0	0	1	1	X	X
---	---	---	---	---	---	---	---

APPENDIX 3

CODING

PIC Programming

```
#include<pic.h >
#include<stdio.h >
#include "delay.c"
#include<string.h>

static void interrupt IntRoutine( );
void LCD_SendData(unsigned char dat);
void LCD_SendData(unsigned char cmd);
void CheckBusy();
int Cnt=0,Oflow=0,ipf=0,dval=0;
short int Flag=0,set=0,Hr=0,Lr=0;
int Adval=0;
float Acv=0,Acc=0,pf=0;
short int First=0,Second=0,Third=0,Fourth=0;
char St[15];
void Send();
void Mscrn();

void main()
{
TRISA=0xff;
TRISB=0x00;
PORTB=0x00;
TRISD=0xf0;
PORTD=0x00;
TRISE=0x00;
TRISC=0x80;
PORTD=0x0f;
PORTC=0x03;
ADCON0=0x81;
ADCON1=0x82;
SPBRG=64; //9600 @ 10Mhz Brgh=1
TXEN=1;
SYNC=0;
BRGH=1;
SPEN=1;
CREN=1;
TICON=0x00;
```

```

TMR1IF=0;
TMR1IE=1;
TMR1L=0;
TMR1IE=0;
TMR1L=0;
TMR1H=0;
TMR1ON=0;
PEIE=1; //Enable peripheral interrupts
GIE=1; //Enable global interrupts
LCD_SendCmd(0x38);
DelayMs(100);
LCD_SendCmd(0x38);
DelayMs(100);
LCD_SendCmd(0x38);
DelayMs(100);
LCD_SendCmd(0x38);
DelayMs(100);
CheckBusy();
LCD_SendCmd(0x06);
CheckBusy();
LCD_SendCmd(0x0c);
CheckBusy();
LCD_SendCmd(0x01);
CheckBusy();
LCD_SendCmd(0x02);
Mscrn();
for(;;)
{
if(RD4)
{
TMR1ON=0;
TMR1L=0;
TMR1H=0;
TMR1ON=1;
}
}

if(RD5)
{
TMR1ON=0;
Hr=TMR1H;
Lr=TMR1L;
}

ADCON0=0x91;
DelayUs(50);

```

```

ADGO=1;
While(ADGO)continue;
Adval=(ADRESH * 256) + ADRESL;
Acv=(float)Adval;
Acv=Acv/4.01;
CheckBusy();
LCD_SendCmd(0x82);
dval = (int)(Acv*10);
St[4] = (dval % 10) + 0x30;
St[3] = '.';
dval /=10;
St[1]=(dval % 10) + 0x30;
dval /= 10;

```

```

St[0] = (dval % 10) + 0x30;
CheckBusy();
LCD_SendData(St[0]);
CheckBusy();
LCD_SendData(St[1]);
CheckBusy();
LCD_SendData(St[2]);
CheckBusy();
LCD_SendData(St[3]);
CheckBusy();
LCD_SendData(St[4]);
ADCON0=0x99;
DelayUs(50);
ADGO=1;
While(ADGO)continue;
Adval=(ADRESH * 256) +ADRESL;
Acc=(float)Adval;
Acc=Acc * 5.0;
if(Acc<100)Acc=0.0;
CheckBusy();
LCD_Sendcmd(0x8a);
dval = (int)(Acc *10);
St[9] = (dval % 10)+0x30;
St[8]='.';
dval /= 10;
St[7] = (dval % 10)+0x30;
dval /= 10;
St[6] = (dval % 10)+0x30;
dval /= 10;

```

```
St[5] = (dval % 10)+0x30;
CheckBusy();
LCD_SendData(St[5]);
CheckBusy();
LCD_SendData(St[6]);
CheckBusy();
LCD_SendData(St[7]);
CheckBusy();
```

```
LCD_SendData(St[8]);
CheckBusy();
LCD_SendData(St[9]);
pf = pf / 6.1;
if(Acc<100)
{
St[13] = ' ';
St[12] = 'C ';
St[11] = 'Z';
St[10] = ' ';
}
else
{
dval = (int)(pf * 100);
St[13] =(dval % 10)+0x30;
dval /=10;
St[12] =(dval % 10)+0x30;
St[11] = '.';
dval /=10;
St[10] =(dval % 10)+0x30;
}
CheckBusy();
LCD_SendData(0xC6);
CheckBusy();
LCD_SendData(St[10]);
CheckBusy();
LCD_SendData(St[11]);
CheckBusy();
LCD_SendData(St[12]);
CheckBusy();
LCD_SendData(St[13]);
if(Pf < .200)
{
PORTD=0x0f;
}
}
```

```
else if(Pf < .350)
{
    PORTD=0x0e;
}
else if(Pf < .400)
{
    PORTD=0x0d;
}

else if(Pf < .450)
{
    PORTD=0x0c;
}
else if(Pf < .500)
{
    PORTD=0x0b;
}
else if(Pf < .550)
{
    PORTD=0x0a;
}
else if(Pf < .600)
{
    PORTD=0x09;
}
else if(Pf < .650)
{
    PORTD=0x08;
}
else if(Pf < .700)
{
    PORTD=0x07;
}
else if(Pf < .750)
{
    PORTD=0x06;
}
else if(Pf < .800)
{
    PORTD=0x05;
}
else if(Pf < .850)
{
    PORTD=0x04;
```

```

    }
    else if(Pf < .900)
    {
        PORTD=0x03;
    }
    else if(Pf < .925)
    {
        PORTD=0x042;
    }
    else if(Pf < .950)
    {
        PORTD=0x01;
    }
    else
    {
        PORTD=0x00;
    }

    Send();
    DelayMs(100);
}
}
void Send()
{
    while(!TXIF)continue;
    TXREG = '{';
    DelayUs(10);
    while(!TXIF)continue;
    TXREG =St[0];
    DelayUs(10);
    while(!TXIF)continue;
    TXREG=St[1];
    DelayUs(10);
    while(!TXIF)continue;
    TXREG=St[2];
    DelayUs(10);
    while(!TXIF)continue;
    TXREG=St[3];
    DelayUs(10);
    while(!TXIF)continue;
    TXREG=St[4];
    DelayUs(10);
    while(!TXIF)continue;
    TXREG=St[5];
}

```

```

        DelayUs(10);
        while(!TXIF)continue;
        TXREG=St[6];
        DelayUs(10);
        while(!TXIF)continue;
        TXREG=St[7];
        DelayUs(10);
        while(!TXIF)continue;
        TXREG=St[8];
        DelayUs(10);
        while(!TXIF)continue;
        TXREG=St[9];
        DelayUs(10);
        while(!TXIF)continue;
        TXREG=St[10];
        DelayUs(10);
        while(!TXIF)continue;
        TXREG=St[11];
        DelayUs(10);
        while(!TXIF)continue;
        TXREG=St[12];
        DelayUs(10);
        while(!TXIF)continue;
        TXREG=St[13];
        DelayUs(10);
        while(!TXIF)continue;
        Cnt = (PORTD & 0x0f);
        if(Cnt<=9)
            TXREG = Cnt + 0x30;
        else
            TXREG = Cnt + 0x37;
        DelayUs(10);
        while(!TXIF)continue;
        TXREG = ‘}’;
        DelayUs(10);
    }
static void interrupt IntRoutine()
{
    if(TMR1IF)
    {
        TMR1IF = 0;
        Flag = 1;
    }
}

```

```

void CheckBusy()
{
    TRISB = 0xff;
    do
    {
        RE0 = 0;
        RE1 = 1;
        RE2 = 1;
        DelayUs(20);
        RE2 = 0;
    }while(RB7);
    TRISB = 0x00;
    PORTB = 0x00;
}

void LCD_SendCmd(unsigned char cmd)
{
    PORTB = cmd;
    RE0 = 0;
    RE1 = 0;
    RE2 = 1;
    DelayUs(20);
    RE2 = 0;
}

void LCD_SendData(unsigned char dat)
{
    PORTB = dat;
    RE0 = 1;
    RE1 = 0;
    RE2 = 1;
    DelayUs(20);
    RE2 = 0;
}

void Mscrn()
{
    CheckBusy();
    LCD_SendCmd(0x01);
    CheckBusy();
    LCD_SendCmd(0x80);
    CheckBusy();
    LCD_SendData('V');
    CheckBusy();
    LCD_SendData(':');
    CheckBusy();
}

```

```

    LCD_SendCmd(0x88);
    CheckBusy();
    LCD_SendData('I');
    CheckBusy();
    LCD_SendData(':');
    CheckBusy();
    LCD_SendCmd(0xC2);
    CheckBusy();
    LCD_SendData('P');
    CheckBusy();
    LCD_SendData('f');
    CheckBusy();
    LCD_SendData(':');
}

```

CODING:

```

Private Sub Form_Load()
MSComm1.PortOpen = True
End Sub

```

```

Private Sub Timer1_Timer()
Rstr = MSComm1.Input
v1 = InStr(1,Rstr,"{")
v2 = InStr(v1+1,Rstr,"}")

```

```

If v1 > 0 And v2 > 0 Then
Rstr = Mid$(Rstr, v1 + 1, v2 - v1 - 1)
Text1.Text = Left$(Rstr, 5)
Text2.Text = Mid$(Rstr, 6, 5)
Text3.Text = Mid$(Rstr, 11, 4)
v3 = Val("&h" & Right$(Rstr, 1))

```

```

If(v3 And &H1) = &H0 Then
Label5.Caption = "Cap. Bank 1 Off"
Else
Label5.Caption = "Cap. Bank 1 On"
End If

```

```

If(v3 And &H2) = &H0 Then
Label6.Caption = "Cap. Bank 2 Off"
Else
Label6.Caption = "Cap. Bank 2 On"

```

End If

```
If(v3 And &H4) = &H0 Then  
Label7.Caption = "Cap. Bank 3 Off"  
Else  
Label7.Caption = "Cap. Bank 3 On"  
End If
```

```
If(v3 And &H8) = &H0 Then  
Label8.Caption = "Cap. Bank 4 Off"  
Else  
Label8.Caption = "Cap. Bank 4 On"  
End If
```

End If

End Sub

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REFERENCES

- [1] Edited by C.V.J.Varma, “Reduction in Transmission and distribution Losses and Remedial Measures”, publication no: 240, central board of Irrigation and Power, New Delhi: 110021.
- [2] W.H.Gothmann, “Digital Electronics an Introduction to theory and practice”,Second Edition , Prentice,USA.
- [3] Proceedings of FICCI Seminar on “Energy savers 88”,New Delhi,1988.
- [4] WINDPRO – October 2004.
- [5] “Intelligent applications for the management of electrical systems in industrial lants”, IEEE April 4-8, 1999, Brazil.
- [6] Predictive Control of Inverter Supplied Electrical Drives. IEEE D-42097 Wuppertal University, Germany.
- [7] Ned Mohan, T.U., William Robbins, *Power Electronics*. 2nd ed. 1995: John Wiley & Sons, Inc.
- [8] Predictive control of power factor in industrial plants, IEEE paper no.PCIC9215
- [9] “Thyristorised power controllers” by G K DUBEY ,S R DORADLA ,A JOSHI,RMK SINHA

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