

# Microprocessor Based Dynamic Braking of Three Phase Induction Motor

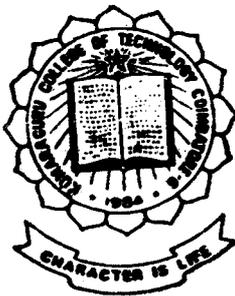
## PROJECT WORK

Submitted in partial fulfilment of the requirements  
for the award of degree of

**BACHELOR OF ENGINEERING**

**in Electrical & Electronics Engineering**

of the Bharathiar University, Coimbatore-641 046



1991 - 92

P-142

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**CERTIFICATE**

This is to Certify that the project entitled  
**Microprocessor Based Dynamic Braking of  
Three Phase Induction Motor**  
has been Submitted by

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S. 2007-2008

In partial fulfilment of the requirements  
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**BACHELOR OF ENGINEERING**

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Branch of the Bharathiar University, Coimbatore-641 046

During the academic year 1991 - '92

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## ACKNOWLEDGEMENT

We are profoundly grateful to our Project Guides **Mr.V.CHANDRASEKARAN, B.E.,** and **Miss.N.UMA DEVI, B.E.,** Associate Lecturers of the Department of Electrical and Electronics Engineering for their valuable guidance and kind encouragement for the successful completion of the project.

Words cannot express our gratitude towards **Dr.K.A.PALANISWAMY, Ph.D., M.I.S.T.E., F.I.E.,** Professor and Head of the Department of Electrical & Electronics Engineering, for his timely advice, valuable and helpful suggestions for a smooth sailing during the course of the project. We also thank him for providing us with the necessary infrastructure to carry out this project.

We are greatly obliged to our Principal, **Major T.S.RAMAMOORTHY, B.E., M.I.S.T.E.,** who was a moving force behind the successful completion from start to stop.

We also extend our sincere thanks to the faculty members of the Department of Electronics & Communication Engineering and the Department of Computer Science and Engineering for their whole-hearted co-operation by providing instruments for the testing purpose of this project.

We would be failing in our duty if we do not thank **Mr.C.KARTHIKEYAN, M.E.**, an Engineer of M/s.TEXMO INDUSTRIES PRIVATE LIMITED for his idea behind which the project has turned out to be a success.

Last but not the least, we would like to thank the laboratory technicians who helped us directly or indirectly for the successful completion of the project.

## SYNOPSIS

"DYNAMIC BRAKING" is one of the important methods of braking an Induction Motor. It is executed by passing a d.c. current through two of the three phases of the motor. In this project, a hardware circuit is designed & fabricated to implement dynamic braking. The d.c. current that passes through the motor produced by a Half Controlled Full Wave Bridge Rectifier. The gate triggering of the SCRs is done by a control circuit.

The command signal to the control circuit is given from a 8085 microprocessor interfaced with a 8253 Programmable Interval Timer. The Master Program is developed and stored in the EPROM. A look-up-table containing various values of number of gate triggering pulses for corresponding values of braking time are stored in the microprocessor. For a specified braking time, the corresponding firing angle for SCRs is selected and they are triggered so as to produce the d.c. current. This activates the contactor in such a way as to disrupt a.c. and sends d.c. thereby dynamic braking is achieved.

## CONTENTS

PAGE NO.

CERTIFICATE

ACKNOWLEDGEMENT

SYNOPSIS

<b>I</b>	<b>INTRODUCTION</b>	1
<b>II</b>	<b>BRAKING OF INDUCTION MOTORS</b>	5
	2.1 Double Cage Induction Motor	5
	2.2 Braking Methods	6
<b>III</b>	<b>CONVERTER</b>	21
	3.1 Fully Controlled Converter	21
	3.2 Half Controlled Bridge Rectifier	23
<b>IV</b>	<b>DESIGN OF HARDWARE</b>	32
	4.1 Block diagram	
	4.2 Circuit diagram	
	4.3 Zero Crossing Detection	33
	4.4 Sequential Firing of SCRs	36
	4.5 Half Controlled Rectifier Circuit	37
	4.6 Power Supply for Control Circuit	38
<b>V</b>	<b>SOFTWARE</b>	49
	5.1 The 8085 Microprocessor - General	49
	5.2 The 8253 Programmable Interval Timer	53
	5.2(i) Control Word Format	57

	<b>PAGE NO.</b>
5.3 Look-up-table	58
5.4 Flow chart	59
5.5 Program	60
<b>VI EXPERIMENTAL SET UP</b>	<b>63</b>
<b>VII CONCLUSIONS</b>	<b>67</b>
<b>REFERENCES</b>	
<b>APPENDIX</b>	
<b>PHOTOGRAPHS</b>	

## CHAPTER I

### INTRODUCTION

Squirrel cage induction motors are the most widely used ones for most machine tool drives due to its simplicity, reliability, low cost and minimum maintenance requirements. Most of the requirements of general purpose machine tools are easily met by these induction motors together with simple manual controls. Gear boxes and stepped pulleys are used to transmit the power to cutting tools or work piece at different finite number of speeds. The use of gear mechanism produces vibrations and noise, hence affects the accuracy of machining.

Better machining timings and surface finish are achieved, if stepless speed control is adopted. Electro-hydraulic and electromagnetic controls are employed to get the desired smooth speed control. With the advent of thyristor controlled drives, these methods have been superseded. At present, in our country, the use of the thyristorized drives is limited to special machine tools only, as the cost of these drives is sufficiently high.

For use such as internal grinding spindles for horological applications, drilling of printed circuit boards, etc., high speed motors are generally employed. These are usually high frequency, three phase induction motors operating upto speeds of 1,80,000 rpm and giving fairly high output powers in small sizes.

The transportation of tubs along rails from the filling place to the pit bottom, where the tubs are run into cages for conveyance by the mine winder to the surface is called haulage. Normally, a squirrel cage motor with high pull-out torque is preferred because of its simple and robust construction. The drive is taken up gradually using a clutch so that the motor need not develop a high starting torque. However, often the loads require different speeds at different stages of haulage. Further, the motors are subjected to frequent starts and stops and also to braking and reversals.

This project envisages the programming of a dynamic braking system using micro-processor, 'DYNAMIC BRAKING' is employed as an effective method of braking induction motors. In this method, braking is achieved by injecting a d.c.current in the stator winding after switching off the a.c.supply. Depending on the magnitude of d.c. current, the motor, and thus the trolley bus can be stopped quickly. The magnitude of d.c. current depends on the load current already flowing in the stator and the braking time required. This can be controlled by the programmable device. The required braking time is entered in the programmable device. A suitable d.c. current has to be selected now. The firing angle for the phase controlled rectifier is determined from the look-up-table for this d.c.current.

The a.c. supply to the Induction Motor is switched off and the d.c. current is injected into the motor and the braking period starts. At the end of the braking time, the motor is brought to rest.

The characteristics of the double cage induction motor, the various braking techniques and the advantages of dynamic braking over other types of braking are elaborated in chapter II.

Chapter III deals with the various types of SCR converters. It explains the half controlled bridge converter in symmetrical configuration which is used in this project to obtain d.c. current necessary for injecting into the motor.

Chapter IV deals with the hardware part of the project which involves the following:

- (i) Zero crossing detection
- (ii) Logic circuits for sequential firing of SCRs with delay angle (firing angle) for generation of d.c.current.
- (iii) Half-controlled rectifier circuit.
- (iv) Power supply for control circuit.

The microprocessor 8085, interfaced with the programmable interval timer 8253, is used as the programmable device

to detect the load current and the speed and to generate the required firing angle for the required d.c. current to achieve braking within the stipulated time.

Chapter V deals with the software for the above purposes. The braking time is entered in the micro-processor. A look-up-table relating the firing angle and the time is provided. The entry of the braking time selects the firing angle from this table and suitable d.c. current required for the braking is generated.

The experimental set-up and results are given in Chapter No.VI.

The details of various components used are given in appendix.

## CHAPTER II

### BRAKING METHODS

#### 2.1 Double Cage Induction Motor

High starting torque being the requirement of trolley buses, special type of induction motors like double cage induction motors are used in them. A double cage induction motor has two independent cages on the same rotor, one is shown in figure 2.1 (a). The outer cage consists of bars of high resistance material while the inner cage is of low resistance material.

Because of the location, the reactance offered by the outer cage will be low and it will be resistive, whereas the inner cage being situated deep in the rotor, will have a large ratio of reactance-to-resistance. The outer cage develops maximum torque at the time of starting. The frequency of the induced emf in the rotor is high at the time of starting and the reactance of the inner cage and hence its impedance will be high. Therefore, very little current flows in it. Most of the starting current is confined to outercage despite its high resistance. Hence, the motor develops a high starting torque due to the high resistance in the rotor.

As the speed increases, the frequency of the rotor emf decreases. The reactance and hence the impedance of the inner cage decreases and becomes very low under normal running conditions. Most of the current then flows through it and hence it develops the greater part of the motor torque while running. In fact, when the speed is normal, frequency of motor emf is so small that the reactances of both cages become practically negligible. The current is carried by the two cages in parallel, giving a low combined resistance.

The torque-speed characteristics of a double cage motor may be approximately considered to be the sum of the torques developed by two motors, one having a high resistance rotor and the other having a low resistance one. Fig.2.1 (b).

## **2.2 Braking Methods**

The motor can be stopped by switching off the supply. But it continues to run for quite sometime due to its stored kinetic energy and it takes some time before it comes to rest. The larger the moment of inertia and speed, greater will be the time taken by it. The process by which the motor can be brought to rest in a short time is called braking.

A motor (along its load) may be brought to rest quickly by using either (i) Friction Braking or Mechanical Braking

(ii) Electric Braking. Mechanical Braking has one drawback- it is difficult to achieve a smooth stop because it depends on the condition of the braking surface as well as on the skill of the operator.

Electric braking methods eliminate the need of brake lining, levers and other mechanical gadgets. It is superior to mechanical braking since it is much quicker and reliable. In electric braking, the kinetic energy of the motor is converted into electrical energy and is dissipated as heat in a resistance or returned to the supply system. The former is called 'plugging' and the latter 'Regenerative'. In addition to this method called "Dynamic Braking". The three classifications of electrical braking are explained below:

**(i) Regenerative braking**

During regenerative braking, electrical energy converted from the kinetic energy is returned to the supply. In the case of induction motors, it is possible if the motor is caused to run at more than its synchronous speed. Several speed-torque characteristics of an induction motor plotted in the various quadrants of the speed-torque co-ordinate axes for different conditions of operation are shown in fig.2.2. The characteristics shown in quadrant I illustrate motoring operation with three

different values of the rotor circuit resistance. As the motor begins to approach the ideal no-load speed i.e., its synchronous speed, the torque is seen to approach zero.

On any further increase in the rotor speed under the effect of some external torque and hence, when  $\omega > \omega_0$ , the motor will operate as a generator parallel to the source of supply and will return electric energy to it. The regenerative braking operation thus set up is represented graphically by the portions of the speed-torque characteristics extended into the upper part of quadrant II. The maximum torque developed on generating operation will reach a higher value than that on motoring operation. In practice, this mode of braking finds application in drives with pole changing motors as well as in hoisting machinery cases. (crane hoists, excavators, etc.).

#### **(ii) Plugging (or) counter-current braking**

It is another method much more widely used in drive practice. This is braking by reversal of stator connections when the motor is running, causing the reversal of the stator rotating field. A counter current operating condition can be set up when the torque  $T_L$  due to the load becomes a driving torque greater than  $T_{St}$ , the starting torque of the motor. To limit the current and to develop the requisite braking torque in a slip ring motor, it is necessary to introduce rheostatic

resistance into the rotor circuit under this counter current braking condition, steady state operation will correspond, to the point with the co-ordinates ( $W_{ss}$  ,  $T_1$  ) Fig.2.3.

### (iii) Dynamic Braking

The basis of this method is to excite the stator windings with d.c. immediately after disconnecting the three phase supply. The unidirectional d.c. will produce fixed electromagnetic poles on the stator. The rotor conductors will have an alternating emf introduced in them as they pass through fixed poles. The alternating rotor emf due to the short circuit of rotor conductors, produce high rotor currents and hence rotor fluxes. These fluxes react against the strong fixed d.c. stator field and thus brings the rotor rapidly to halt. A high  $I^2R$  loss produced instantly in the rotor, dissipates the stored kinetic energy in the form of heat.

The various methods of connecting the stator windings are shown in fig.2.5. In this project where the windings of the motor are delta connected, connection 2 shown in fig.2.5 is used. Referring to fig.2.4 for braking, the induction motor contactor 1L is opened and 2L is closed simultaneously. Contactor 1L switches of the a.c. supply and contactor 2L injects d.c. current to the stator. The speed-torque characteristics of this

braking conditions is given in fig.2.2 in the lower part of quadrant II.

The d.c. current is obtained by a half-controlled SCR bridge. By varying the firing angle to the SCRs, phase control is achieved and the magnitude of d.c. is varied. Figure 2.7 describes the characteristics braking time Vs. percentage of maximum speed for different firing angles. The motor is operated at constant speed and constant load.

The curves 1,2 and 3 describes the characteristics for the firing angle  $= 0^\circ$ ,  $= 30^\circ$  and for  $= 90^\circ$  respectively. It is obvious for that as the firing angle increases the braking time will increase.

The fig.2.6 shows the characteristics braking time Vs. percentage of maximum speed for various load currents. The motor is operated at constant speed and at constant firing angle.

Curve 1 shows the characteristics for full load current. Likewise curve 2 is for half load current and curve 3 is for quarter load current. The characteristics shows that as the load is increased, the braking time will be less.

The fig.2.8 gives the characteristics braking time Vs. percentage of maximum speed for various operating speeds. The motor is operated at constant load and constant speed.

Curve 1 shows the characteristics for 100 percent of the maximum speed. Likewise curve 2 is for 50 percent of the maximum speed. These characteristics show that, the braking time is reduced as the operating speed is reduced.

**(iii) a Dynamic braking in cage induction motor**

Dynamic braking is achieved in cage motor by applying low voltage d.c. to any two terminals of the stator winding, after removing the 3-phase supply to the stator. The d.c. voltage produces unidirectional flux in the stator. Since the rotor is still running due to inertia, the rotor conductors cut the unidirectional flux and so rotor emf is produced. Due to the short-circuited cage rotor current flows in the rotor bars and copper loss is produced. Thus the kinetic energy of rotation is converted into heat energy and so the motor stops quickly. A timing relay removes the low voltage d.c. after a definite time because continuous application of d.c to the stator winding will cause unnecessary heating in the stator winding.

In the fig.2.9, when the 'start' button is pressed momentarily the coil C is energised. Main contacts  $C_1$  close giving 3-Phase supply to the motor and the motor starts running,  $C_2$  is the sealing contact.  $C_3$  is an interlock (normally closed) which opens, so coil DB is isolated and so contacts DB, are open thus preventing application of d.c. to the stator.

When 'stop' button is pressed,  $C_1$  opens removing the 3-phase supply. Sealing contact  $C_2$  opens. Interlock  $C_3$  closes. But  $T_1$  remains closed as it is an OFF-DELAY N.O. contact. So DB is energised and contacts  $DB_1$  close giving d.c. to the stator.  $DB_2$  opens preventing energization of C. Dynamic braking takes place and the motor stops.

After a preset time-interval,  $T_1$  opens thereby energizing DB. Now the d.c. supply is removed and the motor is ready for next start.

#### **b. Jogging in cage motor**

Jogging can be easily achieved in the above circuit (fig.2.9) for dynamic braking by simply including a toggle switch S in series with a sealing contact  $C_2$  .

For normal start, the toggle switch S is kept closed. For jogging it is kept open. Therefore the coil C will be

energized only when the operator keeps pressing the 'start' button. As soon as it is released, C is de-energized and T is de-energized, d.c. is applied to the stator winding and the motor stops quickly. Thus the motor is able to run and stop in short 'jogs'.

### c. Plug-stop and plug-reversal

The direction of torque developed by the cage motor can be reversed by simply interchanging any two supply leads to the stator winding and thus reversing the phase-sequence of the supply. For this purpose, two sets of contacts  $F_1$  and  $R_1$  are necessary as shown in the fig.2.10.

When the 'button FS' is pressed, coil F is energized. Main contacts  $F_1$  close and the motor runs in forward direction. Sealing contact  $F_2$  closes mainting the supply to F. Interlock  $F_3$  opens.

#### Plug reversal

The 'stop' button is pressed momentarily. Coil F is de-energized. Contact  $F_1$  and sealing contact  $F_2$  opens. Interlock  $F_3$  closes. Since the motor is running in clockwise direction, the plug switch contact XY is closed and so the coil R is energized,

as soon as interlock  $F_3$  closes. Now the main contacts  $R_1$  close and so the direction of torque is reversed. Sealing contact  $R_2$  closes and interlock  $R_3$  opens.

The motor speed rapidly drops to zero and it starts running in reverse direction.

### **Plug stop**

If the motor is prevented from running in opposite direction, can be stopped by plugging and it is known as plug stop. For this, the stop button should be pressed continuously until the motor speed becomes zero in the forward direction. At zero speed the contact XY is broken and since the 'stop' button also is open, the coil R is not energized and so the motor stops.

The 'Plug switch' or 'Zero-speed switch' is a mechanical device mounted on the shaft of the motor so that the contact X and Z close for reverse rotation. If the motor is not running both XY and XZ are open (fig 2.10).

### **(iv) Other methods**

A motor may be stopped by applying a friction brake. A variant of this simple method uses a spring-loaded brake with

a thruster. The latter connected across the rotor slip-rings, develops a push-off thrust inversely proportional to rotor speed. Thus a steady creep speed can be obtained (eg. for mine winders), for a speed rise lowers the rotor frequency and voltage, reduces the thrust, allows the brake to tighten and controls the creep.

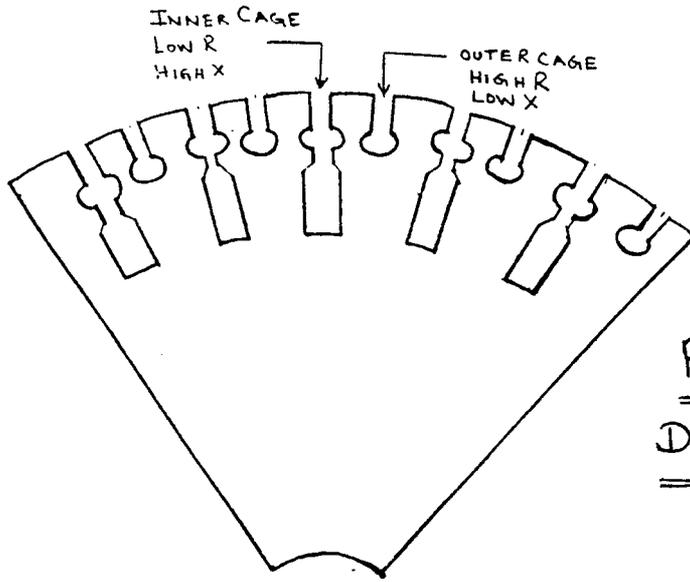


FIG. 2.1(a)  
PUNCHING FOR A  
DOUBLE CAGE ROTOR

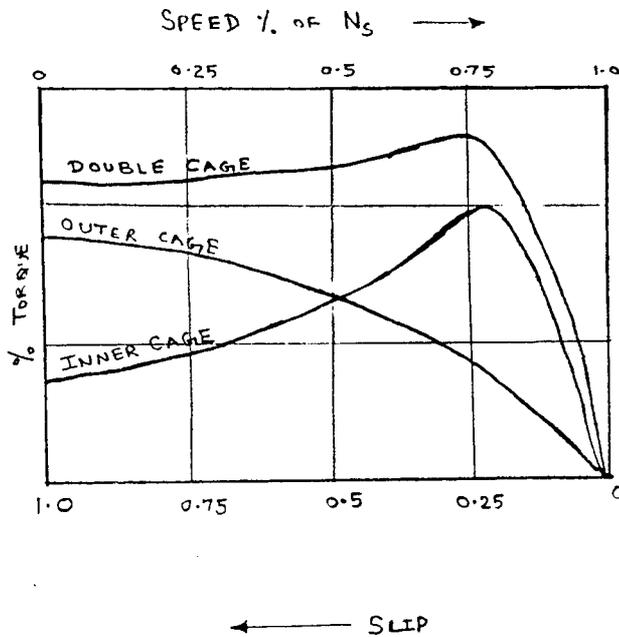


FIG. 2.1(b)  
TORQUE - SPEED  
CHARACTERISTICS  
OF A DOUBLE  
CAGE MOTOR

FIG. 2.2

N-T CHARACTERISTICS OF AN INDUCTION MOTOR FOR DIFFERENT CONDITIONS OF OPERA

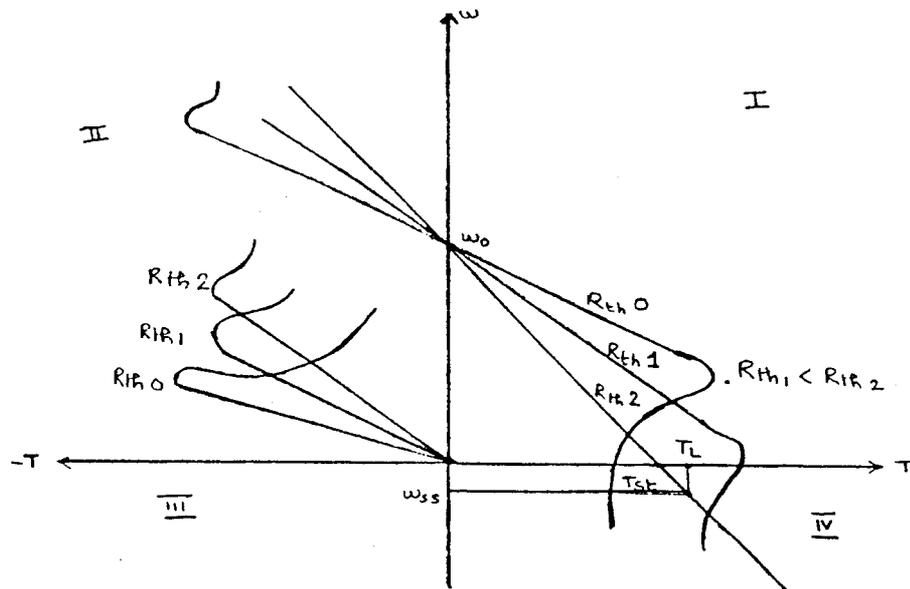


FIG. 2.3

N-T CHARACTERISTICS OF AN INDUCTION MOTOR WHEN TWO OF THE SUPPLY LEADS ARE INTERCHANGED

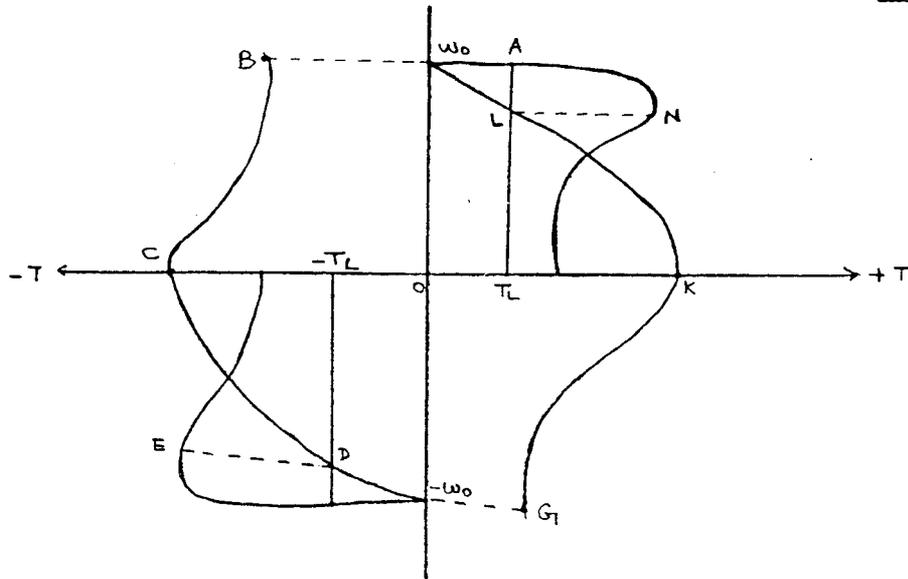


FIG. 2.6 BRAKING TIME VS. % MAX SPEED WHEN MOTOR IS OPERATED AT CONSTANT SPEED AND CONSTANT FIRING ANGLE

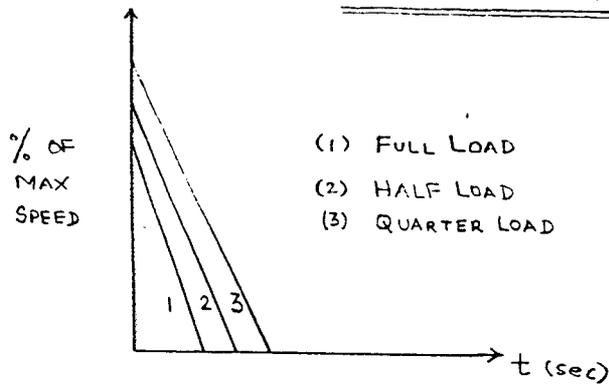


FIG. 2.7 BRAKING TIME VS. % MAX SPEED WHEN MOTOR IS OPERATED AT CONSTANT LOAD AND CONSTANT SPEED

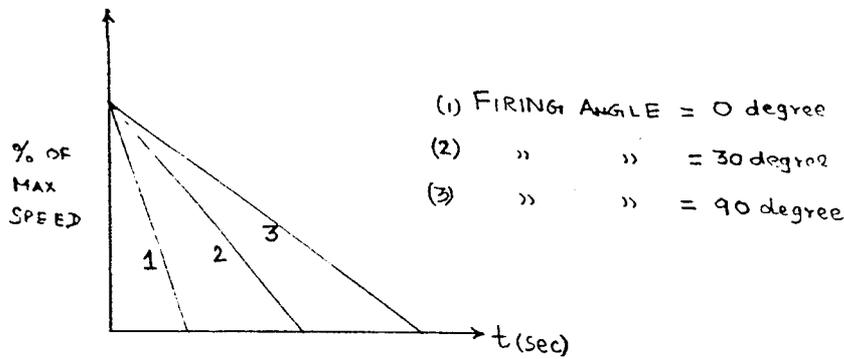


FIG. 2.8 BRAKING TIME VS. % MAX SPEED WHEN MOTOR OPERATED AT CONSTANT LOAD AND CONSTANT FIRING ANGLE

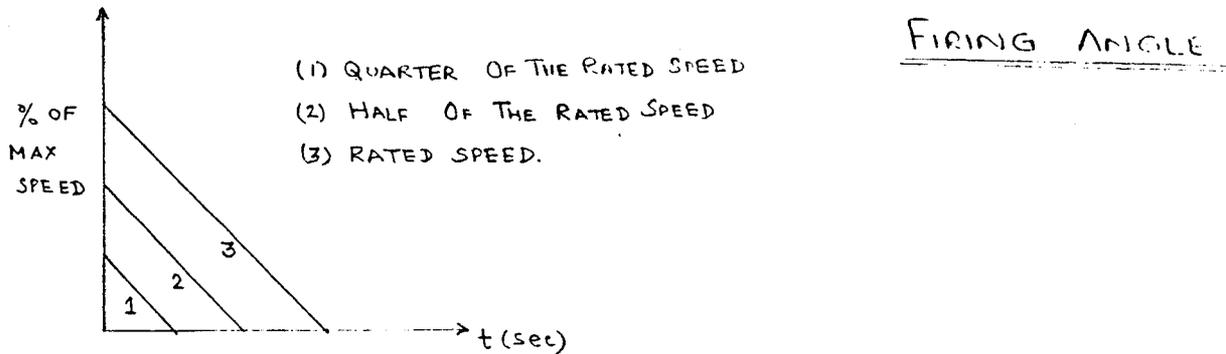


FIG. 2.4 CONNECTIONS OF A SLIP RING MOTOR  
ACCOMPLISHING DYNAMIC BRAKING.

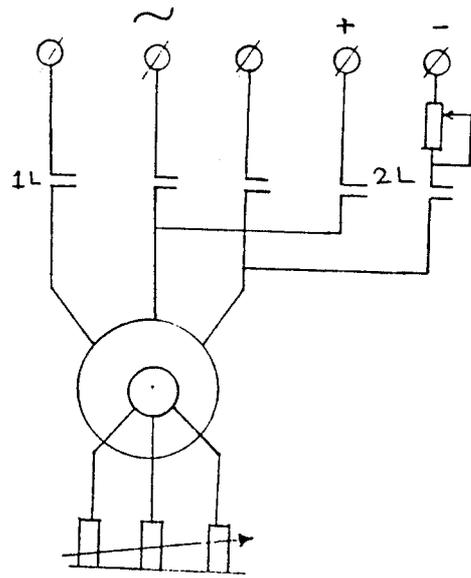
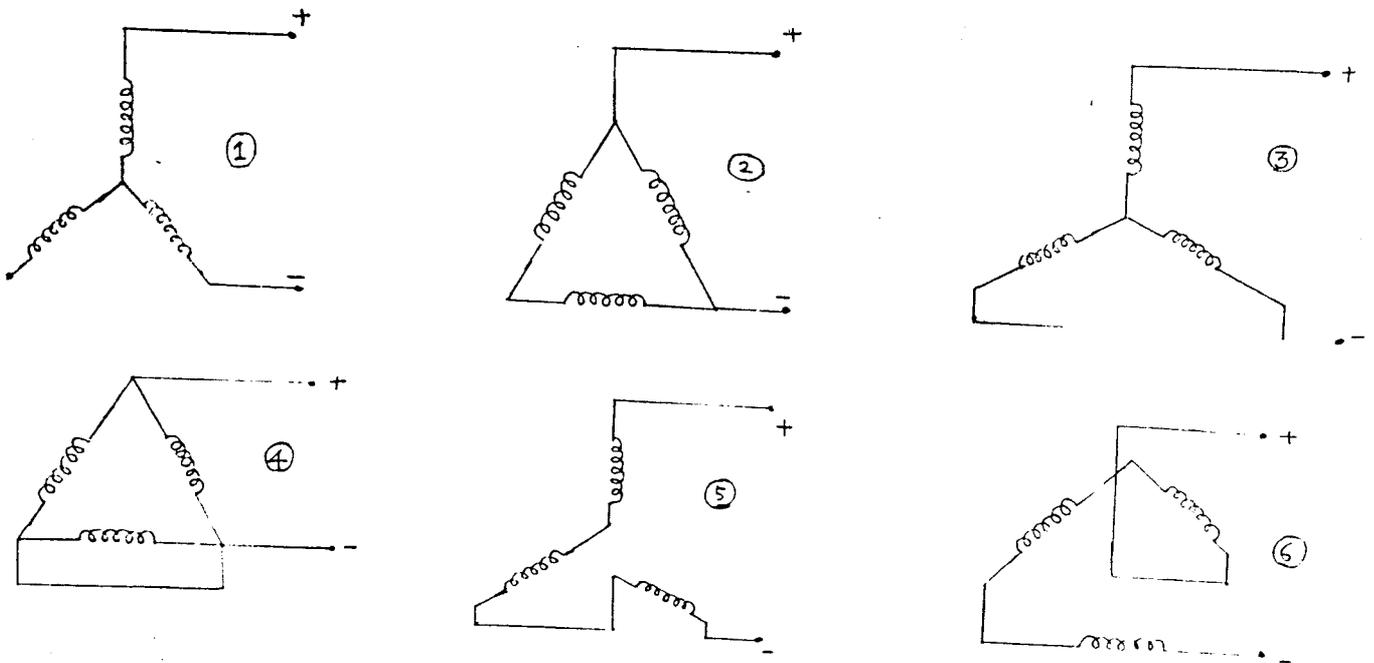


FIG. 2.5 STATOR WINDING CONNECTIONS FOR DYNAMIC B



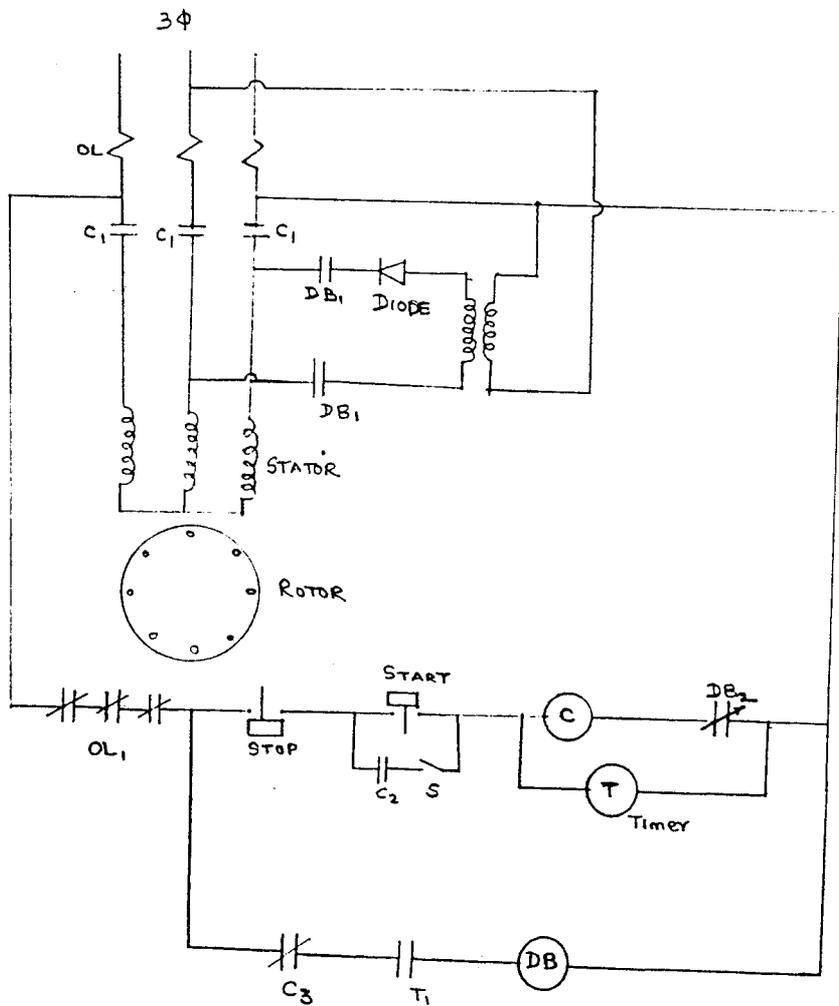
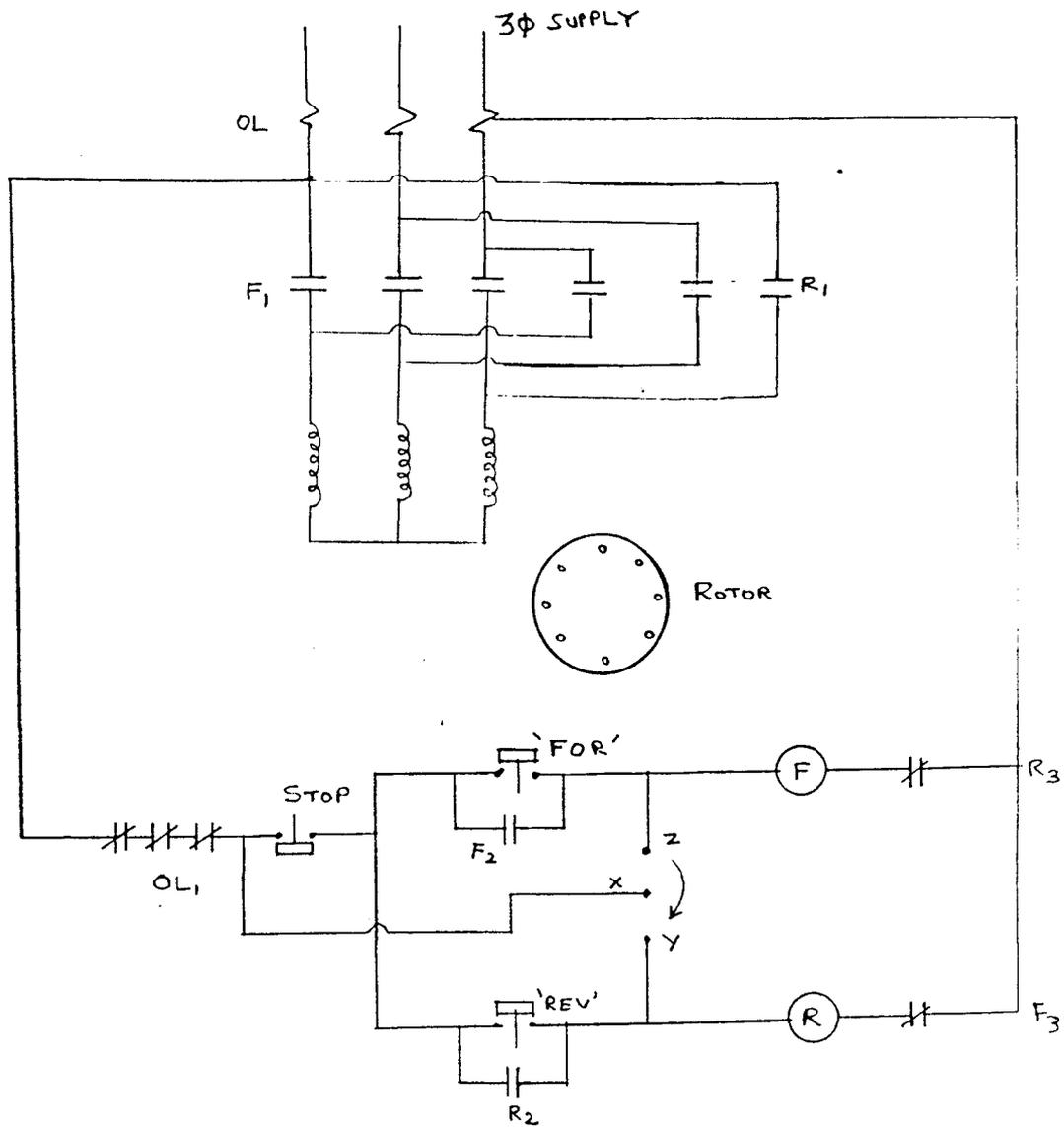


FIG. 2.9 DYNAMIC BRAKING IN CAGE MOTOR

S<sub>1</sub> CLOSED FOR NORMAL RUN

S OPEN FOR JOGGING

FIG. 2.10 CAGE MOTOR - PLUG STOP AND PLUG REVERSAL



## CHAPTER III

### CONVERTER

Earlier a.c. to d.c. conversion was achieved using motor generator sets, mercury arc rectifiers, thyratrons, metal rectifiers, rotary converters etc. With the availability of high power thyristors, presently thyristor converters are used for conversion. The SCR can be turned ON by the Gate Control at any delayed angle (firing angle) with respect to the applied voltage and the average voltage varies with the firing angle and this is known as phase control. The phase controlled thyristor converters make use of natural reversal of a.c. source voltage for commutating the thyristor which is conducting. The converters can be of two quadrant operation if the output voltage can be made either positive or negative with a given polarity of current at the output, and as single quadrant operation if the output voltage cannot be made negative with a given polarity of output current. The two quadrant converter is also known as a fully controlled converter while the latter one is known as half controlled converter.

#### 3.1 Fully controlled converter

The operation of fully controlled single phase bridge converter circuit shown in fig.3.1(a) is described below.

Thyristors  $T_1$ ,  $T_2$  and  $T_3$ ,  $T_4$  are turned on at some delay angle (firing angle) in each positive and negative half cycles of the supply voltage respectively. With the resistive load, the output voltage and current waveforms are shown in fig.3.1(b)., When the supply voltage falls to zero, the current also goes to zero and the appropriate thyristors ( $T_1$ ,  $T_2$ ) in the positive half cycle, ( $T_3$ ,  $T_4$ ) in the negative half cycle are turned off by natural commutation. The supply voltage reverse biases the two thyristors which were previously conducting until the next pair of thyristors is turned on. With the turn on of the other pair of thyristors the supply voltage appears across each thyristor as a reverse bias.

With an inductive load, having sufficient inductance, the load current becomes continuous. Each diagonally connected thyristor pair conducts for one half period of the supply frequency. When  $T_1$  and  $T_2$  are turned on together in the positive half cycle, the current flows from the source, through the thyristor  $T_1$  to the load and back to the source through the thyristor  $T_2$ . By turning on thyristors  $T_3$  and  $T_4$  after one half period from the instant of triggering thyristors  $T_1$  and  $T_2$  a negative voltage appears across the thyristor  $T_1$  and  $T_2$ , reverse biases them and turns them off by line commutation. The current flow through the a.c. source gets reversed, the load current is however uni-directional. Fig. 3.1. (c).

The average output voltage is given by  $V = \frac{2V_m}{\pi} \cos \alpha$ .  
where  $V_m$  is the RMS value of the input alternating voltage.

### 3.2 Half controlled bridge rectifier

In a two quadrant bridge converter if half the total number of thyristors are replaced by diodes, the converter circuit so formed is called the half controlled converter. The advantage of half controlled converters over fully controlled converters are

- (a) since half the thyristors are replaced by diodes, the half controlled cost less than the fully controlled converter.
- (b) The mean d.c. terminal voltage can be continuously controlled from maximum to virtually zero with increased control range of the firing angle.

Fig 3.2 shows the two configurations of the half controlled converter, with the pertinent voltage and current waveforms, for a particular firing angle. The converter circuit with the thyristors  $T_1$  and  $T_2$  connected to form a common cathode as shown in fig.3.2(a) is known as the **Symmetrical Configuration** while the circuit with the thyristors  $T_1$  and  $T_2$  connected to the same a.c. terminal as shown in fig.3.2(b) is known as the **Symmetrical Configuration**.

### Symmetrical Configuration

In this  $T_1$  is turned ON at a firing angle in each positive half cycle.  $T_1$  and  $D_1$  conduct from  $\alpha$  to  $\pi$ . When the supply voltage reverses the diode  $D_2$  is forward biased since diode  $D_1$  is already conducting. The diode  $D_2$  then turns on, and the load current passes through  $D_2$  and  $T_1$ . The supply voltage reverse biases  $D_1$  and then turns it off. Thus the load current freewheels during the interval from  $\pi$  to  $\pi + \alpha$  in each supply cycle. At the instant  $(\pi + \alpha)$  a trigger pulse is applied to the thyristor  $T_2$ . Since it is forward biased, it turns on. Consequently the supply voltage reverse biases  $T_1$  and then turns it off by line commutation. The load current now flows through  $T_2$  and  $D_2$  and the supply current  $i$ , is reversed. The supply current waveform, voltage across the thyristor  $T_1$ , output voltage and output current are shown in fig.3.2(c). Since the conduction intervals of thyristors and diodes are equal, this circuit is known as symmetrical configuration.

### Asymmetrical Configuration

In the converter circuit of fig.3.22 (b),  $T_1$  and  $D_1$  conduct from  $\alpha$  to  $\pi$  and  $T_2$  and  $D_2$  conduct from  $(\pi + \alpha)$  in each supply cycle. The free wheeling action is provided by diodes  $D_1$  and  $D_2$  from 0 to  $\alpha$  and from  $\pi$  to  $(\pi + \alpha)$  in each supply cycle. The supply current waveform voltage across the thyristor  $T_1$ , output voltage and current waveforms for a particular firing

are shown in fig.3.2(d). Due to unequal conduction intervals of thyristors and diodes, this circuit is known as the 'asymmetrical configuration'. The two converter circuits configurations are indistinguishable with regard to the output voltage and current waveform from the figures. However, the internal mechanism is different in the two converter circuits. This project uses symmetrical configuration which has some advantages over asymmetrical configuration. They are:

(a) The thyristors conduct for longer intervals in the symmetrical circuit, the thyristors used in this circuit must have a higher average current rating compared to those in the asymmetrical configuration.

(b) The cathodes of two SCRs are at the same potential in the symmetrical configuration, their gates can be connected and the single gate pulse can be used for triggering either thyristor. The particular thyristor which has the forward bias at the instant of firing will turn on. In the case of asymmetrical configuration separate pulses are to be used.

The expressions for the output voltage  $V_o$  and the fundamental RMS value of the alternating current  $I$  are given as

$$V_o = \frac{\sqrt{2} E}{\pi} (1 + \cos \alpha)$$

E be the RMS value of the a.c input voltage and  $\alpha$  be the firing angle.

$$I = \frac{2\sqrt{2}}{\pi} I_d \cos \alpha/2$$

where  $I_d$  be the direct current output and  $\alpha$  be the firing angle.

From the expression for output voltage  $V_o$ , it will be observed that for a half-controlled circuit the output voltage will always be positive as the firing angle changes from zero to  $\pi$ . In a similar manner, it can be shown that the performance of a three-phase half controlled circuit differs from that of the fully controlled circuit. However, in this case either the top three or bottom three SCRs can be replaced by the diodes for the half-control operation. Fig 3.3(a) shows a three phase half-controlled bridge. The asymmetrical configuration is not used as it introduces imbalance in the line currents on the a.c. side. If the load inductance  $L_d$  is large, the output current  $i_d$  will be maintained continuous.

# SINGLE PHASE BRIDGE CONVERTER

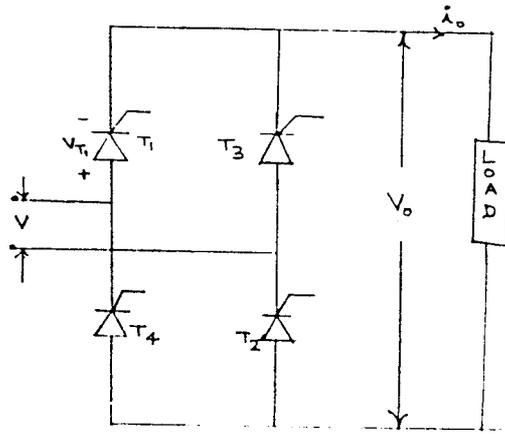


FIG. 3.1(a)

CIRCUIT CONFIGURATION

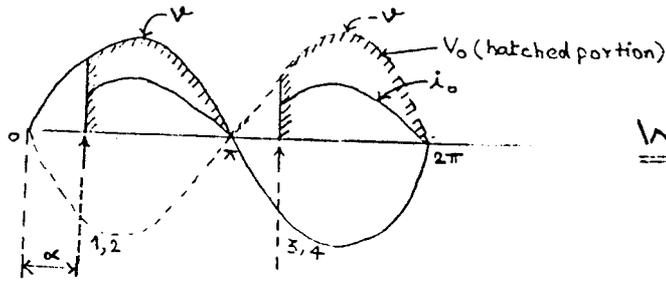


FIG. 3.1(b)

WAVEFORMS WITH RESISTIVE LOAD

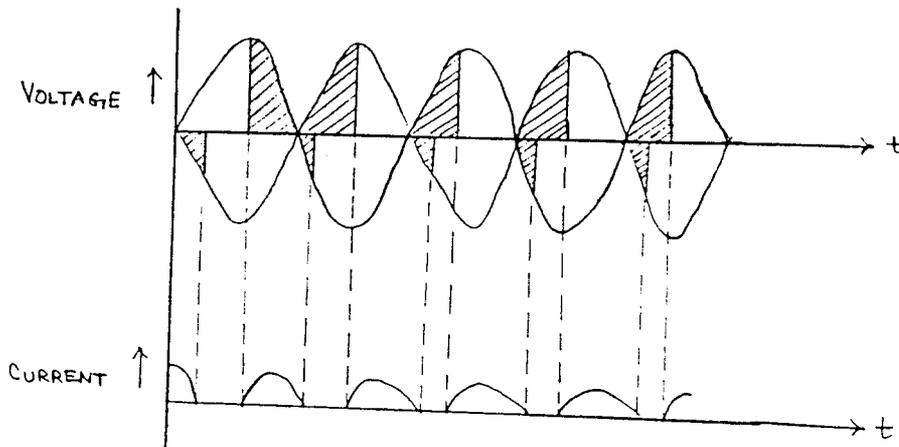


FIG. 3.1(c)

WAVEFORMS WITH

R-L LOAD

# HALF CONTROLLED BRIDGE RECTIFIER

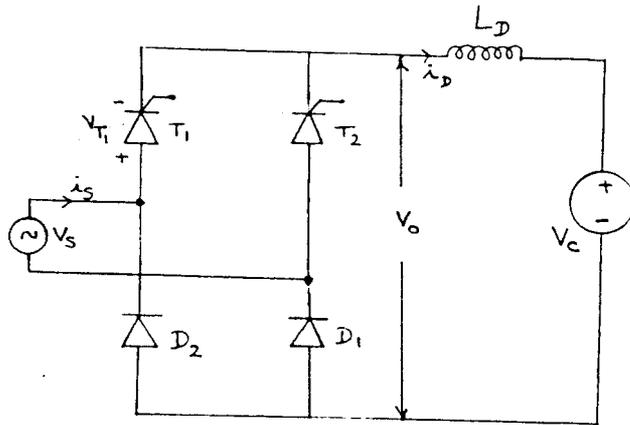


FIG. 3.2 (a)  
SYMMETRICAL  
CONFIGURATION

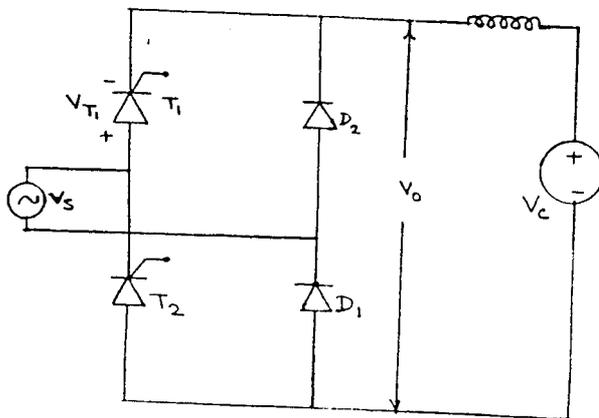
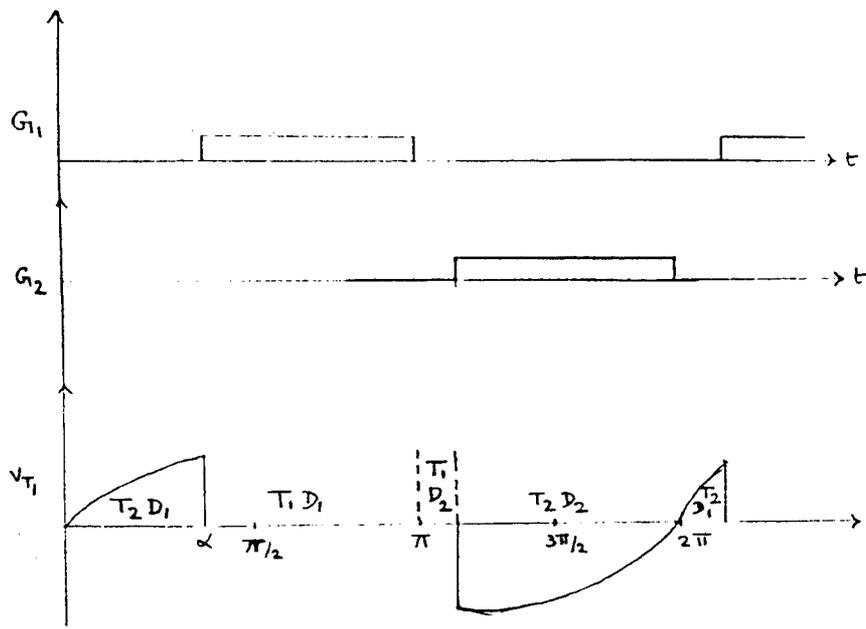


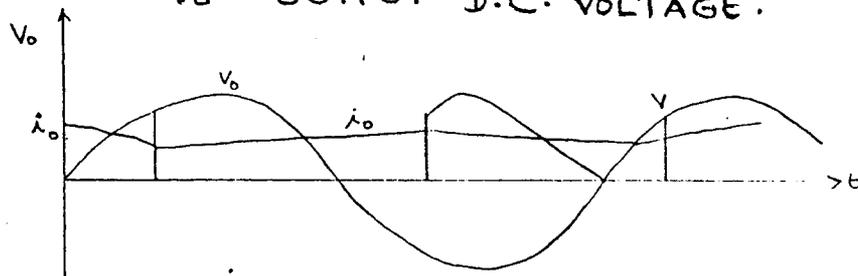
FIG. 3.2 (b)  
ASYMMETRICAL  
CONFIGURATION

FIG. 3.2 (c) WAVEFORMS FOR SYMMETRICAL CONFIGURATION



$V_{T1}$  - VOLTAGE ACROSS THYRISTOR  $T_1$ .

$V_o$  - OUTPUT D.C. VOLTAGE.



$i_o$  - OUTPUT D.C. CURRENT.

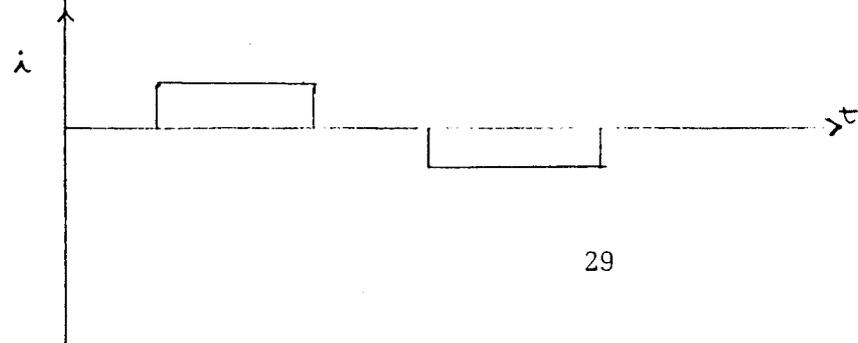


FIG. 3.2(d) WAVEFORMS OF ASYMMETRICAL

CONFIGURATION

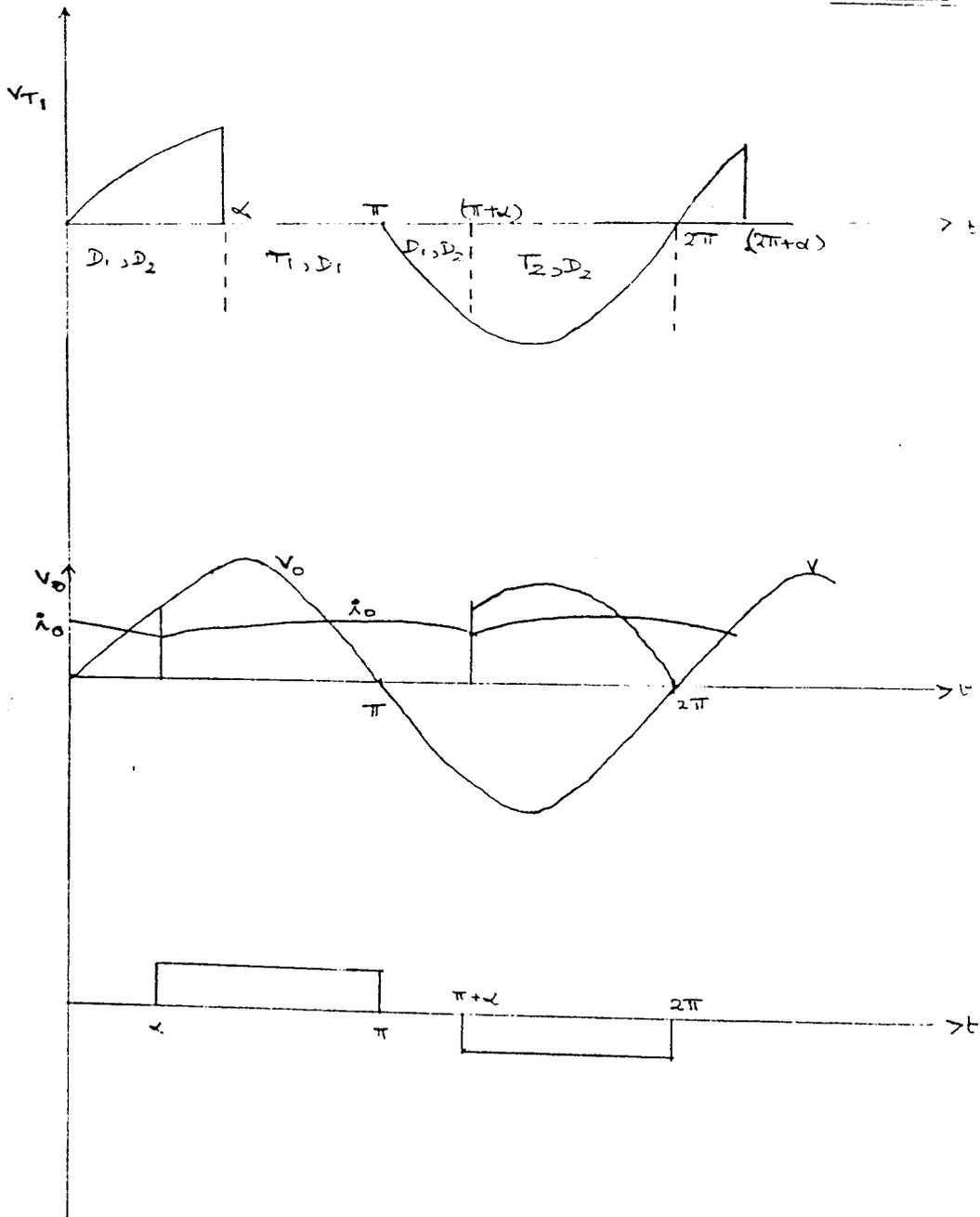
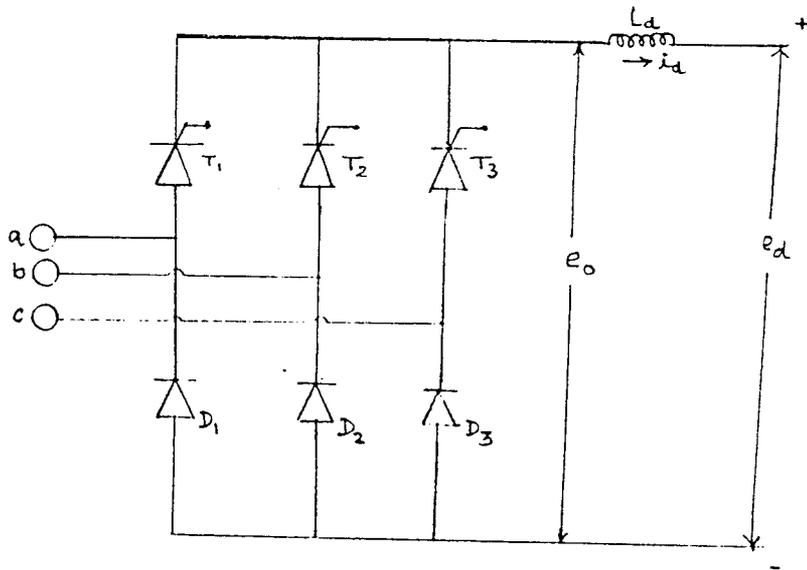


FIG. 3.3(a) THREE PHASE CONVERTER



## CHAPTER IV

### DESIGN OF HARDWARE

The block diagram of the firing circuit is shown in fig.4.1. The comparators 1 & 2 convert the positive and negative half cycles of the alternating voltage (from the 230/7.5-0-7.5 transformer) into square waves. A positive going spike at every zero crossing is obtained as the square wave passes through high pass filters (HPF 1 & HPF 2) and OR gate. This circuit is called Zero Cross Detector.

The output of the Zero Cross Detector is given to the microprocessor. The braking time is entered in the microprocessor. So a delay (firing angle) is generated in the microprocessor. The negative going pulse (output of the microprocessor) is converted into positive going pulse using the inverter. The pulses for firing the SCR 1 and SCR 2 are separated using the AND gates and the duration of the pulses are increased using the R-S flip flop. The firing pulses are applied to the SCRs through a driver.

The hardware part of the project involves the following operations:-

(i) **Zero Crossing Detection** : A positive pulse is obtained at every zero crossing point of the alternating voltage.

(ii) Logic circuits for sequential firing of SCRs with delay. (To obtain continuous firing, to generate the firing angle and to send pulses to SCRs in correct sequence)

(iii) Half controlled rectifier circuit.

(iv) Power supply for control circuits.

#### 4.3 ZERO CROSSING DETECTION

An immediate application of the comparator is the Zero Crossing Detector. It is also called line wave-to-square wave converter. The basic comparator of fig.4.1(a) or 4.1(b) can be used as Zero crossing detector provided that  $V_{ref}$  is set to zero. Fig.4.1(c) shows the inverting comparator used as Zero-Crossing Detector. The output voltage ( $V_o$ ) waveform in fig.4.1(d) shows when & in what direction an input signal  $V_{in}$  crosses zero volts. That is, the output  $V_o$  is driven into negative saturation when the input signal  $V_{in}$  passes through zero in the positive direction. Conversely, when  $V_{in}$  passes through zero in negative direction, the output  $V_o$  switches & saturates positively.

In some applications, the input  $V_{in}$  may be a slowly changing waveform, that is, a low frequency signal. Therefore, it will take  $V_{in}$  more time to cross zero volt. As a result,  $V_o$  may not switch quickly from one saturation voltage to the other. On the other hand, because of the noise at the op-amp's input terminals, the output  $V_o$  may fluctuate between two saturation voltages  $+V_{sat}$  and  $-V_{sat}$ , detecting zero reference crossings for noise voltages as well as  $V_{in}$ . Both of these problems can be cured with the use of regenerative or positive feedback that causes the output  $V_o$  to change faster and eliminate any false output transitions due to noise signals at the input.

The hardware for the zero crossing detector is shown in fig.4.2. The 230V main is stepped down to (7.5-0-7.5V) by the power supply transformer. The 7.5V is attenuated to 1V by the resistors 6.5 K & 1 K. The comparator LM339 converts the positive & negative half cycles into square pulses by comparing the 1V a.c. to the ground level. Only two comparators of the LM339 are used and the rest two are left free. The 1V a.c. is applied to the non-inverting input while the inverting input is grounded.

The first comparator converts the positive half cycle of the sinusoidal alternating voltage into square wave and the second comparator converts the negative half cycle of the sinu-

soidal alternating voltage into square wave. The pin configuration of LM339 is shown in fig.4.2(a).

The square waves are converted into spikes in the high pass filter. The high pass filter is a RC network with  $R = 33K$  and  $C = 0.022 \text{ MFD}$ . The circuit diagram is shown in fig.4.3. The high pass filter allows the high frequency component of the square waves and blocks the low frequency components. So a positive spike is obtained at every positive zero cross over in one channel. A positive spike is obtained at every negative zero cross over in the other channel.

The positive spikes of the two channel are ORed using an 'OR' gate. The OR gate is constructed using the transistors SL100. The circuit diagram is given in fig.4.4. The transistors are operated at either saturation or cut-off but nowhere else along the load line. The load line is given in fig.4.5. Soft saturation means the transistor is barely saturated, the base current is just enough to operate the transistor at the upper end of the load line. Hard saturation means the transistor has sufficient base current to be saturated under all operating conditions. To get hard saturation  $I_{c(sat)}$  is made approximately 10 times the value of  $I_{b(sat)}$ . A ratio of 10:1 is low enough to almost any transistor to remain saturated, despite temperature extremes, transistor replacement, supply voltage changing etc. By using  $470\Omega$  &  $4.7 K$  for collector & base resistances respectively the hard saturation is obtained. So the output of OR gate sends

a positive spike at every zero crossover of the a.c. supply.

#### 4.4 LOGIC CIRCUITS FOR SEQUENTIAL FIRING OF SCRs

The output of the zero crossing detector is sent to the microprocessor and it receives every positive spike. After a delay it sends out a negative going pulse. The Programmable Interval Timer 8253 is interfaced to the microprocessor 8085 for this purpose. As seen from the timing diagram of mode-5 (hardware triggered strobe), explained in the appendix, as soon as the gate is enabled by a raising pulse, the countdown is started. At the end of the count down a negative going pulse is sent out through the 'OUT' pin. The time period of negative going is one clock cycle. The microprocessor is used for the clock input.

The output of the zero crossing detector is sent to the 'GATE' of the programmable interval timer 8253 output pulses are taken from the "OUT" of the PIT 8253. So this project uses counter .

If the count is high, the firing angle will be large. If the count is low, the firing angle will be small. Since the 180 degree is covered by a large count, the resolution will be very high.

The output of the microprocessor is a negative going pulse. It is inverted into positive going pulse by using inverter. The inverter output is ANDed with the comparator outputs to separate positive half cycle firing pulses and negative half cycle firing pulses. The pulse duration is increased for continuous firing by using R-S flip flop. R-S flip flop outputs are ANDed with comparator outputs to stop firing at the end of the respective half cycles. The driving capacity of the AND gates are improved by the transistors SL100 and the SCRs  $T_1$  &  $T_2$  are properly fired. The circuit diagram for the above functions is given in fig.4.6.

The transistors SL100 are used as drives. Their collector currents are limited to maximum gate current (40A) of the SCRs by the collector resistance.

$$\text{Collector current} = 5 \text{ V} / 150 \Omega = 33 \text{ mA}$$

Using 10:1 ratio, the base resistance is 1.2 K.

The firing circuit is shown in fig.4.7 and the voltage waveform at various points in the firing circuit are shown in fig.4.8.

#### 4.5 HALF CONTROLLED RECTIFIER CIRCUIT

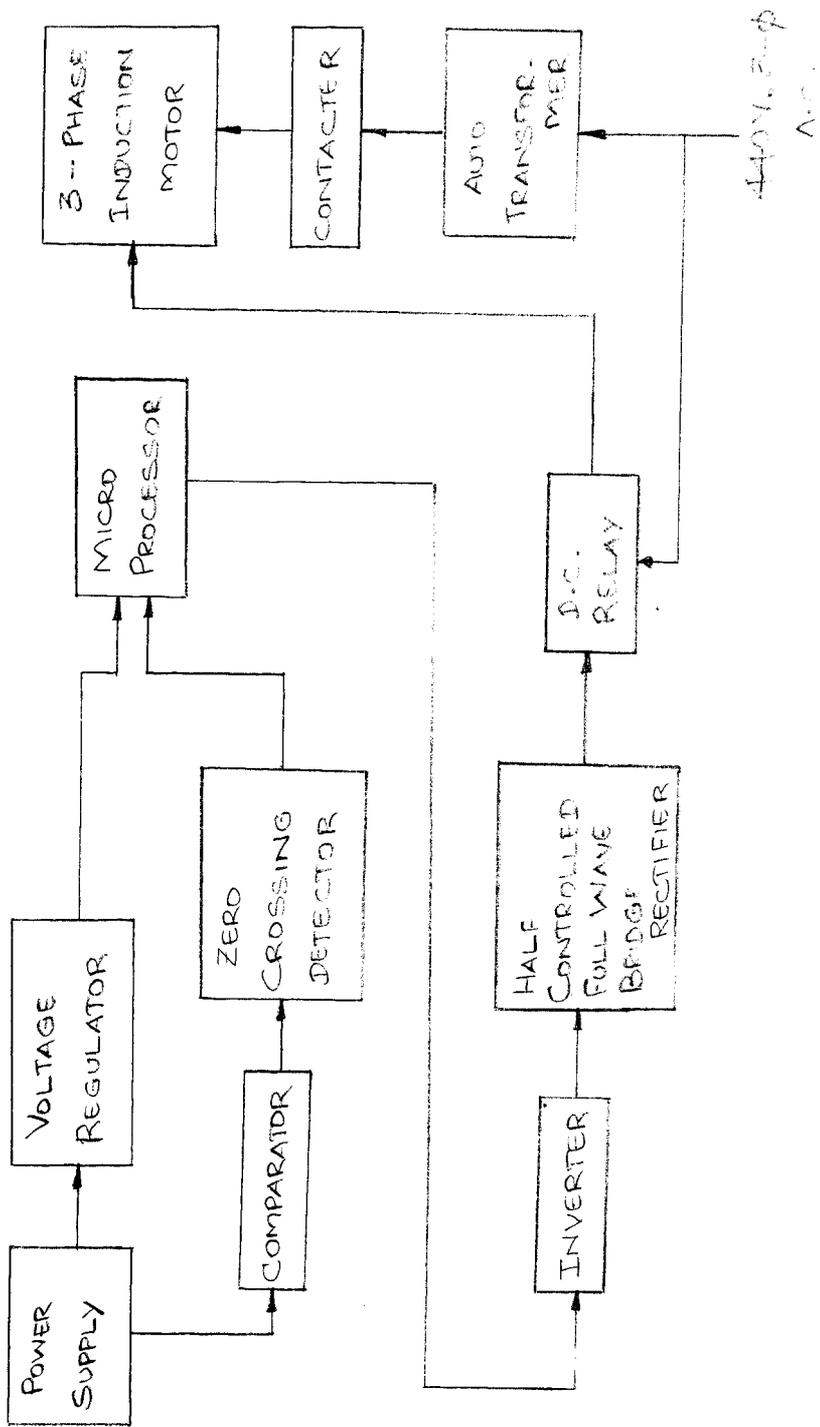
A half controlled bridge rectifier with symmetrical configuration is used in this project to obtain d.c. current necessary

for injecting into the motor during dynamic braking. Two SCRs and two power diodes are used in this project for symmetrical configuration.

#### 4.6 POWER SUPPLY FOR CONTROL CIRCUIT

A 5V power supply is required for the operation of logic gates, IC comparator and d.c.relay. The 12V supply for the comparator LM339 is taken from the microprocessor supply. The circuit diagram of the power supply is shown in fig.4.9. The 230V main is stepped down to 7.5-0-7.5V. A full wave rectifier is constructed using the diodes IN4001. A 1000 MFD, 25V capacitor is used for good regulation.

IC 7805 is used for regulating the output voltage. The input voltage to the IC 7805 is 10V. At the output, 5V regulated d.c. is obtained. The driving capacity of this power supply is 500 mA. A 1MFD, 10V capacitor is connected at the output to reduce the ripples.



Block Diagram



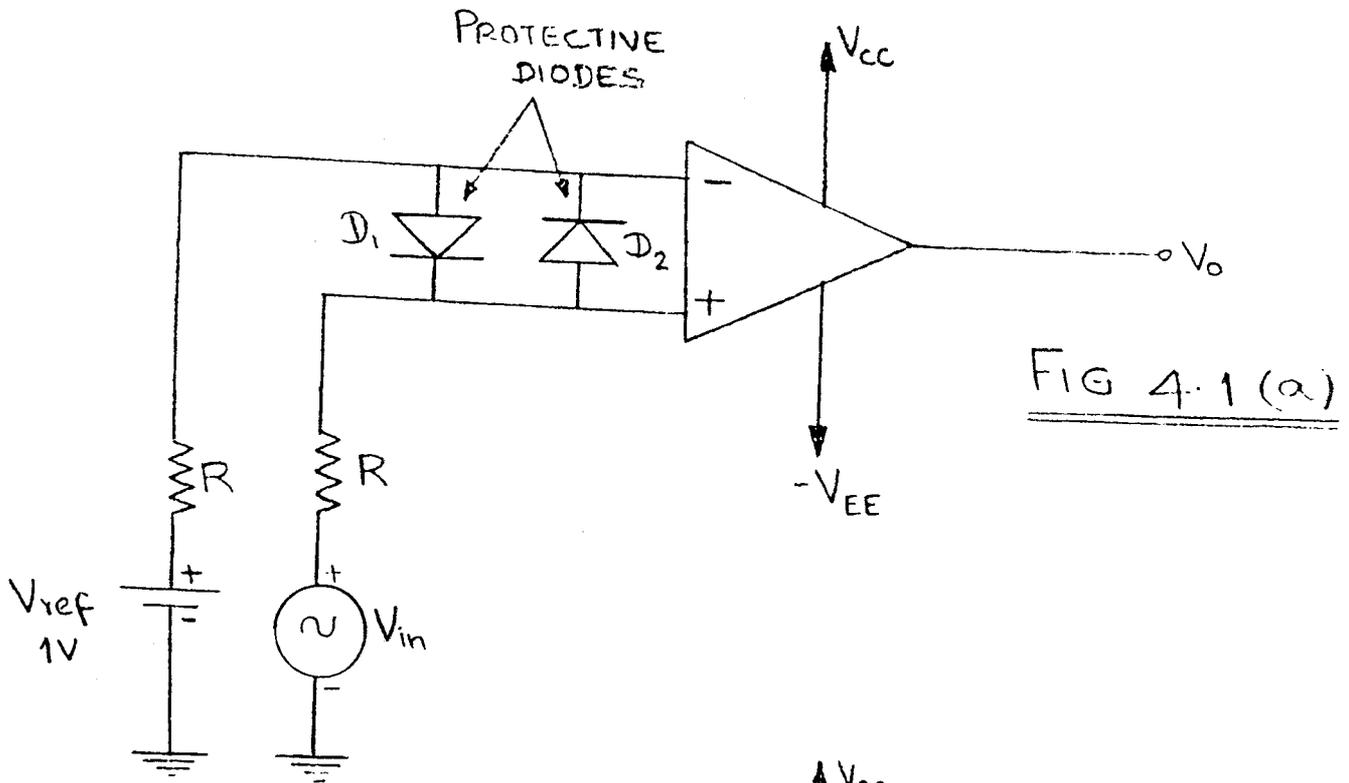


FIG 4.1 (a)

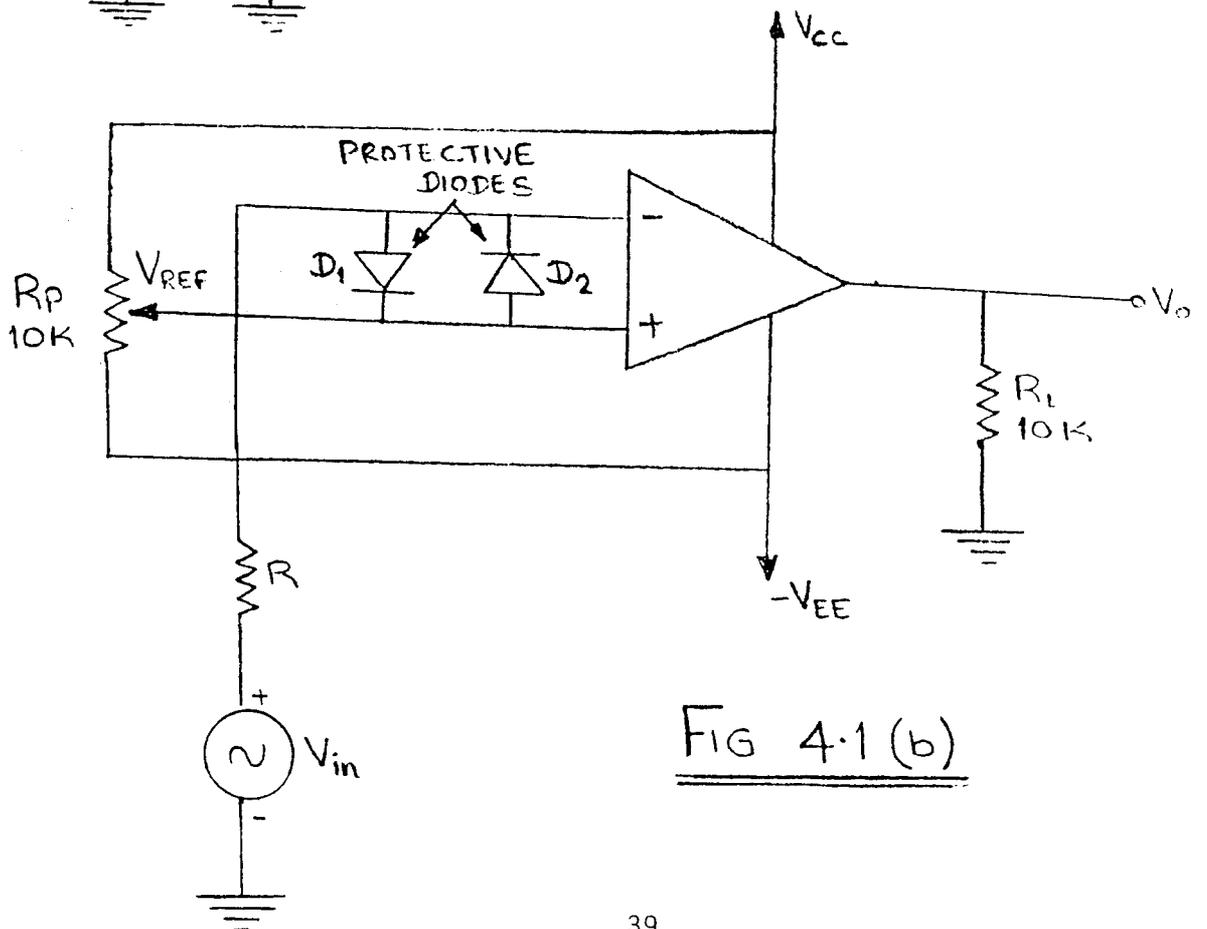


FIG 4.1 (b)

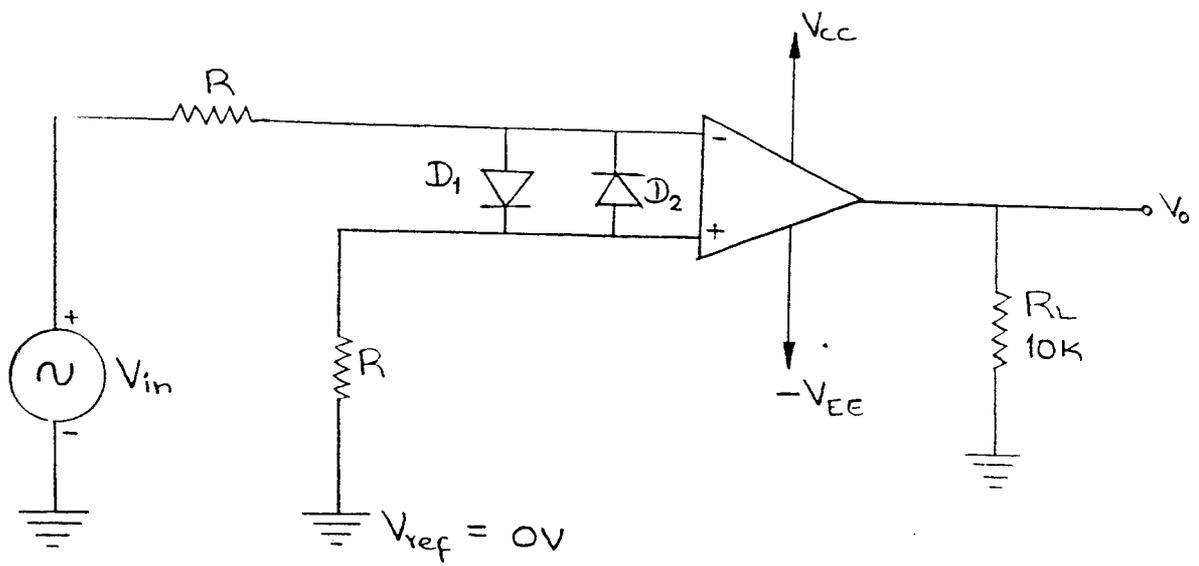


FIG 4.1 (c)

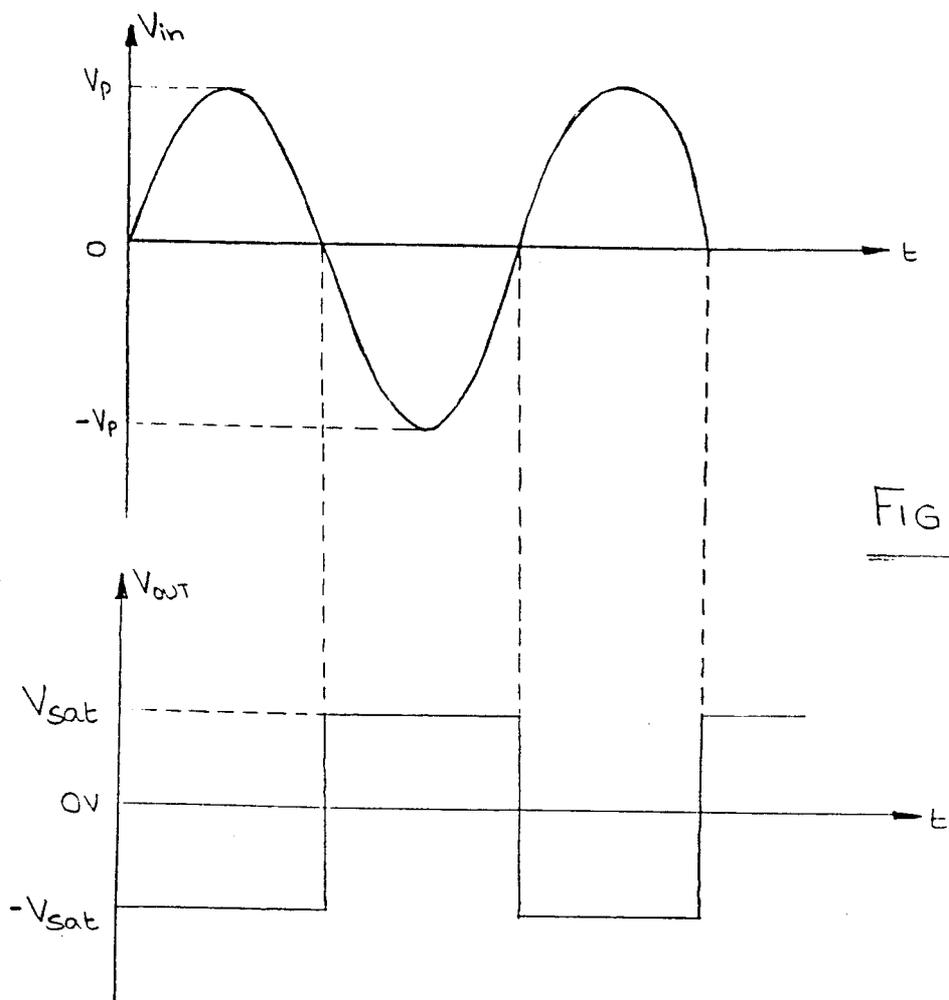


FIG 4.1 (d)

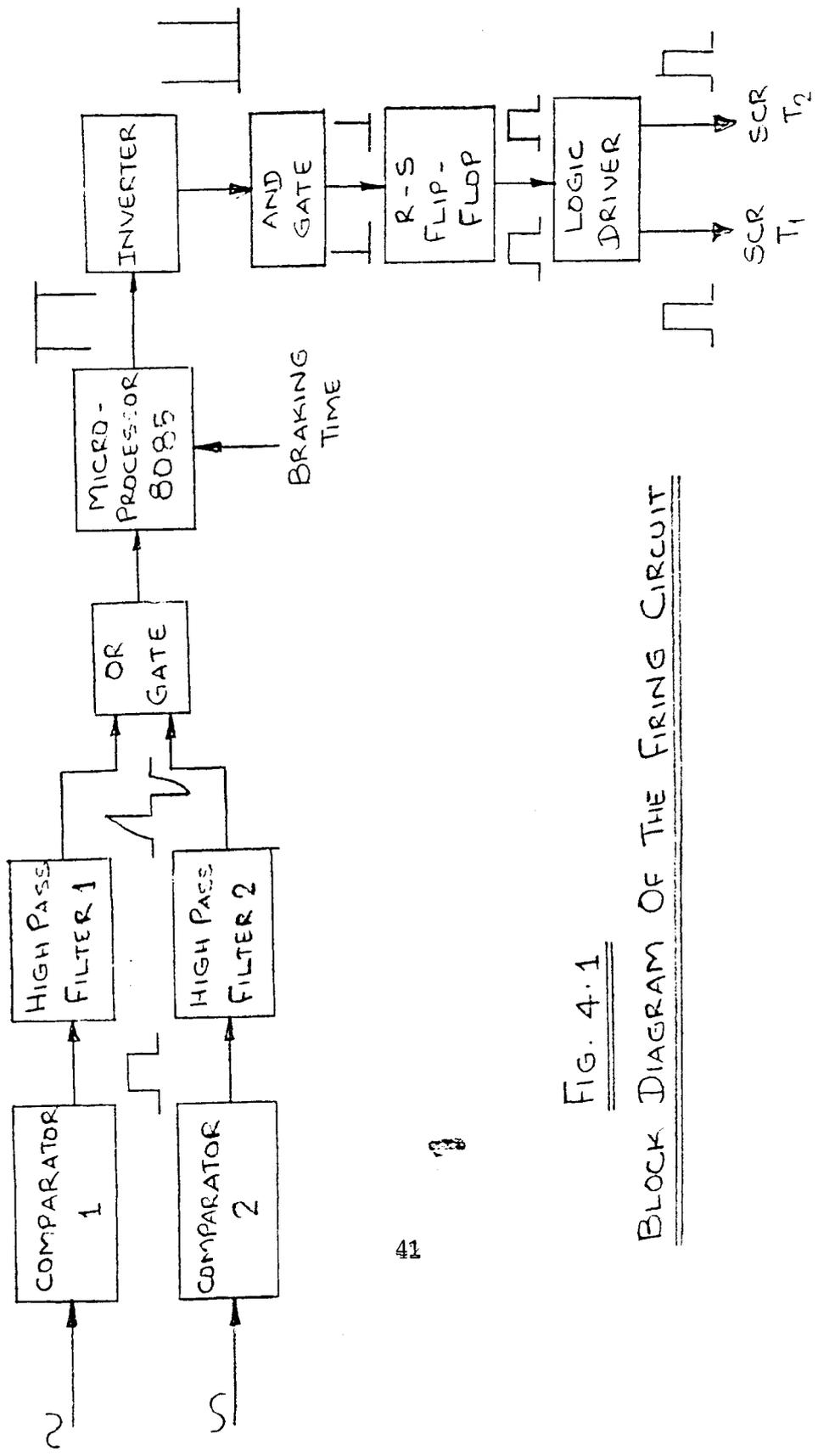


FIG. 4.1

BLOCK DIAGRAM OF THE FIRING CIRCUIT



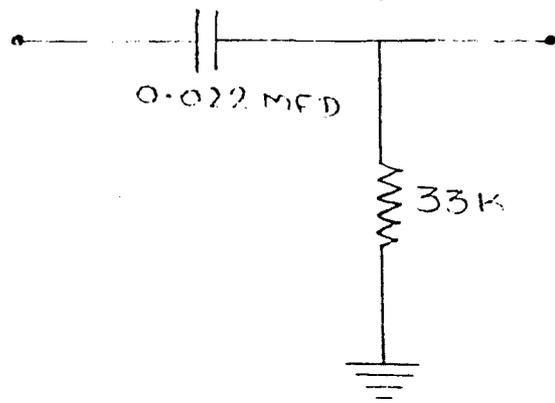


FIG. 4.3 HIGH PASS FILTER

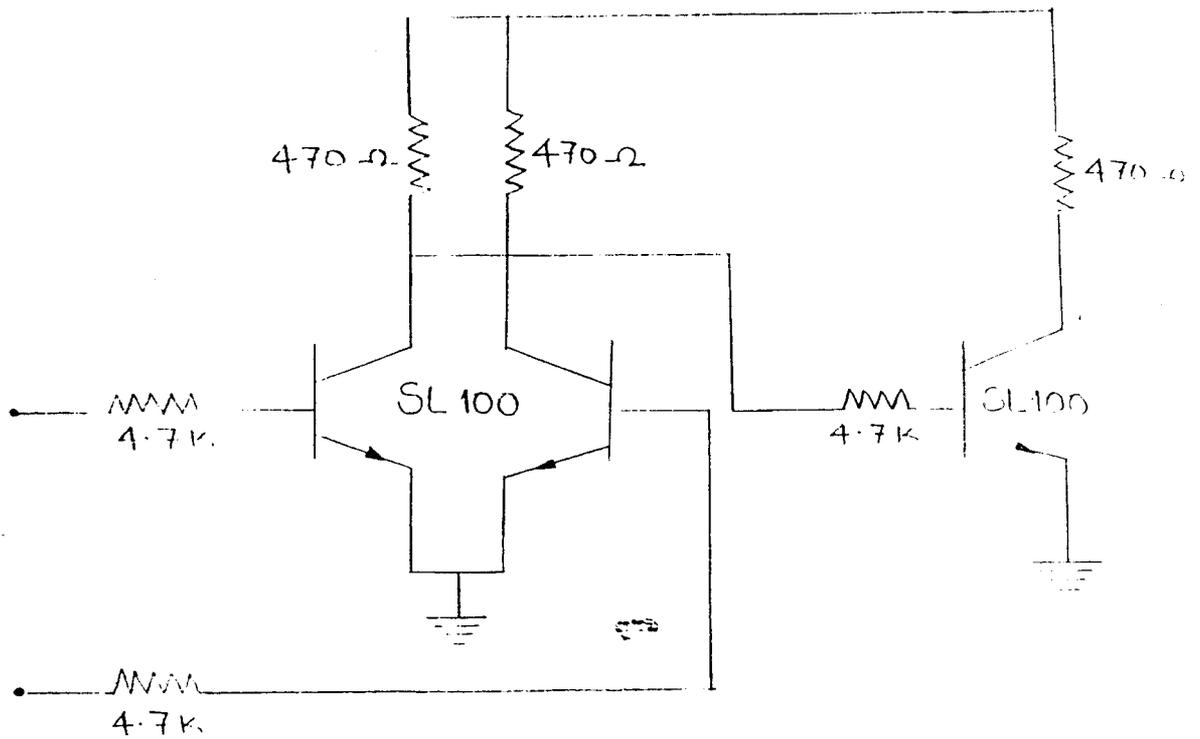


FIG. 4.4 OR GATE

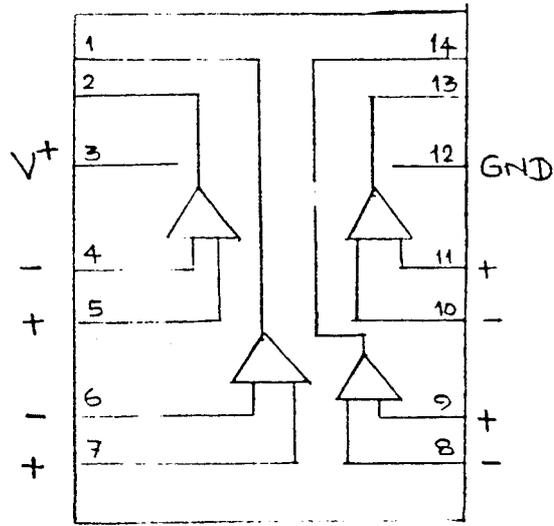


FIG 4.2(a) PIN CONFIGURATION OF LM339

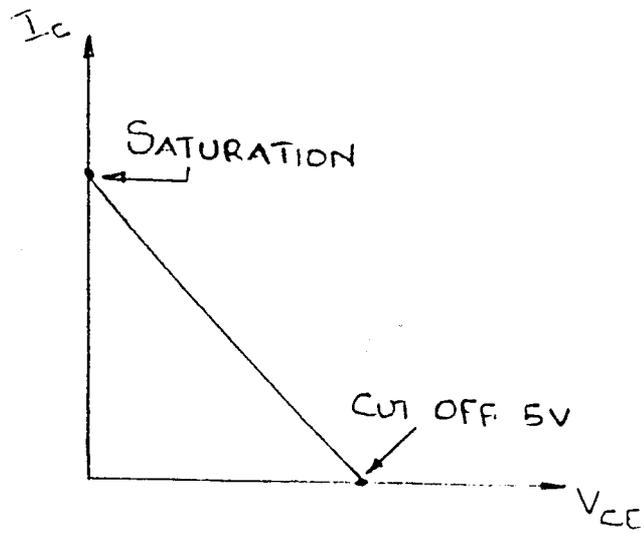


FIG 4.5 LOAD LINE

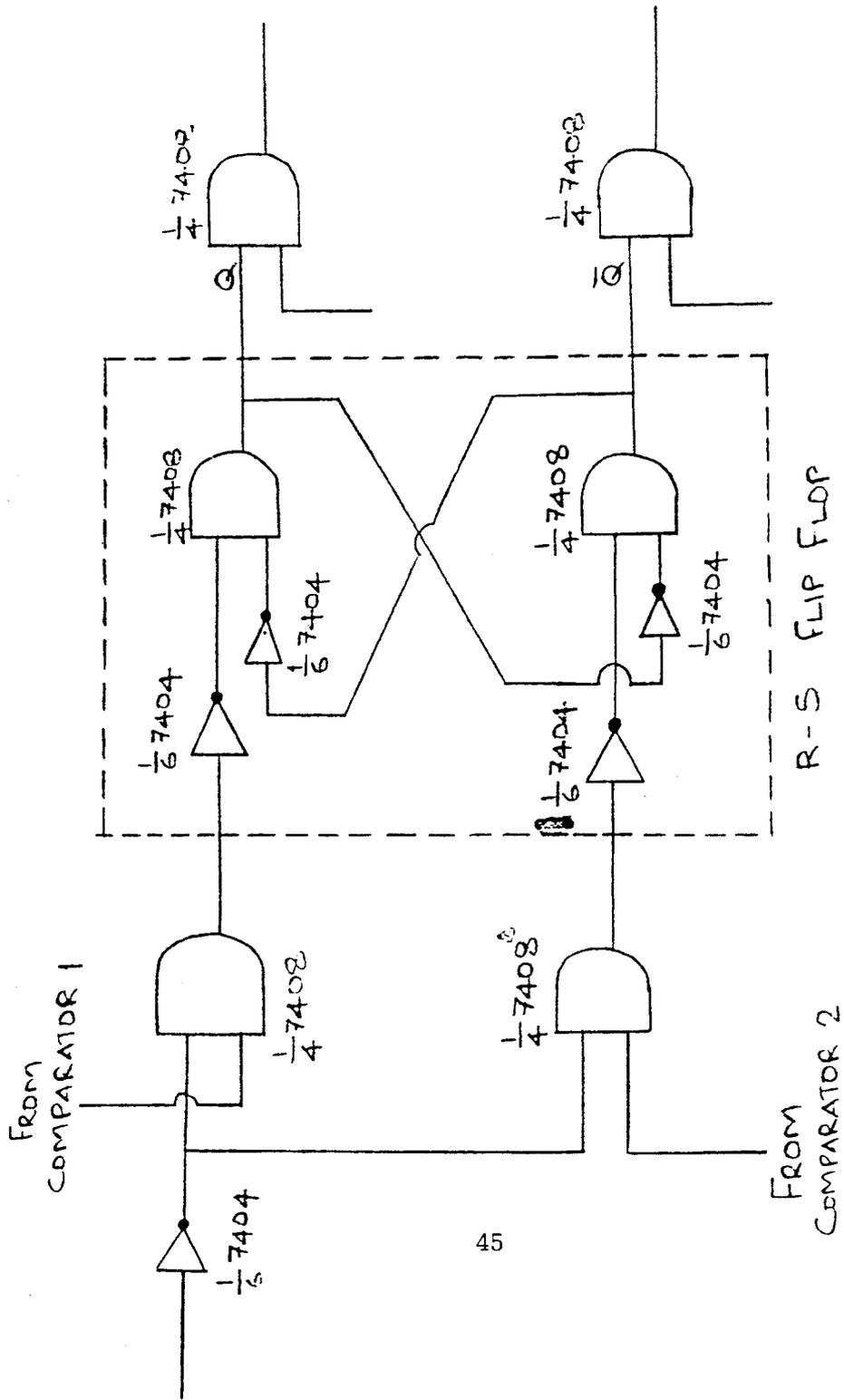
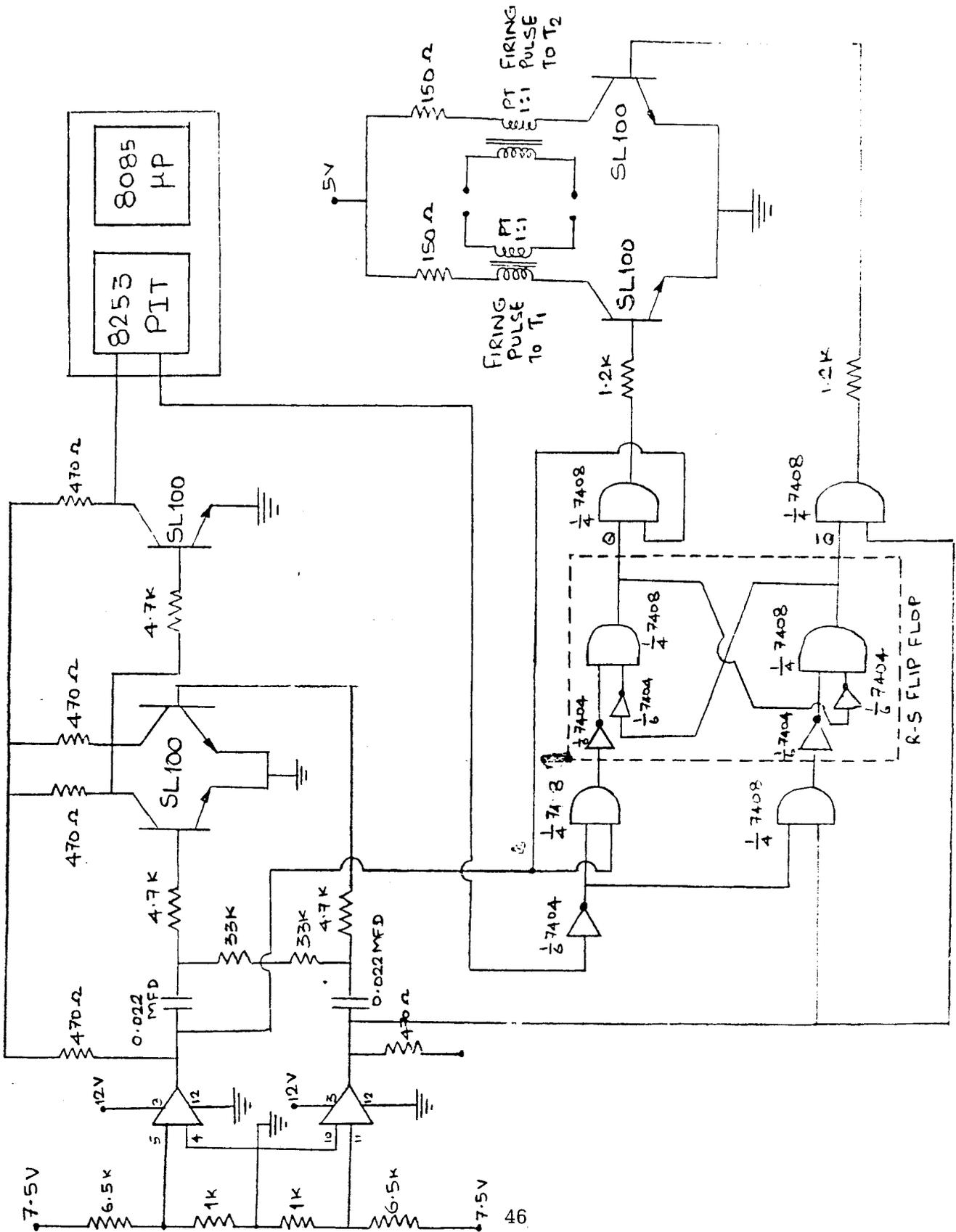
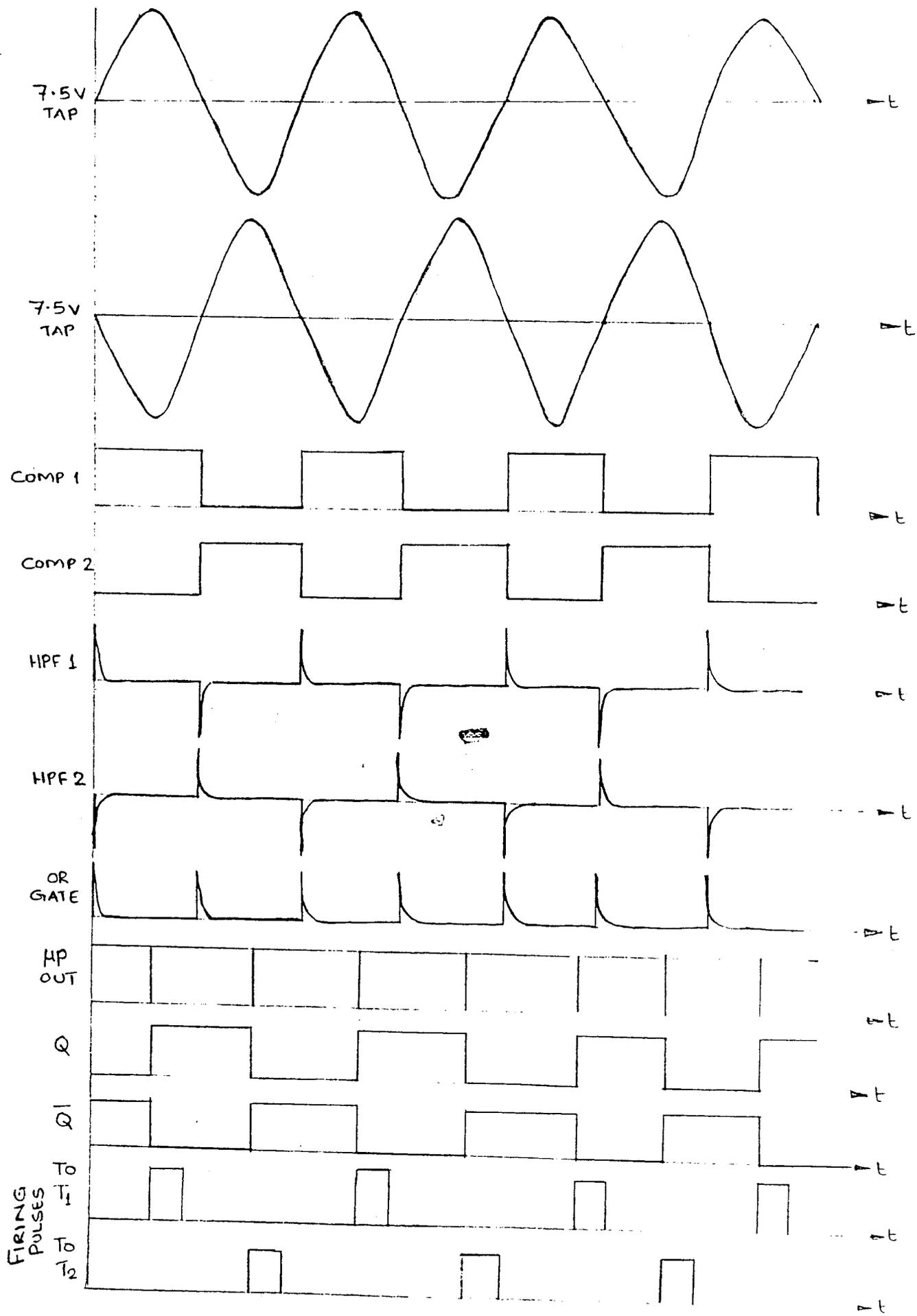


FIG 4.6 LOGIC GATES FOR SEQUENTIAL CIRCUITS OF 2RS





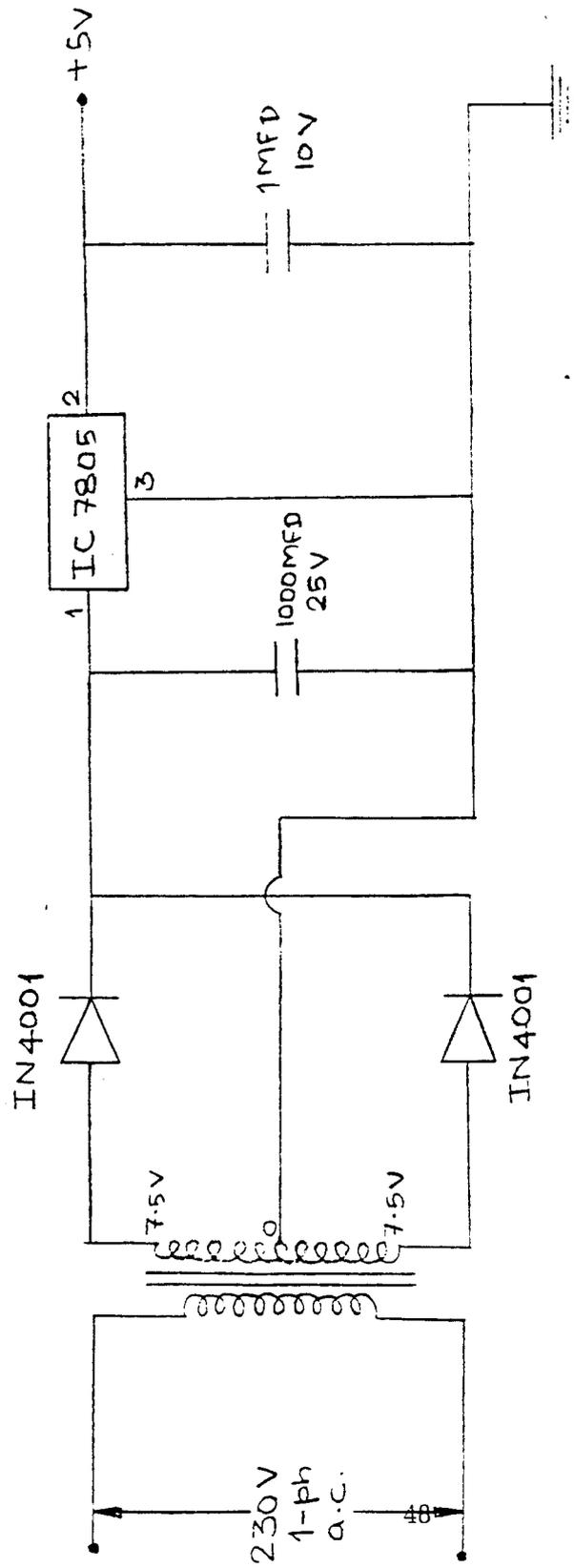


FIG. 4.9 CIRCUIT DIAGRAM OF POWER SUPPLY

## CHAPTER V

### SOFTWARE

#### 5.1 THE 8085 MICROPROCESSOR

The 8085 is an 8-bit general purpose microprocessor capable of addressing 64K of memory. The device has forty pins, requires a +5V single power supply, and can operate with a 3-MHz single-phase clock. The 8085 includes on its chip most of the logic circuitry for performing computing tasks and for communicating with peripherals. However, eight of its bus lines are multiplexed; that is, they are time shared by the low-order address & data.

Fig 5.1 shows the logic pinout of the 8085 microprocessor.

All the signals can be classified into six groups:

1. Address bus
2. Data bus
3. Control and status signals
4. Power supply and frequency signals
5. Interrupts and peripheral initiated signals and
6. Serial Input/output ports.

#### Address Bus

The 8085 has eight signal lines,  $A_{15} - A_8$  which are unidirectional and used as high-order address bus.

### **Multiplexed Address/Data Bus**

The signal lines  $AD_7$  to  $AD_0$  are bidirectional, they serve a dual purpose. They are used as the low-order address bus as well as the data bus. In executing an instruction, during the earlier part of the cycle, these lines are used as the low-order address bus. During the later part of the cycle these lines are used as the data bus. However, the lower order address bus can be separated from these signals by using a latch.

### **Control and Status Signals**

This group of signals include two control signals ( $\overline{RD}$  and  $\overline{WR}$ ), three status signals ( $IO/\overline{M}$ ,  $S_1$  and  $S_0$ ) to identify the nature of the operation and one special signal (ALE) to indicate the beginning of the operation. These signals are as follows:

#### **\* ALE - Address Latch Enable**

This is a positive going pulse generated every time the 8085 begins an operation; it indicates that the bits on  $AD_7$  -  $AD_0$  are address bits. This signal is used primarily to latch the low-order address from the multiplexed bus and generate a separate set of eight address lines,  $A_7$  to  $A_0$ .

\*  $\overline{RD}$  - Read

This is a read control signal (active low). This signal indicates that the selected Input/Output or memory device is to be read and data are available on the data bus.

\*  $\overline{WR}$  - Write

This is a write control signal (active low). This signal indicates that the data on the data bus are to be written into a selected memory or Input/Output location.

\*  $IO/\overline{M}$

This is a status signal used to differentiate between Input/Output and memory operations. When it is high, it indicates an Input/Output operation; when it is low, it indicates a memory operation. This signal is combined with  $\overline{RD}$  (Read) and  $\overline{WR}$  (Write) to generate Input/Output and memory control signals.

\*  $S_1$  and  $S_0$

These status signals, similar to  $IO/\overline{M}$ , can identify various operations, but they are rarely used in small systems.

## Power Supply and Clock Frequency

The power supply and frequency signals are as follows:

\*  $V_{CC}$  : +5V Power supply

\*  $V_{SS}$  : Ground reference

\*  $X_1, X_2$ : A crystal is connected at these two pins. The frequency is internally divided by two, therefore, to operate a system at 3 MHz, the crystal should have frequency of 6 MHz.

### \* CLK (OUT) - Clock output

This signal can be used as the system clock for other devices.

## Interrupts and externally initiated operations

The 8085 has five interrupt signals than can be used to interrupt a program execution. One of the signals, INTR (Interrupt Request) is identical to the 8080A microprocessor interrupt signal (INT). The microprocessor acknowledges an interrupt by the  $\overline{INTA}$  (Interrupt Acknowledge) signal.

### \* $\overline{RESET\ IN}$

When the signal on this pin goes low, the program counter is set to zero, the buses are tri-stated and the MPU is reset.

## **\* RESET OUT**

This signal indicates that the MPU is being reset. The signal can be used to reset other devices.

## **Serial I/O Ports**

The 8085 has two signal inputs to implement the serial transmission: SID (Serial Input Data) and SOD (Serial Output Data).

## **5.2 THE 8253 PROGRAMMABLE INTERVAL TIMER**

The 8253 Programmable interval timer/counter is functionally similar to the software-designed counters and timers. It generates accurate time delays and can be used for applications such as real-time clock, an event counter, a digital one-shot, a square wave generator and a complex waveform generator.

The 8253 includes three identical 16 bit counters that can operate independently in any one of the six modes. It is packaged in a 24 pin DIP and requires a single +5V power supply. To operate a counter, a 16 bit count is loaded in its register and, on command, it begins to decrement the count until it reaches zero. At the end of the count, it generates a pulse that can be used to interrupt the MPU. The counter can count either

in binary or BCD. In addition, a count can be read by the MPU while the counter is decrementing.

### **Block diagram of the 8253**

Fig.5.2 is the block diagram of the 8253; it includes three counters (0,1 and 2), a data bus buffer, Read/Write control logic and a control register. Each counter has two input signals - clock (CLK) and GATE - and one output signal - OUT.

### **Data Bus Buffer**

This tri-state, 8 bit, bidirectional buffer is connected to the data bus of the MPU.

### **Control logic**

The control section has five signals:  $\overline{RD}$  (Read) ,  $\overline{WR}$  (Write),  $\overline{CS}$  (chip select) and the address lines  $A_0$  and  $A_1$ . In the peripheral I/O mode, the  $\overline{RD}$  and  $\overline{WR}$  signals are connected to  $\overline{IOR}$  and  $\overline{IOW}$  respectively. In memory-mapped I/O, these are connected to  $\overline{MEMR}$  (Memory Read) and  $\overline{MEMW}$  (Memory write). Address lines  $A_0$  and  $A_1$  of the MPU are usually connected to lines  $A_0$  and  $A_1$  of the 8253 and  $\overline{CS}$  is tied to a decoded address.

The control word register and counters are selected according to the signals on lines  $A_0$  &  $A_1$  as shown below:

$A_1$	$A_0$	Selection
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control register

### **Control Word Register**

This register is accessed when lines  $A_0$  and  $A_1$  are at logic 1. It is used to write a command word which specifies the counter to be used, its mode, and either a Read or a Write operation. However, the control word register is not available for a Read operation. The control word format is shown in fig.5.3.

### **Mode**

The 8253 can operate in six different modes as shown in fig.5.4. The gate of a counter is used either to disable or enable counting.

### **Programming the 8253**

The 8253 can be programmed to provide various types of output through write operations, or to check a count while

counting through Read operations. The details of these operations are given below:

### **Write operations**

To initialise a counter, the following steps are necessary:

1. Write a control word into the control register.
2. Load the low-order byte of a count in the counter register.
3. Load the high-order byte of a count in the counter register.

With a clock (maximum 2 MHz) and an appropriate gate signal to one of the counters, the above steps should start the counter and provide appropriate output according to the control word.

### **Read Operations**

In some applications, especially in event counters, it is necessary to read the value of the count in progress. This can be done by either of the two methods. One method involves reading a count after inhibiting the counter to be read. The second method involves reading a count while the count is in progress (known as reading on the fly).

In the first method, counting is stopped by controlling the gate input or the clock input of the selected counter, and two I/O read operations are performed by the microprocessor unit. The first I/O operation reads the low-order byte, and the second I/O operation reads the high-order byte.

In the second method, an appropriate control word is written into the control register to latch a count in the output latch, and two I/O read operations are performed by the MPU.

#### 5.2(i) CONTROL WORD FORMAT

The control word is formed for the Mode 5 from the control word format. The braking time is entered in the microprocessor. A look-up-table relating the firing angle and time is provided. The entry of the braking time selects the firing angle from this table and suitable current required for the braking is generated.

This project uses counter of the 8253, for which  $D_7 =$  and  $D_6 =$  . The least significant bit is sent first and then most significant bit is sent next. So  $D_5 =$  and  $D_4 =$  .  $D_3 =$  ,  $D_2 =$  ,  $D_1 =$  . The count is in binary. So  $D_0 = 0$ .

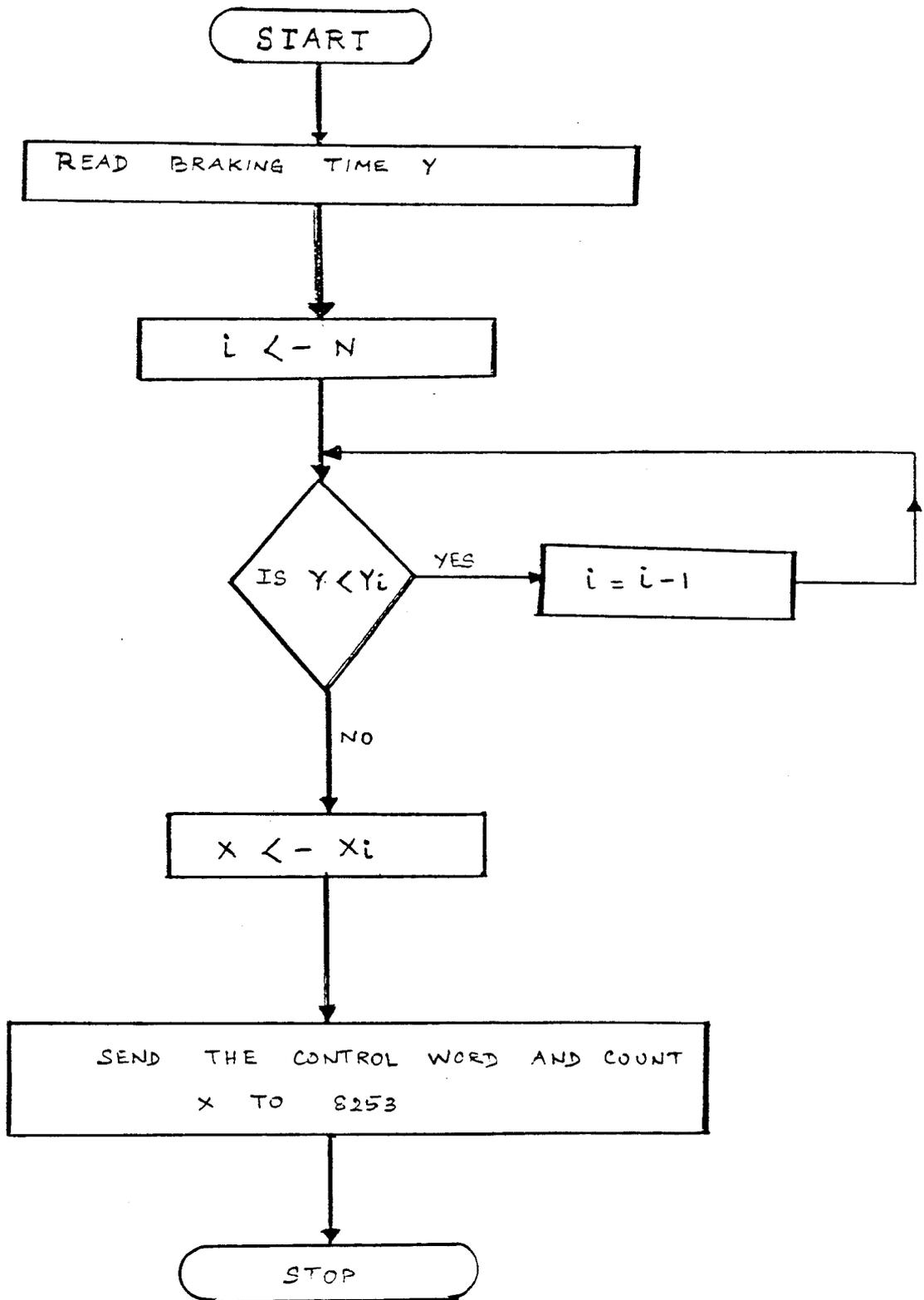
The control word is,

D<sub>7</sub> D<sub>6</sub> D<sub>5</sub> D<sub>4</sub> D<sub>3</sub> D<sub>2</sub> D<sub>1</sub> D<sub>0</sub>

=

### 5.3 LOOK-UP-TABLE

In the working model, the induction motor is operated at a load of 2.3A and rated speed of 1440 rpm. The table forming braking time Vs the count is found out experimentally and the data are stored in memory location in the form of number of counts. If the braking time is entered, on execution of the program the corresponding count is selected. The count is sent to the PIT 8253, the SCRs are properly fired and the required direct current is obtained.



## 5.5. PROGRAM

OP.CODE	LABEL	MNEMONIC
0E		MVI C,17
3A		LDA 8300
21		LXI H, 8101
BE	AG:	CMP M
DA		JC OUT
23		INX H
0D		DCR C
C2		JNZ AG
26	OUT:	MVI H, 82
3E		MVI A,BA
D3		OUT 83
3E		MVI A,10
D3		OUT 82
7E		MOV A,M
D3		OUT 82
76		HLT

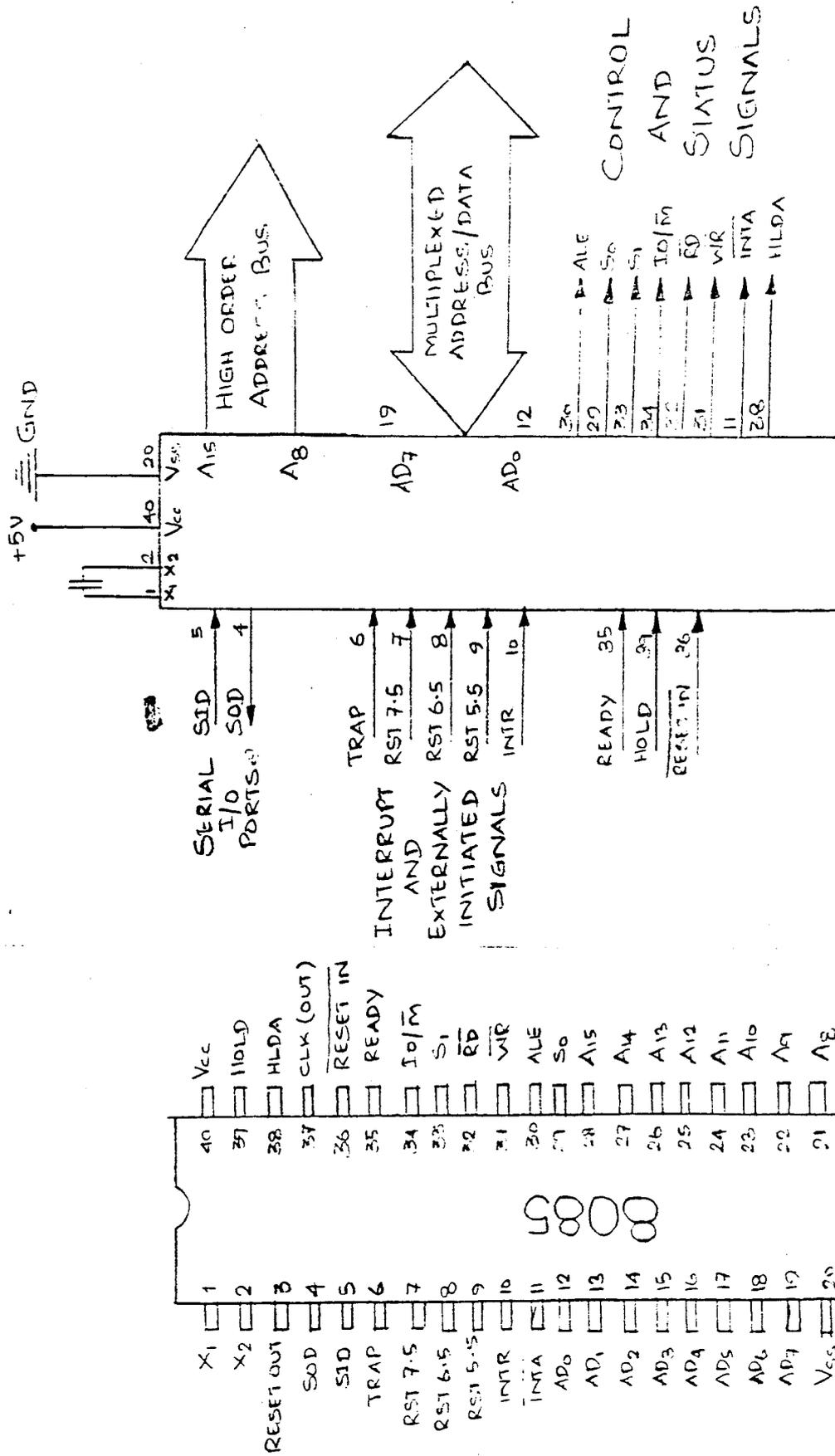


FIG 5.1 8085 MICROPROCESSOR PIN OUT AND SIGNALS

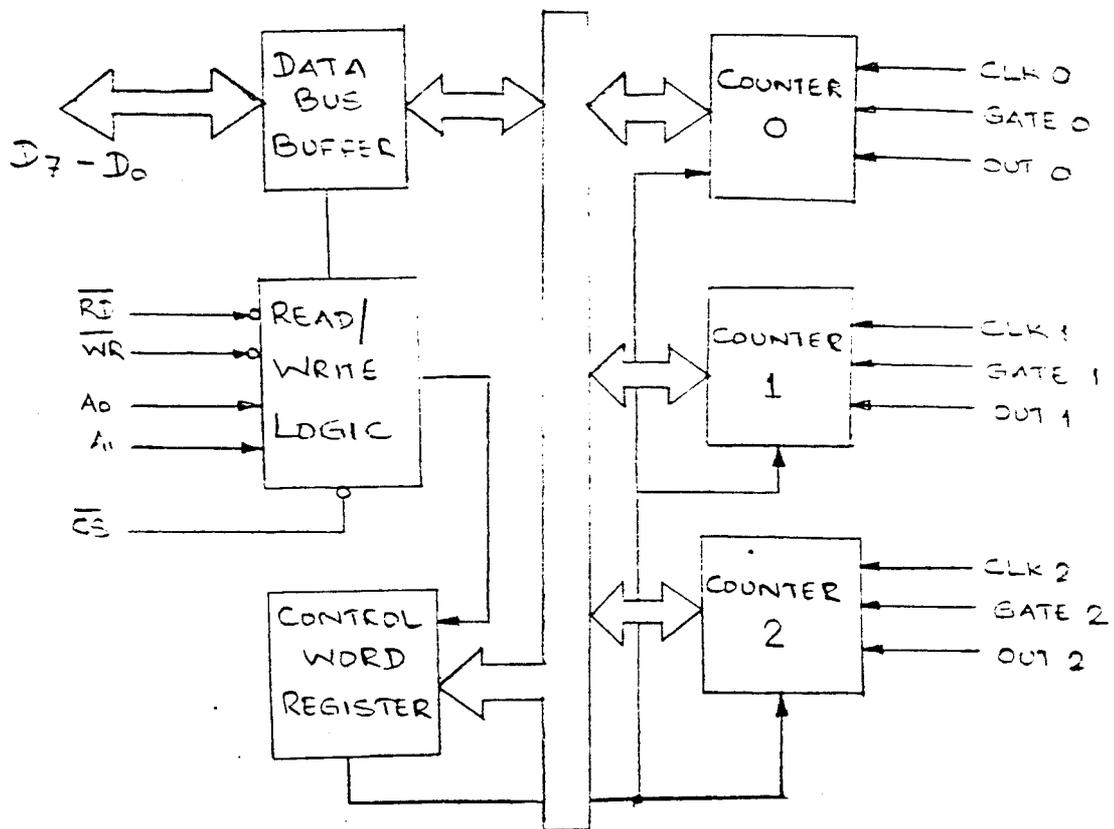


FIG 5.2 8253 BLOCK DIAGRAM

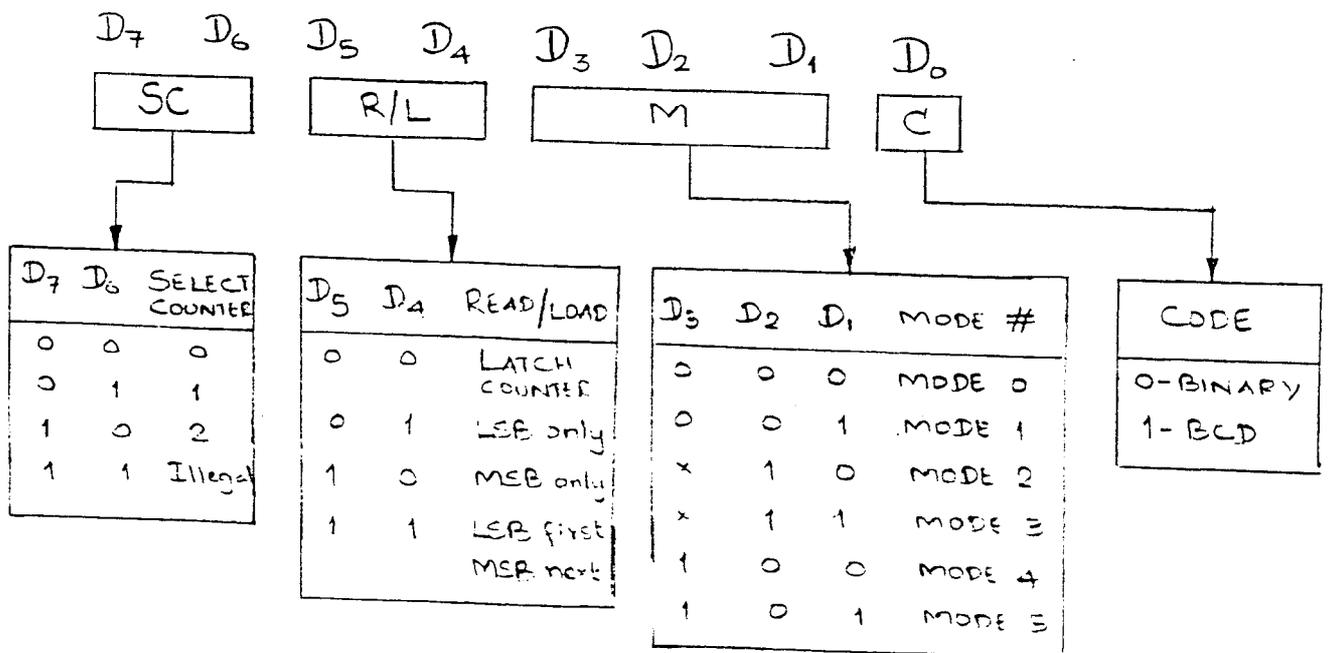


FIG 5.3 CONTROL WORD FORMAT

## CHAPTER VI

### EXPERIMENTAL SET UP

This project is tested on a three h.p. squirrel cage induction motor with a load of 2.3A and rated speed of 1440 rpm. The name plate details of the above motor are given below:

Stator winding	:	Delta connected
Voltage	:	415 V
Current	:	4.6 A
Frequency	:	50 Hz
Phase	:	3 phase
Speed	:	1440 rpm

The details of the microprocessor used in this project are given below:

Manufacturer Name	:	PRECITRON
CPU	:	INTEL 8085
Clock	:	MHz
RAM	:	

The overall circuit diagram is shown in fig.6.1. A contactor is used to cut off the 3 phase a.c. input to the motor

and to send the d.c. current simultaneously. The contactor has three normally closed and two normally opened contacts. Three normally closed contacts are used to 'ON-OFF' the three phase a.c. supply. Two normally opened contacts are used to 'ON-OFF' the d.c. supply from the SCR bridge. The energizing coil of the contactor which is given 415V a.c. supply is controlled by a 5V d.c. relay.

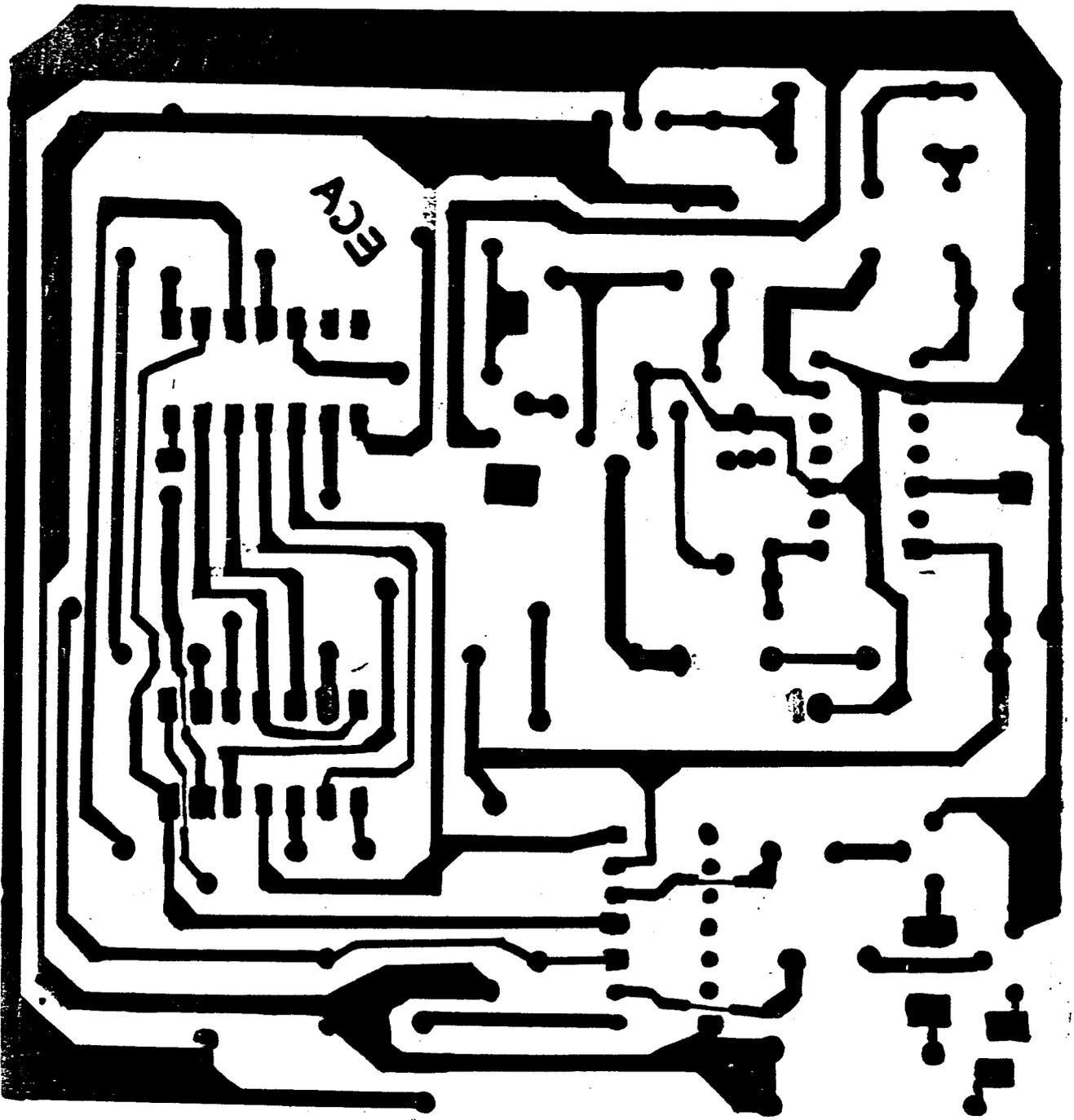
An autotransformer is used for starting the induction motor. A current limiting rheostat (67.5 ,6.5A) is used to limit the d.c.current injected into the stator. 230V a.c. input is given to the SCR bridge.

The braking time is entered in the LOC and the micro-processor program is executed. On execution the count corresponding to the braking time is selected and is sent to the counter

To brake the induction motor, the 5V d.c. relay is energised, which in turn energises the contactor. The contactor cuts the 3 phase a.c. supply and sends the d.c. current to the stator winding. The firing angle is already-set in the micro-processor by the execution of the braking time. After the motor stops, the direct current should be cut off.

Since the dynamic braking is used, there is no reverse rotation of the motor after standstill. By this method, the braking torque can be varied. So a smooth braking can be applied to the induction motor.

It may be applied to conveyor schemes, to fluid flow schemes for applying smooth braking for different loads. This project suggests a program to achieve the dynamic braking using microprocessor control.



## CHAPTER VII

### CONCLUSION

This project is designed, fabricated and tested on a three h.p. three phase squirrel cage induction motor and is found to be successful. Dynamic braking of an induction motor provides a retarding torque and as a result of which, the speed of the motor decreases and becomes zero. There are certain advantages of this method as compared to mechanical braking methods.

Less maintenance is required, whereas mechanical brakes require adjustment and replacement of the brake linings. No dirt is produced, whereas the wear out of mechanical brakes produces dust. Dynamic braking is smooth without snatching.

Dynamic braking, may be employed for any one of the following purposes:

- i) reducing the time taken to stop the motor.
- ii) stopping exactly at specified points, for example, in lifts; sometimes such precise stops are necessary for reasons for safety.

- iii) feeding back, at least a portion of the power, to the supply network.

### **Test Results**

During normal running condition with 50% load on the motor (i.e. 2.3A) and the motor stopped by switching off the mains and without any signal from our designed circuit, the motor stops in 6 seconds. When dynamic braking is applied and with all the other conditions on the motor remaining the same, the motor stops in 3.5 seconds. This means that the braking time of the motor is reduced by 41.6% from the previous value.

## REFERENCES

1. M.G.SAY, The Performance and Design of Alternating current Machines, CBS Publishers & Distributors, New Delhi,1983.
2. R.K.SUGANDHI and K.K.SUGANDHI, Thyristor - Theory and Applications, Wiley Eastern Limited, 1983.
3. M.RAMAMOORTHY, An Introduction to thyristors and their applications, East-West Press Pvt.Ltd.,1987.
4. M.S.BERDE, Thyristor Engineering, Khanna Publishers,1988.
5. RAMAKANT A.GAYAKWAD, Op-Amps and Linear Integrated Circuits, Prentice Hall of India Ltd., April, 1991.
6. R.S.GAONKAR, Microprocessor Architecture, Programming and Applications with the 8085/8080A, Wiley Eastern Limited, 1988.
7. A.P.MALVINO and D.P.LEACH, Digital Principles and Applications, Tata McGraw Hill International Editions, New Delhi, 1988.

8. R.S.RAMASWAMY, Control & Maintenance of Electrical Machines, Second Edition, June,1990, Priya Publishers, Trichy.
9. S.K.PILLAI, A First Course on Electrical Drives, Wiley Eastern Limited, 1988.
10. F.K.AMOURI & M.F.ALKABAJIE, Dynamic Braking of three phase compensated induction motor using Microprocessor  
Journal of The Institution of Engineers (India), EL.Vol.69.  
Feb,1989.

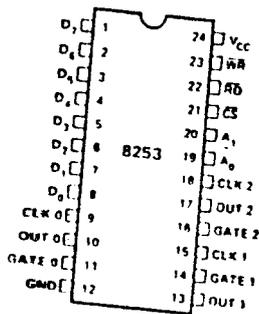


# 8253/8253-5 PROGRAMMABLE INTERVAL TIMER

- MCS-85™ Compatible 8253-5
- 3 Independent 16-Bit Counters
- DC to 2 MHz
- Programmable Counter Modes
- Count Binary or BCD
- Single +5V Supply
- 24-Pin Dual In-Line Package

The Intel® 8253 is a programmable counter/timer chip designed for use as an Intel microcomputer peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP. It is organized as 3 independent 16-bit counters, each with a count rate of up to 2 MHz. All modes of operation are software programmable.

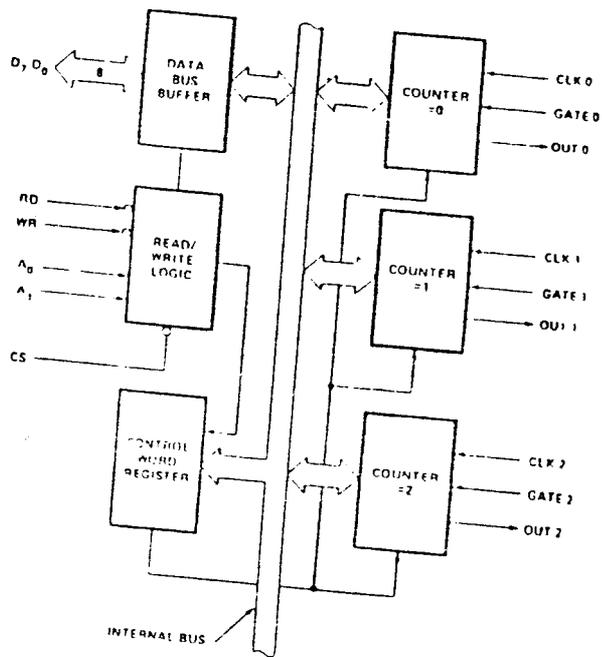
## PIN CONFIGURATION



## PIN NAMES

D <sub>7</sub> D <sub>0</sub>	DATA BUS (8 BIT)
CLK N	COUNTER CLOCK INPUTS
GATE N	COUNTER GATE INPUTS
OUT N	COUNTER OUTPUTS
RD	READ COUNTER
WR	WRITE COMMAND OR DATA
CS	CHIP SELECT
A <sub>0</sub> A <sub>1</sub>	COUNTER SELECT
V <sub>CC</sub>	+5 VOLTS
GND	GROUND

## BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

### General

The 8253 is a programmable interval timer/counter specifically designed for use with the Intel™ Microcomputer systems. Its function is that of a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the 8253 to match his requirements, initializes one of the counters of the 8253 with the desired quantity, then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

### Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the 8253
2. Loading the count registers.
3. Reading the count values.

### Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

#### RD (Read)

A "low" on this input informs the 8253 that the CPU is inputting data in the form of a counters value.

#### WR (Write)

A "low" on this input informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.

### A0, A1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

### CS (Chip Select)

A "low" on this input enables the 8253. No reading or writing will occur unless the device is selected. The CS input has no effect upon the actual operation of the counters.

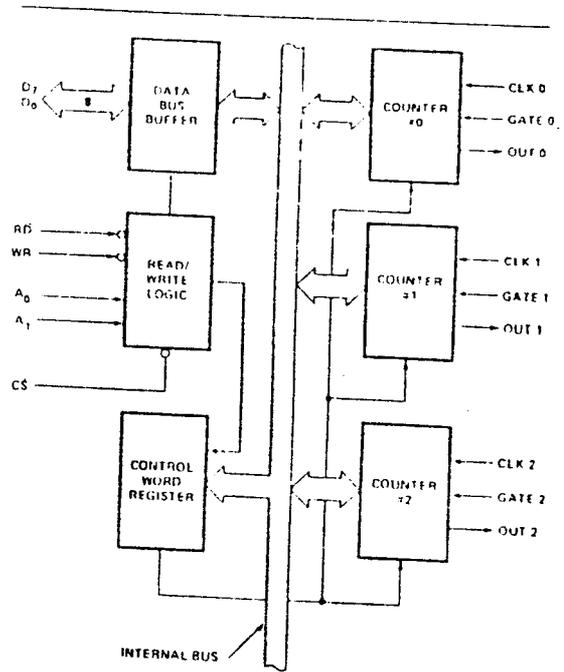


Figure 1. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

CS	RD	WR	A <sub>1</sub>	A <sub>0</sub>	Function
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No Operation 3 State
1	X	X	X	X	Disable 3 State
0	1	1	X	X	No Operation 3 State

**Control Word Register**

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

**Counter #0, Counter #1, Counter #2**

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate Mode configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

**8253 SYSTEM INTERFACE**

The 8253 is a component of the Intel™ Microcomputer Systems and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The CS can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel® 8205 for larger systems.

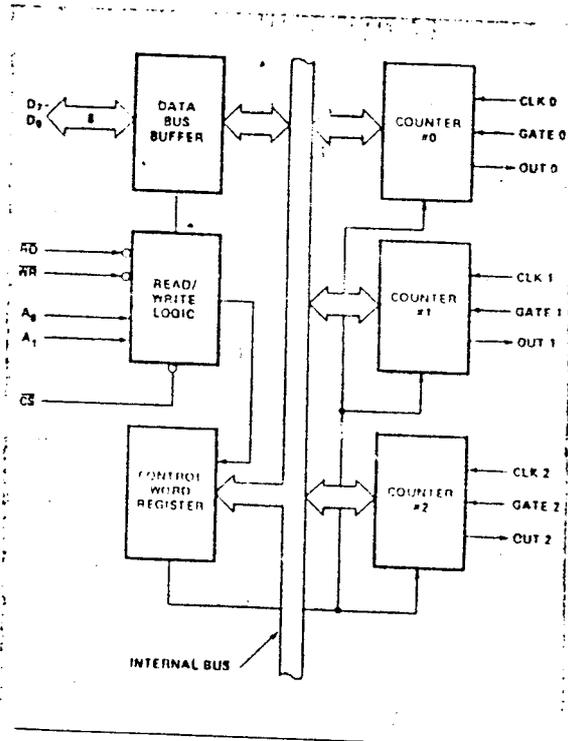


Figure 2. Block Diagram Showing Control Word Register and Counter Functions

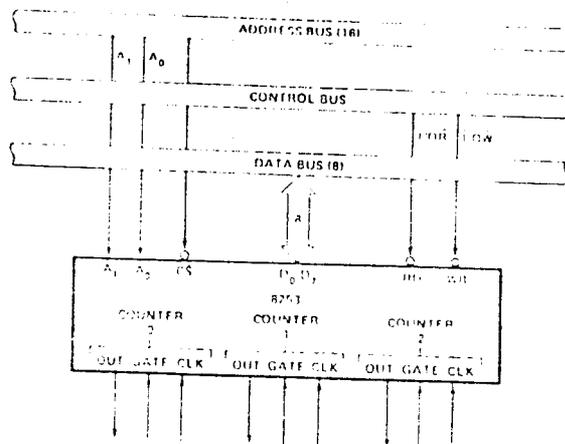


Figure 3. 8253 System Interface

## OPERATIONAL DESCRIPTION

### General

The complete functional definition of the 8253 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. These control words program the MODE, loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

### Programming the 8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register (A0, A1 = 11).

### Control Word Format

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

### Definition of Control

#### SC — Select Counter:

SC1		SC0		
0	0	0	0	Select Counter 0
0	0	0	1	Select Counter 1
1	0	0	0	Select Counter 2
1	0	0	1	Illegal

#### RL — Read/Load:

RL1		RL0		
0	0	0	0	Counter Latching operation (see READ/WRITE Procedure Section)
1	0	0	0	Read/Load most significant byte only.
0	1	0	0	Read/Load least significant byte only.
1	1	0	0	Read/Load least significant byte first, then most significant byte.

#### M — MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

#### BCD:

0	Binary Counter 16 bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

### Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

### MODE Definition

**MODE 0: Interrupt on Terminal Count.** The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

- (1) Write 1st byte stops the current counting.
- (2) Write 2nd byte starts the new count.

**MODE 1: Programmable One-Shot.** The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

**MODE 2: Rate Generator.** Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

**MODE 3: Square Wave Rate Generator.** Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for  $(N + 1)/2$  counts and low for  $(N - 1)/2$  counts.

**MODE 4: Software Triggered Strobe.** After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

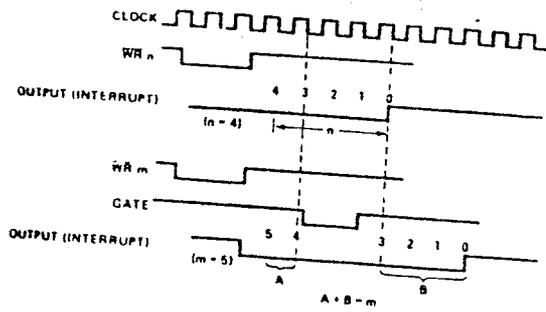
If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is low. Reloading the counter register will restart counting beginning with the new number.

**MODE 5: Hardware Triggered Strobe.** The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

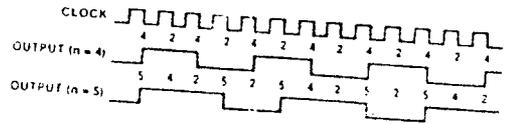
Modes	Signal Status	Low Or Going Low	Rising	High
	0		Disables counting	
1			1) Initiates counting 2) Resets output after next clock	
2		1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3		1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4		Disables counting		Enables counting
5			Initiates counting	

Figure 4. Gate Pin Operations Summary

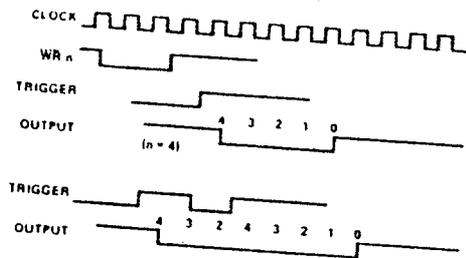
**MODE 0: Interrupt on Terminal Count**



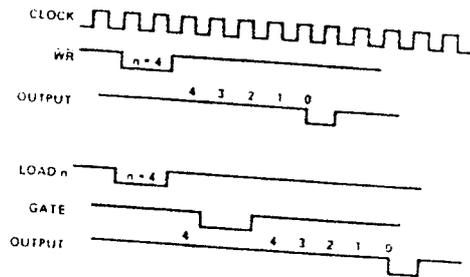
**MODE 3: Square Wave Generator**



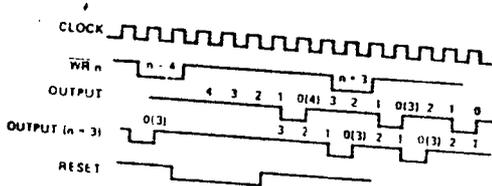
**MODE 1: Programmable One-Shot**



**MODE 4: Software Triggered Strobe**



**MODE 2: Rate Generator**



**MODE 5: Hardware Triggered Strobe**

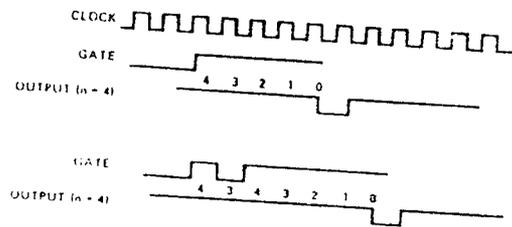


Figure 5. 8253 Timing Diagrams

## 8253 READ/WRITE PROCEDURE

### Write Operations

The systems software must program each counter of the 8253 with the mode and quantity desired. The programmer must write out to the 8253 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent. (SC0, SC1)

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it must be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeroes into a count register will result in the maximum count ( $2^{16}$  for Binary or  $10^4$  for BCD). In MODE 0 the new count will not restart until the load has been completed. It will accept one of two bytes depending on how the MODE control words (RL0, RL1) are programmed. Then proceed with the restart operation.

	MODE Control Word Counter n
LSB	Count Register byte Counter n
MSB	Count Register byte Counter n

Note: Format shown is a simple example of loading the 8253 and does not imply that it is the only format that can be used.

Figure 6. Programming Format

		A1	A0
No. 1	MODE Control Word Counter 0	1	1
No. 2	MODE Control Word Counter 1	1	1
No. 3	MODE Control Word Counter 2	1	1
No. 4	LSB Count Register Byte Counter 1	0	1
No. 5	MSB Count Register Byte Counter 1	0	1
No. 6	LSB Count Register Byte Counter 2	1	0
No. 7	MSB Count Register Byte Counter 2	1	0
No. 8	LSB Count Register Byte Counter 0	0	0
No. 9	MSB Count Register Byte Counter 0	0	0

Note: The exclusive addresses of each counter's count register make the task of programming the 8253 a very simple matter, and maximum effective use of the device will result if this feature is fully utilized.

Figure 7. Alternate Programming Formats

**Read Operations**

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The 8253 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A0, A1 inputs to the 8253 the programmer can select the counter to be read (remember that no read operation of the mode register is allowed A0, A1=11). The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter must be inhibited either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows:

- first I/O Read contains the least significant byte (LSB)
- second I/O Read contains the most significant byte (MSB)

Due to the internal logic of the 8253 it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read then two bytes must be read before any loading WR command can be sent to the same counter.

**Read Operation Chart**

A1	A0	RD	
0	0	0	Read Counter No. 0
0	1	0	Read Counter No. 1
1	0	0	Read Counter No. 2
1	1	0	Illegal

**Reading While Counting**

In order for the programmer to read the contents of any counter without effecting or disturbing the counting operation the 8253 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically when the programmer wishes to read the contents of a selected counter on the fly, he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter and the contents of the latched register is available.

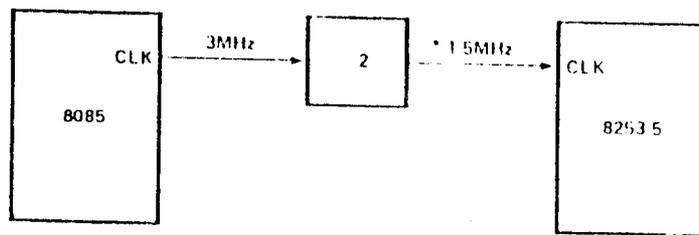
**MODE Register for Latching Count**

A0, A1 = 11

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

- SC1, SC0 specify counter to be latched
- D5, D4 = 00 designates counter latching operation
- X = don't care

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed. This command has no effect on the counter's mode.



\*If an 8085 clock output is to drive an 8253 5 clock input, it must be reduced to 2 MHz or less.

Figure 8. MCS 85™ Clock Interface\*