ONLINE MONITORING OF ENERGY CONSUMPTION AND MAXIMUM DEMAND

A PROJECT REPORT

Submitted by

P.KANAKARAJ (71201105016)
R.R.KARTHICK (71201105018)
S.MALATHY (71201105023)
S.SUBHA PRIYA (71201105058)

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in

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Under the guidance of
Prof.N.Kalaiarasi

KUMARAGURU COLLEGE OF TECHNOLOGY,
COIMBATORE - 641006

ANNA UNIVERSITY :: CHENNAI - 600 025

ANNA UNIVERSITY : CHENNAI-600 025

BONAFIDE CERTIFICATE

Certified that this project report titled " **ONLINE MONITORING OF ENERGY CONSUMPTION AND MAXIMUM DEMAND** " is the bonafide work of

P.KANAKARAJ	-	**Register No. 71201105016**
R.R.KARTHICK	-	**Register No. 71201105018**
S.MALATHY	-	**Register No. 71201105023**
S.SUBHA PRIYA	-	**Register No. 71201105058**

who carried out the project work under my supervision.

Signature of the Head of the Department

Signature of the guide

16/4/05

Prof.K.Regupathy Subramanian,B.E.,M.Sc.
HOD/EEE,
Kumaraguru college
of technology

Mrs.N.Kalaiarasi,M.E,
Asst.Professor ,EEE,
Kumaraguru college
of technology

CERTIFICATE OF EVALUATION

College : KUMARAGURU COLLEGE OF TECHNOLOGY

Branch : Electrical & Electronics Engineering

Semester : Eighth Semester

Sl.No.	Name of the Students	Title of the Project	Name of the Supervisor with Designation
01	P.Kanakaraj	"ONLINE MONITORING OF ENERGY CONSUMPTION AND MAXIMUM DEMAND"	Mrs.N.Kalaiarasi, M.E. Asst.Professor
02	R.R.Karthick		
03	S.Malathy		
04	S.Subha Priya		

The report of the project work submitted by the above students in partial fulfillment for the award of Bachelor of Engineering degree in Electrical & Electronics Engineering of Anna University were evaluated and confirmed to be report of the work done by the above students.

(INTERNAL EXAMINER)

18/4/05

(EXTERNAL EXAMINER)

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Abstract

ABSTRACT

In present scenario, each and every analog system present in the world is getting digitized and automated. The need for automation comes in due to precision and accuracy. It is an added advantage of monitoring the parameters like energy, power factor of any industries at remote end. The maximum demand of the industries must be kept within the limit specified by Electricity board. Accurate record of any maximum demand limit violations can be made for future references.

Taking account of all above factors, our project includes designing and fabricating a system to measure the necessary parameters using PIC Microcontroller. The datas are transmitted through telephone lines with the use FSK modulation technique. The datas are received, demodulated and then interfaced with personal computer. A LCD display connected to the PIC microcontroller displays the necessary parameters at the transmitter end. Battery back-up and EEPROM are provided for storage and retrieval of energy value during power shutdown.

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LIST OF ABREVIATIONS

ALU	-	Arithmetic Logic Unit
AM	-	Amplitude Modulator
ASK	-	Amplitude Shift Keying
CT	-	Current Transformer
DFSK	-	Demodulator Frequency Shift Keying
DCE	-	Data Communication Equipment
DTE	-	Data Terminal Equipment
DTL	-	Diode Transistor Logic
EIA	-	Electronic Industries Association
EEPROM	-	Electrically Erasable and Programmable Read Only Memory
FSK	-	Frequency Shift Keying
FM	-	Frequency Modulation
GPR	-	General Purposes Register
LCD	-	Liquid Crystal Display
PIC	-	Peripheral Interface Controller
PSK	-	Phase Shift Keying
PLL	-	Phase Locked Loop
PT	-	Potential Transformer
RAM	-	Random Access Memory
RISC	-	Reduced Instruction Set Computer
TTL	-	Transistor Transistor Logic
VCO	-	Voltage Controlled Oscillator
USART	-	Universal Synchronous and Asynchronous Receiver and Transmitter
XOR	-	Exclusive OR gate

Chapter 1

Introduction

1. INTRODUCTION

Our project deals with online monitoring of energy consumption and maximum demand through telephone line networks. Power is an essential requirement of all industries and the maximum demand of the industries should be kept well within the boundaries specified by Electricity Board. Hence it is essential to make monitoring of these parameters.

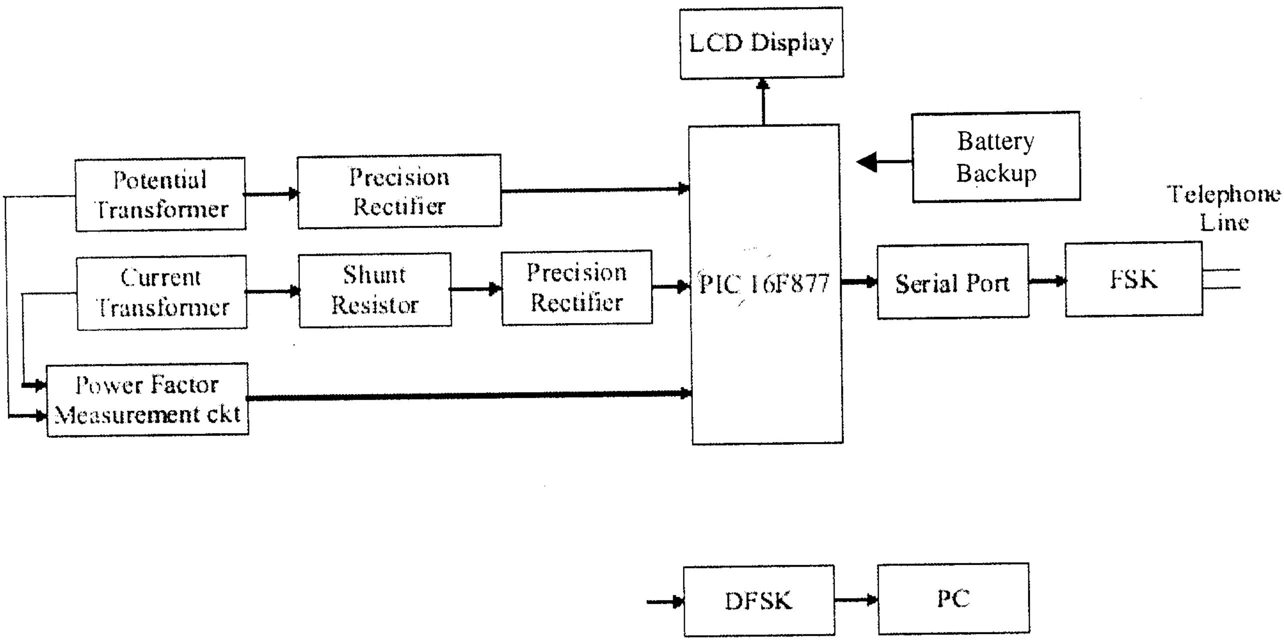
In olden days analog meters were used for measuring energy in the industries. The analog meters lags in precision and accuracy due to the frequently occurring errors such as

- Incorrect phase displacement error.
- Frictional error.
- Creeping error.

Thus in our project the digital meters is used instead of conventional analog meters. The digital meters have many advantages over analog meters such as the readings are precise and accurate, the lifetime is high as no mechanical moving parts and also the efficiency is improved.

The digital meter is designed using PIC microcontroller. The datas are transmitted from PIC microcontroller using telephone lines. FSK modulator and demodulator are used in the transmitting and receiving end respectively. Thus the energy and maximum demand are monitored in the personal computer.

1.1 BLOCK DIAGRAM



The block diagram comprises of two main parts namely transmitter and receiver. In the transmitter side voltage, current and powerfactor signals are sensed and given to the microcontroller. Energy and maximum demand are calculated in the PIC microcontroller. A LCD display connected to the PIC microcontroller displays the necessary parameters on the transmitter side. The datas are transmitted through telephone lines. FSK modulation technique is used to interface the datas with the telephone lines.

In the receiver side the modulating signal is recovered using FSK demodulator. The datas are then interfaced with personal computer.

The voltage and current signal is sensed and stepped down using potential transformer and current transformer respectively. The signals are then given to precision rectifier to be converted into an equivalent dc signals. The voltage measurement circuit and the current measurement circuits are alike except that a current measurement circuit consists of a shunt resistor. The output is then given to PIC microcontroller.

The same voltage and current signals are given to power factor measurement circuit. The circuit comprises of zero crossing detector along with IC5 to calculate the time lag between voltage and current signals from which power factor can be calculated. The output of the IC5 is also given to the PIC microcontroller.

The voltage, current and power factor is then manipulated in the PIC microcontroller and the power, energy and maximum demand are calculated. The Peripheral Interface Controller used is PIC 16F877.The presence of an inbuilt A to D converter; power saving sleep mode and many other features has made this PIC suitable for this project.

The voltage, current, power factor and energy are displayed using a LCD display. The maximum demand is also displayed whenever the demand is exceeded.

In the case of power failure, the microcontroller is powered by the 3V batteries in series, which provides voltages in the range of 4.5V to 5.5V. The serial EEPROM is available to provide non-volatile storage. Hence this circuit provides the additional advantage of viewing the energy even at the times of power failure.

The above mentioned parameters are then transmitted through telephone lines to the personal computer at the receiving end. At the transmitting end a FSK modulator is used to modulate the signal suitable for the transmission. IC6 is used to design the FSK modulator. At the receiving end, a FSK demodulator receives the datas and retrieves the original signal. IC7 is used to build the demodulator circuit. The datas are then interfaced with personal computer.

Chapter 2

Hardware

2. HARDWARE DESCRIPTION

2.1 POWER SUPPLY CIRCUIT

Power supplies are extensively used in all industrial application. It provides regulated ripple free output waveform.

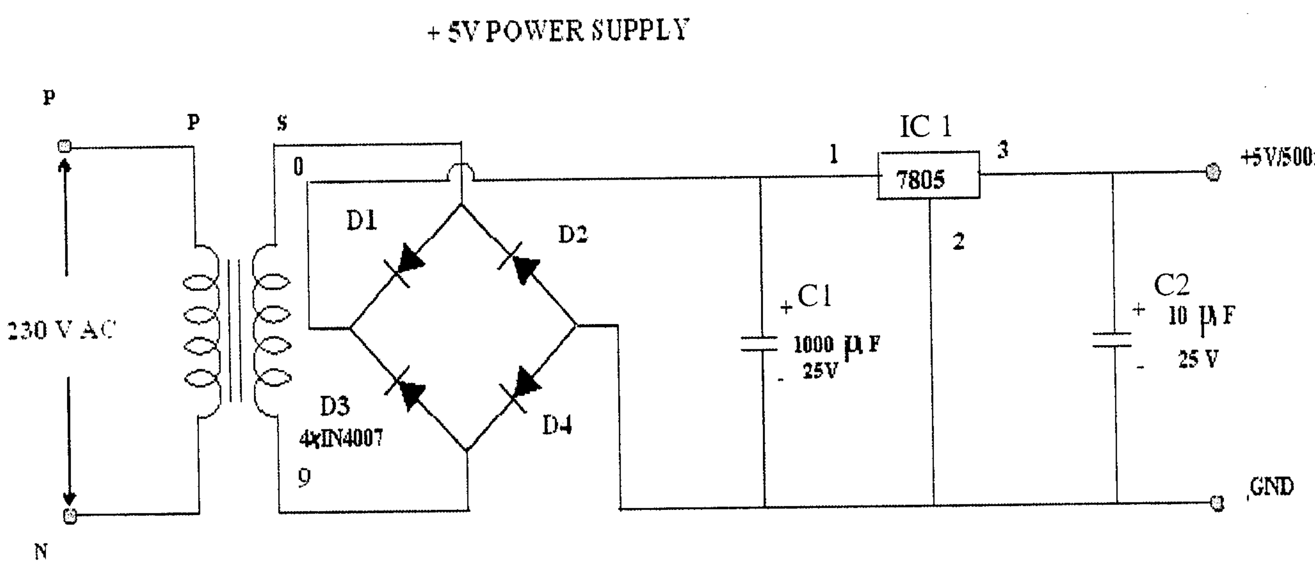


Figure 2.1.1 Power supply circuit

The present chapter introduces the operation of power supply circuits built using rectifiers, filters, and then voltage regulators. Starting with an ac voltage, a DC voltage is obtained by rectifying the AC voltage, then filtering to a DC level, and finally, regulating to obtain a desired fixed DC voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a even if the input DC voltage varies, or the output load connected to the DC voltage changes.

A block diagram below in figure 2.2.2 the parts of a typical power supply. The AC voltage is connected to a transformer, which steps that AC voltage down to the level for the desired AC output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a steady dc voltage.

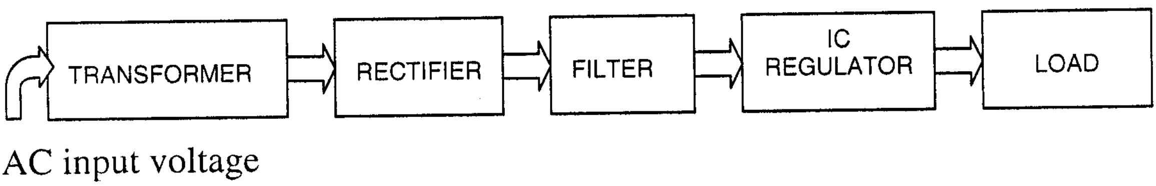


Figure 2.2.2 Power Supply Block Diagram

The resulting DC voltage usually has some ripple or AC voltage variation. The DC voltage is then given to a regulator circuit. A regulator circuit provides a DC voltage that not only has much less ripple voltage but also remains the same even if the input DC voltage varies, or the load connected to the output DC voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units.

2.1.1 STEP DOWN TRANSFORMER

The AC voltage is applied to the primary winding of a power transformer. It is stepped down to required value. In our circuit, the transformer of 230V / 9V, 15V-0-15V is used to perform the step down operation from 230V AC to required voltages at the secondary windings. The reason for selection of such a transformer is that +5V DC can be got from 9V AC and +12V,-12V can be got from 15V-0-15V.

2.1.2 RECTIFIER UNIT

In the power supply unit, rectification is normally achieved using full wave bridge rectifier. For positive half cycle, diode D1 and D4 conducts together and for negative half cycle diode D2 and D3 conducts. Thus the output is obtained for both positive and negative cycles.

2.1.3 FILTERING UNIT

Filter circuits, in which usually capacitor is acting as a surge arrester, always, follow the rectifier unit. This capacitor is also called as a decoupling capacitor or a bypassing capacitor, is not only used to 'short' the ripple to ground but also to leave the frequency of the DC to appear at the output.

2.1.4 VOLTAGE REGULATOR

It plays an important role in any power supply unit. The primary purpose of a regulator is to aid the rectifier and filter circuit in providing a constant DC voltage to the device. Power supplies without regulators have an inherent problem of changing DC voltage values due to variations in the load or due to fluctuations in the AC voltage. With a regulator connected to the DC output, the voltage can be maintained within a close tolerant region of the desired output.

The series 78XX regulators provide fixed regulated voltages from 5 to 24 V. IC1, is connected to provide voltage regulation with output from this unit of +5V dc. An unregulated input voltage is filtered by capacitor C1 and connected to the IC's terminal 1. The IC's terminal 3 provides a regulated +5V, which is filtered by capacitor C2 (mostly for any high-frequency noise). The third IC's terminal 2 is connected to ground (GND). While the input voltage may vary over some permissible voltage range, and the output load may vary over some acceptable range, the output voltage remains constant within specified voltage variation limits. A table of positive voltage regulated ICs is provided in table

TABLE 2.1.1 POSITIVE VOLTAGE REGULATORS IN 7800 SERIES

IC Part	Output Voltage (V)	Minimum Vi (V)
7805	+5	7.3
7806	+6	8.3
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7

2.2 VOLTAGE MEASUREMENT

Voltage measurement circuit comprises of a potential transformer and precision rectifier. Potential transformer is used for sensing and stepping down the voltage signal. Precision rectifier converts the AC signal into an equivalent DC signal. The PT output is also used for power factor manipulation. The output of this circuit (Vout) is given to Microcontroller and a linear programming is executed in the controller to manipulate and acquire original voltage of the transformer.

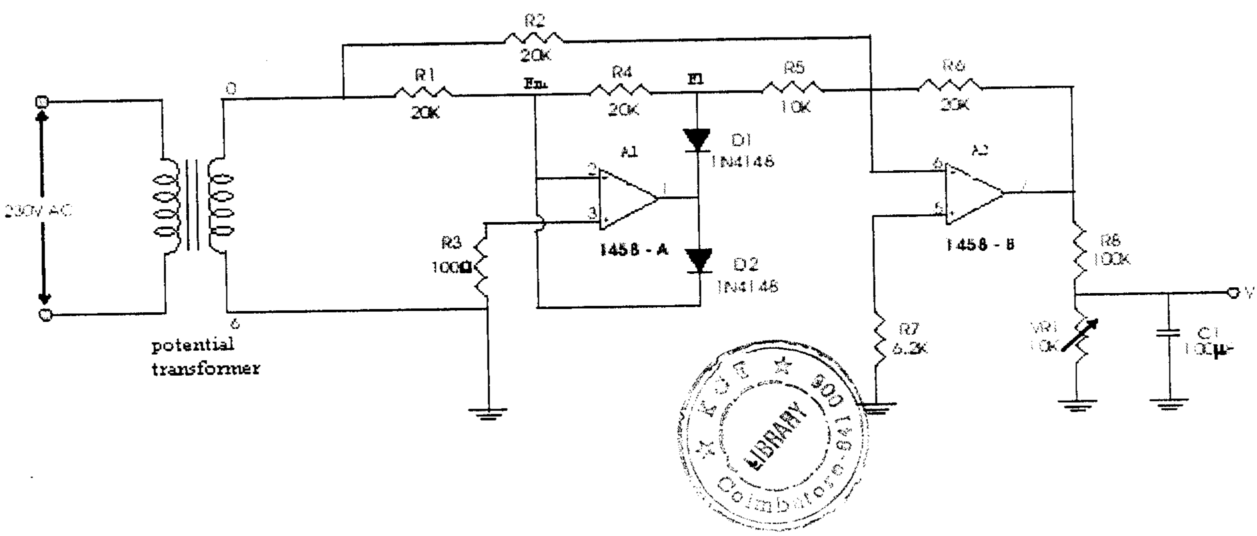


Figure 2.2.1 Voltage Measurement Circuit

2.2.1 POTENTIAL TRANSFORMER

The primary winding of the potential transformer is connected across the line carrying the voltage to be measured and the voltage circuit is connected across the secondary winding. The design of potential transformers is quite similar to that of a power transformer but the loading of a potential transformer is always small, sometimes only a few volt-amperes. The normal secondary voltage rating is 6 V.

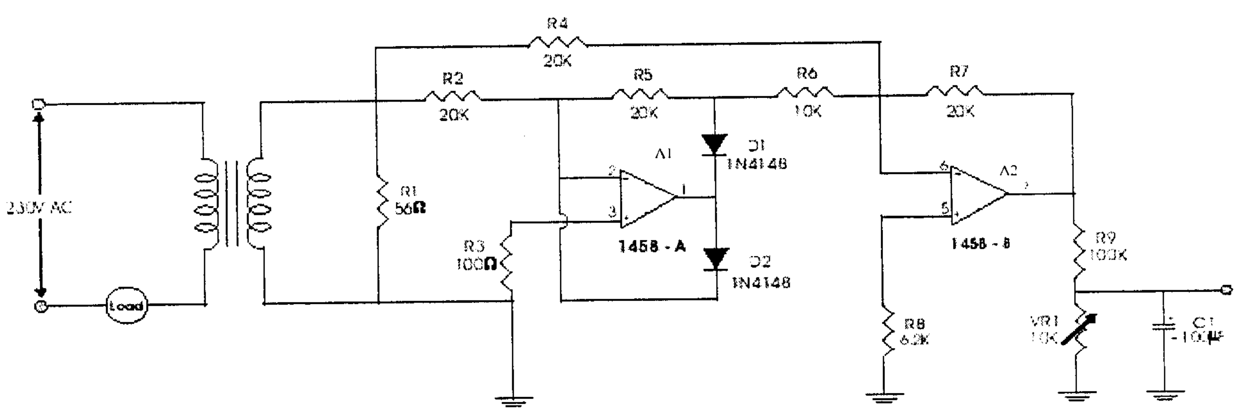
2.2.2 ABSOLUTE VALUE CIRCUITS (FULL-WAVE PRECISION RECTIFIER)

An absolute-value circuit, or full-wave precision rectifier, can be implemented by summing the output of a half-wave rectifier and its input with the proper phase and amplitude relations. This circuit will be the starting point for a number of other absolute-value circuits, which have evolved from this basic form.

In this circuit, A1 is an inverting rectifier similar to the figure. The output from A1 is added to the original input signal in A2 (a summing mixer) with the signal amplitude and phase relations shown. Negative alterations of Ein feeds A2 through R2 resistor, and E1 feed A2 through a R5 resistor. The net effect of this scaling is that, for equal amplitudes of Ein and E1, E1will provide twice as much current into the summing point. This fact is used to advantage here, as the negative alteration of E1 produces twice the input current of that caused by the positive alternation of Ein. This causes a current of precisely half the amplitude, which E1 alone would generate due to the receiver and having Ein non-existent during this half cycle, and it results in a positive going output at A2. During negative alterations of Ein, E1 is absent and Ein produces the alternate positive output swing that, in summation, produces the desired full-wave rectified response. As before, operation with the opposite output polarity is possible by reversing D1 and D2.

2.3 CURRENT MEASUREMENT

The current measurement circuit consists of Current transformer of turns ratio 100:1.The Current Transformer's primary winding is connected in series with the line. The secondary of the Current Transformer is connected to a precision rectifier network. The CT is rated at 15A/150mA.The shunt resistor R1 is connected across the secondary of the CT. AC voltage proportional to the current flowing through the secondary of the CT is given as the input to the rectifier unit and by a similar procedure as seen in case of voltage measurement, we get pure DC at the output stage of the rectifier.



2.4 POWER FACTOR MEASUREMENT

The Power Factor measurement circuit comprises of zero crossing detector, buffer using transistor and an XOR gate. PT and CT are used to provide the voltage and current signals respectively. The secondary winding is connected to ZCD, where the sine wave is converted into square wave at the output.

In inverting Zero crossing detector, time varying signal is applied at the inverting input terminal. The output of the Zero crossing detector swings between two voltage levels according to the input voltage applied. Thus a square wave is obtained as the output. Hence the circuit is also called as sine to square wave generator.

The pulsating output is given as an input to the buffer. Corresponding to the input, the buffer provides 0V or 5V as an output which is then given to the XOR gate. The output of the gate depends upon the input given. The truth table of XOR gate is

$$F = XY' + X'Y$$

Table 2.4.1 Truth Table

X	Y	F
L	L	L
L	H	H
H	L	H
H	H	L

The IC5 output will be high during the non-overlapping period of voltage and current, which is the indirect measure of lag or lead between voltage and current. A timer is incremented during the non-overlapping period; its value in millisecond is equivalent to corresponding phase angle in degrees. Leading or lagging power factor is determined based on the pulse at the output of voltage's Zero Crossing Detector during non-overlapping period.

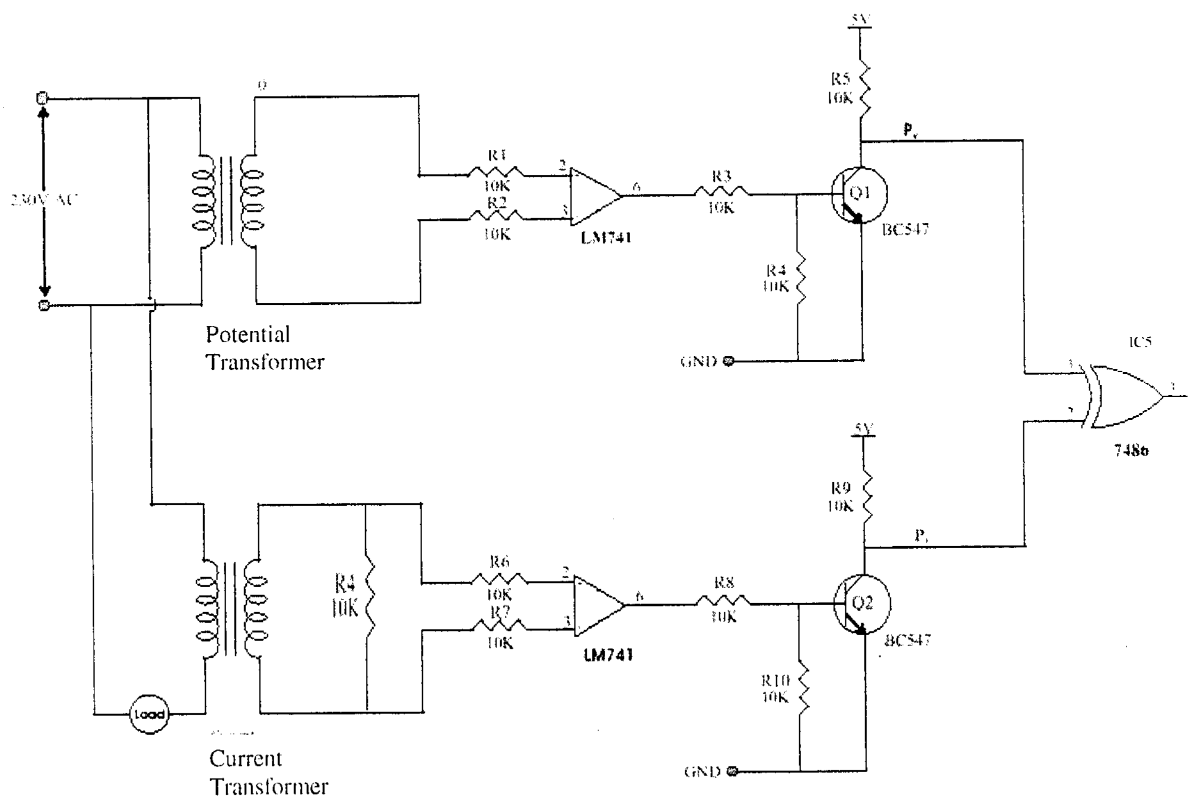


Figure 2.4.1 Power Factor Measurement Circuit

2.5. BATTERY BACKUP CIRCUIT

In general in the conventional analog meters the reading of the meter can be noted even if there is any possible power failure. But this is not the case regarding the digital circuits and hence a battery backup is provided in any case of power failure. The battery backup section consists of two 3V batteries, B1 and B2, in series with diodes D9A and D9B, and an inbuilt serial EEPROM in PIC microcontroller.

2.5.1. BATTERIES

In the event of power failure, the 3V batteries in series, which provides voltages in the range of 4.5V to 5.5V at the cathode of D9B.The 3V batteries used are lithium ion cell batteries, which power the microcontroller. The batteries have a 180-mAh rating.

2.5.2. DC POWER SUPPLY

IC2 is a low dropout 5.0V regulator. Diode D6 in series with diode D1 increases the virtual ground point for regulator IC2 by one schottky diode drop. Diode D1 provides the virtual ground point for regulator IC2, which is one diode drop above ground potential. The regulated output of IC2 adds to the diode drop at IC2 GND terminal.

Diode D8, D15, and diode D9, provides an output of 4.5V – 5.5V from batteries B1 and B2.Diode D13, limits voltage undershoot at the output of 5V regulator IC2 when the AC input voltage drops out. Clamping the IC2 output at ground potential prevents the regulator from sensing a negative output voltage and entering an output shut down mode when AC input voltage returns.

Battery operation requires D8 and D13 to have a low reverse current specification. These diodes which have a reverse leakage current of 200 nA at maximum reverse peak voltage.

2.5.3. SERIAL EEPROM

The inbuilt serial EEPROM is available in PIC microcontroller to provide non-volatile storage for key parameters during power failures. The last calculated watt-hour value should be added to the last cumulative watt-hour value previously written to the serial EEPROM. The resulting sum should be written to the serial EEPROM. The serial EEPROM is 256x8 byte electrically erasable PROM ~~that operates down to 1.8V~~.

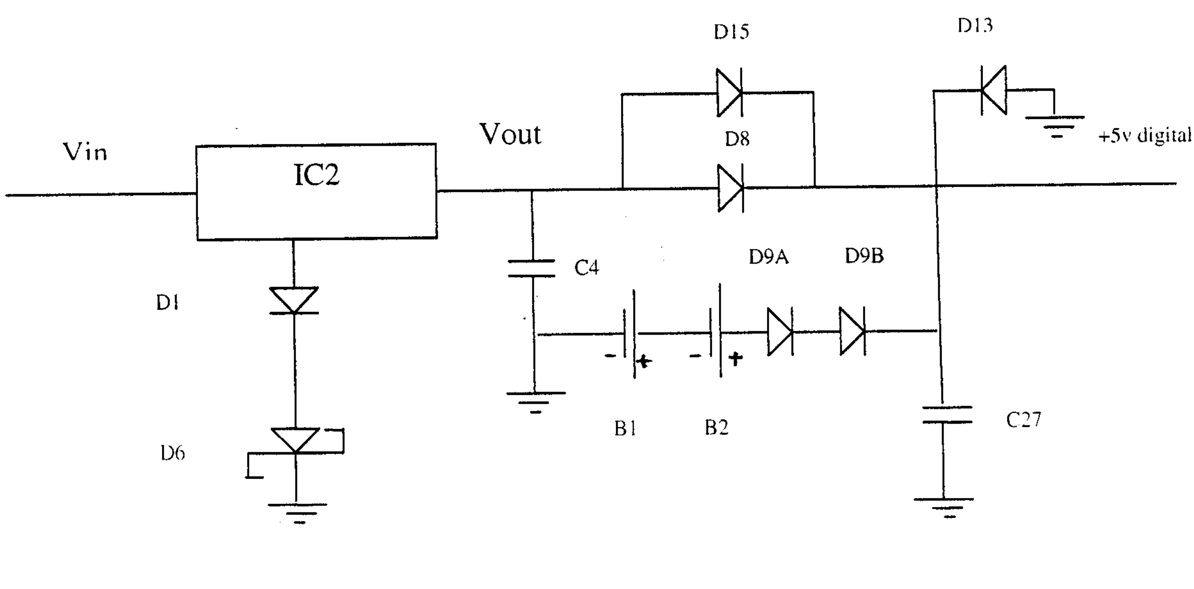


Figure 2.5.1 Battery Backup Circuit

Chapter 3

3.PIC16F877

3.1 GENERAL DESCRIPTION

All PIC employ an advanced RISC architecture. PIC microcontroller has following architectural features to attain the high performance:

- ❖ Harvard architecture
- ❖ Long word instructions
- ❖ Single word instruction
- ❖ Orthogonal instruction
- ❖ Instruction pipeline
- ❖ Register file architecture

The instruction and data bus of Harvard architecture allows a 14-bit wide instruction word with separate 8-bit wide data bus. The two stage instruction pipeline allows all instruction to execute in single cycle except for program branches which requires two cycle. Only 35 instructions are to be learned.

The PIC family has special feature to reduce external components thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options of which the single RC pin oscillator, which minimizes power consumption. Highly reliable Watch Dog Timer with its own on chip RC oscillator provides protection against software lock-up.

The device has flash memory, which allows it to be used for prototyping and protection. The circuit reprogram ability allows the code to be updated without devices to be removed from the end application where the

3.2 HIGH PERFORMANCE RISC CPU FEATURE

All instructions are single cycle except for program branches, which are two cycles. Operating speed is DC - 20 MHz clock input, 14 bit wide instruction, 8 bit wide data bus, 14 interrupts, up to 8Kx 14 words of FLASH Program Memory, up to 368 x 8 bytes of Data Memory (RAM), up to 256 x 8 bytes of EEPROM data memory.

3.3 PERIPHERAL FEATURES

- Timer0: 8-bit timer/counter with 8-bit prescaler.
- Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep via external crystal/clock.
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler.
- Two Capture, Compare, PWM modules
    - Capture is 16-bit, max. resolution is 12.5 ns.
    - Compare is 16-bit, max. resolution is 200 ns.
    - PWM max. resolution is 10-bit.
- 10-bit multi-channel Analog-to-Digital converter.
- Universal Synchronous Asynchronous Receiver.
- Transmitter (USART/SCI) with 9-bit address detection.
- Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls (40/44-pin only).

3.4 INPUT/OUTPUT PORTS

The input/output ports are used to interface the external peripherals with the microcontroller. Some of these input/output ports are multiplexed with an alternate function for the peripherals, which are in-built in the micro controller. In general when a peripherals is enable that pin may not be use a general-purpose input/output pin.

The analog channels present in the PORT A and PORT E are used as analog inputs for the voltage and current signals. These pins are configured as an input pins.

The PORT D is configured as an output port in order to communicate the 8 bit data for the LCD module. The three pins from PORT C are used as control line for the LCD module.

In PORT B the pins RB0 and RB5 are used as input pin and RB3 as output pin. The pin RB0 is connected with XOR gate output for the power factor calculations. The pin RB5 is connected with an external key provided to display the energy value during the power shut down periods. RB3 is connected to transistor driven buzzer unit. Its gives 5V signal to the transistor base whenever the maximum demand is exceeded and an alarm will be produced.

The pin RC6/TX is used for serial communication through USART module. It is also configured as output pin and connected to MAX-232 input. The above said input/output pins are shown in the Figure 3.1

3.5 A/D MODULE

PIC micro controller has a 10-bit A/D module. It consists of the following registers,

- A/D Result High Register (ADRESH).
- A/D Result Low Register (ADRESL).
- A/D Control Register 0 (ADCON0).
- A/D Control Register 1(ADCON1).

ADCON1 register is used to configure the analog and digital I/O pins and ADCON0 for selecting the channels and to start the A/D conversion process.

The ADRESH:ADRESL register contains the 10-bit result of the A/D conversion when the conversion is completed. The result is loaded in this A/D result register pair. The voltage and current signal are converted into10 bit equivalent digital value. These values are then get manipulated in the microcontroller, for power and energy calculation.

3.6 TIMER 0 MODULE

This module operates in either 8-bit timer/counter mode. In our project it is used as timer for time calculations.

The timer mode is selected by clearing bit T0CS of OPTION_REG<5>. The prescalar range is selected as 1: 256. The timer 0 module will increment after every 256 instruction cycles.

From the increment of TMR0 register the seconds are incremented and the time calculation are made to calculate the energy and to display the parameters on LCD.

3.7 TIMER 1 MODULE

It is a 16-bit timer/counter consisting of two 8-bit register (TMR1H and TMR1L). These register pair increments from 0000 to FFFFh.

This module is used as timer in order to calculate the time period of XOR gate output pulse, from the time period power factor can be calculated.

The timer1 control register (T1CON) is used to set the pre scalar value and to start the timer to increment the register pair (TMR1H and TMR1L). are made to increment on the rising edge and stopped at falling edge of the count pulse. The incremented values are then used for the calculation of power factor.

3.8 USART

The Universal Synchronous Asynchronous Receiver Transmitter (USART) module is one of two serial I/O modules. It is also known as serial communications interface. This module is configured as an asynchronous system that can used to communicate with personal

The following register are used to configure in asynchronous mode:

- TXSTA - Transmit status and control register.
- SPBRG - Baud rate generator register.
- RCSTA - Receive status and control register

The TXSTA register is used to enable the transmission, select asynchronous mode (to set Low/High baud rate) and to check the TSR register is empty or full.

The SPBRG register has the value of baud rate to be generated. The formula used is-

Baud rate=Fosc/16(X+1)

Where F osc – frequency of oscillator.

X – SPBRG register value

In our project 110-baud rate is used with SPBRG register value as 141. RCSTA register is used to select and enable serial port.

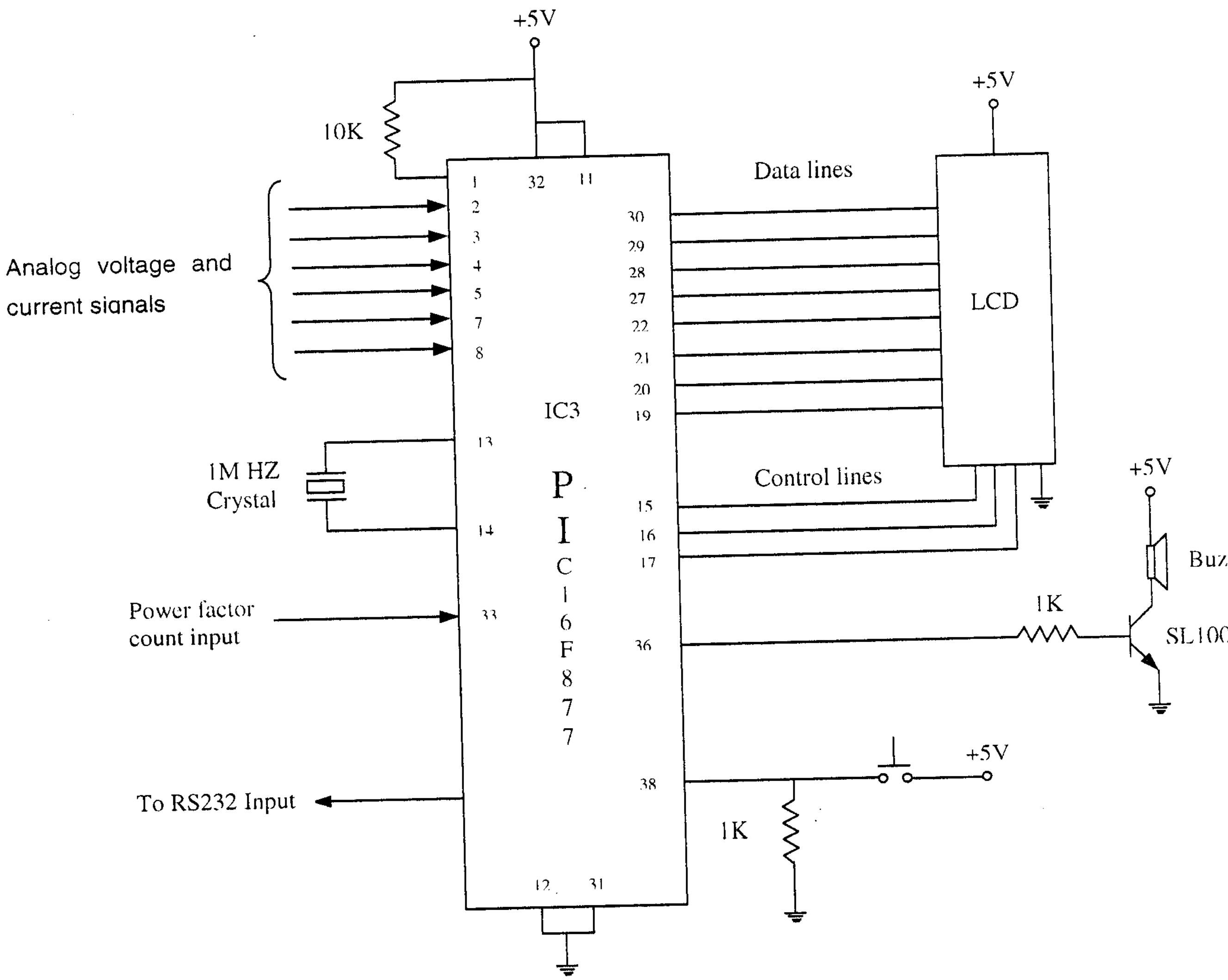


Figure 3.1 PIC Circuit

Chapter 4

LCD Display

4. LCD DISPLAY

Liquid crystal displays (LCDs) have materials, which combine the properties of both liquids and crystals. Rather than having a melting point, they have a temperature range within which the molecules are almost as mobile as they would be in a liquid, but are grouped together in an ordered form similar to a crystal. An LCD consists of two glass panels, with the liquid crystal material sand witched in between them. The inner surface of the glass plates are coated with transparent electrodes which define the character, symbols or patterns to be displayed polymeric layers are present in between the electrodes and the liquid crystal, which makes the liquid crystal molecules to maintain a defined orientation angle.

One each polarizer are pasted outside the two glass panels. These polarizers would rotate the light rays passing through them to a definite angle, in a particular direction. When the LCD is in the off state, light rays are rotated by the two polarizers and the liquid crystal, such that the light rays come out of the LCD without any orientation, and hence the LCD appears transparent.

When sufficient voltage is applied to the electrodes, the liquid crystal molecules would be aligned in a specific direction. The light rays passing through the LCD would be rotated by the polarizer, which would result in activating / highlighting the desired characters. The LCD's are lightweight with only a few millimeters thickness. Since the LCD's consume less power, they are compatible with low power electronic circuits, and can be powered for long durations. The LCD doesn't generate light and so light is needed to read the display. By using backlighting, reading is possible in the dark. The LCD's have long life and a wide operating temperature range.

Chapter 5

Transmitter

5.TRANSMITTER

The purpose of a communication system is to deliver a message signal from an information source in recognizable form to a user destination, with the source and the user being physically separated from each other. When the distance involved is large, it will not be economical to provide separate wires for communication purposes. In fact, for such long distance the telephone line provides a very good medium for transmission of information.

Within a limited environment, digital data can be transmitted directly as base band pulses. However, for transmission over telephone cables, it is necessary to encode the signals in forms in which spectra are shifted to higher frequencies. Hence we have combined the various advantages of telephone lines and digital communication for monitoring various electrical parameters.

5.1 MODULATION

The transmitter modifies the message signal into a form suitable for transmission over a channel. This modification is achieved by means of a process known as modulation, which involves varying some parameters of a carrier wave in accordance with the message signal.

5.1.1 MODULATION TECHNIQUES

The basic methods for binary transmission are amplitude shift keying (ASK), frequency shift keying (FSK), phase shift keying (PSK).

- ASK involves turning a carrier on and off to represent the binary values.
- FSK involves switching between two frequencies to represent the binary data.
- PSK involves switching between two phase to represent the binary data.

Here in our project we use FSK due to various advantages.

5.1.2 ADVANTAGES OF FSK

Principle benefits include: immunity to "adverse environment" conditions, the ability to transmit data across commutates or sparking sources the transmission of any type of data over any two conductor wire, shielded or unshielded, twisted or untwisted, including existing in-place writing .In summary, the FSK Advantage results in user-friendly ease of installation, operation and reconfiguration as well as significantly enhanced range, accuracy, reliability, and data integrity in hostile, harsh environments with the utmost in transparency . The advantage of FSK over on-off keyed continuous wave is that it rejects unwanted signals (noise) that are weaker than the desired signal. A signal is always present in the FSK receiver, automatic volume control methods may be used to minimize the effects of signal fading caused by ionosphere variations. The amount of inherent signal-to-noise ratio improvement of FSK over AM is approximately 3 to 4 dB.

This improvement is because the signal energy of FSK is always present while signal energy is present for only one-half the time in AM systems. Noise is continuously present in both FSK and AM, but is eliminated in FSK reception. Under the rapid fading and high-noise conditions that commonly exist in the high frequency (hf) region, FSK shows a marked advantage over AM. Overall improvement is sometimes expressed as the ratio of transmitted powers required to give equivalent transmission results over the two systems.

Such a ratio varies widely, depending on the prevailing conditions. With little fading, the ratio may be entirely the result of the improvement in signal-to-noise ratio and may be under 5 dB. However, under severe fading conditions, large amounts of power often fail to give good results for AM transmission. At the same time, FSK may be satisfactory at nominal power.

The power ratio (FSK versus AM) would become infinite in such a case.

5.2 BINARY FSK

Frequency shift keying (FSK) is the most common form of digital modulation in the High frequency radio spectrum, and has important applications in telephone circuits. Binary FSK (usually referred to simply as FSK) is a modulation scheme typically used to send digital information

The data are transmitted by shifting the Frequency of a continuous carrier in a binary manner to one or the other of two discrete frequencies. One frequency is designated as the "mark" frequency and the other as the "Space" frequency. The mark and space correspond to binary one and zero, respectively. By convention, mark corresponds to the higher Radio frequency. Figure 5.2.1 shows the relationship between the data and the transmitted signal.

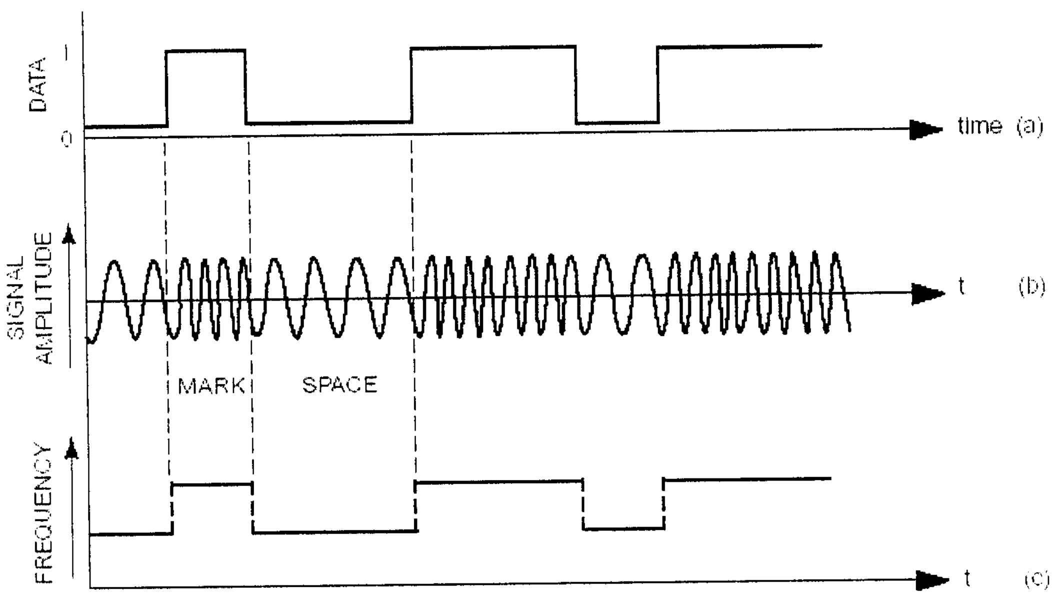
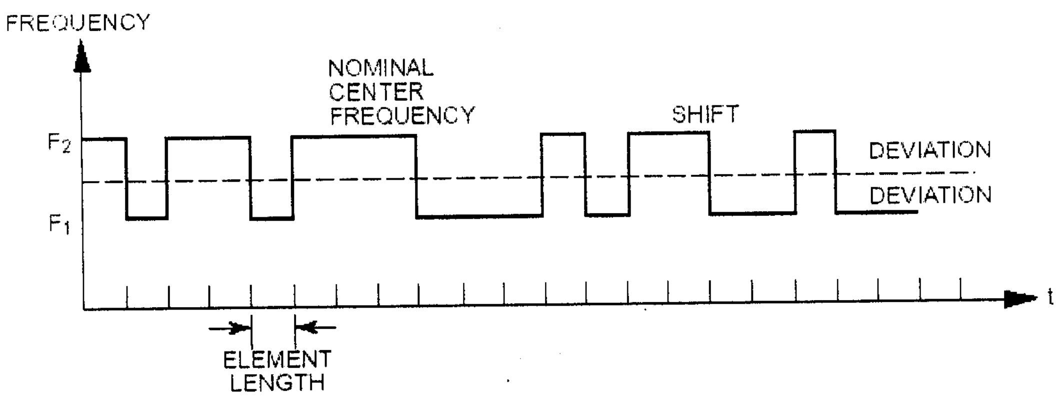


Figure 5.2.1 FSK Modulation

The minimum duration of a mark or space condition is called the element length. Typical values for element length are between 5 and 22 milliseconds, but element lengths of less than 1 microsecond and greater than 1 second have been used. Bandwidth constraints in telephone channels and signal propagation considerations in HF channels generally require the element length to be greater than 0.5 millisecond. An alternate way of specifying element length is in terms of the keying speed. The keying speed in "bauds" is equal to the inverse of the element length in seconds. Frequency measurements of the FSK signal are usually stated in terms of "shift" and center frequency. The shift is the frequency difference between the mark and space frequencies. Shifts are usually in the range of 50 to 1000 Hertz. The nominal center frequency is half way between the mark and space frequencies. The deviation is equal to the absolute value of the difference between the center frequency and the mark or space frequencies. The deviation is also equal, numerically, to one half of the shift.



$$\text{SHIFT} = |F_2 - F_1|$$

$$\text{CTR FREQ} = \frac{F_2 + F_1}{2}$$

$$\text{DEVIATION} = \frac{\text{SHIFT}}{2} = \left|\frac{F_2 + F_1}{2}\right|$$

$$\text{KEYING SPEED IN BAUDS} = \frac{1}{\text{ELEMENT LENGTH (IN SECONDS)}}$$

Figure 5.2.2 FSK Parameter

5.3 FSK GENERATOR

In our project, we use function generator (IC6) to generate two different frequencies to represent the binary data. The frequency which represents bit1, is called mark frequency and the one, which represents bit0, is called as space frequency.

5.3.1 MODULATOR IC

The XR-2206 (IC6) is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01Hz to more than 1MHz. The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage, while maintaining low distortion.

5.3.1.1 SYSTEM DESCRIPTION

The IC6 is comprised of four functional blocks; a voltage-controlled oscillator (VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches. The VCO produces an output frequency proportional to an input current, which is set by a resistor from the timing terminals to ground. With two timing pins, two discrete output frequencies can be independently produced for FSK generation applications by using the FSK input control pin. This input controls the current switches, which select one of the timing resistor currents, and routes it to the VCO.

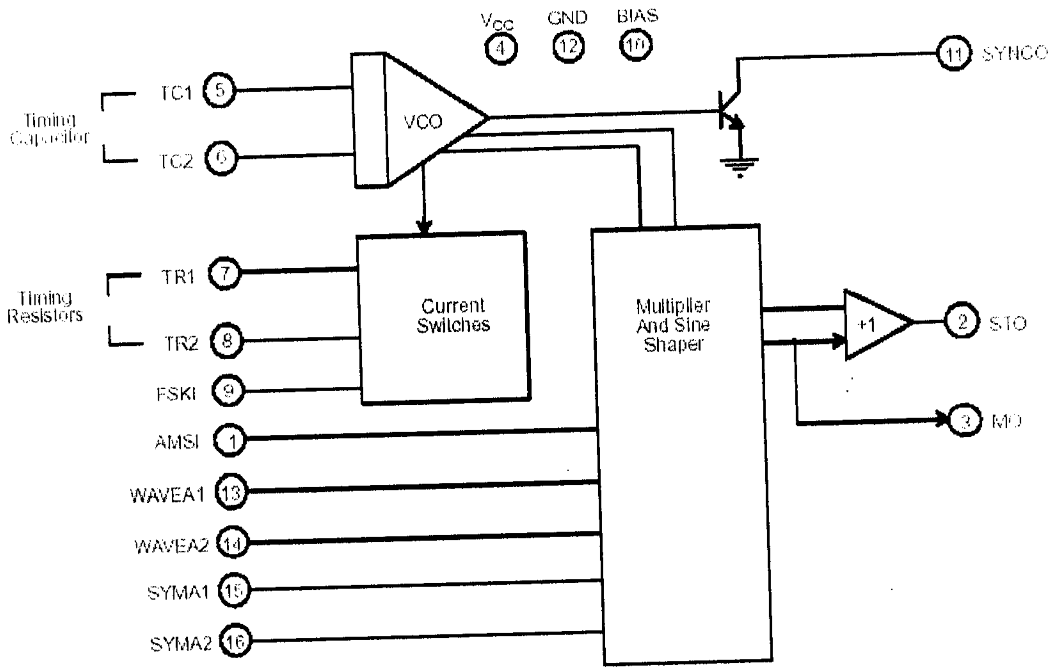


Figure 5.3.1.1 Block Diagram of IC6

5.3.1.2 FREQUENCY-SHIFT KEYING GENERATION

The IC6 can be operated with two separate timing resistors, R 1 and R 2, connected to the timing Pin 7 and 8, respectively. Depending on the polarity of the logic signal at Pin 9, either one or the other of these timing resistors is activated. If Pin 9 is open-circuited or connected to a bias voltage >= 2V, only R 1 is activated. Similarly, if the voltage level at Pin 9 is <=1V, only R 2 is activated. Thus, the output frequency can be keyed between two levels. f 1 and f 2 , as:

$$f_1 = 1/R_1 C \text{ and } f_2 = 1/R_2 C$$

For split-supply operation, the keying voltage at Pin 9 is referenced to V -. Mark and space frequencies can be independently adjusted by the choice of timing resistors, R 1 and R 2; the output is phase-continuous during transitions. The keying signal is applied to Pin 9. The circuit can be converted to split-supply operation by simply replacing ground with V -.

The pin 9 FSK input terminal of IC6 can be also used to provide the waveform generator with FSK operation, here a keying or pulse waveform is fed directly to pin 9 and circuit action is such that when this keying waveform is greater than +2V relative to –ve supply rail pin 7.R1 timing resistor is selected, but when the keying waveform is below +1V pin 8 R2 timing resistor is selected instead.

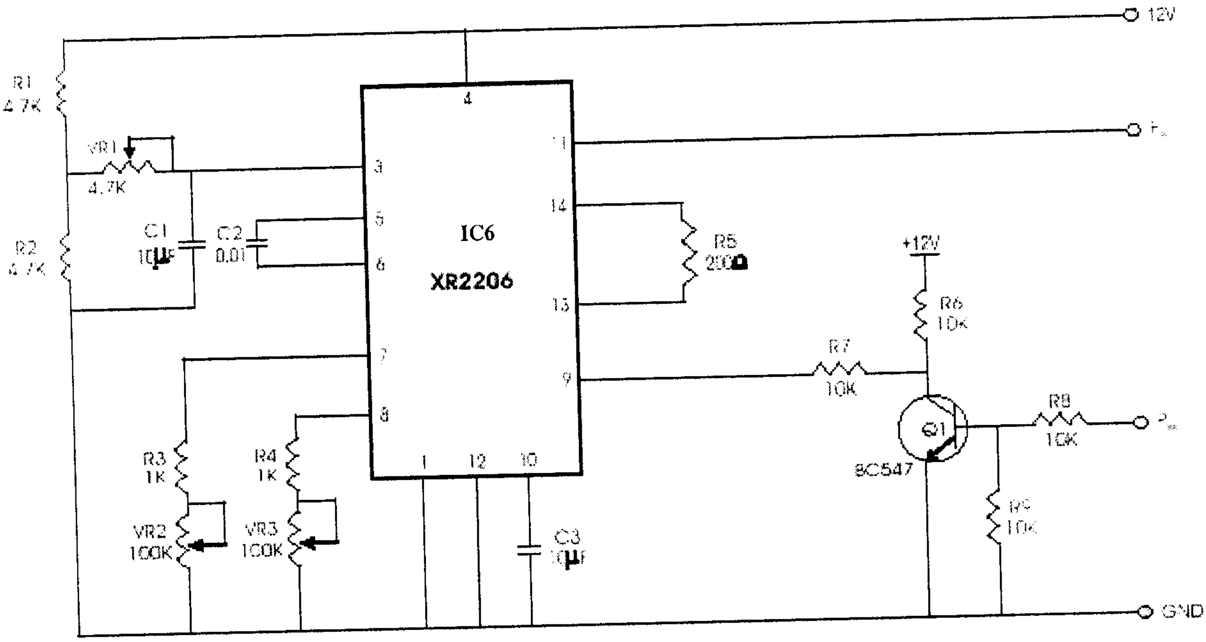


Figure 5.3.1.2 FSK Modulator

Chapter 6

Receiver

6. RECEIVER

The transmitted data are retrieved using a FSK demodulator circuit. The modulating signal is recovered from the demodulator circuit and interface to PC using RS232 logic.

6.1 FSK DEMODULATOR

A demodulator is a device that recovers the original information from a modulated signal (a signal that is modulated onto a carrier frequency). There are a large numbers of options for FSK detectors.

Some important considerations, which should be kept in mind, are sensitivity (ie does the detector require volts or micro volts to operate), maximum carrier frequency, and bandwidth. PLLs are a good option: eg the NE565 (up to .5 MHz). Thus in our project IC7 used as FSK demodulator.

The IC7 is a general purpose phase-locked-loop. The main advantages are accuracy and excellent rise time integrity. This signal may be fed through a capacitive coupling network to the Phase Detector reference input, Pin 3, and provides good matching for the input.

6.2 PHASE LOCKED LOOPS (PLL)

6.2.1 BASIC PRINCIPLES

The basic block diagram of PLL consists of

- Phase detector\comparator
- Low pass filter
- Error amplifier
- Voltage Controller Oscillator (VCO)

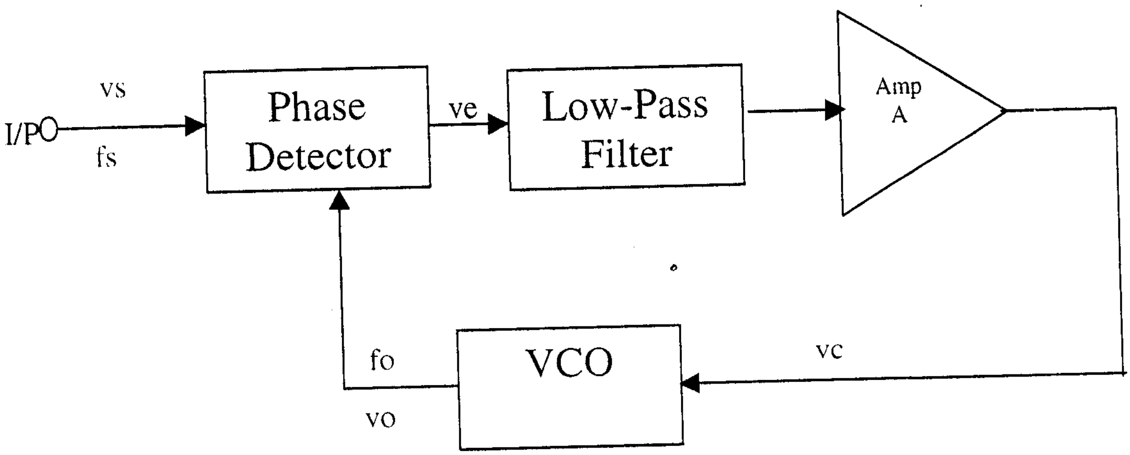


Figure 6.2.1.1 Block Diagram of PLL

The VCO is a free running multi-vibrator and operates at a set frequency f0 called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a DC control voltage Vc to an appropriate terminal of the IC. The frequency deviation is directly proportional to the DC control voltage and hence it is called as "Voltage Controller Oscillator", or in short VCO.

If an input signal Vs of frequency fs is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v0 of the VCO. If the two signals differ in frequency and\or phase, an error voltage Ve is generated. The phase detector is basically a multiplier and produces the sum (Fs+F0) and difference (Fs-F0) components at its output. The high frequency component (FS+F0) is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage V0 to VCO. The signal Vc shifts the VCO frequency in a direction to reduce the frequency difference between F0 and Fs. Once this action starts, we say that the signal is in capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is said to be locked. Once locked, the output frequency of VCO is identical to Fs expect for a finite phase difference. This phase difference generates a control voltage Vc to shift the VCO frequency from F0 to Fs and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages

- Free running
- Capture
- Locked or tracking

As capture starts, a small sine wave appears. This is due to the difference frequency between the VCO and the input signal. The DC component of the beat drives the VCO towards lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The difference in the frequency becomes smaller and a larger DC component is passed by the filter, shifting VCO frequency further. The process continues until the VCO locks on to the

The low pass filter controls the capture range. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond. We say that the signal is out of the capture band. However, once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band. Thus tracking range is always larger than the capture range.

Some of the important definitions in relation to PLL are:

LOCK-IN RANGE: once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range is usually expressed as a percentage of F0, the VCO frequency.

CAPTURE RANGE: The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of F0.

PULL-IN TIME: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

6.3 DEMODULATOR IC

6.3.1 GENERAL DESPRIPTION

The IC7 (IC PLL 565) is general purpose phase locked loops containing a stable, highly linear voltage controlled oscillator for low distortion FSK demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system bandwidth, response speed, capture and pull in range may be adjusted over a wide range with an external resistor and capacitor. The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.

565 is available as a 14_pin DIP package and as 10 pin metal can package. The output of the VCO (both inputs pins 2 and 3 grounded) is given by

$$\mathbf{F0=0.25/\,(Rt+Ct)\ Hz}$$

where Rt and Ct are the external resistor and capacitor connected to pin 8 and pin9. A value between 2Kohms and 20Kohms is recommended for Rt. The VCO free running frequency is adjusted with Rt and Ct to be the centre of the input frequency range. It may be seen that phase locked loop is internally broken between the VCO output and phase comparator input. A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare F0 with input signal Fs. Capacitor C is connected between pin 7 and pin 10 to make a low pass filter with the internal resistance of 3.6 Kohms.

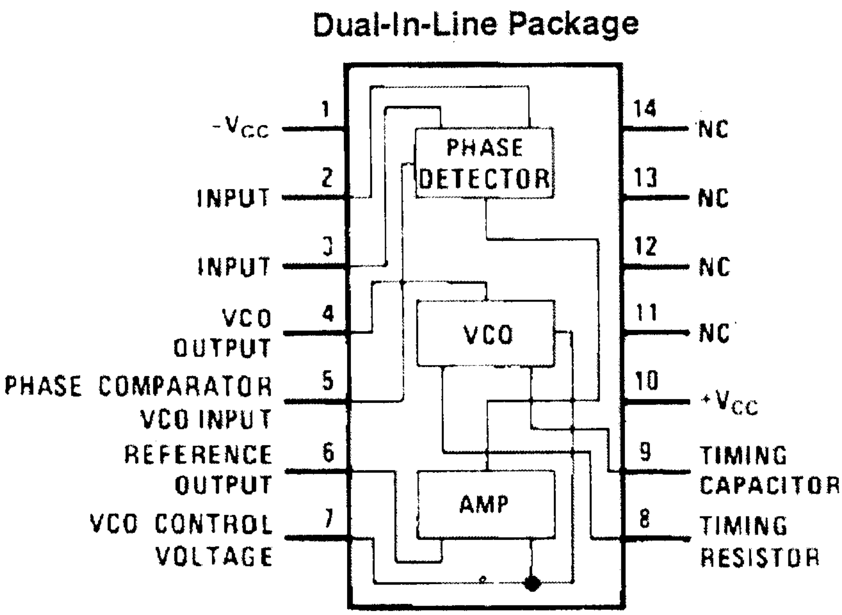


Figure 6.3.1.1 Pin Diagram of IC7

6.3.2 FEATURE

- 200 ppm/ deg C frequency stability of the VCO.
- Power supply range of 5 to 12 volts .
- 0.2% linearity of demodulated output.
- Linear triangle wave with in phase zero crossings available.
- TTL and DTL compatible phase detector input and square wave output.
- Adjustable hold in range .

6.3.3 FSK DEMODULATOR

The binary data can be retrieved using a FSK demodulator. The frequency range is 1070 Hz to 1270 Hz. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding DC shift at the output. A three stage filter removes the carrier component and the output signal is made logic compatible by a voltage comparator.

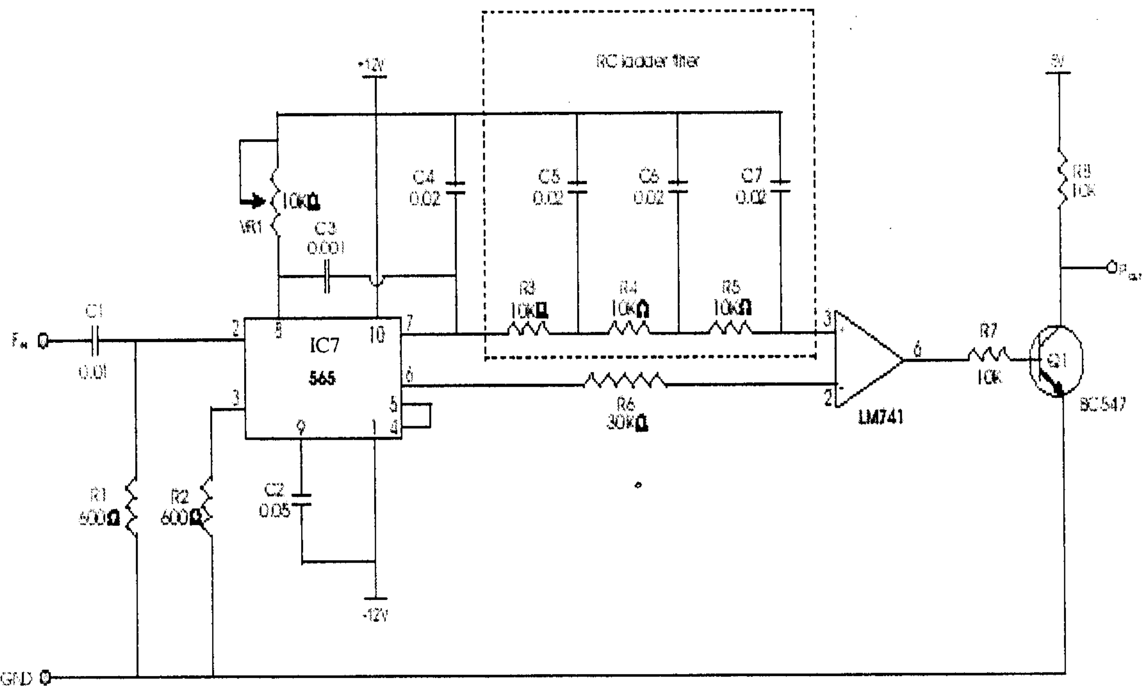


Figure 6.3.3.1 FSK Demodulator

Chapter 7

RS 232

7.RS232

7.1 RS232 SERIAL DATA STANDARD

In the 1900's as the use of time-share computer terminals became more widespread; modems were developed so that terminals could use phone lines to communicate with distant computers. Modems and other devices which are used to send serial data are often referred to as data communication equipment or DCE. The terminals or computers that are sending or receiving the data are referred to as data terminal equipment or DTE. In response to the need for signal and handshake standards between DTE and DCE, the Electronic Industries Association (EIA) developed standard RS-232. This standard also describes the voltage levels, impedance levels, rise and fall times, maximum bit rates, and maximum capacitance for these signal lines.

The voltage levels for all Rs-232 signals are as follows. A logic high, or mark, is a voltage between -3V and -15V under load (-25V under no load). A logic low or space is a voltage between 3V and 15V under load (25V under no load). Voltage such as 12V is commonly used. The output signal level usually swings between +12V and -12V. The "dead area" between +3V and-3V is designed to absorb line noise. Many receivers designed for RS-232 are sensitive to differentials of 1V or less.

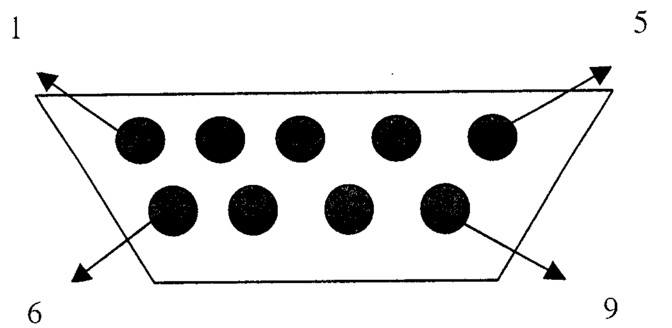


Figure 7.1 Pin diagram of RS232

TABLE 7.1 RS232 PIN ASSIGNMENTS

Pin1	Received line signal detector (data carrier detect)
Pin2	Received data
Pin3	Transmit data
Pin4	Data terminal ready
Pin5	Signal ground
Pin6	Data set ready
Pin7	Request to send
Pin8	Clear to send
Pin9	Ring indicator

7.1.1 PIN DESCRIPTION

1. DTR (Data Terminal Ready)

When the terminal is turned on, after going through a self-test, it sends out signal DTR to indicate that it is ready for communication.

2. DSR (Data Set Ready)

When DCE is turned on and has gone through the self-test, it asserts DSR to indicate that it is ready to communicate.

3. RTS (Request to Send)

When DTE device has a byte to transmit, it asserts RTS to signal the modem that it has a byte of data transmit.

4. CTS (Clear To Send)

In response to RTS when the modem has room for storing the data it is to receive, it sends out signal CTS to the DTE (PC) to indicate that it can receive the data now.

5. DCD (Data Carrier Detect)

The modem assert signal DCD to inform the DTE (PC) that a valid carrier has been detected and that contact between it and other modem is established.

6. RI (Ring Indicator)

An output from the modem (DCE) and an input to a PC (DTE) indicates that the telephone is ringing. It goes on and off in synchronization with the ringing sound.

While signals DTR and DSR are used by the PC and modem respectively, to indicate that they are alive and well, it is RTS and CTS that actually control the flow of data. RTS and CTS are also referred to as hardware control flow signals.

This concludes the description of the most important pins of the RS232 handshake signals plus TxD, RxD and ground. Ground is also referred to as SG (signal ground).

7.2 MAX 232

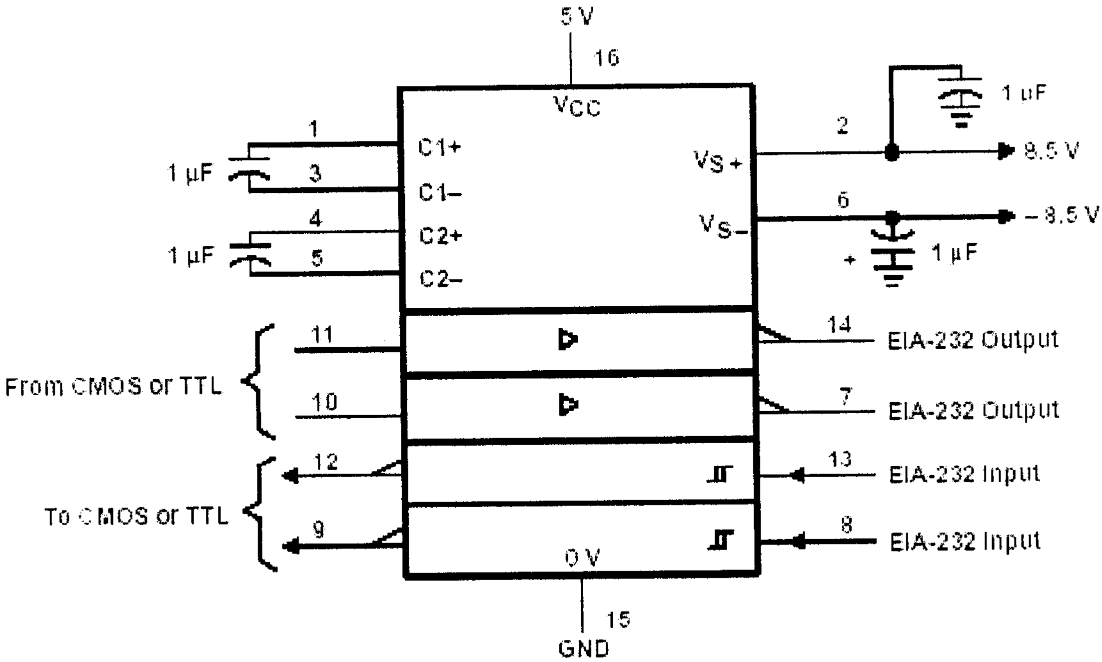


Figure 7.2.1 Typical operating circuit

The MAX232 device is a dual driver/receiver that includes a capacitive voltage generator to supply EIA-232 voltage levels from a single 5-V supply. Each receiver converts EIA-232 inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V and a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into EIA-232 levels.

Each of the two transmitters is a CMOS inverter powered by +10v internally generated supply. The input is TTL and CMOS compatible with a threshold of about 26% of Vcc. The input if an unused transmitter section can be left unconnected, an internal pull up resistor connected between transistor input and Vcc will pull the input high forming the unused transistor output low. The open circuit output voltage swing is guaranteed to meet RS 232 specification +5V output swing under the worst of both transmitter driving the minimum load impedance, the Vcc input at 4.5V and maximum allowable ambient temperature typical voltage with 5kΩ and Vcc = +9V.

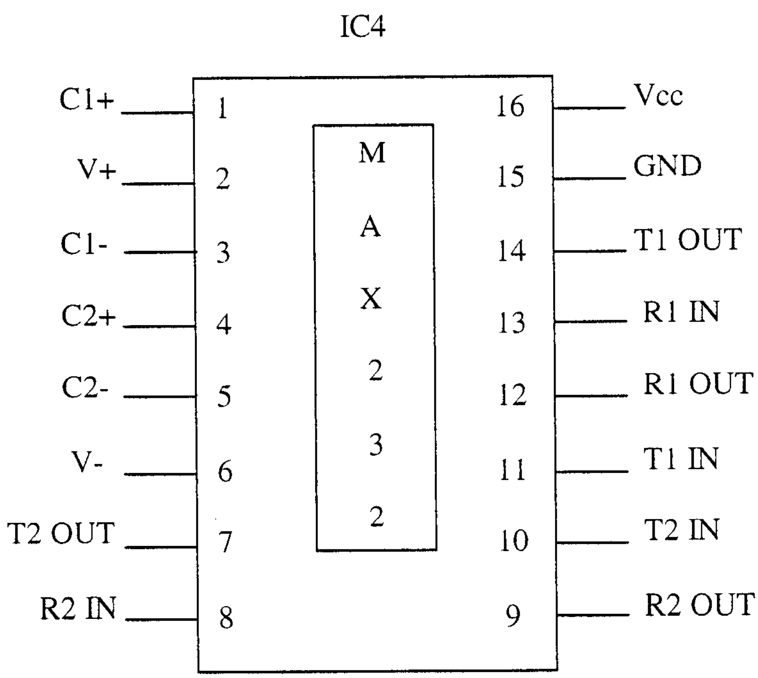


Figure 7.2.2 Pin Diagram of max 232

7.2.1 ELECTRICAL CHARACTERISTICS OF MAX 232

Vcc = 6V.

V+ = 12V.

V- = 12V.

7.2.1.1 INPUT VOLTAGE

T1 in, T2 in = -0.3 to (Vcc + 0.3V)

R1 in, R2 in = +30V or –30V.

7.2.1.2 OUTPUT VOLTAGE

TI out, T2 out = ((V+) + 0.3V) to ((V-) + 0.3V).

R1 out, R2 out = -0.3V to (Vcc + 0.3V).

Power dissipation = 375 mW.

Output resistance = 300Ω.

Conclusion

CONCLUSION

Initially the hardware of our project has been designed and tested successfully. The assembly codes for PIC Micro controller for calculation of necessary parameters were developed. In addition to that, battery backup circuit and EEPROM for storage of previous values was implemented.

The difficulties, which experienced, were the noise overlapping the data during transmission.

This project would serve its purpose where remote monitoring of the system is needed and maximum demand should be maintained within the limits. Apart from this it can be employed for domestic applications also.

FUTURE ENHANCEMENT

- Instead of telephone lines for transmission, wireless communication can be adopted.

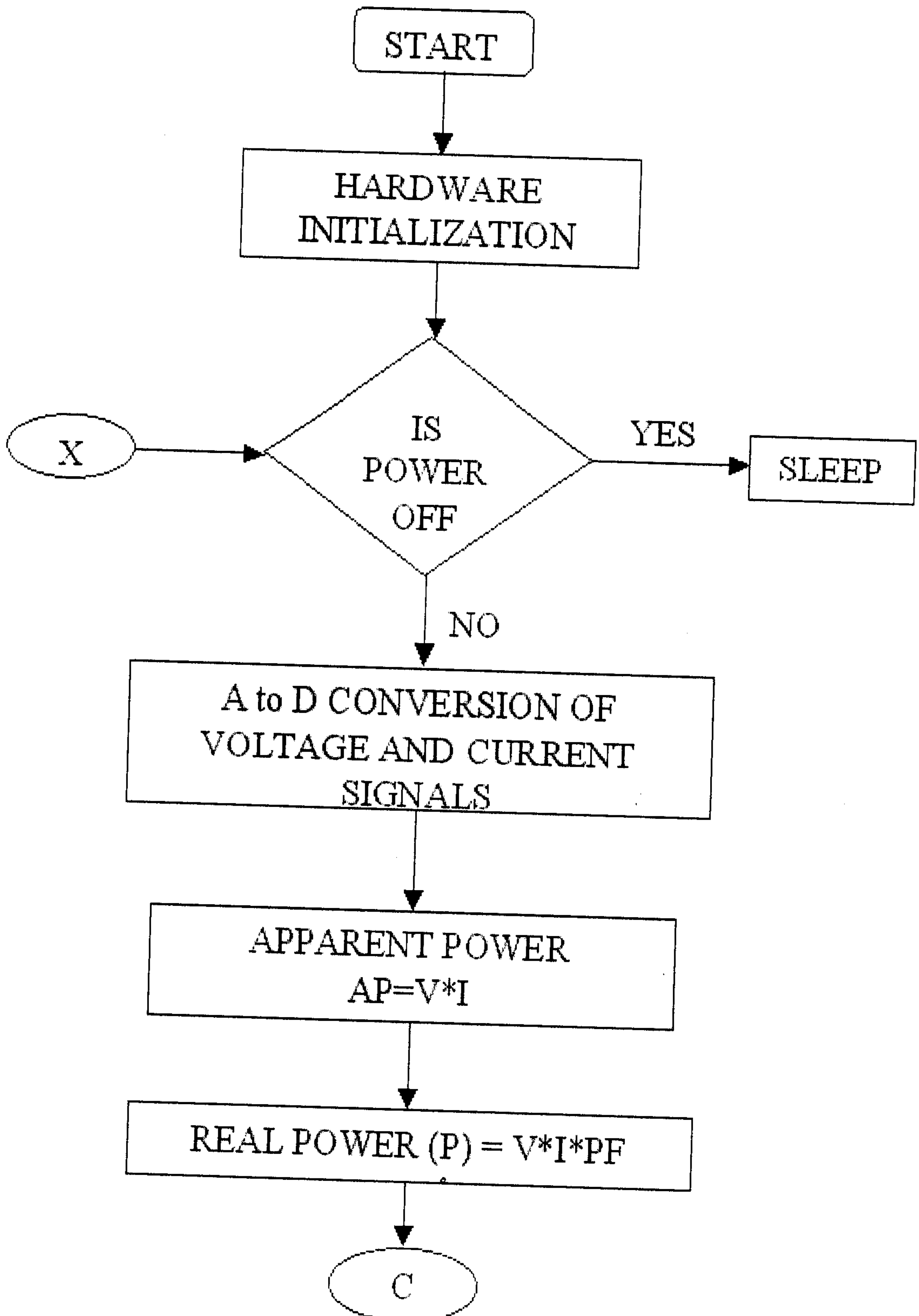
- Maximum demand if exceeded can be controlled by disconnecting the excess loads using relays.

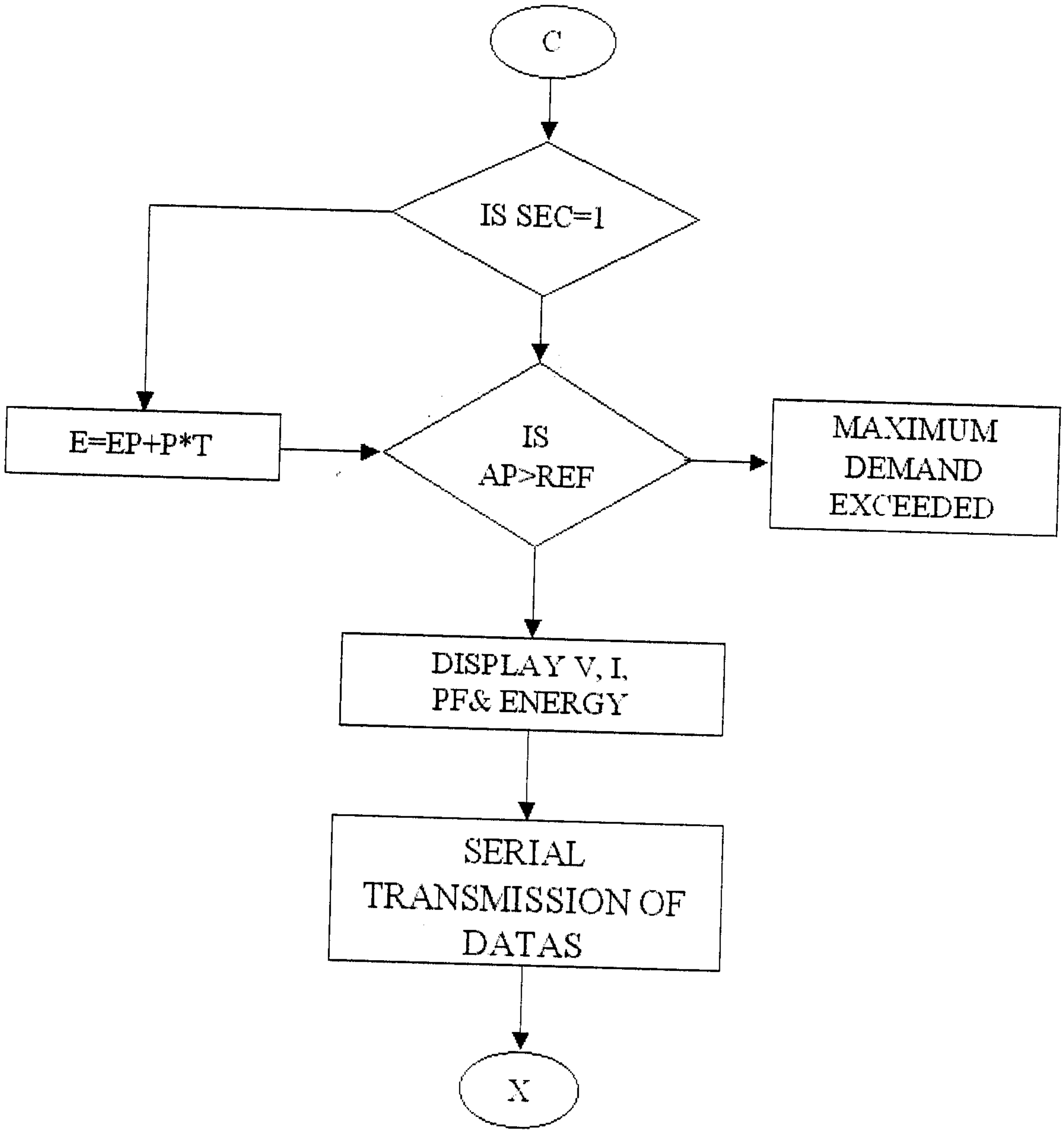
- Electricity bill can also be calculated and displayed.

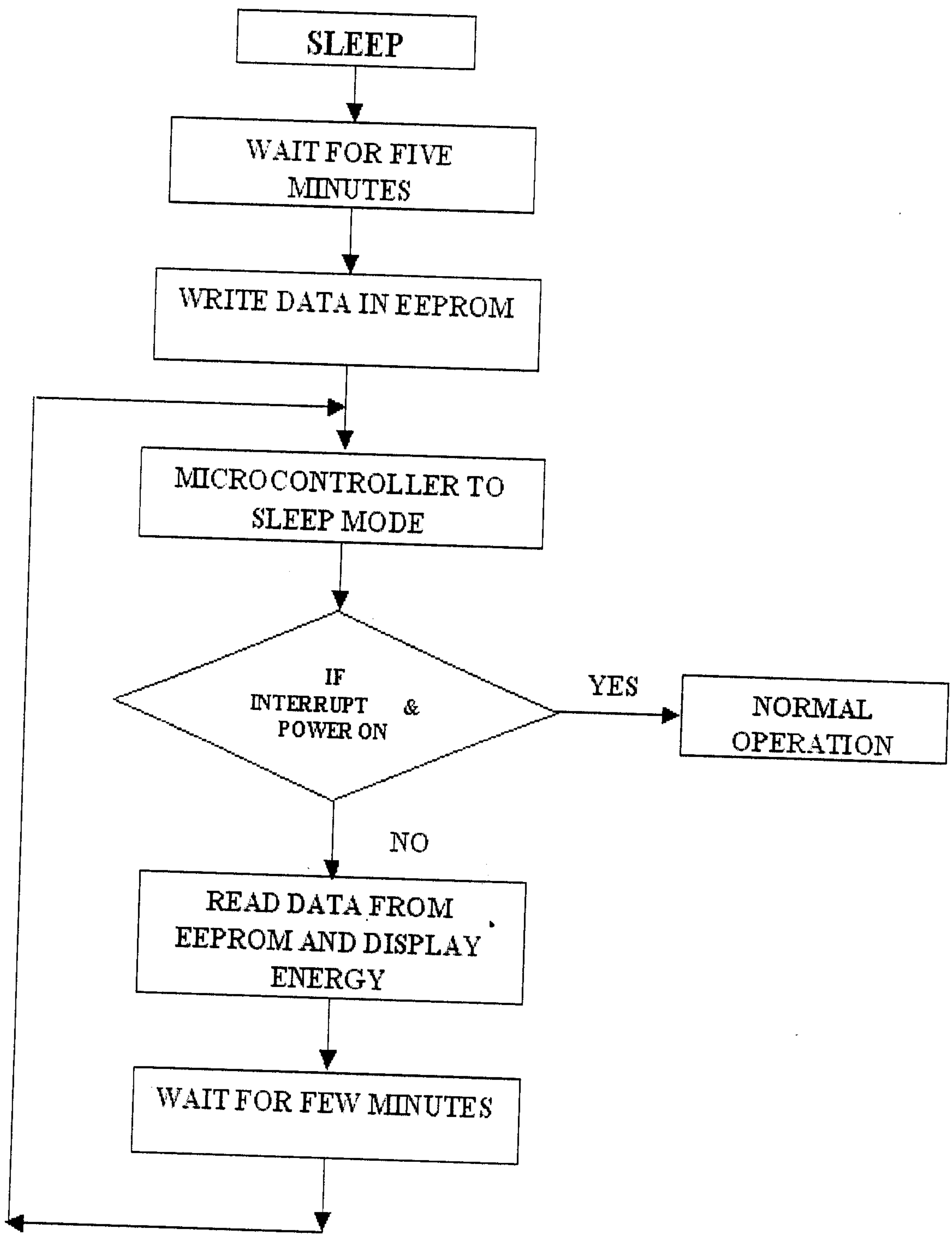
Appendix

APPENDIX 1

FLOWCHART




C
IS SEC=1
E=EP+P*T
IS
AP>REF
MAXIMUM
DEMAND
EXCEEDED
DISPLAY V, I,
PF& ENERGY
SERIAL
TRANSMISSION OF
DATAS
X


SLEEP
WAIT FOR FIVE MINUTES
WRITE DATA IN EEPROM
MICROCONTROLLER TO SLEEP MODE
IF INTERRUPT & POWER ON
YES
NORMAL OPERATION
NO
READ DATA FROM EEPROM AND DISPLAY ENERGY
WAIT FOR FEW MINUTES

PIC CODING

```
#include<pic.h>
#include<math.h>
#include "lcd.h"
static bit input @((unsigned) &PORTB*8+0);
bank1 unsigned char v1,v2,v3,i1,i2,i3,sec=0,ss,ad_flag=0,count,pulse_f;
unsigned char pf,t,numb;
unsigned long k,ap,p;
unsigned int val,l,e,ep;
float x,y;
bit disp_f,f,md,s0,s1,s2,flag,disp,read,wr_bit,tt,set;

void main()
 {
  ADCON1=0X80;
  TRISC=0XF0;
  TRISA=0XFF;
  TRISD=0;
  TRISB=0xFF;
  OPTION=0X87;
  GIE=1;
  PEIE=1;
  T0IE=1;
  TMR0=0;
  e=0;
  wr_bit=1;
  lcd_init();
  clear_lcd();
  SPBRG=242;
  SPEN=1;
  display_string(" DIGITAL METER ");
  while(1)
   {
     sleep();
     ADCON0=0x81;
     ADGO=1;
     while(ADGO);
     v1=((ADRESH*256)+ADRESL);
     ADCON0=0x89;
```

```
 v2=((ADRESH*256)+ADRESL);
 ADCON0=0x91;
 ADGO=1;
 while(ADGO);
 v3=((ADRESH*256)+ADRESL);
 ADCON0=0x99;
 ADGO=1;
 while(ADGO);
 i1=((ADRESH*256)+ADRESL);
 ADCON0=0xa1;
 ADGO=1;
 while(ADGO);
 i2=((ADRESH*256)+ADRESL);
 ADCON0=0xa9;
 ADGO=1;
 while(ADGO);
 i3=((ADRESH*256)+ADRESL);
 cal_powerfact();
 calcu_power();
 calcu_energy();
 transmit_values();
 if(s0==1 && disp_f)
  {
   s0=0;
   disp_f=0;
   display_scr1();
   s1=1;
   }
if(s1==1 && disp_f)
   {
    s1=0;
    disp_f=0;
    display_scr2();
    s2=1;
    }
}

void interrupt isr()
{
 if(RBIF)
```

```
  RBIF=0;
  if(RB7)
   {
    disp=0;
   }
  }
 if(T0IF)
  {
   T0IF=0;
   count++;
   if(count==15)
    {
     count=0;
     sec++;
    }
   if(sec==5)
    {
     sec=0;
    }
   }
}
void sleep()
{
  if(!RB7)
   {
    RBIE=1;
   }
 sleep:;
  if(!RB7 && RB5==0)
   {
    if(t==5)
    {
     T0IE=0;
     lcd_off();
     if(wr_bit)
      {
       write_data();
      }
     asm("SLEEP");
    }
   else
```

```
  t=0;
 if(disp)
  {
    lcd_on();
    T0IE=1;
    disp=0;
    goto sleep;
  }
 if(read && tt)
   {
   lcd_on();
   T0IE=1;
   }
}
cal_powerfact()
{
  TMR1IE=0;
  while(input==0);
  TMR1ON=1;
  while(input==1);
  TMR1ON=0;
  x=(TMR1H<<8)+TMR1L;
  y=cos(x);
  y=y*100;
  pf=y;
}
calcu_power()
{
 l=v1*i1;
 l=l/10;
 ap=ap+l;
 k=(long)l*pf;
 p=k+p;
 l=v2*i2;
 l=l/10;
 ap=l+ap;
 k=(long)l*pf;
 p=k+p;
}
calcu_energy()
{
```

```
{
 f=0;
 e=(int)(p/1200);
 e=ep+e;
 ep=e;
 }
}
display_scr1()
 {
   display_voltage1();
   display_energy();
 }

display_scr2()
 {
   display_voltage2();
   display_energy();
 }

display_scr3()
 {
  display_voltage3();
  display_energy();
 }
display_voltage1()
 {
   unsigned char temp=0;

   display('R');
   display(' ');
   display((v1/100)+0x30);
   display((i1/100)+0x30);
   display((pf/100)+0x30);

 }
void display_energy()
 {
  unsigned int temp;
  display('E');
  if(md==1)
   {
```

```
  display((ap/10000)+0x30);
  }
}
transmit_values()
 {
  unsigned int temp=0;
  ser_tx((v1/100)+0x30);
  ser_tx((v2/100)+0x30);
  ser_tx((v3/100)+0x30);
  ser_tx((i1/100)+0x30);
  ser_tx((i2/100)+0x30);
  ser_tx((i3/100)+0x30);
  ser_tx((pf/100)+0x30);
  ser_tx((e/10000)+0x30);
  ser_tx((ap/10000)+0x30);
 }
void ser_tx(unsigned char te)
 {
  TXREG=te;
  while(!TRMT);
  TRMT=0;
 }
```

VB CODING

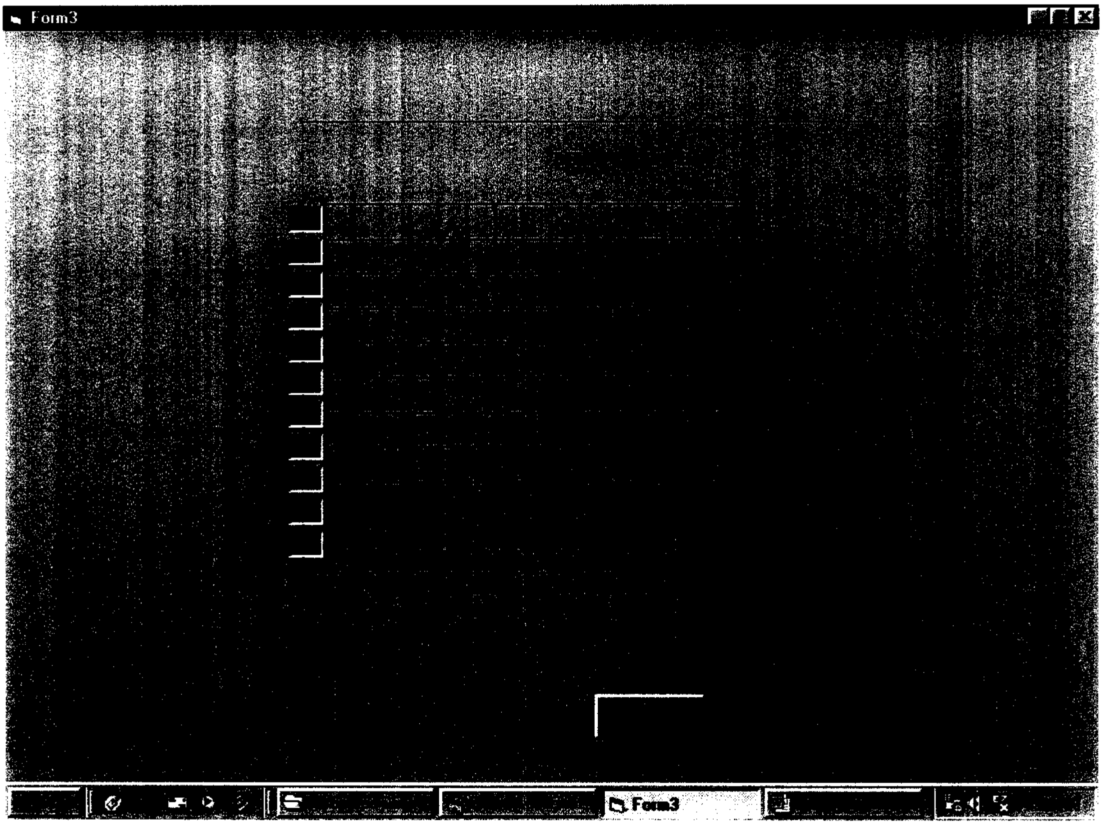
```
Dim i, j, k As Integer
Dim dat As String
Dim tes As String
Private Sub Command1_Click()
If i = 0 Then
Command4.Visible = True
i = 1
Else
Command4.Visible = False
i = 0
End If
End Sub

Private Sub Command2_Click()
If j = 0 Then
Command5.Visible = True
j = 1
Else
Command5.Visible = False
j = 0
End If
End Sub

Private Sub Command3_Click()
If k = 0 Then
Command6.Visible = True
k = 1
Else
Command6.Visible = False
k = 0
End If
End Sub

Private Sub Command4_Click()
Form2.Show
End Sub

Private Sub Command7_Click()
```

```
Private Sub Form_Load()
MSComm1.CommPort = 1
MSComm1.Settings = "110,N,8,1"
MSComm1.PortOpen = True
End Sub

Private Sub Text1_Change()
  If ((Mid$(Text1.Text, 1, 1)) = "Z" Or (Mid$(Text1.Text, 1, 1)) = "X")
Then
    If (Len(Form1.Text1.Text) >= 58) Then
      dat = Text1.Text
      Text1.Text = ""
      Form2.Text1.Text = Mid$(dat, 1, 1)
      Form2.Label2.Caption = Mid$(dat, 3, 3)
      Form2.Label4.Caption = Mid$(dat, 7, 3)
      Form2.Label6.Caption = Mid$(dat, 11, 3)
      Form2.Label8.Caption = Mid$(dat, 15, 4)
      Form2.Label10.Caption = Mid$(dat, 20, 4)
      Form2.Label12.Caption = Mid$(dat, 25, 4)
      Form2.Label14.Caption = Mid$(dat, 30, 4)
      Form2.Label16.Caption = Mid$(dat, 30, 4)
      Form2.Label18.Caption = Mid$(dat, 30, 4)
      Form2.Label20.Caption = Mid$(dat, 43, 6)
      Form2.Label22.Caption = Mid$(dat, 50, 6)
      tes = Form2.Label22.Caption
    End If
  Else
     Text1.Text = ""
End Sub
Private Sub Timer1_Timer()
Form1.Text1.Text = Form1.Text1.Text + MSComm1.Input
End Sub

Private Sub Timer1_Timer()
If Text1.Text = "X" Then
Open CommonDialog1.FileName For Append As #1
Print #1, "DEMAND=" & Form2.Label22.Caption
Print #1, "DATE=" & Date
Print #1, "TIME=" & Time
Print #1, "--------------------------------------"
Close #1
```

VB DISPLAY

FRONT PANEL: VB DISPLAY 1

DISPLAY OF VOLTAGE, CURRENT AND NECESSARY PARAMETERS



FRONT PANEL: VB DISPLAY 2

GRAPH FOR DEMAND Vs TIME.

APPENDIX 2

National Semiconductor

May 2000

LM78XX
Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expanded to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

Features

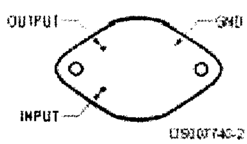
- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

Voltage Range

LM7805C	5V
LM7812C	12V
LM7815C	15V

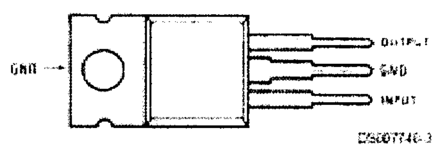
Connection Diagrams

Metal Can Package
TO-3 (K)
Aluminum



Bottom View
Order Number LM7805CK,
LM7812CK or LM7815CK
See NS Package Number KC02A

Plastic Package
TO-220 (T)



Top View
Order Number LM7805CT,
LM7812CT or LM7815CT
See NS Package Number T03B

MOTOROLA

LM2931 Series

LOW DROPOUT VOLTAGE REGULATORS

Low Dropout Voltage Regulators

The LM2931 series consists of positive fixed and adjustable output voltage regulators that are specifically designed to maintain proper regulation with an extremely low input–to–output voltage differential. These devices are capable of supplying output currents in excess of 100 mA and feature a low bias current of 0.4 mA at 10 mA output.

Designed primarily to survive in the harsh automotive environment, these devices will protect all external load circuitry from input fault conditions caused by reverse battery connection, two battery jump starts, and excessive line transients during load dump. This series also includes internal current limiting, thermal shutdown, and additionally, is able to withstand temporary power–up with mirror–image insertion.

Due to the low dropout voltage and bias current specifications, the LM2931 series is ideally suited for battery powered industrial and consumer equipment where an extension of useful battery life is desirable. The 'C' suffix adjustable output regulators feature an output inhibit pin which is extremely useful in microprocessor–based systems.

- Input–to–Output Voltage Differential of < 0.6 V @ 100 mA
- Output Current in Excess of 100 mA
- Low Bias Current
- 60 V Load Dump Protection
- –50 V Reverse Transient Protection
- Internal Current Limiting with Thermal Shutdown
- Temporary Mirror–Image Protection
- Ideally Suited for Battery Powered Equipment
- Economical 5–Lead TO–220 Package with Two Optional Leadforms
- Available in Surface Mount SOP–8, D^2PAK and DPAK Packages

(See Following Page for Ordering Information.)

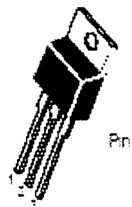
FIXED OUTPUT VOLTAGE

Z SUFFIX
PLASTIC PACKAGE
CASE 29

Pin 1. Output
2. Ground
3. Input

T SUFFIX
PLASTIC PACKAGE
CASE 221A

Heatsink surface connected to Pin 2.



Pin 1. Input
2. Ground
3. Output

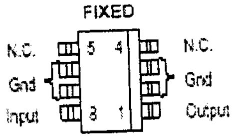
DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)

DT–1 SUFFIX
PLASTIC PACKAGE
CASE 369
(DPAK)

D2T SUFFIX
PLASTIC PACKAGE
CASE 936
(D^2PAK)

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

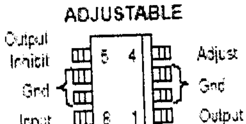
FIXED



(Top View)

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)

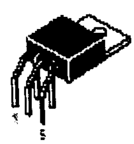
ADJUSTABLE



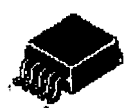
ADJUSTABLE OUTPUT VOLTAGE

Pin 1. Adjust
2. Output Inhibit
3. Ground
4. Input
5. Output

TH SUFFIX
PLASTIC PACKAGE
CASE 314A

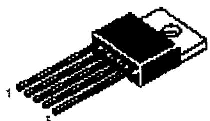


TV SUFFIX
PLASTIC PACKAGE
CASE 314B



D2T SUFFIX
PLASTIC PACKAGE
CASE 936A
(D^2PAK)

T SUFFIX
PLASTC PACKAGE
CASE 314D



Healsink surface (shown as

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, V_O = 3.0 V, I_O = 10 mA, R_1 = 27 k, C_O = 100 μF, $C_{O(ESR)}$ = 0.3 Ω, T_J = 25°C [Note 4].)

Characteristic	Symbol	LM2931C			Unit
		Min	Typ	Max	
ADJUSTABLE OUTPUT					
Reference Voltage (Note 5, Figure 18) I_O = 10 mA, T_J = 25°C I_O ≤ 100 mA, T_J = −40 to +125°C	V_{ref}	 1.14 1.08	 1.20 –	 1.26 1.32	V
Output Voltage Range	V_O range	3.0 to 24	2.7 to 29.5	–	V
Line Regulation (V_{in} = V_O + 0.6 V to 26 V)	Regline	–	0.2	1.5	mV/V
Load Regulation (I_O = 5.0 mA to 100 mA)	Regload	–	0.3	1.0	%/V
Output Impedance I_O = 10 mA, ΔI_O = 1.0 mA, f = 10 Hz to 10 kHz	Z_O	–	40	–	mΩ/V
Bias Current I_O = 100 mA I_O = 10 mA Output Inhibited ($V_{th(OI)}$ = 2.5 V)	I_B	 – – –	 6.0 0.4 0.2	 – 1.0 1.0	mA
Adjustment Pin Current	I_{Adj}	–	0.2	–	μA
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	–	140	–	μVrms/V
Long–Term Stability	S	–	0.4	–	%/kHR
Ripple Rejection (f = 120 Hz)	RR	0.10	0.003	–	%/V
Dropout Voltage I_O = 10 mA I_O = 100 mA	V_I–V_O	 – –	 0.015 0.16	 0.2 0.6	V
Over–Voltage Shutdown Threshold	$V_{th(OV)}$	26	29.5	40	V
Output Voltage with Reverse Polarity Input (V_{in} = −15 V)	$-V_O$	−0.3	0	–	V
Output Inhibit Threshold Voltages Output "On": T_J = 25°C T_J = −40° to +125°C Output "Off": T_J = 25°C T_J = −40° to +125°C	$V_{th(OI)}$	 – – 2.50 3.25	 2.15 – 2.26 –	 1.90 1.20 – –	V
Output Inhibit Threshold Current ($V_{th(OI)}$ = 2.5 V)	$I_{th(OI)}$	–	30	50	μA

NOTES: 4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
5. The reference voltage on the adjustable device is measured from the output to the adjust pin across R_1.

APPLICATIONS INFORMATION

The LM2931 series regulators are designed with many protection features making them essentially blow–out proof. These features include internal current limiting, thermal shutdown, overvoltage and reverse polarity input protection, and the capability to withstand temporary power–up with mirror–image insertion. Typical application circuits for the fixed and adjustable output device are shown in Figures 17 and 18.

The input bypass capacitor C_{in} is recommended if the regulator is located an appreciable distance (≥ 4″) from the supply input filter. This will reduce the circuit's sensitivity to the input line impedance at high frequencies.

This regulator series is not internally compensated and thus requires an external output capacitor for stability. The capacitance value required is dependent upon the load current, output voltage for the adjustable regulator, and the type of capacitor selected. The least stable condition is encountered at maximum load current and minimum output voltage. Figure 22 shows that for operation in the "Stable" region, under the conditions specified, the magnitude of the output capacitor impedance $|Z_O|$ must not exceed 0.4 Ω. This limit must be observed over the entire operating temperature range of the regulator circuit.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the electrolyte freezes, around −30°C, the capacitance will decrease and the equivalent series resistance (ESR) will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of −40° to +85°C and −55° to +105°C are readily available. Solid tantalum capacitors may be a better choice if small size is a requirement, however, the maximum $|Z_O|$ limit over temperature must be observed.

Note that in the stable region, the output noise voltage is linearly proportional to $|Z_O|$. In effect, C_O dictates the high frequency roll–off point of the circuit. Operation in the area titled "Marginally Stable" will cause the output of the regulator to exhibit random bursts of oscillation that decay in an under–damped fashion. Continuous oscillation occurs when operating in the area titled "Unstable". It is suggested that oven testing of the entire circuit be performed with maximum load, minimum input voltage, and minimum ambient temperature.

Internally Compensated, High Performance Dual Operational Amplifiers

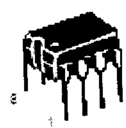
MC1458, C

The MC1458, C was designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short Circuit Protection
- Wide Common Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch–Up

DUAL OPERATIONAL AMPLIFIERS
(DUAL MC1741)

SEMICONDUCTOR TECHNICAL DATA



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

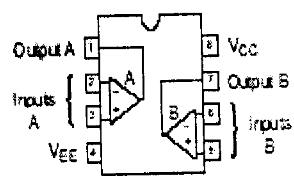
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 –18	Vdc
Input Differential Voltage	V_{ID}	±30	V
Input Common Mode Voltage (Note 1)	V_{ICM}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Junction Temperature	T_J	150	°C

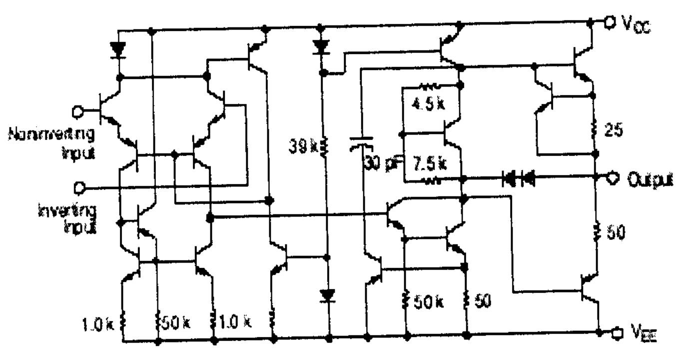
NOTES: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Supply voltage equal to or less than 15 V.

PIN CONNECTIONS



(Top View)

Representative Schematic Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1458CD, D	T_A = 0° to +70°C	SO–8
MC1458CP1, P1		Plastic DIP

Publication Order Number:

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted. (Note 3))

Characteristic	Symbol	MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤ 10 k)	V_{IO}	–	2.0	6.0	–	2.0	10	mV
Input Offset Current	I_{IO}	–	20	200	–	20	300	nA
Input Bias Current	I_{IB}	–	80	500	–	80	700	nA
Input Resistance	r_i	0.3	2.0	–	–	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±11	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k) (V_O = ±10 V, R_L = 10 k)	A_{VOL}	 20 –	 200 –	 – –	 – 20	 – 200	 – –	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection (R_S ≤ 10 k)	CMR	70	90	–	60	90	–	dB
Supply Voltage Rejection (R_S ≤ 10 k)	PSR	–	30	150	–	30	–	µV/V
Output Voltage Swing (R_S ≤ 10 k) (R_S ≤ 2.0 k)	V_O	 ±12 ±10	 ±14 ±13	 – –	 ±11 ±9.0	 ±14 ±13	 – –	V
Output Short Circuit Current	I_{SC}	–	20	–	–	20	–	mA
Supply Currents (Both Amplifiers)	I_D	–	2.3	5.6	–	2.3	8.0	mA
Power Consumption	P_C	–	70	170	–	70	240	mW
Transient Response (Unity Gain) (V_I = 20 mV, R_L ≥ 2.0 kΩ, C_L ≤ 100 pF) Rise Time (V_I = 20 mV, R_L ≥ 2.0 kΩ, C_L ≤ 100 pF) Overshoot (V_I = 10 V, R_L ≥ 2.0 kΩ, C_L ≤ 100 pF) Slew Rate	 t_{TLH} os SR	 – – –	 0.3 15 0.5	 – – –	 – – –	 0.3 15 0.5	 – – –	 µs % V/µs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{high} to T_{low} unless otherwise noted. (Note 3))*

Characteristic	Symbol	MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	–	–	7.5	–	–	12	mV
Input Offset Current (T_A = 0° to +70°C)	I_{IO}	–	–	300	–	–	400	nA
Input Bias Current (T_A = 0° to +70°C)	I_{IB}	–	–	800	–	–	1000	nA
Output Voltage Swing (R_S ≤ 10 k) (R_S ≤ 2 k)	V_O	 ±12 ±10	 ±14 ±13	 – –	 – ±9.0	 – ±13	 – –	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2 k) (V_O = ±10 V, R_L = 10 k)	A_{VOL}	 15 –	 – –	 – –	 – 15	 – –	 – –	V/mV

*T_{low} = 0°C for MC1458, C T_{high} = +70°C for MC1458, C

NOTE: 3. Input pins of an unused amplifier must be grounded for split supply operation or biased at least 3.0 V above V_{EE} for single supply operation.

MICROCHIP

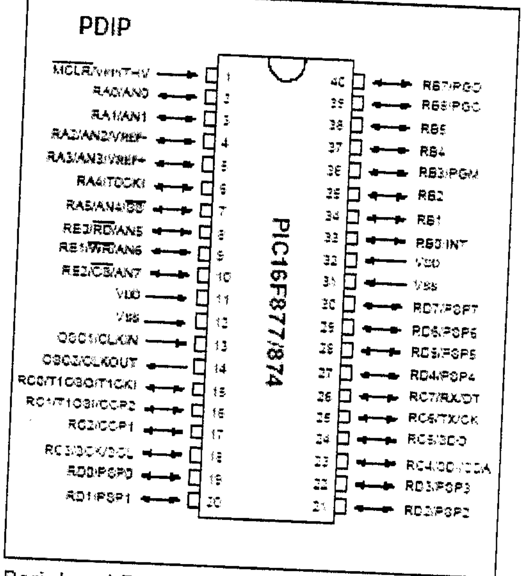
PIC16F87X

28/40-pin 8-Bit CMOS EEPROM/Flash Microcontrollers

Microcontroller Core Features:

- High-performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory,
  Up to 368 x 8 bytes of Data Memory (RAM)
  Up to 256 x 8 bytes of EEPROM data memory
- ★ **Pinout compatible to the PIC16C73/74/76/77**
- Interrupt capability (up to 14 internal/external interrupt sources)
- Eight level deep hardware stack
- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS EPROM/EEPROM technology
- Fully static design
- In-Circuit Serial Programming™ via two pins
- ★ Only single 5V source needed for programming
- ★ In-Circuit Debugging via two pins
- Processor read/write access to program memory
- Wide operating voltage range: 2.5V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial and Industrial temperature ranges
- Low-power consumption:
  - < 2 mA typical @ 5V, 4 MHz
  - 20 µA typical @ 3V, 32 kHz
  - < 1 µA typical standby current

Pin Diagram

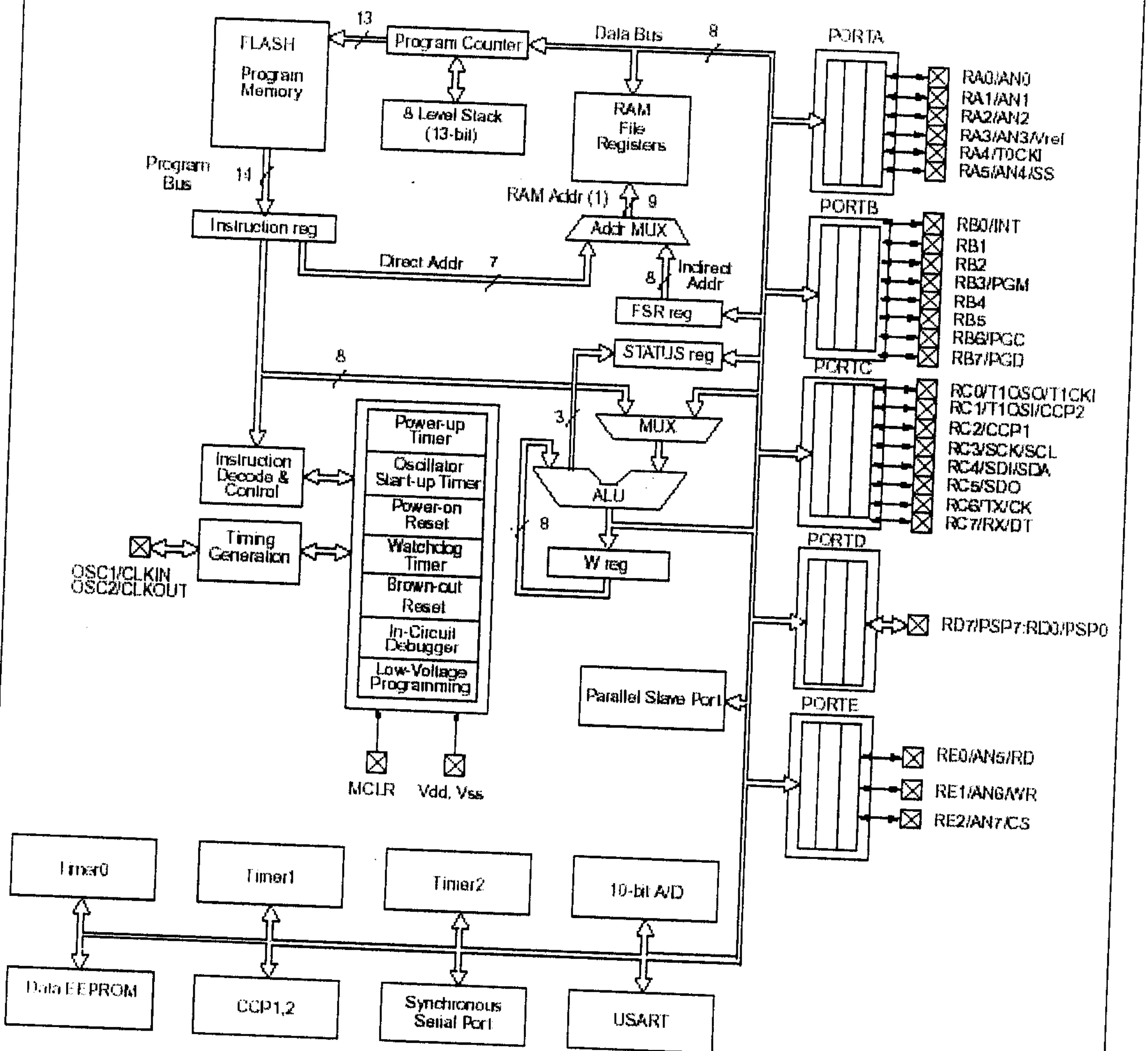


Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
- Capture is 16-bit, max. resolution is 12.5 ns, Compare is 16-bit, max. resolution is 200 ns, PWM max. resolution is 10-bit
- ★ 10-bit multi-channel Analog-to-Digital converter
- ★ Synchronous Serial Port (SSP) with SPI™ (Master Mode) and I²C™ (Master/Slave)
- ★ Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) 8-bits wide, with external $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

PIC16F877 BLOCK DIAGRAM

Device	Program Flash	Data Memory	Data EEPROM
PIC16F874	4K	192 Bytes	128 Bytes
PIC16F877	8K	368 Bytes	256 Bytes



Note 1: Higher order bits are from the STATUS register.

PIC16F877/876 REGISTER FILE MAP

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h		107h		187h
PORTD (1)	08h	TRISD (1)	88h		108h		188h
PORTE (1)	09h	TRISE (1)	89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved(2)	18Eh
TMR1H	0Fh		8Fh	EEADRH	10Fh	Reserved(2)	18Fh
T1CON	10h		90h	General Purpose Register 16 Bytes	110h	General Purpose Register 16 Bytes	190h
TMR2	11h	SSPCON2	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h		95h		115h		195h
CCPR1H	16h		96h		116h		196h
CCP1CON	17h		97h		117h		197h
RCSTA	18h	TXSTA	98h		118h		198h
TXREG	19h	SPBRG	99h		119h		199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh		19Bh
CCPR2H	1Ch		9Ch		11Ch		19Ch
CCP2CON	1Dh		9Dh		11Dh		19Dh
ADRESH	1Eh	ADRESL	9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h–7Fh	General Purpose Register 80 Bytes	A0h–EFh	General Purpose Register 80 Bytes	120h–16Fh	General Purpose Register 80 Bytes	1A0h–1EFh
		accesses 70h-7Fh	F0h–FFh	accesses 70h-7Fh	170h–17Fh	accesses 70h - 7Fh	1F0h–1FFh

Bank 0 | Bank 1 | Bank 2 | Bank 3

▒ Unimplemented data memory locations, read as '0'.

* Not a physical register.

Note 1: These registers are not implemented on 28-pin devices.

2: These registers are reserved, maintain these registers clear.

10.0 UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART)

The Universal Synchronous Asynchronous Receiver Transmitter (USART) module is one of the two serial I/O modules. (USART is also known as a Serial Communications Interface or SCI). The USART can be configured as a full duplex asynchronous system that can communicate with peripheral devices such as CRT terminals and personal computers, or it can be configured as a half duplex synchronous system that can communicate with peripheral devices such as A/D or D/A integrated circuits, Serial EEPROMs etc.

The USART can be configured in the following modes:

- Asynchronous (full duplex)
- Synchronous - Master (half duplex)
- Synchronous - Slave (half duplex)

Bit SPEN (RCSTA<7>), and bits TRISC<7:6>, have to be set in order to configure pins RC6/TX/CK and RC7/RX/DT as the Universal Synchronous Asynchronous Receiver Transmitter.

The USART module also has a multi-processor communication capability using 9-bit address detection.

FIGURE 10-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER (ADDRESS 98h)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7: **CSRC**: Clock Source Select bit
<u>Asynchronous mode</u>
Don't care
<u>Synchronous mode</u>
1 = Master mode (Clock generated internally from BRG)
0 = Slave mode (Clock from external source)

bit 6: **TX9**: 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5: **TXEN**: Transmit Enable bit
1 = Transmit enabled
0 = Transmit disabled
Note: SREN/CREN overrides TXEN in SYNC mode.

bit 4: **SYNC**: USART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3: **Unimplemented**: Read as '0'

bit 2: **BRGH**: High Baud Rate Select bit
<u>Asynchronous mode</u>
1 = High speed
0 = Low speed
<u>Synchronous mode</u>
Unused in this mode

bit 1: **TRMT**: Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0: **TX9D**: 9th bit of transmit data. Can be parity bit.

10.1 USART Baud Rate Generator (BRG)

The BRG supports both the Asynchronous and Synchronous modes of the USART. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. In asynchronous mode bit BRGH (TXSTA<2>) also controls the baud rate. In synchronous mode bit BRGH is ignored. Table 10-1 shows the formula for computation of the baud rate for different USART modes which only apply in master mode (internal clock).

Given the desired baud rate and Fosc, the nearest integer value for the SPBRG register can be calculated using the formula in Table 10-1. From this, the error in baud rate can be determined.

Example 10-1 shows the calculation of the baud rate error for the following conditions:

Fosc = 16 MHz
Desired Baud Rate = 9600
BRGH = 0
SYNC = 0

EXAMPLE 10-1: CALCULATING BAUD RATE ERROR

Desired Baud rate = Fosc / (64 (X + 1))

9600 = 16000000 /(64 (X + 1))

X = ⌊25.042⌋ = 25

Calculated Baud Rate = 16000000 / (64 (25 + 1))

= 9615

Error = (Calculated Baud Rate - Desired Baud Rate) / Desired Baud Rate

= (9615 - 9600) / 9600

= 0.16%

It may be advantageous to use the high baud rate (BRGH = 1) even for slower baud clocks. This is because the FOSC/(16(X + 1)) equation can reduce the baud rate error in some cases.

Writing a new value to the SPBRG register, causes the BRG timer to be reset (or cleared), this ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

10.1.1 SAMPLING

The data on the RC7/RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin.

TABLE 10-1 BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = FOSC/(64(X+1))	Baud Rate= FOSC/(16(X+1))
1	(Synchronous) Baud Rate = FOSC/(4(X+1))	NA

X = value in SPBRG (0 to 255)

TABLE 10-2 REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used by the BRG.

11.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The analog-to-digital (A/D) converter module has five inputs for the 28-pin devices, and eight for the other devices.

The analog input charges a sample and hold capacitor. The output of the sample and hold capacitor is the input into the converter. The converter then generates a digital result of this analog level via successive approximation. This A/D conversion, of the analog input signal, results in a corresponding 10-bit digital number.

The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in sleep, the A/D clock must be derived from the A/D's internal RC oscillator.

The A/D module has four registers. These registers are:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register0 (ADCON0)
- A/D Control Register1 (ADCON1)

The ADCON0 register, shown in Figure 11-1, controls the operation of the A/D module. The ADCON1 register, shown in Figure 11-2, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be the voltage reference) or as digital I/O.

FIGURE 11-1: ADCON0 REGISTER (ADDRESS: 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **ADCS1:ADCS0**: A/D Conversion Clock Select bits
00 = Fosc/2
01 = Fosc/8
10 = Fosc/32
11 = FRC (clock derived from an RC oscillation)

bit 5-3: **CHS2:CHS0**: Analog Channel Select bits
000 = channel 0, (RA0/AN0)
001 = channel 1, (RA1/AN1)
010 = channel 2, (RA2/AN2)
011 = channel 3, (RA3/AN3)
100 = channel 4, (RA5/AN4)
101 = channel 5, (RE0/AN5)(1)
110 = channel 6, (RE1/AN6)(1)
111 = channel 7, (RE2/AN7)(1)

bit 2: **GO/$\overline{\text{DONE}}$**: A/D Conversion Status bit
If ADON = 1
1 = A/D conversion in progress (setting this bit starts the A/D conversion)
0 = A/D conversion not in progress (This bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1: **Unimplemented**: Read as '0'

bit 0: **ADON**: A/D On bit
1 = A/D converter module is operating
0 = A/D converter module is shutoff and consumes no operating current

Note 1: These channels are not available on the 28-pin devices.

TABLE 13-2 PIC16CXXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status Affected	Notes
				MSb			LSb		
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

EXAR ...the analog plus company™

XR-2206

Monolithic Function Generator

June 1997-3

FEATURES

- Low-Sine Wave Distortion, 0.5%, Typical
- Excellent Temperature Stability, 20ppm/°C, Typ.
- Wide Sweep Range, 2000:1, Typical
- Low-Supply Sensitivity, 0.01%V, Typ.
- Linear Amplitude Modulation
- TTL Compatible FSK Controls
- Wide Supply Range, 10V to 26V
- Adjustable Duty Cycle, 1% TO 99%

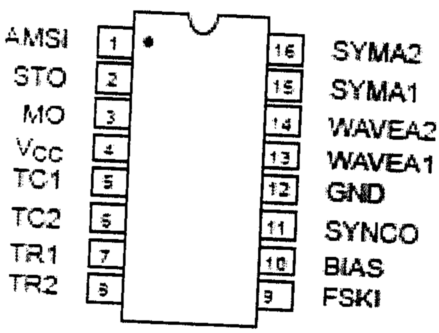
APPLICATIONS

- Waveform Generation
- Sweep Generation
- AM/FM Generation
- V/F Conversion
- FSK Generation
- Phase-Locked Loops (VCO)

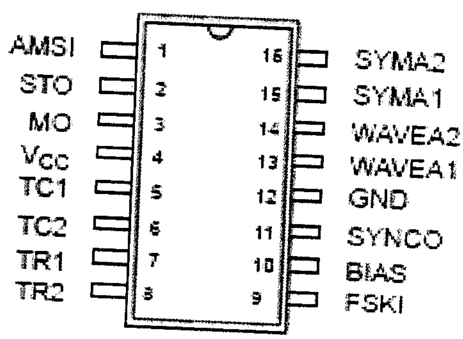
GENERAL DESCRIPTION

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01Hz to more than 1MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage, while maintaining low distortion.



16 Lead PDIP, CDIP (0.300")



16 Lead SOIC (Jedec, 0.300")

DC ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of *Figure 2* Vcc = 12V, T_A = 25°C, C = 0.01µF, R_1 = 100kΩ, R_2 = 10kΩ, R_3 = 25kΩ Unless Otherwise Specified. S_1 open for triangle, closed for sine wave.

Parameters	XR-2206M/P Min.	XR-2206M/P Typ.	XR-2206M/P Max.	XR-2206CP/D Min.	XR-2206CP/D Typ.	XR-2206CP/D Max.	Units	Conditions
General Characteristics								
Single Supply Voltage	10		26	10		26	V	
Split-Supply Voltage	±5		±13	±5		±13	V	
Supply Current		12	17		14	20	mA	$R_1 \geq$ 10kΩ
Oscillator Section								
Max. Operating Frequency	0.5	1		0.5	1		MHz	C = 1000pF, R_1 = 1kΩ
Lowest Practical Frequency		0.01			0.01		Hz	C = 50µF, R_1 = 2MΩ
Frequency Accuracy		±1	±4		±2		% of f_o	$f_o = 1/R_1C$
Temperature Stability Frequency		±10	±50		±20		ppm/°C	0°C ≤ T_A ≤ 70°C $R_1 = R_2$ = 20kΩ
Sine Wave Amplitude Stability[2]		4800			4800		ppm/°C	
Supply Sensitivity		0.01	0.1		0.01		%/V	V_{LOW} = 10V, V_{HIGH} = 20V, $R_1 = R_2$ = 20kΩ
Sweep Range	1000:1	2000:1			2000:1		$f_H = f_L$	f_H @ R_1 = 1kΩ f_L @ R_1 = 2MΩ
Sweep Linearity								
10:1 Sweep		2			2		%	f_L = 1kHz, f_H = 10kHz
1000:1 Sweep		8			8		%	f_L = 100Hz, f_H = 100kHz
FM Distortion		0.1			0.1		%	±10% Deviation
Recommended Timing Components								
Timing Capacitor: C	0.001		100	0.001		100	µF	*Figure 5*
Timing Resistors: R_1 & R_2	1		2000	1		2000	kΩ	
Triangle Sine Wave Output[1]								*Figure 3*
Triangle Amplitude		160			160		mV/kΩ	*Figure 2*, S_1 Open
Sine Wave Amplitude	40	60	80		60		mV/kΩ	*Figure 2*, S_1 Closed
Max. Output Swing		6			6		Vp-p	
Output Impedance		600			600		Ω	
Triangle Linearity		1			1		%	
Amplitude Stability		0.5			0.5		dB	For 1000:1 Sweep
Sine Wave Distortion								
Without Adjustment		2.5			2.5		%	R_1 = 30kΩ
With Adjustment		0.4	1.0		0.5	1.5	%	See *Figure 7* and *Figure 8*

DC ELECTRICAL CHARACTERISTICS (CONT'D)

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
Amplitude Modulation								
Input Impedance	50	100		50	100		kΩ	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
Square-Wave Output								
Amplitude		12			12		Vp-p	Measured at Pin 11.
Rise Time		250			250		ns	C_L = 10pF
Fall Time		50			50		ns	C_L = 10pF
Saturation Voltage		0.2	0.4		0.2	0.6	V	I_L = 2mA
Leakage Current		0.1	20		0.1	100	µA	V_{CC} = 26V
FSK Keying Level (Pin 9)	0.8	1.4	2.4	0.8	1.4	2.4	V	See section on circuit controls
Reference Bypass Voltage	2.9	3.1	3.3	2.5	3	3.5	V	Measured at Pin 10.

PRINCIPLES OF OPERATION

Description of Controls

Frequency of Operation:

The frequency of oscillation, f_o, is determined by the external timing capacitor, C, across Pin 5 and 6, and by the timing resistor, R, connected to either Pin 7 or 8. The frequency is given as:

$$f_o = \frac{1}{RC}\ Hz$$

and can be adjusted by varying either R or C. The recommended values of R, for a given frequency range, as shown in *Figure 5*. Temperature stability is optimum for 4kΩ < R < 200kΩ. Recommended values of C are from 1000pF to 100µF.

Frequency-Shift Keying

The XR-2206 can be operated with two separate timing resistors, R_1 and R_2, connected to the timing Pin 7 and 8, respectively, as shown in *Figure 13*. Depending on the polarity of the logic signal at Pin 9, either one or the other of these timing resistors is activated. If Pin 9 is open-circuited or connected to a bias voltage ≥ 2V, only R_1 is activated. Similarly, if the voltage level at Pin 9 is ≤1V, only R_2 is activated. Thus, the output frequency can be keyed between two levels, f_1 and f_2, as:

$f_1 = 1/R_1C$ and $f_2 = 1/R_2C$

For split-supply operation, the keying voltage at Pin 9 is referenced to V-.

National Semiconductor

May 1999

LM565/LM565C Phase Locked Loop

General Description

The LM565 and LM565C are general purpose phase locked loops containing a stable, highly linear voltage controlled oscillator for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system — bandwidth, response speed, capture and pull in range — may be adjusted over a wide range with an external resistor and capacitor. The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.

The LM565H is specified for operation over the −55°C to +125°C military temperature range. The LM565CN is specified for operation over the 0°C to +70°C temperature range.

Features

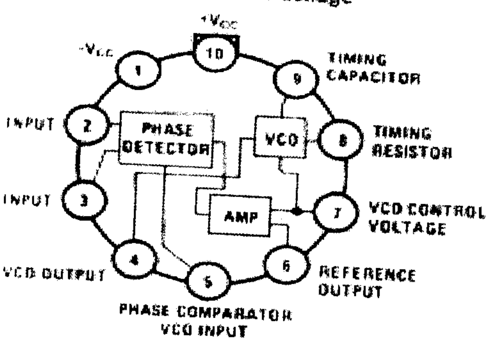
- 200 ppm/°C frequency stability of the VCO
- Power supply range of ±5 to ±12 volts with 100 ppm/% typical
- 0.2% linearity of demodulated output
- Linear triangle wave with in phase zero crossings available
- TTL and DTL compatible phase detector input and square wave output
- Adjustable hold in range from ±1% to > ±60%

Applications

- Data and tape synchronization
- Modems
- FSK demodulation
- FM demodulation
- Frequency synthesizer
- Tone decoding
- Frequency multiplication and division
- SCA demodulators
- Telemetry receivers
- Signal regeneration
- Coherent demodulators

Connection Diagrams

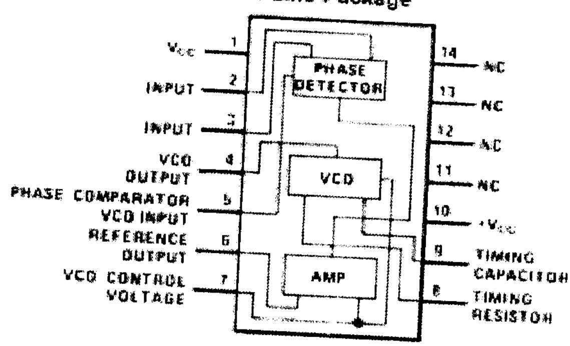
Metal Can Package



DS007853-2

Order Number LM565H
See NS Package Number H10C

Dual-In-Line Package



DS007853-3

Order Number LM565CN
See NS Package Number N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±12V
Power Dissipation (Note 2)	1400 mW
Differential Input Voltage	±1V
Operating Temperature Range	
LM565H	−55°C to +125°C
LM565CN	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

AC Test Circuit, T_A = 25°C, V_{CC} = ±6V

Parameter	Conditions	LM565 Min	LM565 Typ	LM565 Max	LM565C Min	LM565C Typ	LM565C Max	Units
Power Supply Current			8.0	12.5		8.0	12.5	mA
Input Impedance (Pins 2, 3)	−4V < V_2, V_3 < 0V	7	10			5		kΩ
VCO Maximum Operating Frequency	C_o = 2.7 pF	300	500		250	500		kHz
VCO Free-Running Frequency	C_o = 1.5 nF R_o = 20 kΩ f_o = 10 kHz	−10	0	+10	−30	0	+30	%
Operating Frequency Temperature Coefficient			−100			−200		ppm/°C
Frequency Drift with Supply Voltage			0.1	1.0		0.2	1.5	%/V
Triangle Wave Output Voltage		2	2.4	3	2	2.4	3	V_{p-p}
Triangle Wave Output Linearity			0.2			0.5		%
Square Wave Output Level		4.7	5.4		4.7	5.4		V_{p-p}
Output Impedance (Pin 4)			5			5		kΩ
Square Wave Duty Cycle		45	50	55	40	50	60	%
Square Wave Rise Time			20			20		ns
Square Wave Fall Time			50			50		ns
Output Current Sink (Pin 4)		0.6	1		0.6	1		mA
VCO Sensitivity	f_o = 10 kHz		6600			6600		Hz/V
Demodulated Output Voltage (Pin 7)	±10% Frequency Deviation	250	300	400	200	300	450	mV_{p-p}
Total Harmonic Distortion	±10% Frequency Deviation		0.2	0.75		0.2	1.5	%
Output Impedance (Pin 7)			3.5			3.5		kΩ
DC Level (Pin 7)		4.25	4.5	4.75	4.0	4.5	5.0	V
Output Offset Voltage $\|V_7 - V_6\|$			30	100		50	200	mV
Temperature Drift of $\|V_7 - V_6\|$			500			500		µV/°C
AM Rejection		30	40			40		dB
Phase Detector Sensitivity K_D			0.68			0.68		V/radian

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given. However, the typical value is a good indication of device performance.

Note 2: The maximum junction temperature of the LM565 and LM565C is +150°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W junction to ambient or +45°C/W junction to case. Thermal resistance of the dual-in-line package is +65°C/W.

Applications Information

In designing with phase locked loops such as the LM565, the important parameters of interest are:

FREE RUNNING FREQUENCY

$$f_o \cong \frac{0.3}{R_o C_o}$$

LOOP GAIN: relates the amount of phase change between the input signal and the VCO signal for a shift in input signal frequency (assuming the loop remains in lock). In servo theory, this is called the "velocity error coefficient."

$$\text{Loop gain} = K_o K_D \left(\frac{1}{\text{sec}}\right)$$

$$K_o = \text{oscillator sensitivity} \left(\frac{\text{radians/sec}}{\text{volt}}\right)$$

$$K_D = \text{phase detector sensitivity} \left(\frac{\text{volts}}{\text{radian}}\right)$$

The loop gain of the LM565 is dependent on supply voltage, and may be found from:

$$K_o K_D = \frac{33.6\, f_o}{V_c}$$

f_o = VCO frequency in Hz

V_c = total supply voltage to circuit

Loop gain may be reduced by connecting a resistor between pins 6 and 7; this reduces the load impedance on the output amplifier and hence the loop gain.

HOLD IN RANGE: the range of frequencies that the loop will remain in lock after initially being locked.

$$f_H = \pm \frac{8\, f_o}{V_c}$$

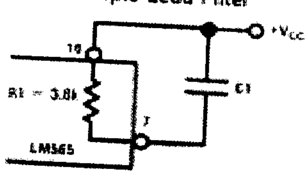
f_o= free running frequency of VCO

V_c= total supply voltage to the circuit

THE LOOP FILTER

In almost all applications, it will be desirable to filter the signal at the output of the phase detector (pin 7); this filter may take one of two forms:

Simple Lead Filter



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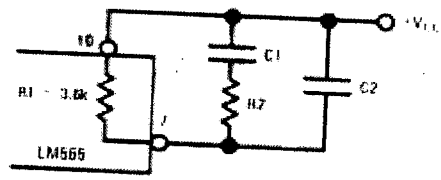
Lag-Lead Filter



DS007853-12

A simple lag filter may be used for wide closed loop bandwidth applications such as modulation following where the frequency deviation of the carrier is fairly high (greater than 10%), or where wideband modulating signals must be followed.

The natural bandwidth of the closed loop response may be found from:

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_o K_D}{R_1 C_1}}$$

Associated with this is a damping factor:

$$\delta = \frac{1}{2}\sqrt{\frac{1}{R_1 C_1 K_o K_D}}$$

For narrow band applications where a narrow noise bandwidth is desired, such as applications involving tracking a slowly varying carrier, a lead lag filter should be used. In general, if $1/R_1C_1 < K_o K_D$, the damping factor for the loop becomes quite small resulting in large overshoot and possible instability in the transient response of the loop. In this case, the natural frequency of the loop may be found from

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_o K_D}{\tau_1 + \tau_2}}$$

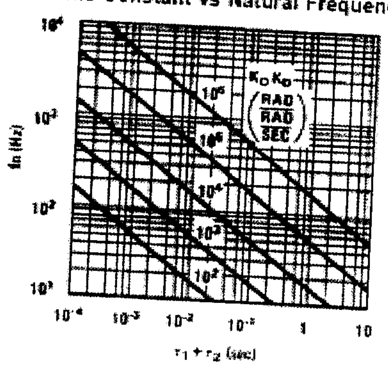
$$\tau_1 + \tau_2 = (R_1 + R_2)\, C_1$$

R_2 is selected to produce a desired damping factor δ, usually between 0.5 and 1.0. The damping factor is found from the approximation:

$$\delta \approx \pi\, \tau_2 f_n$$

These two equations are plotted for convenience.

Filter Time Constant vs Natural Frequency



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APPENDIX 3

LISTS OF IC

IC NUMBER	IC NAME
IC1	IC 7805
IC2	LM2931AZ-5.0
IC3	PICI6F877
IC4	MAX232
IC5	XOR GATE
IC6	XR2206
IC7	NE565