ENERGY EFFICIENT CONTROL OF LOW RPM DRIVE

(APPLICATION-GRINDER)

A PROJECT REPORT

Submitted by

APARNA.S	**71201105002**
DIVYA .J	**71201105012**
SATHYA.K.U	**71201105050**
SUBATRA.G	**71201105057**

In partial fulfillment for the award of degree

of

BACHELOR OF ENGINEERING

IN

ELECTRICAL AND ELECTRONICS ENGINEERING

Under the guidance of

Dr.T.M.Kameswaran

KUMARAGURU COLLEGE OF TECHNOLOGY::COIMBATORE

ANNA UNIVERSITY::CHENNAI 600025

APRIL-2005

ANNA UNIVERSITY::CHENNAI 600025

BONAFIDE CERTIFICATE

ertified that this project report "**ENERGY EFFICIENT CONTROL OF THE
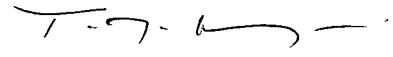.OW RPM DRIVE** "(APPLICATION-GRINDER) is a bonafide work of

APARNA.S	**71201105002**
DIVYA.J	**71201105012**
SATHYA.K.U	**71201105050**
SUBATRA.G	**71201105057**

who carried out the project work under my supervision.

(SIGNATURE)   (SIGNATURE)

HEAD OF DEPARTMENT   **GUIDE**
Dr.K.Regupathy Subramanian   **Dr.T.M.Kameswaran**
Dept. of EEE (DEAN R&D)   **DEAN**
Kumaraguru College of   Kumaraguru College of
Technology,   Technology,
Coimbatore-6   Coimbatore-6.

CERTIFICATE OF EVALUATION

College   : KUMARAGURU COLLEGE OF TECHNOLOGY

Branch   : Electrical & Electronics Engineering

Semester   : Eighth Semester

Sl. No.	Name of the Students	Title of the Project	Name of the Supervisor with Designation
01	Aparna.S	**Energy efficient control of low rpm drive**	Dr.T.M.Kameswaran Dean.
02	Divya.J		
03	Sathya.K.U		
04	Subatra.G		

The report of the project work submitted by the above students in partial fulfillment for the award of Bachelor of Engineering degree in Electrical & Electronics Engineering of Anna University was evaluated and confirmed to be report of the work done by the above students.
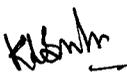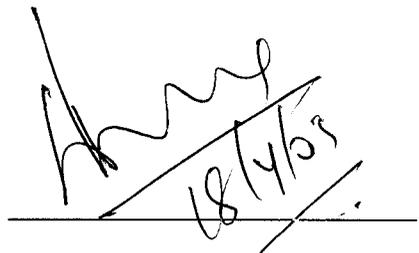
Certificate

TO WHOM SO EVER IT MAY CONCERN

This is to certify that the following students

APARNA.S	01EEE02
DIVYA.J	01EEE12
SATHYA.K.U	01EEE44
SUBATRA.G	01EEE49

of Electrical and Electronics Engineering Department of Kumaraguru College of Technology have done their project work and testing in our industry. Their conduct during that period was good.

For AARVEE INDUSTRIES.

A. Jayanthi
Partner

(JEYANTHI.A)
Managing Director

IS : 8472   IS : 12225   IS : 9079-89

ACKNOWLEDGEMENT

ACKNOWLEDGEMENT

CONTENTS

TABLE OF CONTENTS

ABSTRACT

ABSTRACT

Electronics circuitry is slowly replacing the conventional mechanical components in almost every application ranging from domestic to industrial, thereby avoiding wear and tear and the maintenance problems. This project also has a similar objective.

The application considered here is the domestic grinder used in every household. For the grinders the operating speed required is very low (around 200 rpm) for which a direct low rpm motor does not exist. In the existing grinders the speed reduction is obtained by means of a belt or a gear mechanism which have their own limitations.

This project aims at replacing the conventional speed reduction technique by the power electronic circuitry. This technique enables to establish direct coupling between the motor and drum thereby reducing the transmission losses incurred in the conventional technique.

Intensive research work is being carried out in the grinder industry to find out innovative techniques to provide direct coupling between the motor and the drum.

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

is the rating of the machine in Kilo Volt Ampere (KVA)

is the No of phases

$_{ph}$ is the o/p voltage per phase in volts (V)

$_h$ is the current per phase in Ampere (A)

is the number of poles.

frequency in Hertz (Hz)

$_s$ (Rpm) synchronous speed of the motor in revolutions per minute

is the flux in Weber

$_{ph}$ is the number of turns per phase.

$_w$ is the winding factor

is the efficiency of the machine

Cos φ is the power factor

$_{av}$ is the magnetic loading in Tesla

$_c$ is the electric loading in Ampere/metre

is the diameter of the rotor in metre.

is the core length of the stator & rotor in metre.

$_s$ (Rps) revolutions per second

is the torque in Newton meter (Nm)

$_i$ is the input voltage in volts

$_o$ is the output voltage in volts

$_{ref}$ reference voltage in volts

$_{comp}$ compensating resistor

ND ground

orse power (hp) = 746 Kilowatt (Kw)

CHAPTER I

EXISTING SETUP

INTRODUCTION

The conventional wet grinders are designed in such a way that the high rpm produced by a single phase fractional horse power induction motor is stepped down to a low rpm using a belt mechanism or a gear mechanism. The low rpm is then fed to the rotating part by means of a shaft, which in turn is coupled to the drum arrangement.

The belt mechanism and the gear mechanism along with their disadvantages are explained below.

BELT MECHANISM

A common method of transmitting power from an electric motor to the driven unit is through the use of belts. Advantages of belt drives include minimal maintenance and lubrication requirements, smoothing of sudden shock loads, and quietness. In general, belting systems are less expensive than most other power transmission systems, and offer the flexibility to vary the speed of the driven load without altering the driver speed by simply replacing the sheave(s).

Belt drives are used to transmit power between a drive unit and a driven unit. For example, if we have an electric motor and a contact roll on a conveyor, we need a way to transmit the power from the electric motor to the roll. This can be done easily and efficiently with a belt drive unit. Belt drives can consist of one or multiple belts, depending on the load that the unit must transmit.

Belt drives for power transmissions are classified as frictional drives.
A. Belts transmit power by friction contact between the belt and the driving or driven sheaves.
B. Belts are available in various types like flat belts, V-belts, Synchronous belts, Multi-ribbed belts.

To obtain the best service for the belt

    1. Select the correct belt for the job

    2. Ensure the belt is installed properly, and used properly

Selection Considerations are-

    ➢ Environmental conditions,

    ➢ Type of drive required

    ➢ Driver/driven RPM

Belt mechanism
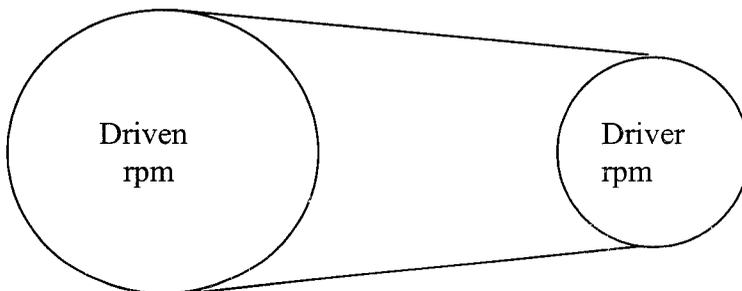
Figure 1.1

    ➢ Horsepower requirements

    ➢ Pulley diameters and center requirements

    ➢ Take up allowance and design

- ➢ Space limitations for operation
- ➢ Pulsating and shock load conditions
- ➢ Static dissipation requirements
- ➢ Belt availability and inventory considerations
- ➢ Belt construction and service life

The disadvantages of belt mechanism are:

- ➢ Belt mechanism involves transmission losses .Efficient coupling cannot be achieved.
- ➢ Belts cannot be used where exact timing and speed is required (except timing belts)
- ➢ Belts are easily damaged by oil, grease, abrasives, some chemicals, and heat
- ➢ Belts can be noisy, also loose or worn belts can be a major cause of machinery vibration
- ➢ Limitations on power throughput
- ➢ Inaccuracies in positioning due to slippage
- ➢ stretching of belt over time

GEAR MECHANISM

Since most machines that are driven by electric motors operate at speeds well below normal speed, some form of speed reducer is usually needed. Gears are extensively used for such purposes. The speed reducing gears may be built into the driven machine, or the gear unit may be made a part of the motor. Sometimes, the speed reducer is a separate unit.gearmotors, having the motor and the reducer built as an integral unit, are frequently used both for economy and for saving space but they have the following disadvantages.

1)   Most gear reducers are irreversible, i.e., the motor cannot be turned from the slow speed shaft, because the momentum of the load during stopping or starting may damage the gears.

2)   Many of these motors, particularly double reduction universal motors, can deliver more torque than the gears can handle continuously.

3)   Care should, be exercised to avoid applying these motors to devices that can become jammed-lest the gears be jammed.

4)   Frequent lubrication is required.

5)   Noisy in operation.

CHAPTER II

PRESENT DESIGN

INTRODUCTION

Our project comprises of efficient control of the low rpm drive, which will replace the belt or the gear set up. This principle when employed in applications requiring low rpm the losses due to gear and belt are avoided. This makes the grinder (or any other application involving speed reduction) design simple and in turn the structure as a whole becomes compact. Efficient control can be obtained for a speed of about 200 to 250 rpm. By using this design efficient coupling can be accomplished..

WORKING

The overall design can be split into two parts-

> ➤ The frequency reduction circuit.
> ➤ Fabrication of a motor suitable for the application

Frequency reduction circuit
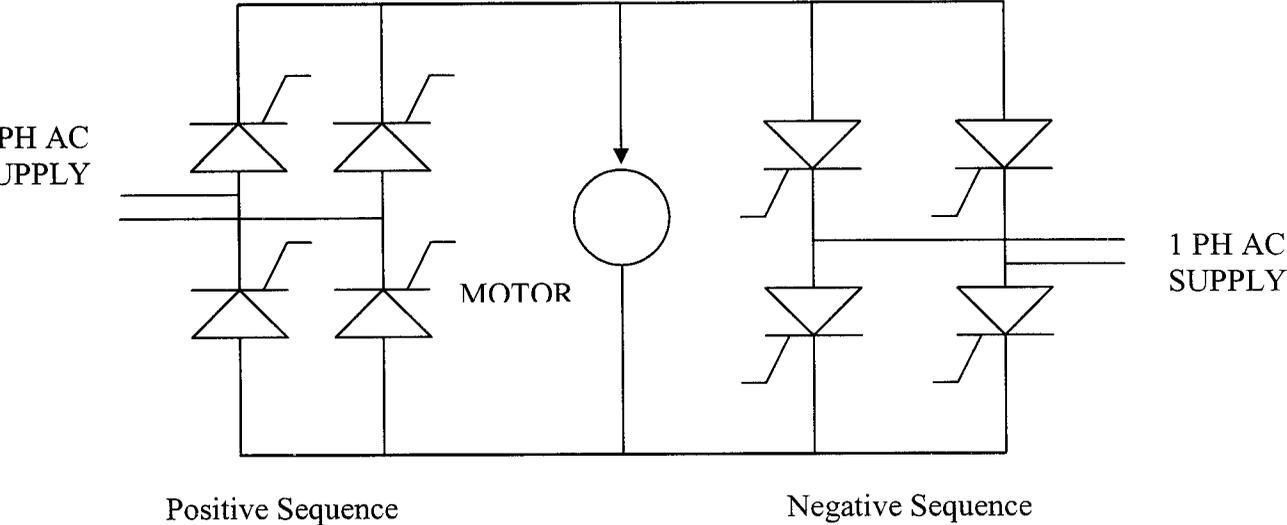
Figure 2.1

Direct Frequency Reducer:

A cycloconverter is a naturally commutated frequency changer. The alternating output voltages are obtained by selecting suitable portions of the alternating input voltages. For a given value and frequency of the input voltage, the cycloconverter allows the value and frequency of the output voltages to be continuously varied.

By controlling the frequency and depth of phase modulation of the firing angles of the converters it is possible to control the frequency and amplitude of the output voltage. Thus the cycloconverter has a facility for continuous and independent control over both its output frequency and voltage.

The basic principle of an ideal cycloconverter is to continuously modulate the firing angles of the individual converters, so that it produces a sinusoidal output. Thus the voltages of the generators have the same amplitude frequency and phase, the voltage at the output terminals of the cycloconverter is equal to the voltage of either of the generators. It is possible for the mean power to flow either to or from the output terminals and the cycloconverter is inherently capable of the operation with loads of any phase angle within a complete spectrum of 360 degrees.

Each two quadrant converter is represented as an alternating voltage

its output terminals. The phase controlled converters (thyristors) connected in series with the voltage source shows the unidirectional conduction of each two quadrant converter. The ripple in the output voltage of the converter is neglected the converter becomes ideal and represents the desired output.

Single phase ac to single phase ac bridge type converter is employed here in our project. Here two single phase fully controlled bridges are connected in opposite directions .Bridge1 supplies load current in the positive half of the output cycle and bridge2 supplies load current in the negative half of the output cycle. The two bridges should not conduct together as this will produce a short circuit at the input. The load current may be continuous or discontinuous depending upon the firing angle and the load power factor.

When the load current is positive the firing pulses to the thyristors of bridge2 will be inhibited and bridge will be gated. Similarly when the load current is negative bridge2 will be gated and the firing pulses will not be applied to the thyristors in bridge1. Thus the firing control scheme involves the conduction of one converter at a time and the changeover of firing pulses from one converter to the other should be periodic according to the output frequency.

Waste heat is produced in thyristors due to the current flowing through them. The heat sink helps to dissipate (remove) the heat produced

FIRING CIRCUIT

The basic requirements for successful firing of a thyristor are that the current supplied to the gate should:

1) Be of adequate amplitude and sufficiently short rise time.
2) Be of adequate duration.
3) Occur at a time when the main circuit conditions are favorable to conduction.

The thyristor are at line potential and the trigger circuit is referenced with respect to a logic ground associated with the control input. Therefore the zero crossing detection of line voltage synchronization and the gate pulse generated with the gate trigger circuit must be isolated from the line potential by means of pulse transformers or isolation transformers. The gate trigger circuit also requires a dc power supply referenced with respect to the logic ground potential. This D.C. voltage can be supplied by rectifying the output of the line voltage synchronization transformer.

The ac synchronization voltage is converted into ramp voltage in the delay angle block which gets synchronized to the zero crossing of the line voltage's ramp voltage, which has constant peak-to-peak amplitude, is compared with a control voltage. During alternate half cycles when the ramp voltage equals the control voltage, a pulse signal of controllable duration is

range between 0-180 degree by means of a potentiometer and the delay angle is proportional to the control voltage. The general block diagram of the gate –trigger circuit is shown in the figure.

Block diagram of firing circuit
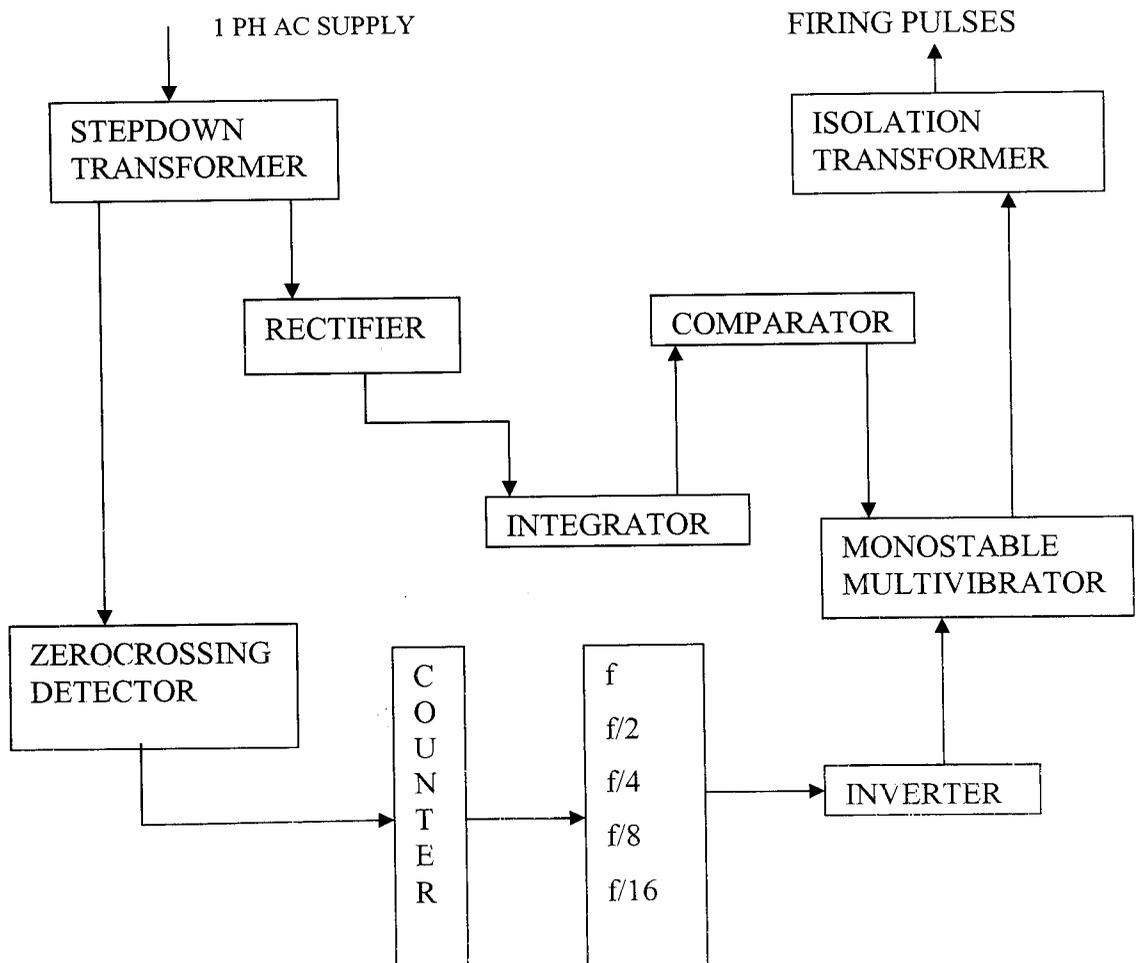
➢ The single phase ac supply is rectified using a single phase bridge type rectifier and the regulated output is integrated resulting in a ramp output.

➢ The ramp output compared with the reference voltage using a comparator.

➢ The output of comparator is given as trigger pulse to the 555 Timer configured in Monostable mode.

➢ With the help of counter and zero crossing detectors the frequency is adjusted. An inverter is used along with counter to provide separate gating pulses for the negative sequence thyristors.

➢ For the positive sequence pulses the pulse is taken directly from the counter without any inversion.

➢ The output from the counter is given as reset pulse to the 555 Timer.

➢ The output of the Monostable multivibrator is the trigger pulse, given to the thyristors via the pulse transformer.

➢ The pulse transformer couples the trigger pulse generator to the thyristors in order to obtain electrical isolation between the two circuits

The working of the individual blocks is explained as follows

Integrator

Integrator circuitry
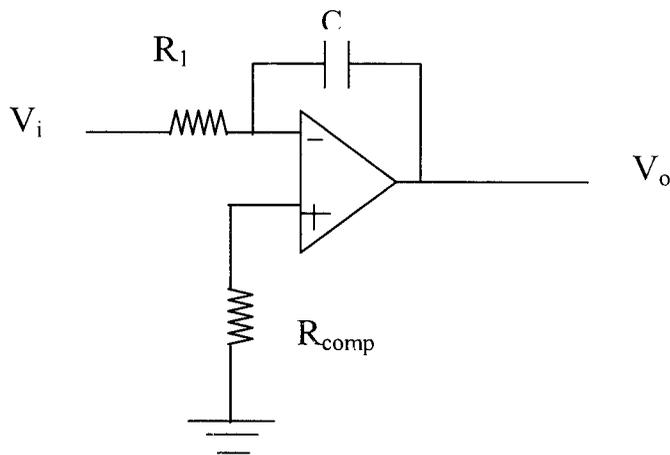
Figure 2.3

A circuit in which output voltage is directly proportional to the integral of the input is known as an *integrator or the integration amplifier.* Such a circuit is obtained by using operational amplifier in the inverting configuration with the feedback resistor replaced by a capacitor

C is the integration constant and is proportional to the value of the output voltage at time equal to zero seconds. The output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant R_1C

For example if the input is a sine wave, the output will be a cosine wave; or if the input is a square wave output is a triangular wave

The output waveform of the integrator is as follows

Integrator output
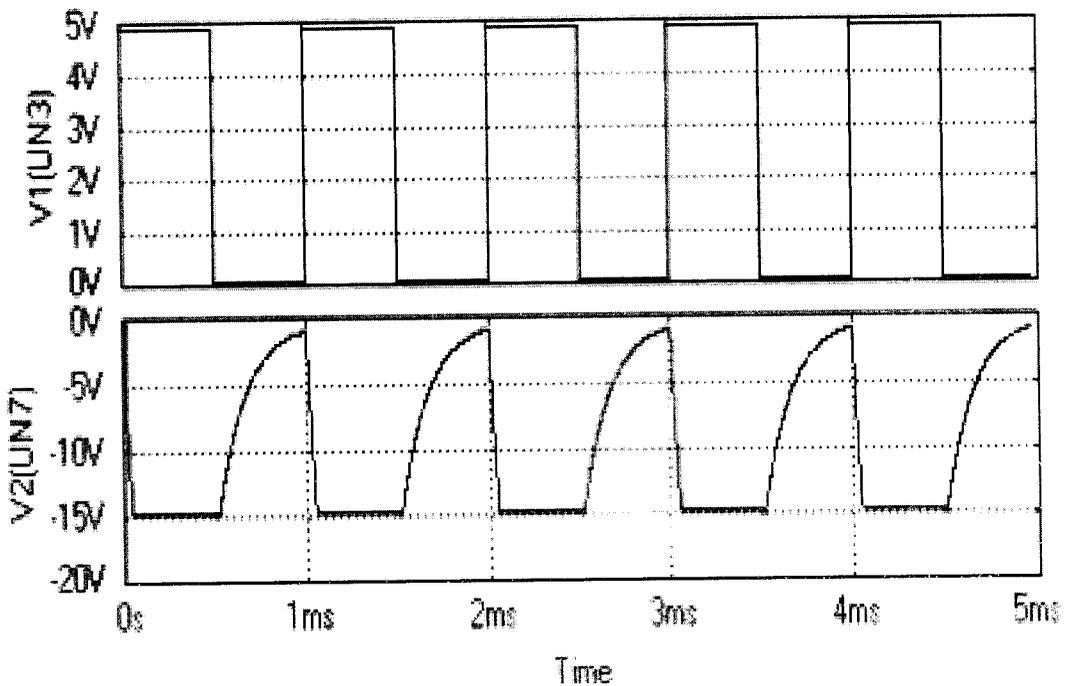
Figure 2.4

Comparator

A 'comparator' is circuit that compares an input voltage with a reference voltage. The output of the comparator then indicates whether the input signal is either above or below the reference voltage

Comparator Circuit
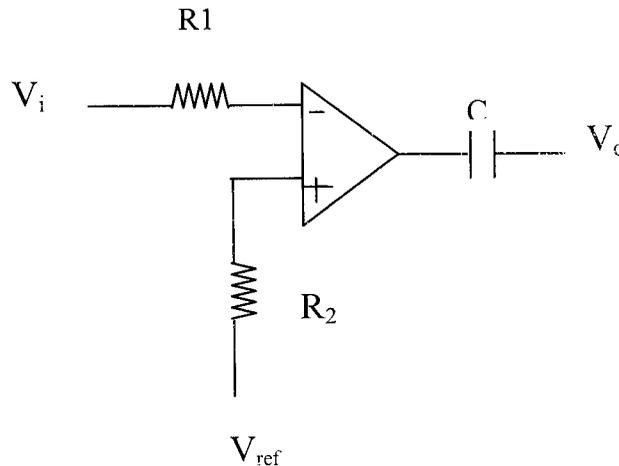
Figure 2.5

The output is switched ON or OFF depending on the relative voltages at the PLUS and MINUS inputs of the comparator, sees the rules below. The inputs are quite sensitive and a difference of only a few millivolts between the two will cause the output to turn on or off. Reference voltage is fixed at one-half of the supply voltage while the input voltage is

variable from zero to the supply voltage. In theory the reference and input voltages can be anywhere between zero and the supply voltage but there are practical limitations on the actual range depending on the particular device used.

Zero crossing detector:

A zero crossing threshold detector is an electronic circuit that consists of an operational amplifier with an input voltage at its positive input often used in conjunction with other circuit elements; it usually functions as a simple voltage switch.

When the input voltage is positive, the output voltage is a positive value, when the input voltage is negative; the output voltage is a negative value. The magnitude of the output voltage is a property of the operational amplifier and its power supply.

555 timer configured in monostable mode:
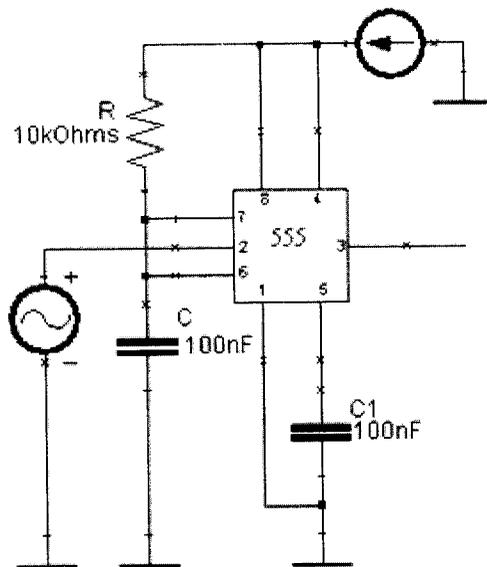
Figure 2.6

Monostable multivibrator often called a *one shot* multivibrator is a pulse generating circuit in which the duration of this pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby state, the output of the circuit is approximately zero or a logic-low level. When external trigger pulse is applied output is forced to go high (V_{CC}). The time for which output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low

until trigger pulse is again applied. Then the cycle repeats. The monostable circuit has only one stable state (*output low*) hence the name *monostable*.

Operation:

555 Internal Diagram
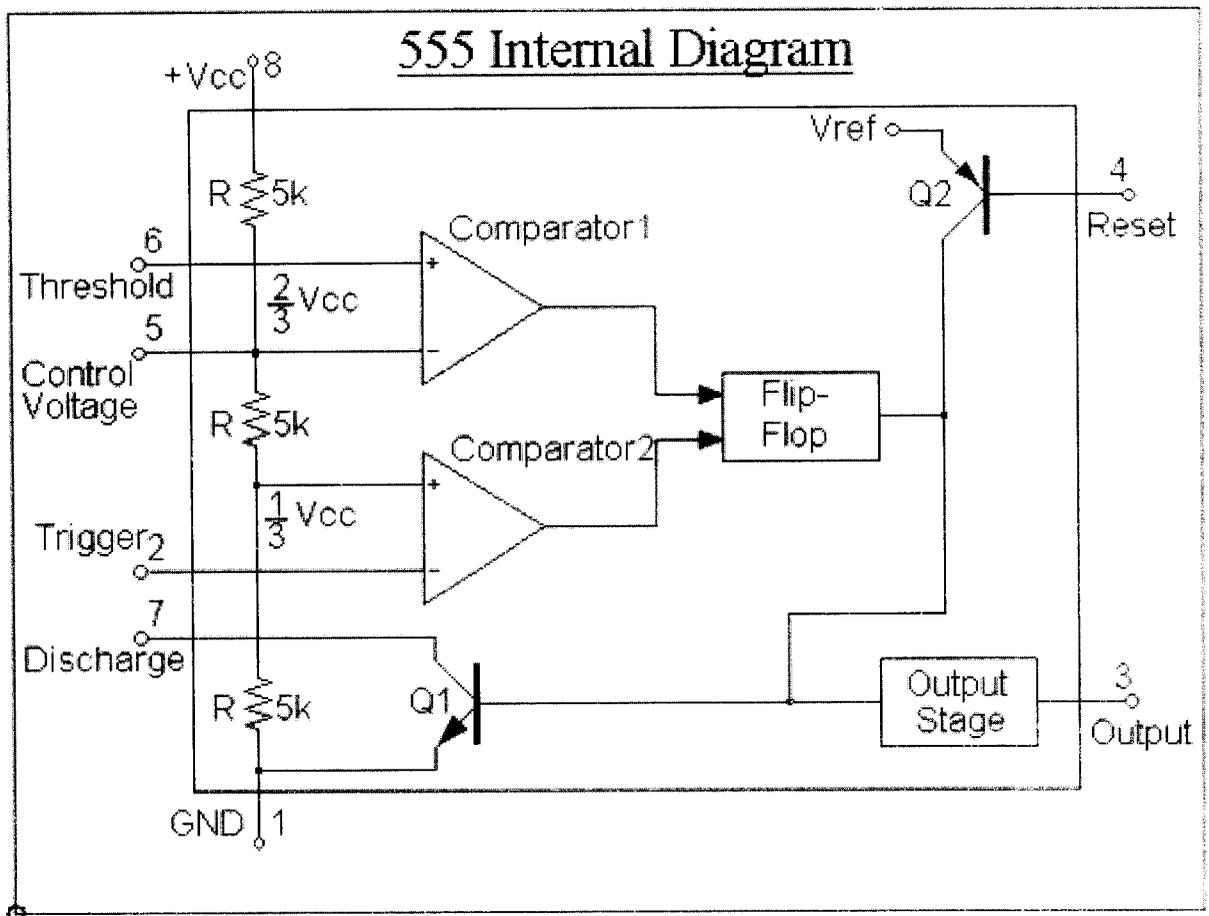
Figure 2.7

Initially when the circuit is in the stable state i.e. , when the output is low, transistor Q1 is ON and the capacitor C is shorted out to ground. Upon the application of a negative trigger pulse to pin 2, transistor Q1 is turned

OFF, which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up towards V_{CC} through R. When the voltage across the capacitor equals 2/3 V_{CC}, comparator 1's output switches from low to high, which in turn drives the output to its low state via the output of the flip-flop. At the same time the output of the flip-flop turns transistor Q1 ON and hence the capacitor C rapidly discharges through the transistor. The output of the monostable remains low until a trigger pulse is again applied. Then the cycle repeats.

The pulse width of the trigger input must be smaller than the expected pulse width of the output waveform. Also the trigger pulse must be a negative going input signal with amplitude larger than 1/3 V_{CC}.

The time during which the output remains high is given by

$$t = 1.1RC \quad seconds$$

Where R is in Ohms and C is in Farads.

Once triggered, the circuit's output will remain in the high state until the set time, t elapses. The output will not change its state even if an input trigger is applied again during this time interval t. The circuit can be reset during the timing cycle by applying negative pulse to the reset terminal. The output will remain in the low state until a trigger is again applied.

The output waveform of Monostable multivibrator may be observed as.

Monostable multivibrator
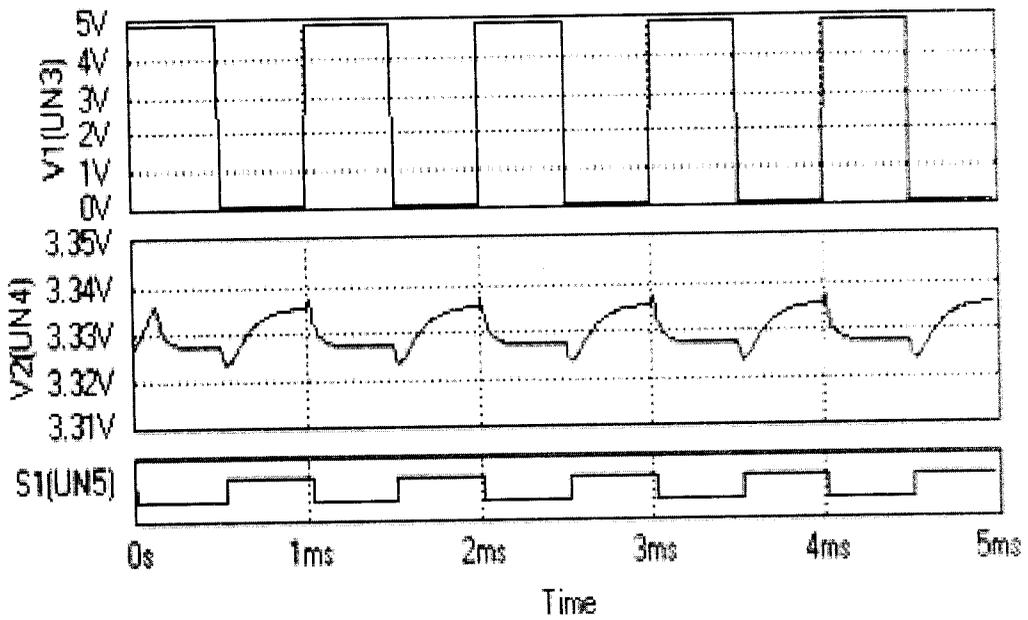
Figure 2.8

Pulse Transformer

Pulse transformers are basically the transformers which couple a source of pulses of electrical energy to a load with its shape and other properties unchanged. The pulses can be repetitive or non-repititive.the pulse transformer finds applications in communication, power electronics, digital electronics, and fast pulse generation and so on.

Pulse Transformer circuit

1:1:1 Pulse Transformer

SCR T1

Unilateral Trigger Pulse Generator

SCR T2
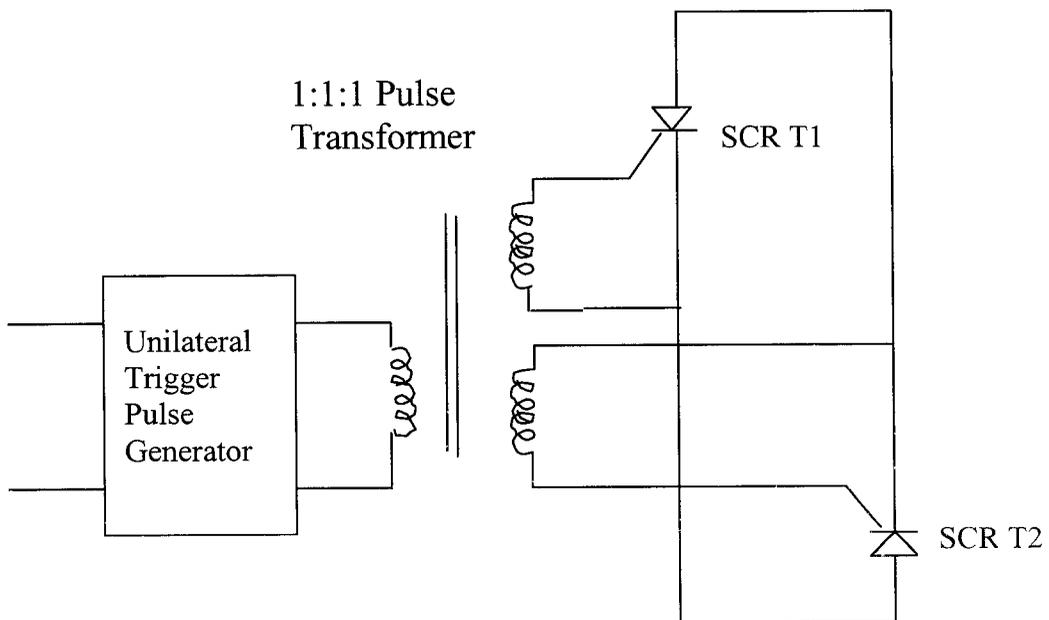
Figure 2.9

In power electronic circuits pulse transformer is particularly used for triggering the thyristors, triacs and so on. Pulse transformers used in the

pulse generators and can deliver few volts at pulse widths of a few microseconds

Pulse transformers are often used to couple a trigger pulse generator to a thyristor in order to obtain electrical isolation between the two circuits. The transformers commonly used for thyristor control are either 1:1 two-winding or 1:1:1 three winding types. The fig shows the way of using the pulse transformer to drive an inverse parallel pair of SCRs. A full isolation is provided by the three winding transformer. Pulse generator must supply sufficient energy to trigger both SCRs and the pulse transformer must supply sufficient gate current to both SCRs under worst conditions of unbalanced gate impedances

The design of "signal" type of pulse transformer focuses on the delivery of a signal at the output. The transformer delivers a "pulse-like" signal or a series of pulses. The turn's ratio of the pulse transformer can be used to adjust signal amplitude and provide impedance matching between the source and load. Pulse transformers are often used in the transmittal of digital data and in the gate drive circuitry of transistors, F.E.T.s, S.C.R.s, and etc. In the latter application, the pulse transformers may be referred to as "gate transformers" or "gate drive transformers". Signal type of pulse transformers handle relatively low levels of power. For digital data transmission, transformers are designed to minimized signal distortion.

Counter:

Counters are strings of flip flops where the output of one feeds the input of the next. A sequence of input pulses causes the pattern of flip flop outputs to increment or count over the binary, decimal, or other sequence.

Asynchronous or ripple counters are arranged in such a way that the output of one flip flop changes the state of the next. In a long chain of ripple counter stages, the last flip flop changes its state considerably later than the first FF due to propagation delays in each stage. Problems occur if this delay is longer than the response time of other logic elements connected to the circuit. An even more serious source of error results because the outputs of a ripple counter during changes of state often correspond to intermediate states outside of the intended sequence. If the output lines are connected to logic which can respond to these in-between states, glitches can occur that are so fast the error may be difficult to track down

Modulus: The *modulus* is the number of distinct states the counter goes through before repeating. The modulus of a 4-bit binary counter is 16.

Symmetry: A counter is *symmetric* if the outputs are all square waves. A binary counter is symmetric, but a BCD counter is not, since the D output is high for only 2 of the 10 states.

Count Direction: The sequence of output states may go up, down, or selectable.

Synchronism: A transition between states may propagate along the FF chain (*asynchronous* or ripple) or take place at the same time for each FF (*synchronous* or clocked).

Reset and Parallel Load: All counters need a *reset*, usually to the zero state. Counters also have *parallel load* capability to preset the counter to an arbitrary binary word. This is used, for example, in generating a counter of arbitrary modulus.

Cascadability and Unit Cascadability: Most counters can be *cascaded*, with the most significant bit output of one connected to the input of the next. This allows more precision, with a modulus equal to the *product* of modules in the chain.

MOTOR

Induction motor the most widely used ac motor in 90% of the mechanical power used in industry. The reasons are low cost, rugged construction, absence of commutator, good operating characteristics .The physical size of motor for a given output rating is relatively small. It is a singly excited motor although motor is equipped with both field and armature windings. The field winding is connected to the ac supply and the current is made to flow in the armature conductors by induction which interacts with the field thereby producing a net unidirectional field. Such motors are also called asynchronous motors. They are reversible and can operate in both motoring and generating mode based on the direction of rotation.

➢ Single phase induction motors are more preferred compared to three phase motors because of the following reasons:

➢ It is economical, as power requirements for individual loads are small

➢ Simple in construction, easy to repair and comparatively cheaper in cost.

Because of the above reasons motors of comparatively small ratings (Fractional kilowatt) are manufactured in large number. An indication of this is from the fact that the sum of total of all fractional kilowatt motors far exceeds the total of the integral kilowatt motors of all types.

Induction motors are classified as split phase shaded pole motors and repulsion start induction motor according to the method of producing starting torque.

Construction

The construction of induction motor is very simple compared to dc motor synchronous motor. The essential features are laminated stator core carrying a single phase winding, laminated rotor core of cage type, a stiff shaft to preserve the very short air gap. Frame to form the stator housing and carry the end covers. The end coverings receive the ball bearings with their clamping plates.

Frame

It is the outer body of the motor; it functions as a support to stator core and winding to protect the inner parts of the machine and also serves as a ventilating housing .the frame is die caste.

The advantage of die casting is that it facilitates the use of thicker cross section of frame where greater mechanical strength is required .the frame should be strong and rigid as the air gap length of the induction motor is very small if the frame is not rigid the rotor will not remain concentric with stator giving rise to unbalanced magnetic pull.

Stator core

The stator core is to carry the alternating flux which produces hysteresis and eddy current loss. in order to reduce eddy current and hysteresis loss, in the stator core it is assembled of high grade low electrical loss silicon steel punching of thickness 0.35mm.the punchings are insulated from one another by coating of varnish or oxide produced by heat treatment. The stampings are assembled under hydraulic pressure and are keyed to the frame.carefull alignment is required to prevent rubbing between rotor and stator. The air gap between rotor and stator is made small to minimize air gap reluctance. Stator stampings consists of semi closed slots to minimize air gap reluctance and excessive tooth losses.

Stator winding

It is wound for a definite number of poles. As per the requirement of speed. The greater the number of poles lesser the speed for a given frequency. Single phase induction motors are usually provided with concentric winding .with concentric coil the number of turns per coil can be adjusted to provide an approximately sinusoidal distribution of mmf along the air gap.

Single phase squirrel cage motors normally have two stator windings one of them usually have few turns of much thin wire, and the two windings

heaviest wire is known as main winding and the other is called auxiliary winding. The main winding is placed in the bottom of the slots and the starting winding is placed on the top.

Rotor
Squirrel cage rotor

In cage construction copper, brass or aluminum bars are placed as rotor conductors' parallel to the shaft and close to the rotor surface. The conductors are not insulated from the core since the rotor currents naturally flow through the path of least resistance that is the rotor conductors. at both the ends of the rotor the rotor conductors are all short circuited by continuous end rings of similar material to that of the rotor conductors. The rotor conductors and their end rings form complete closed circuit resembling a squirrel cage. the cage structure is formed by aluminum cast (under pressure into the slots of the rotor).the slot on the rotor are always not parallel to the motor shaft but are usually skewed in order to obtain uniform torque, reduce the magnetic locking of the stator and the rotor and reduce the magnetic humming noise while running.

Slots on the rotor are either of semi closed type or totally closed type because there is little difficulty in inserting the rotor bars in such slots. The advantage of semi closed and totally closed slots is that the effective cross section area of the air gap is increased therefore magnetizing current is reduced. Such slots also reduce the pulsation flux in the individual teeth

Squirrel cage rotor windings are perfectly symmetrical and have the advantage of being adaptable to any number of pole pairs. the distribution of current due to electromagnetic induction in the rotor bars vary from bar to bar sinusoidally and depends upon the position and time, assuming sinusoidal distribution of the radial flux density in space and also the applied voltage to be varying sinusoidally with time.

Modern capacitor start motors employ ac electrolytic capacitor .an electrolytic capacitor is formed by winding two sheets of etched aluminum foil separated by two layers of insulating paper into a cylindrical shape.

The unit is impregnated with an electrolyte usually ethylene glycolol or a derivative .an anodic film is later produced on each foil by electrochemical means. The voltage rating of the capacitor is not necessarily the same as that of the motor.

Bearings

General types of the bearings used are –Ball bearing and Roller bearing. Roller Bearing is used in the driving end and Ball bearings are used in the non driving end.

Principle

When the stator winding of a single phase induction motor is connected to a single phase ac supply, a magnetic field is developed whose axis is always along the axis of the stator coil with the alternating current in the fixed stator coil, the mmf wave is stationary in space but pulsates in magnitude and varies sinusoidally with time. Currents are induced in the rotor conductors by transformer action, these currents being in such a direction as to oppose the stator mmf. thus the axis of the rotor mmf wave

Coincides with that of the stator field, the torque angle is zero and no torque is developed at starting. however if the rotor of such a motor is given a push by hand , or by another means in either direction ,it will pick up speed and continue to rotate in the same direction developing operating torque. Thus a single phase induction motor is not self starting and needs special starting mechanisms.

The performance characteristics of the single phase induction motor, in general are of those of that of three phase induction motor. However it is inferior for a given frame size,. This is due to the presence of backward rotating field.

MOTOR SPECIFICATIONS:

Power rating (hp) : 1/5   Voltage rating (V) : 230 V

Current rating (A) : 2 A   Speed (rpm)   : 960 rpm

No of poles   : 6

Stator

Core length   : 25mm

Stator diameter   : 127mm

No: of slots   : 36

Thickness of stampings : 0.52mm

No: of turns per pole   : 120

Type of winding   : concentric

Rotor

Length   : 25mm

Rotor diameter   : 75mm

Type   : squirrel cage rotor

Thickness of stamping : 0.56mm

Air gap   : 0.28mm

DESIGN:

Normal frequency design

➤   KVA rating of the machine $Q = m\,E_{ph}\,I_{ph}\,10^{-3}$

Where   Q is the KVA rating of the machine

         m is the No of phases

         E_{ph} is the o/p voltage per phase

         I_{ph} is the current per phase * 10^{-3}

Where f is the frequency.

         Φ is the flux.

         T_{ph} is the number of turns per phase.

         K_w is the winding factor.

➤ $f = p\,N_s\,/\,120.$

     $N_s = 120 * 50/6$

       $= 1000$ rpm

     Where p is the number of poles.

         N_s is the synchronous speed of the motor

KVA rating of a machine $Q = \dfrac{(hp * 0.746)}{\acute{\eta}\,\cos\varphi}$

Where hp is the horse power rating of the motor

     $\acute{\eta}$ is the efficiency of the machine

     Cos φ is the power factor

     hp=0.2; $\acute{\eta}$ =0.7, cos φ=0.7

     => Q =0.3045

Therefore

$$Q = 1.11 \, K_w \, (\Pi \, D \, L \, B_{av}) \, (\Pi \, D \, ac) \, n_s * 10^{-3}$$

$$Q = C_o \, D^2 \, L \, n_s$$

Where $C_o = 11 \, B_{av} ac \, K_w * 10^{-3}$

$\qquad B_{av}$ is the magnetic loading in Tesla

$\qquad B_{av} = (p \, \Phi)/ (\Pi \, D \, L)$

$\qquad ac$ is the electric loading in Ampere/metre

$\qquad ac = (I_z \, Z)/ (\Pi \, D)$

Assuming the values of electric and magnetic loading as 0.5 Tesla and 15000 A/m.

$C_o = 52.52$

Substituting in the above formulae we get

$D^2 \, L = 1.5 * 10^{-4}$

Corresponding to the availability of 36 slots

$D = 7.5$ cm & $L = 2.5$ cm

$\Phi = B_{av} (\Pi \, D \, L/p)$

$\Rightarrow \Phi = 0.5$ mWb

Low frequency design:

> KVA rating of the machine $Q = m\, E_{ph}\, I_{ph}\, 10^{-3}$

Where   Q is the KVA rating of the machine

   m is the No of phases

   E_{ph} is the o/p voltage per phase

   I_{ph} is the current per phase $* 10^{-3}$

Where f is the frequency.

   Φ is the flux.

   T_{ph} is the number of turns per phase.

   K_w is the winding factor.

> $f = p\, N_s\, /\, 120.$

   $N_s = 120* 12.5/6$

   $= 250$ rpm

Where p is the number of poles.

   N_s is the synchronous speed of the motor

KVA rating of a machine $Q = \dfrac{(hp * 0.746)}{\acute{\eta}\ cos\ \varphi}$

Where hp is the horse power rating of the motor

   $\acute{\eta}$ is the efficiency of the machine

   Cos φ is the power

hp=0.2; $\acute{\eta}$ =0.7, cos φ=0.7

=> Q =0.3045

Therefore

$$Q = 1.11\, K_w\, (\Pi\, D\, L\, B_{av}\,)\, (\Pi\, D\, ac\,)\, n_s * 10^{-3}$$

$$Q = C_o\, D^2\, L\, n_s$$

Where $C_o = 11\, B_{av}ac\, K_w * 10^{-3}$

B_{av} is the magnetic loading in Tesla

$B_{av} = (p\, \Phi)/ (\Pi\, D\, L)$

ac   is the electric loading in Ampere/metre

$ac = (I_z\, Z)/ (\Pi\, D)$

where D is the diameter of the rotor.

L is the core length of the stator

Assuming the values of electric and magnetic loading as 0.6 Tesla and 12000 A/m.

$C_o = 50.42$

Substituting in the above formulae we get

$D^2\, L = 1.96 * 10^{-3}$.

Corresponding to the availability of 48 slots

D=0.2m & L = 5 cm

CHAPTER III

PERFORMANCE ANALYSIS

The speed torque curve of the motor considered is shown below:
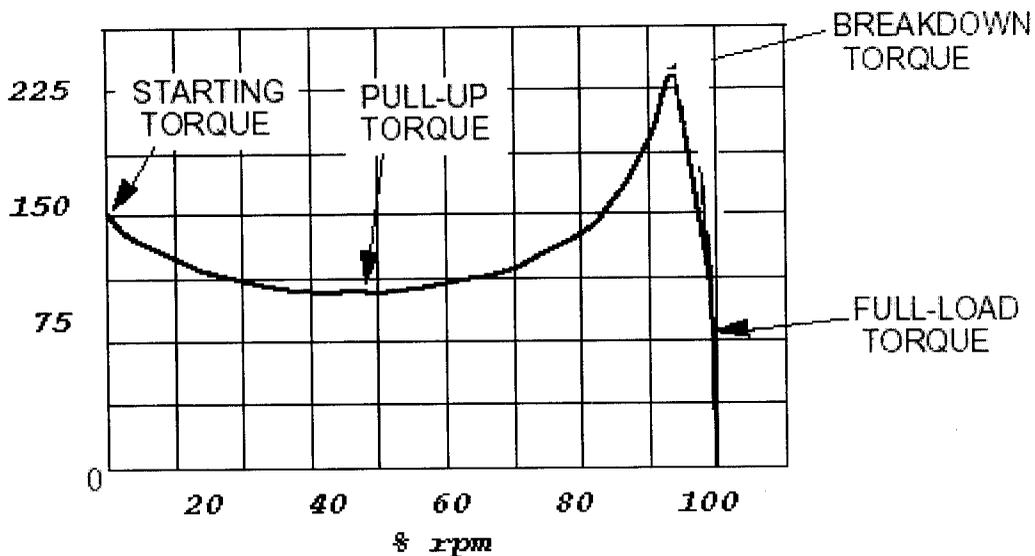
Speed –Torque characteristics

Figure 3.1

The horsepower and torque output of an induction motor can be calculated by these formulas:

TORQUE= HP * K

RPM

(HP=0.2, RPM=220)

Where $K = 7124$ (This value is taken when power is expressed in HP and torque is in Nm)

The speed torque characteristics of the motor when it is operated at normal voltage and reduced frequency level is shown below.
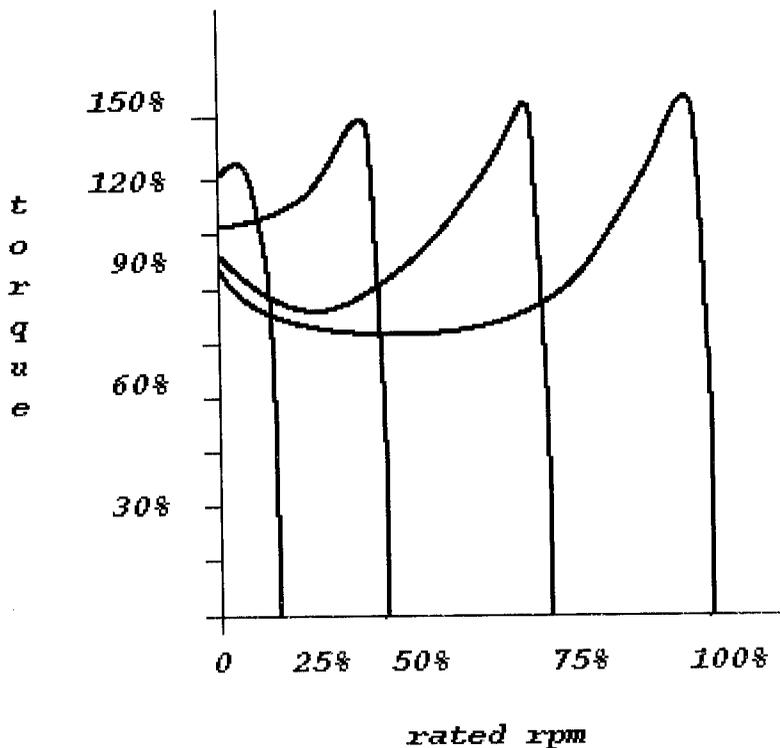
Figure 3.2

Starting efficiency = Locked rotor torque

Locked rotor current

$= 1.25/ 1.62$

Hint: the locked rotor current and torque are expressed as a percentage of full load current and torque.

No load parameters:

S.no	Voltage (volts)	Current (Ampere)	Input power (watts)	Power factor
1	230	0.55	130	0.86
2	230	0.6	132	0.8

Table 1

Load parameters:

s.no	Voltage (volts)	Current (Ampere)	Input power (watts)	Output power (watts)	efficiency
1	230	0.8	165	119	0.72
2	230	0.83	168	118	0.7

Table 2

Note:

1 Conventional design

COMPARATIVE STUDY

Feature	Belt	Gear	Present design
Speed reduction	Obtained using shieves and belt.	Obtained by varying the gear ratio.	Obtained by tapping the required frequency.
Coupling	Indirect	Indirect	Direct
Noise	Noisy	Noisy	Noiseless
Lubrication	Lubrication not required	Frequent lubrication	Lubrication not required.
Load	Stretching and Slippage of belts at high loads.	Gears get jammed at high inertia loads.	Has no effect on the speed reduction circuit.
Mechanical losses	Friction and wear and tear.	Friction and wear and tear.	No mechanical component involved.
Cost of the application considered.	Rs.3000 (approx)	Rs.2000 (approx)	Rs.3000 (approx)

Table 3

REASONS FOR OPTING THIS DESIGN

Direct low rpm motor is not feasible-

➢ Diameter and length not within permissible design limits. The stampings for which are not available.

➢ Required torque will not be produced.

The present design offers the following advantages:

✓ As it employs natural commutation; it does not require auxiliary circuits for turning off the thyristors.

✓ Being a direct converter, it is extremely efficient, as the current flowing from input to output only passes through one or two semiconductor devices.

✓ It is inherently reversible in the current and voltage, since it consists of one or three four quadrant rectifiers depending on whether it has a single phase or a three phase output.

✓ It benefits from the substantial industrial experience acquired using four quadrant rectifiers.

✓ Device control and protection present little difficulty.

✓ The positive aspect of using a cycloconverter is the greater flexibility with respect the shape of the ac voltage.

In equipment fed by the 50 or 60 Hz industrial mains supply, cycloconverters are mainly used as variable frequency power supplies for

reducer between the motor and the driven load. Nowadays the load is coupled directly to the motor which is supplied at a frequency of between 0 and 5 or 10 Hz, for example using a cycloconverter.

Cascaded systems involve 2 stages of power conversion –rectification and inversion in which the load current must pass through at least 2 power switching devices in series .this increases the conduction losses .direct frequency changer or cycloconverter has the advantage of only one stage of power conversion current can flow from input to output through only one switching device so that conduction losses are minimized. Cycloconverters are inherently capable of reversed power flow without additional components, so that regenerative systems need only the appropriate control function.

COST ANALYSIS

The cost of the present day grinders employing belt or gear mechanism ranges from Rs 2000 to Rs 6000.as the application we have considered is a consumer product here is brief analysis of the cost of the present design.

Cost of various components used:

Counter (4040)	Rs 5
Inverter (7404)	Rs 6
555 timer	Rs 5
IC 741	Rs 4.50
Regulator ICs (7805, 7812)	Rs 8
Pulse transformer	Rs 22
Thyristors (25TTS12)	Rs 65

The total cost of the frequency reducing circuit including the various miscellaneous components and the fabrication is around Rs 2000/-

The total cost of the principle employed including the motor is less than Rs 3000

CONCLUSION

By using the power electronics frequency reduction circuitry, the speed reduction is obtained to the desired level .and the required features are obtained. Due to the enormous cost in making total frame, which requires new tools and moulds, the overall setup could not be achieved. . But for the mass production of the application considered the cost of single unit will be very less. The circuit developed can be used as an alternative for any application involving belt or gear mechanism

APPENDIX

APPENDIX 1

POWER SUPPLY:

The present chapter introduces the operation of power supply circuits built using filters, rectifiers, and then voltage regulators. Starting with an ac voltage, a steady dc voltage is obtained by rectifying the ac voltage, then filtering to a dc level, and finally, regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies, or the output load connected to the dc voltage changes.

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in fig . The ac voltage, typically 120 V rms, is connected to a transformer, which steps that ac voltage down to the level for the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation. A regulator circuit can use this dc input to provide a dc voltage that not only has much less ripple voltage but also remains the same dc value even if the input dc voltage varies somewhat, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units

```
TRANSFORMER ----> RECTIFIER ----> REGULATOR ---> FILTER ---> LOAD
```
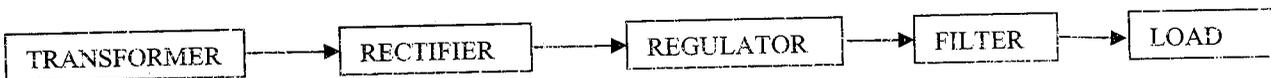
IC VOLTAGE REGULATORS:

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. Although the internal construction of the IC is somewhat different from that described for discrete voltage regulator circuits, the external operation is much the same. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustably set voltage.

A power supply can be built using a transformer connected to the ac supply line to step the ac voltage to a desired amplitude, then rectifying that ac voltage, filtering with a capacitor and RC filter, if desired, and finally regulating the dc voltage using an IC regulator. The regulators can be selected for operation with load currents from hundreds of milli amperes to tens of amperes, corresponding to power ratings from milliwatts to tens of watts.

THREE-TERMINAL VOLTAGE REGULATORS:

Fig shows the basic connection of a three-terminal voltage regulator IC to a load. The fixed voltage regulator has an unregulated dc input voltage, Vi, applied to one input terminal, a regulated output dc voltage, Vo, from a second terminal, with the third terminal connected to ground. For a selected regulator, IC device specifications list a voltage range over which the input voltage can vary to maintain a regulated output voltage over a range of load current. The specifications also list the amount of output voltage change resulting from a change in load current (load regulation) or in input voltage (line regulation).

Fixed Positive Voltage Regulators:


```
        IN      OUT
        7805
From    GND
Transforme
r
                GND
```
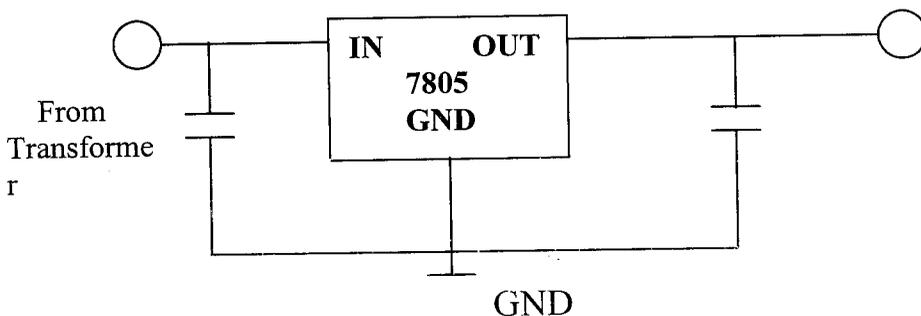
The series 78 regulators provide fixed regulated voltages from 5 to 24 V. Figure shows how one such IC, a 7812, is connected to provide voltage regulation with output from this unit of +12V dc. An unregulated input voltage Vi is filtered by capacitor C1 and connected to the IC's IN terminal. The IC's OUT terminal provides a regulated +12V which is filtered by

permissible voltage range, and the output load may vary over some acceptable range, the output voltage remains constant within specified voltage variation limits. These limitations are spelled out in the manufacturer's specification sheets. A table of positive voltage regulated ICs is provided in table .

Positive Voltage Regulators in 7800 series

IC Part	Output Voltage (V)	Minimum Vi (V)
7805	+5	7.3
7806	+6	8.3
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7
7818	+18	21.0
7824	+24	27.1

February 1995

LM78XX Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expanded to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

Voltage Range

LM7805C	5V
LM7812C	12V
LM7815C	15V

Schematic and Connection Diagrams
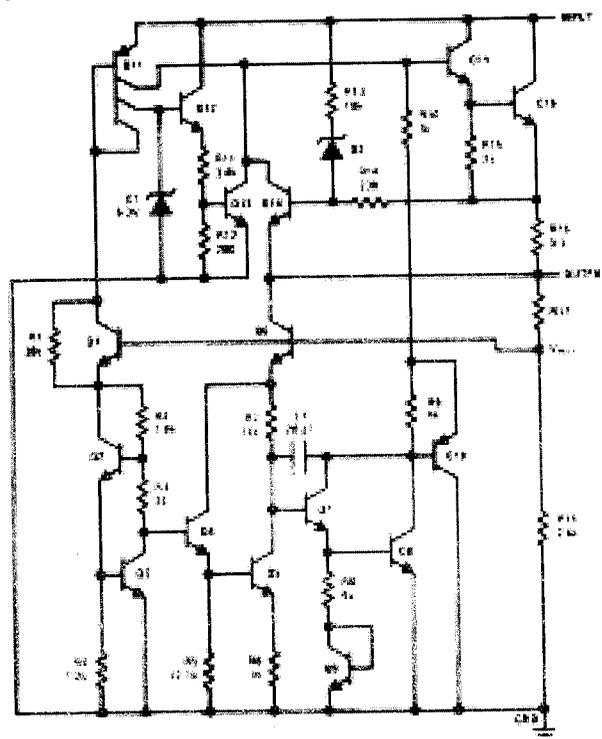
Metal Can Package
TO-3 (K)
Aluminum

Bottom View

Order Number LM7805CK,
LM7812CK or LM7815CK
See NS Package Number KC02A

Plastic Package
TO-220 (T)
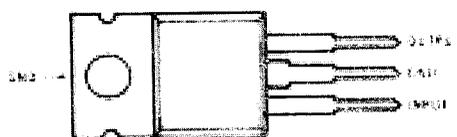
Top View

Order Number LM7805CT,
LM7812CT or LM7815CT
See NS Package Number T03B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage (V_O = 5V, 12V and 15V)   35V
Internal Power Dissipation (Note 1)   Internally Limited
Operating Temperature Range (T_A)   0°C to +70°C

Maximum Junction Temperature
  (K Package)   150°C
  (T Package)   150°C
Storage Temperature Range   −65°C to +150°C
Load Temperature (Soldering, 10 sec.)
  TO-3 Package K   300°C
  TO-220 Package T   230°C

Electrical Characteristics LM78XXC (Note 2) 0°C ≤ T_J ≤ 125°C unless otherwise noted.

|	Output Voltage		5V			12V			15V			
	Input Voltage (unless otherwise noted)		10V			19V			23V			Units
Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	T_J = 25°C, 5 mA ≤ I_O ≤ 1A	4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A	4.75		5.25	11.4		12.6	14.25		15.75	V
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(7.5 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)			V
ΔV_O	Line Regulation	I_O = 500 mA, T_J = 25°C		3	50		4	120		4	150	mV
		ΔV_{IN}	(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
		0°C ≤ T_J ≤ +125°C			50			120			150	mV
		ΔV_{IN}	(8 ≤ V_{IN} ≤ 30)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			V
		I_O ≤ 1A			50			120			150	mV
		ΔV_{IN}	(7.5 ≤ V_{IN} ≤ 20)			(14.6 ≤ V_{IN} ≤ 27)			(17.7 ≤ V_{IN} ≤ 30)			V
		0°C ≤ T_J ≤ +125°C			25			60			75	mV
		ΔV_{IN}	(8 ≤ V_{IN} ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			V
ΔV_O	Load Regulation	T_J = 25°C, 5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150	mV
		250 mA ≤ I_O ≤ 750 mA			25			60			75	mV
		5 mA ≤ I_O ≤ 1A, 0°C ≤ T_J ≤ +125°C			50			120			150	mV
I_Q	Quiescent Current	I_O ≤ 1A	T_J = 25°C			8			8			8	mA
			0°C ≤ T_J ≤ +125°C			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A			0.5			0.5			0.5	mA
		T_J = 25°C, I_O ≤ 1A			1.0			1.0			1.0	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)			V
		I_O ≤ 500 mA, 0°C ≤ T_J ≤ +125°C			1.0			1.0			1.0	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
V_N	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		40			75			90		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz { I_O ≤ 1A, T_J = 25°C or I_O ≤ 500 mA	62	80		55	72		54	70		dB
		0°C ≤ T_J ≤ +125°C	62			55			54			dB
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			V
R_O	Dropout Voltage	T_J = 25°C, I_{OUT} = 1A		2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz		8			18			19		mΩ
	Short-Circuit Current	T_J = 25°C		2.1			1.5			1.2		A
	Peak Output Current	T_J = 25°C		2.4			2.4			2.4		A
	Average TC of V_{OUT}	0°C ≤ T_J ≤ +125°C, I_O = 5 mA		0.6			1.5			1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	T_J = 25°C, I_O ≤ 1A		7.5			14.6			17.7		V

Note 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

Note 2: All characteristics are measured with capacitor across the input of 0.22 µF, and a capacitor across the output of 0.1 µF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

APPENDIX 2

555 TIMER

The internal diagram for a 555 timer is shown in the figure.

555 Internal Diagram
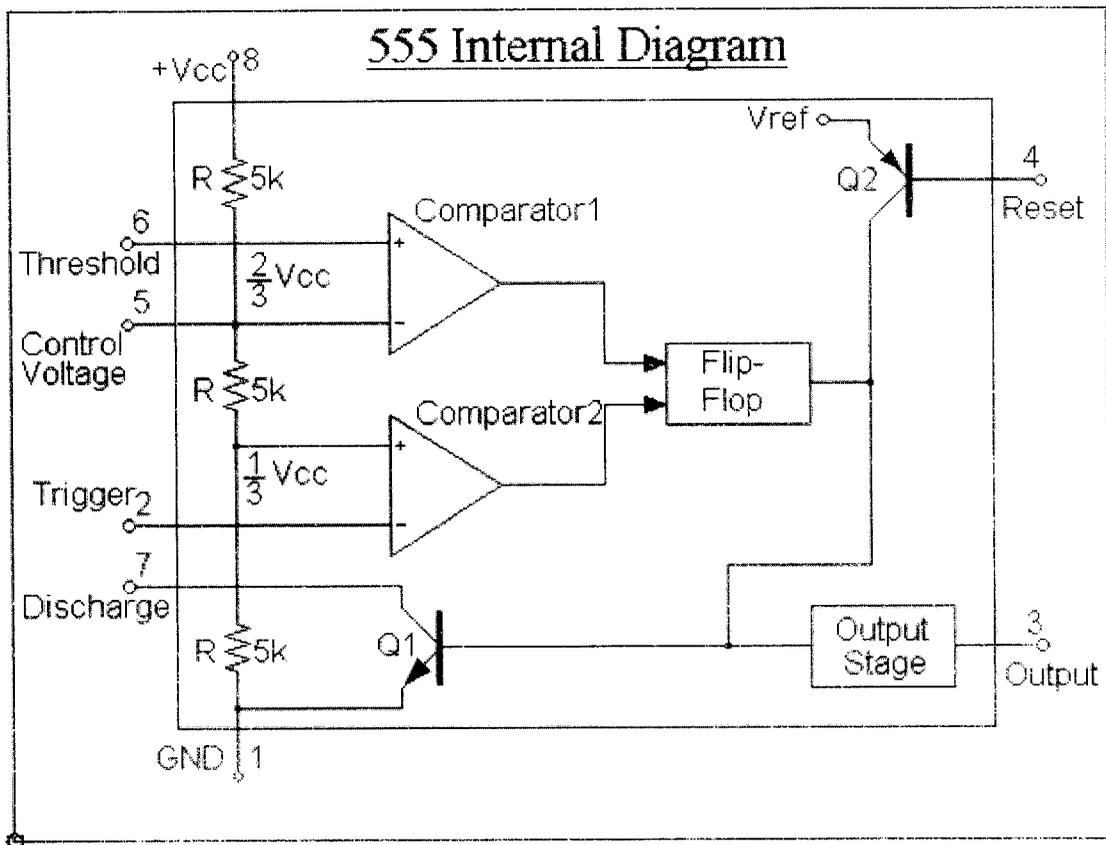
Pin1: Ground. All voltages are measured with respect to this terminal.

Pin2: Trigger. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. The output is low if the voltage at this pin is greater than 2/3 V_{CC}. When a negative going pulse of amplitude greater than 1/3 V_{CC} is applied to this pin, comparator 2 output goes low, which in turn switches the output of the timer high. The output remains high as long as the trigger terminal is held at a low voltage.

Pin3: Output. There are two ways by which a load can be connected to the

supply voltage $+V_{CC}$. When the output is low the load current flows through the load connected between pin3 and $+V_{CC}$ into the output terminal and is called sink current. The current through the grounded load is zero when the output is low. For this reason the load connected between pin 3 and $+V_{CC}$ is called the normally on load and that connected between pin 3 and ground is called normally off-load. On the other hand, when the output is high the current through the load connected between pin 3 and $+V_{CC}$ is zero. The output terminal supplies current to the normally off load. This current is called source current. The maximum value of sink or source current is 200mA.

Pin4: Reset. The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to $+V_{CC}$ to avoid any possibility of false triggering.

Pin5: Control Voltage. An external voltage applied to this terminal changes the threshold as well as trigger voltage. Thus by imposing a voltage on this pin or by connecting a pot between this pin and ground, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with a $0.01\mu F$ Capacitor to prevent any noise problems.

Pin6: Threshold. This is the non-inverting input of comparator 1, which monitors the voltage across the external capacitor. When the voltage at this pin is greater than or equal to the threshold voltage $2/3\ V_{CC}$, the output of comparator 1 goes high, which inturn switches the output of the timer low.

Pin7: Discharge. This pin is connected internally to the collector of transistor Q1. When the output is high Q1 is OFF and acts as an open circuit to external capacitor C connected across it. On the other hand, when the output is low, Q1 is saturated and acts as a short circuit, shorting out the external capacitor C to ground.

Pin8: $+V_{CC}$. The supply voltage of $+5V$ to $+18V$ is applied to this pin with respect to ground.

Absolute Maximum Parameters: Maximum means that the op-amp can safely tolerate the maximum ratings as given in the data section of such op-

performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The μA741 is short-circuit protected and allows for nulling of the offset voltage. The μA741 is manufactured by Fairchild Semiconductor.

Supply Voltage (+/-Vs): The maximum voltage (positive and negative) that can be safely used to feed the op-amp. Dissipation (P_d): The maximum power the op-amp is able to dissipate, by specified ambient temperature (500mW @ 80° C).

Differential Input Voltage (V_{id}): This is the maximum voltage that can be applied across the + and - inputs.

Input Voltage (V_{icm}): The maximum input voltage that can be simultaneously applied between both input and ground also referred to as the common-mode voltage. In general, the m Operating Temperature (T_a): This is the ambient temperature range for which the op-amp will operate within the manufacture's specifications. Note that the military grade version (μA741)has a wider temperature range than the commercial, or hobbyist, grade version (μA741C).

Output Short-Circuit Duration: This is the amount of time that an op-amp's ouput can be short-circuited to either supply voltage.

Input Parameters:

Input Offset Voltage (V_{oi})This is the voltage that must be applied to one of the input pins to give a zero output voltage. Remember, for an ideal op-amp, output offset voltage is zero!

Input Bias Current (I_b)This is the average of the currents flowing into both inputs. Ideally, the two input bias currents are equal.

Input Offset Current (I_{os})This is the difference of the two input bias currents when the output voltage is zero.

Input Voltage Range (V_{cm})The range of the common-mode input

Input Resistance (Z_i)The resistance 'looking-in' at either input with the remaining input grounded.

Output Parameters:

Output Resistance (Z_{oi})The resistance seen 'looking into' the op-amp's output.

Output Short-Circuit Current (I_{osc})This is the maximum output current that the op-amp can deliver to a load.

Output Voltage Swing (V_o max)Depending on what the load resistance is, this is the maximum 'peak' output voltage that the op-amp can supply without saturation or clipping.

Dynamic Parameters:

Open-Loop Voltage Gain (A_{ol})The output to input voltage ratio of the op-amp without external feedback.

Large-Signal Voltage GainThis is the ratio of the maximum voltage swing to the charge in the input voltage required to drive the ouput from zero to a specified voltage (e.g. 10 volts).

Slew Rate (SR)The time rate of change of the ouput voltage with the op-amp circuit having a voltage gain of unity (1.0).

Other Parameters:

Supply Current This is the current that the op-amp will draw from the power supply.

Common-Mode Rejection Ratio (CMRR) A measure of the ability of the op-amp' to reject signals that are simultaneously present at both inputs. It is the ratio of the common-mode input voltage to the generated output voltage, usually expressed in decibels (dB).

will be present. That is, a signal applied to the input of one section of a dual op-amp will produce a finite output signal in the remaining section, even though there is no input signal applied to the unused section.

Op amp741-

Open-Loop Gain: Lets have a look how the 'ideal' amplifier would look like in Fig. 5-1. The search for an ideal amplifier is, of course, a futile exercise. The characteristics of the operational amplifier are good enough, however, to allow us to treat it as ideal. Below are some amplifier properties that make this so.

1. Gain—infinite

2. Input impedance--infinite

3. Output impedance--zero

4. Bandwidth--infinite

5. Voltage out--zero (when voltages into each other are equal)

6. Current entering the amp at either terminal--extremely small

Electrical Ratings: Electrical characteristics for op-amps are usually specified for a certain (given) supply voltage and ambient temperature. Also, other factors may play an important role such as certain load and/or source resistance. In general, all parameters have a typical minimum/maximum value in most cases.

```
offset null  1 ⌐⌐   8 n/c
  inv. input 2        7 V+
non-inv. input 3      6 output
         V- 4         5 offset null
           8-Pin
```

```
     n/a 1 ⌐⌐  14 n/a
     n/a 2      13 n/a
offset null 3   12 n/a
 inv. input 4   11 V+
non-inv. input 5 10 output
        V- 6     9 offset null
       n/a 7     8 n/a
         14-Pin
```
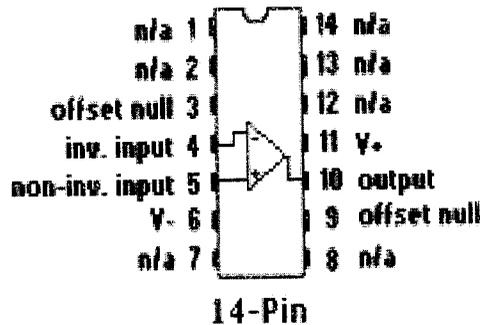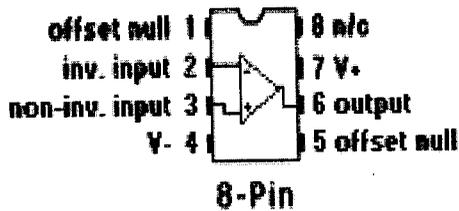
Definition of 741-pin functions:

(Pin 1 (Offset Null): Offset nulling, see Fig. 11. Since the op-amp is the differential type, input offset voltage must be controlled so as to minimize offset. Offset voltage is nulled by application of a voltage of opposite polarity to the ofset. An offset null-adjustment potentiometer may be used to compensate for offset voltage. The null-offset potentiometer also compensates for irregularities in the operational amplifier manufacturing process which may cause an offset. Consequently, the null potentiometer is recommended for critical applications. See 'Offset Null Adjustment' for method.

Pin 2 (Inverted Input): All input signals at this pin will be inverted at output pin 6. Pins 2 and 3 are very important (obviously) to get the correct input signals or the op amp can not do its work.

Pin 3 (Non-Inverted Input): All input signals at this pin will be processed normally without invertion. The rest is the same as pin 2.

Pin 4 (-V): The V- pin (also referred to as Vss) is the negative supply voltage terminal. Supply-voltage operating range for the 741 is -4.5 volts (minimum) to -18 volts (max), and it is specified for operation between -5 and -15 Vdc. The device will operate essentially the same over this range of voltages without change in timing period. Sensitivity of time interval to supply voltage change is low, typically 0.1% per volt. (Note: Do not confuse the -V with ground).

<u>Pin 6</u> (Output): Output signal's polarity will be the oposite of the input's when this signal is applied to the op-amp's inverting input. For example, a sine-wave at the inverting input will output a square-wave in the case of an inverting comparator circuit.

<u>Pin 7</u> (posV): The V+ pin (also referred to as Vcc) is the positive supply voltage terminal of the 741 Op-Amp IC. Supply-voltage operating range for the 741 is +4.5 volts (minimum) to +18 volts (maximum), and it is specified for operation between +5 and +15 Vdc. The device will operate essentially the same over this range of voltages without change in timing period. Actually, the most significant operational difference is the output drive capability, which increases for both current and voltage range as the supply voltage is increased. Sensitivity of time interval to supply voltage change is low, typically 0.1% per volt.

<u>Pin 8</u> (N/C): The 'N/C' stands for 'Not Connected'. There is no other explanation. There is nothing connected to this pin, it is just there to make it a standard 8-pin package.

Counter :

General characteristics

- **Supply:** 3 to 15V, small fluctuations are tolerated.
- **Inputs** have very high impedance (resistance), this is good because it means they will not affect the part of the circuit where they are connected. However, it also means that unconnected inputs can easily pick up electrical noise and rapidly change between high and low states in an unpredictable way. This is likely to make the chip behave erratically and it will significantly increase the supply current. To prevent problems all unused inputs MUST be connected to the supply (either +Vs or 0V), this applies even if that part of the chip is not being used in the circuit!
- **Outputs** can sink and source only about 1mA if you wish to maintain the correct output voltage to drive CMOS inputs. If there is no need to

supply, or 10mA with a 9V supply (just enough to light an LED). To switch larger currents you can connect a transistor.

- **Fan-out:** one output can drive up to 50 inputs.
- **Gate propagation time**: typically 30ns for a signal to travel through a gate with a 9V supply, it takes a longer time at lower supply voltages.
- **Frequency**: up to 1MHz, above that the 74 series is a better choice.
- **Power consumption** (of the chip itself) is very low, a few µW. It is much greater at high frequencies, a few mW at 1MHz for example. There are many ICs in the 4000 series and this page only covers a selection, concentrating on the most useful gates, counters, decoders and display drivers. For each IC there is a diagram showing the pin arrangement and brief notes explain the function of the pins where necessary. The notes also explain if the IC's properties differ substantially from the standard characteristics listed above.

12-stage binary ripple counter

74HC/HCT4040

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4040 are high-speed Si-gate CMOS devices and are pin compatible with "4040" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4040 are 12-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve parallel outputs (Q_0 to Q_{11}). The counter advances on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

APPLICATIONS

- Frequency dividing circuits
- Time delay circuits
- Control counters

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	$\overline{CP}$ to Q_0		14	18	ns
	Q_n to Q_{n+1}		8	8	ns
f_{max}	maximum clock frequency		90	79	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	20	20	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC   the condition is V_I = GND to V_{CC}

For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

12-stage binary ripple counter

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	Q_0 to Q_{11}	parallel outputs
10	$\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
11	MR	master reset input (active HIGH)
16	V_{CC}	positive supply voltage

Fig.1 Pin configuration.

Fig.2 Logic symbol.

Fig.3 IEC logic symbol.
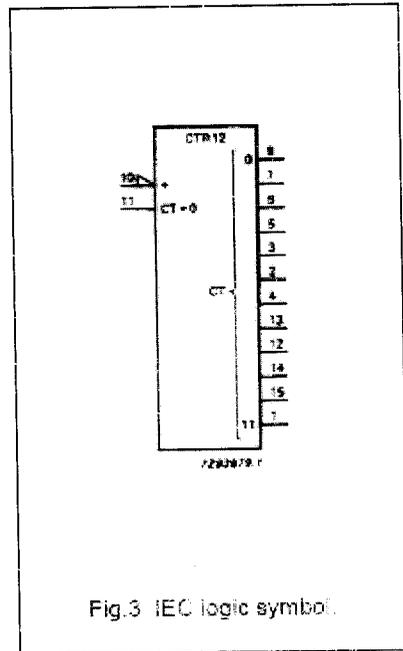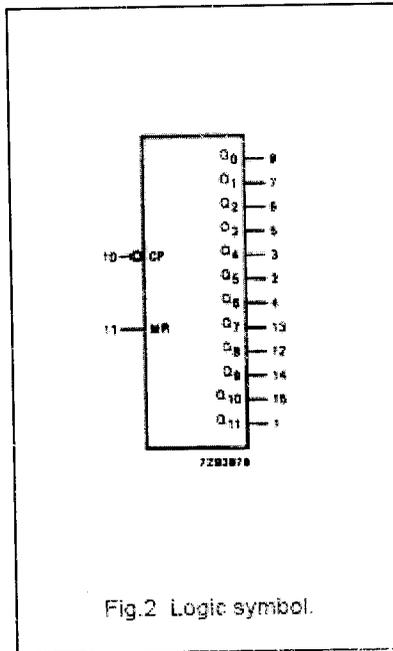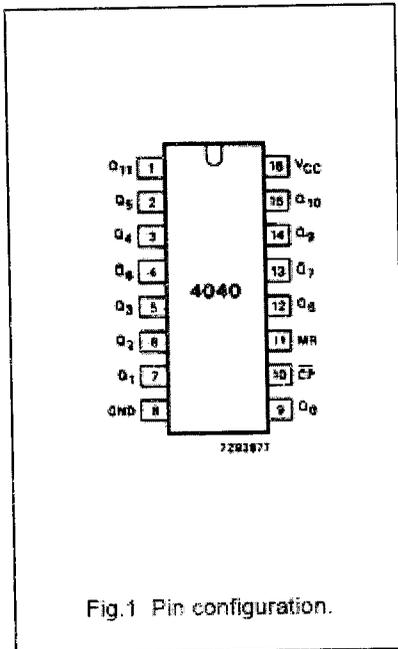
12-stage binary ripple counter

Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	Q_n
↑	L	no change
↓	L	count
X	H	L

Notes

1. H = HIGH voltage level
    L = LOW voltage level
    X = don't care
    ↑ = LOW-to-HIGH clock transition
    ↓ = HIGH-to-LOW clock transition

Fig.5 Logic diagram.

12-stage binary ripple counter

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

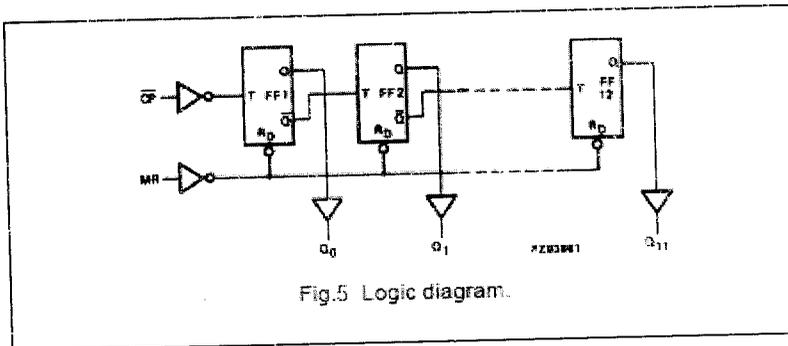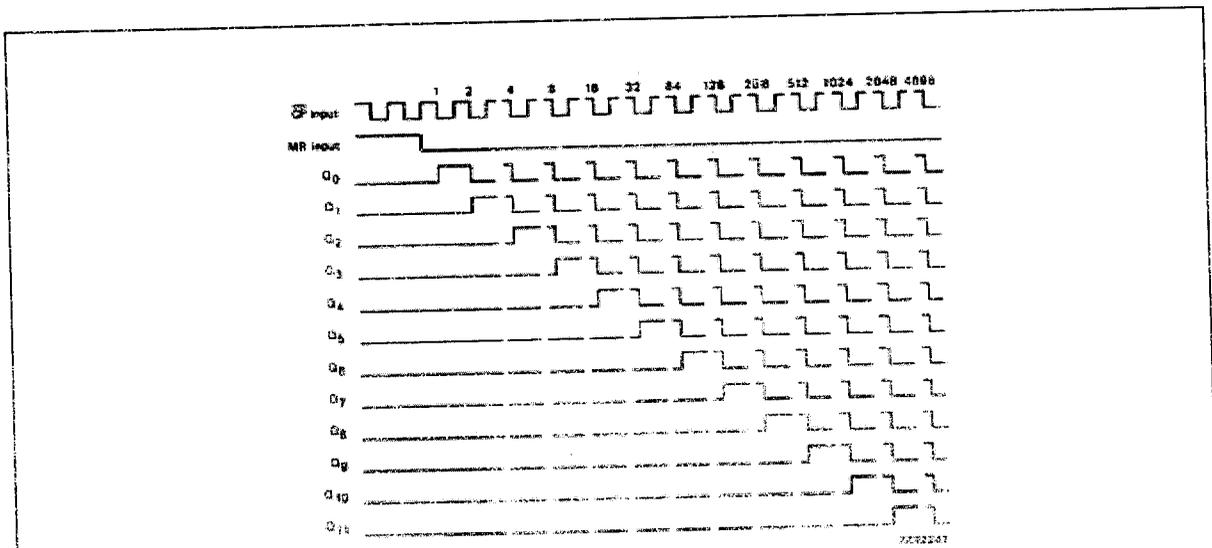| SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{CP}$ to Q_0		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t_{PHL}/ t_{PLH}	propagation delay Q_n to Q_{n+1}		28 10 8	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig.7
t_{PHL}	propagation delay MR to Q_n		61 22 18	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.7
t_W	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_W	master reset pulse width; HIGH	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_{rem}	removal time MR to $\overline{CP}$	50 10 9	8 3 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.7
f_{max}	maximum clock pulse frequency	6.0 30 35	27 62 98		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.7

12-stage binary ripple counter

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see '74HC/HCT/HCU/HCMOS Logic Family Specifications'.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$	0.85
MR	1.10

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HCT							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{CP}$ to Q_0		19	40		50		60	ns	4.5	Fig.7
t_{PHL}/ t_{PLH}	propagation delay Q_n to Q_{n+1}		10	20		25		30	ns	4.5	Fig.7
t_{PHL}	propagation delay MR to Q_n		23	45		56		68	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.7
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig.7
t_W	master reset pulse width; HIGH	16	8		20		24		ns	4.5	Fig.7
t_{rem}	removal time MR to $\overline{CP}$	10	2		13		15		ns	4.5	Fig.7
f_{max}	maximum clock pulse frequency	30	72		24		20		MHz	4.5	Fig.7

FAIRCHILD
SEMICONDUCTOR™

DM7404
Hex Inverting Gates

General Description

This device contains six independent gates each of which
performs the logic INVERT function.

Ordering Code:

Order Number	Package Number	Package Description
DM7404M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
DM7404N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram
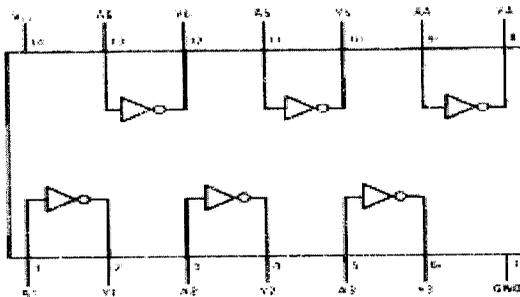
Function Table

$$Y = \overline{A}$$

Inputs	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage   7V

Input Voltage   5.5V

Operating Free Air Temperature Range   0°C to +70°C

Storage Temperature Range   −65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.4	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−18		−55	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		6	12	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		18	33	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			15	ns

APPENDIX 3

ASI

NPN SILICON RF POWER TRANSISTOR

DESCRIPTION:

The **ASI CBSL100** is Designed for

FEATURES:

- Input Matching Network
-
- *Omnigold™* Metalization System

MAXIMUM RATINGS

I_C	25 A
V_{CBO}	60 V
V_{CEO}	30 V
V_{EBO}	3.0 V
P_{DISS}	310 W @ T_C = 25 °C
T_J	-65 °C to +200 °C
T_{STG}	-65 °C to +150 °C
θ_{JC}	0.6 °C/W

PACKAGE STYLE .400 BAL FLG (C)
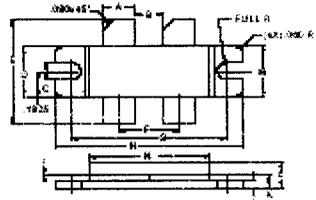
DIM	MINIMUM	MAXIMUM
A	.230 / 5.84	.230 / 5.84
B		.210 / 5.33
C	.120 / 3.06	.130 / 3.30
D	.380 / 9.66	.380 / 9.91
E	.765 / 19.41	.820 / 20.83
F		.435 / 11.06
G		1.095 / 27.84
H	1.335 / 33.91	1.345 / 34.16
I	.003 / 0.08	.007 / 1.18
J	.060 / 1.52	.070 / 1.78
K	.082 / 2.08	.100 / 2.54
L		.205 / 5.21
M	.385 / 10.33	.407 / 10.34
N	.850 / 21.59	.870 / 22.10

ORDER CODE: ASI10585

CHARACTERISTICS T_C = 25 °C

SYMBOL	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
BV_{CBO}	I_C = 100 mA	60			V
BV_{CEO}	I_C = 100 mA	30			V
BV_{EBO}	I_E = 50 mA	3.0			V
I_{CES}	V_{CE} = 28 V			10	mA
h_{FE}	V_{CE} = 5.0 V I_C = 3.0 A	15		70	---
P_G	V_{CE} = 24 V I_{CO} = 2 X 100 mA f = 960 MHz	8.0			dB
IMD	P_{OUT} = 100 W		-32		dBc
η_C		45			%

NPN general purpose transistors

BC546; BC547; BC548

LIMITING VALUES

in accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BC546		–	80	V
	BC547		–	50	V
	BC548		–	30	V
V_{CEO}	collector-emitter voltage	open base			
	BC546		–	65	V
	BC547		–	45	V
	BC548		–	30	V
V_{EBO}	emitter-base voltage	open collector			
	BC546		–	6	V
	BC547		–	6	V
	BC548		–	5	V
I_C	collector current (DC)		–	100	mA
I_{CM}	peak collector current		–	200	mA
I_{BM}	peak base current		–	200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\ °C$; note 1	–	500	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	0.25	K/mW

Note

1. Transistor mounted on an FR4 printed-circuit board.

NPN general purpose transistors

BC546; BC547; BC548

CHARACTERISTICS

$T_j = 25\ °C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0$; $V_{CB} = 30$ V	–	–	15	nA
		$I_E = 0$; $V_{CB} = 30$ V; $T_j = 150\ °C$	–	–	5	μA
I_{EBO}	emitter cut-off current	$I_C = 0$; $V_{EB} = 5$ V	–	–	100	nA
h_{FE}	DC current gain	$I_C = 10\ μA$; $V_{CE} = 5$ V; see Figs 2, 3 and 4				
	BC546A; BC547A; BC548A		–	90	–	
	BC546B; BC547B; BC548B		–	150	–	
	BC547C; BC548C		–	270	–	
h_{FE}	DC current gain	$I_C = 2\ mA$; $V_{CE} = 5$ V; see Figs 2, 3 and 4				
	BC546A; BC547A; BC548A		110	180	220	
	BC546B; BC547B; BC548B		200	290	450	
	BC547C; BC548C		420	520	800	
	BC547; BC548		110	–	800	
	BC546		110	–	450	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\ mA$; $I_B = 0.5\ mA$	–	90	250	mV
		$I_C = 100\ mA$; $I_B = 5\ mA$	–	200	600	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = 10\ mA$; $I_B = 0.5\ mA$; note 1	–	700	–	mV
		$I_C = 100\ mA$; $I_B = 5\ mA$; note 1	–	900	–	mV
V_{BE}	base-emitter voltage	$I_C = 2\ mA$; $V_{CE} = 5$ V; note 2	580	660	700	mV
		$I_C = 10\ mA$; $V_{CE} = 5$ V	–	–	770	mV
C_c	collector capacitance	$I_E = i_e = 0$; $V_{CB} = 10$ V; $f = 1$ MHz	–	1.5	–	pF
C_e	emitter capacitance	$I_C = i_c = 0$; $V_{EB} = 0.5$ V; $f = 1$ MHz	–	11	–	pF
f_T	transition frequency	$I_C = 10\ mA$; $V_{CE} = 5$ V; $f = 100$ MHz	100	–	–	MHz
F	noise figure	$I_C = 200\ μA$; $V_{CE} = 5$ V; $R_S = 2\ kΩ$; $f = 1$ kHz; $B = 200$ Hz	–	2	10	dB

Notes

1. V_{BEsat} decreases by about 1.7 mV/K with increasing temperature.

2. V_{BE} decreases by about 2 mV/K with increasing temperature.

International Rectifier

25TTS.. SERIES

PHASE CONTROL SCR

V_T < 1.25V @ 16A

I_{TSM} = 200A

V_R / V_D = 1200V

Description/Features

The 25TTS.. new series of silicon controlled recti-
fiers are specifically designed for medium power
switching and phase control applications. The
glass passivation technology used has reliable
operation up to 125° C junction temperature.

Typical applications are in input rectification (soft
start) and these products are designed to be used
with International Rectifier input diodes, switches
and output rectifiers which are available in identi-
cal package outlines.

Output Current in Typical Applications

Applications	Single-phase Bridge	Three-phase Bridge	Units
Capacitive input filter T_A = 55°C, T_J = 125°C, common heatsink of 1°C/W	18	22	A

Major Ratings and Characteristics

Characteristics	25TTS..	Units
$I_{T(AV)}$ Sinusoidal waveform	16	A
I_{RMS}	25	A
V_{RRM} / V_{DRM}	800 and 1200	V
I_{TSM}	250	A
V_T @ 16 A. T_J = 25°C	1.25	V
dv/dt	500	V/us
di/dt	150	A/us
T_J	-40 to 125	°C

TO-220AC
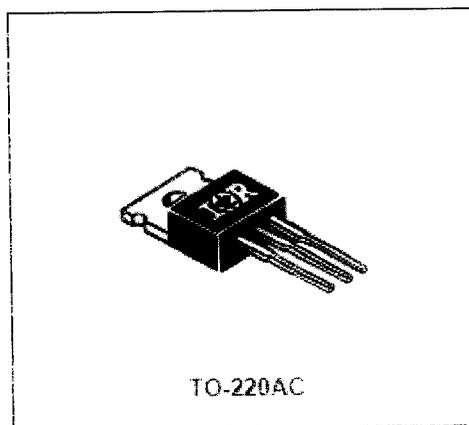
Also available in SMD-220 package (series 25TTS..S)

Voltage Ratings

Part Number	V_{RRM}, maximum peak reverse voltage V	V_{DRM}, maximum peak direct voltage V	I_{RRM}/I_{DRM} 125°C mA
25TTS08	800	800	5
25TTS12	1200	1200	

Absolute Maximum Ratings

Parameters		25TTS..	Units	Conditions
$I_{T(AV)}$	Max. Average On-state Current	16	A	50% duty cycle @ T_C = 90° C, sinusoidal wave form
I_{RMS}	Max. RMS On-state Current	25		
I_{TSM}	Max. Peak One Cycle Non-Repetitive	210		10ms Sine pulse, rated V_{RRM} applied
	Surge Current	250		10ms Sine pulse, no voltage reapplied
I^2t	Max. I^2t for fusing	220	A^2s	10ms Sine pulse, rated V_{RRM} applied
		310		10ms Sine pulse, no voltage reapplied
$I^2\sqrt{t}$	Max. $I^2\sqrt{t}$ for fusing	3100	$A^2\sqrt{s}$	t = 0.1 to 10ms, no voltage reapplied
V_{TM}	Max. On-state Voltage Drop	1.25	V	@ 16A, T_J = 25°C
r_t	On-state slope resistance	12.0	mΩ	T_J = 125°C
$V_{T(TO)}$	Threshold Voltage	1.0	V	
I_{RM}/I_{DM}	Max. Reverse and Direct	0.5	mA	T_J = 25 °C	V_R = rated V_{RRM}, V_{DRM}
	Leakage Current	5.0		T_J = 125 °C	
I_H	Max. Holding Current	100	mA	Anode Supply = 6V, Resistive load, Initial I_T=1A
I_L	Max. Latching Current	200	mA	Anode Supply = 6V, Resistive load
dv/dt	Max. rate of rise of off-state Voltage	500	V/μs	
di/dt	Max. rate of rise of turned-on Current	150	A/μs	

Triggering

Parameters		25TTS..	Units	Conditions
P_{GM}	Max. peak Gate Power	8.0	W	
$P_{G(AV)}$	Max. average Gate Power	2.0		
$+ I_{GM}$	Max. paek positive Gate Current	1.5	A	
$- V_{GM}$	Max. paek negative Gate Voltage	10	V	
I_{GT}	Max. required DC Gate Current to trigger	80	mA	Anode supply = 6V, resistive load, T_J = - 10°C
		45		Anode supply = 6V, resistive load, T_J = 25°C
		20		Anode supply = 6V, resistive load, T_J = 125°C
V_{GT}	Max. required DC Gate Voltage to trigger	2.6	V	Anode supply = 6V, resistive load, T_J = - 10°C
		2.0		Anode supply = 6V, resistive load, T_J = 25°C
		1.0		Anode supply = 6V, resistive load, T_J = 125°C
V_{GD}	Max. DC Gate Voltage not to trigger	0.25		T_J = 125°C, V_{DRM} = rated value
I_{GD}	Max. DC Gate Current not to trigger	2.0	mA	T_J = 125°C, V_{DRM} = rated value

Switching

Parameters		25TTS..	Units	Conditions
t_{gt}	Typical turn-on time	0.9	µs	T_J = 25°C
t_{rr}	Typical reverse recovery time	4		T_J = 125°C
t_q	Typical turn-off time	110		

Thermal-Mechanical Specifications

Parameters			25TTS..	Units	Conditions
T_J	Max. Junction Temperature Range		-40 to 125	°C	
T_{stg}	Max. Storage Temperature Range		-40 to 125		
R_{thJC}	Max. Thermal Resistance Junction to Case		1.1	°C/W	DC operation
R_{thJA}	Max. Thermal Resistance Junction to Ambient		62		
R_{thCS}	Typ. Thermal Resistance Case to Ambient		0.5		Mounting surface, smooth and greased
wt	Approximate Weight		2 (0.07)	g (oz.)	
T	Mounting Torque	Min.	6 (5)	Kg-cm	
		Max.	12 (10)	(lbf-in)	
	Case Style		TO-220AC		

Ordering Information Table

Device Code

25	T	T	S	12
①	②	③	④	⑤
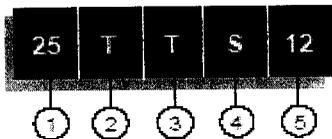
1 - Current Rating, RMS value

2 - Circuit Configuration

    T = Single Thyristor

3 - Package

    T = TO-220AC

4 - Type of Silicon

    S = Converter Grade

5 - Voltage code: Code x 100 = V_{RRM}

08	=	800V
12	=	1200V
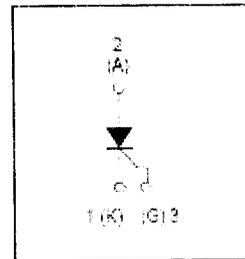
Rectifiers

1N4001G to 1N4007G

FEATURES

- Glass passivated
- High maximum operating temperature
- Low leakage current
- Excellent stability
- Available in ammo-pack.

DESCRIPTION

Rugged glass package, using a high temperature alloyed construction

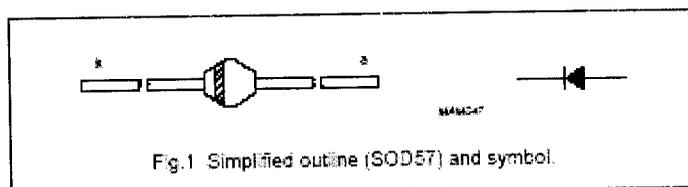This package is hermetically sealed and fatigue free as coefficients of expansion of all used parts are matched.

Fig.1 Simplified outline (SOD57) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V$_{RRM}$	repetitive peak reverse voltage				
	1N4001G		–	50	V
	1N4002G		–	100	V
	1N4003G		–	200	V
	1N4004G		–	400	V
	1N4005G		–	600	V
	1N4006G		–	800	V
	1N4007G		–	1000	V
V$_R$	continuous reverse voltage				
	1N4001G		–	50	V
	1N4002G		–	100	V
	1N4003G		–	200	V
	1N4004G		–	400	V
	1N4005G		–	600	V
	1N4006G		–	800	V
	1N4007G		–	1000	V
I$_{F(AV)}$	average forward current	averaged over any 20 ms period; T$_{amb}$ = 75 °C; see Fig.2	–	1.00	A
		averaged over any 20 ms period; T$_{amb}$ = 100 °C; see Fig.2	–	0.75	A
I$_F$	continuous forward current	T$_{amb}$ = 75 °C; see Fig.2	–	1.00	A
I$_{FRM}$	repetitive peak forward current		–	10	A
I$_{FSM}$	non-repetitive peak forward current	half sinewave; 60 Hz	–	30	A
T$_{stg}$	storage temperature		–65	+175	°C
T$_j$	junction temperature		–65	+175	°C

Rectifiers

ELECTRICAL CHARACTERISTICS

$T_j = 25\,°C$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_F	forward voltage	$I_F = 1\,A$; see Fig.3	1.1	V
$V_{F(AV)}$	full-cycle average forward voltage	$I_{F(AV)} = 1\,A$	0.8	V
I_R	reverse current	$V_R = V_{Rmax}$	10	µA
		$V_R = V_{Rmax}$; $T_{amb} = 100\,°C$	50	µA
$I_{R(AV)}$	full-cycle average reverse current	$V_R = V_{RRMmax}$; $T_{amb} = 75\,°C$	30	µA

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\,j\text{-}tp}$	thermal resistance from junction to tie-point	lead length = 10 mm	48	K/W
$R_{th\,j\text{-}a}$	thermal resistance from junction to ambient	note 1	100	K/W

Note

1. Device mounted on epoxy-glass printed-circuit board, 1.5 mm thick; thickness of copper ≥40 µm, see Fig.4.
   For more information please refer to the "General Part of associated Handbook".

DC COMPONENTS CO., LTD.

RECTIFIER SPECIALISTS

1N 4001A / RL 101
THRU
1N 4007A / RL 107

TECHNICAL SPECIFICATIONS OF SILICON RECTIFIER

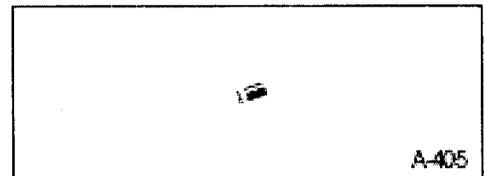### VOLTAGE RANGE - 50 to 1000 Volts   CURRENT - 1.0 Ampere

FEATURES

* High reliability
* Low leakage
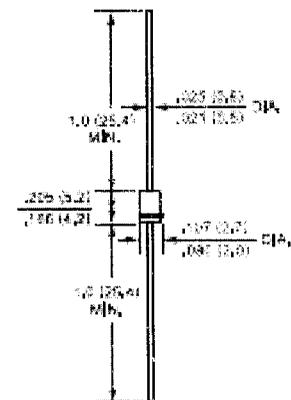* Low forward voltage drop
* High current capability

MECHANICAL DATA

* Case : Molded plastic
* Epoxy: UL 94V-0 rate flame retardant
* Lead: MIL-STD-202E, Method 208 guaranteed
* Polarity: Color band denotes cathode end
* Mounting position: Any
* Weight: 0.22 gram

A-405

Dimensions in inches and (millimeters)

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25 °C ambient temperature unless otherwise specified.
Single phase, half wave, 60 Hz, resistive or inductive load.
For capacitive load, derate current by 20%.

		1N4001A	1N4002A	1N4003A	1N4004A	1N4005A	1N4006A	1N4007A	
	SYMBOL	RL101	RL102	RL103	RL104	RL105	RL106	RL107	UNITS
Maximum Recurrent Peak Reverse Voltage	VRRM	50	100	200	400	600	800	1000	Volts
Maximum RMS Voltage	VRMS	35	70	140	280	420	560	700	Volts
Maximum DC Blocking Voltage	VDC	50	100	200	400	600	800	1000	Volts
Maximum Average Forward Rectified Current at TA = 55°C	IO				1.0				Amps
Peak Forward Surge Current, 8.3 ms single half sine-wave superimposed on rated load (JEDEC Method)	IFSM				30				Amps
Maximum Instantaneous Forward Voltage at 1.0A DC	VF				1.1				Volts
Maximum DC Reverse Current @TA = 25°C at Rated DC Blocking Voltage @TA = 100°C	IR			5.0 / 500					uAmps
Maximum Full Load Reverse Current, Average, Full Cycle .375" (9.5mm) lead length at TL = 75°C					30				uAmps
Typical Junction Capacitance (Note)	CJ				15				pF

REFERENCES:

1. Armensky E V, Falk G B, (1978), "Fractional Horse power Electrical Machines"., MIR publishers.

2. Cyril G Veinott, Joseph E Marten (1987), 4th edition, "Fractional and Sub Fractional Horsepower Electric Motors", McGrawHill Book Company.

3. Edwin P Anderson, (1969)," Audels Electric Motor Guide", D B Taraporevala Sons & Co Pvt Ltd.

4. Gupta J B, (2000),"Theory & Performance of Electrical Machines" S K Kataria & sons.

5. Dr Rai H M, 3rd edition," Principles of Electrical Machine Design", Satyaprakashan.

6. Rombaut C, Seguier G, Bausiere R, (1987);"power electronic converters: A/C-A/C conversion"., vol 2, North Oxford academic.

7. Roy Choudhury D,Shail Jain,(2001),"Linear Integrated Circuits", New Age International (P) Ltd, publishers.

8. Sawhney A K, (2003);"A Course in Electrical Machine Design", Dhanpat rai & Co.

9. Shanmuga Sundaram A, Gangadharan G, Palani R, (1985);"electrical machine design data book"., Wiley eastern.

10. Singh M D, Khanchandani K B, (1998),"Power Electronics", Tata McGraw Hill publishing company Ltd.