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Design and Implementation of Impedance Source Inverter for UPS Application



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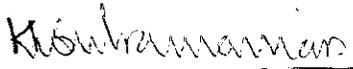
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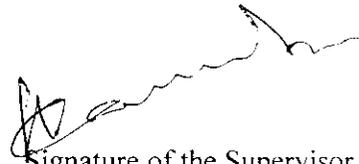
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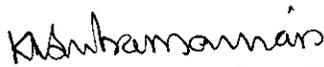
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ABSTRACT

This project introduces an Impedance Source and control to the three phase inverter of uninterrupted power supply which has become an indispensable element of many data processing installations, from desktop PCs to mainframe computer systems.

This new design replaces the existing voltage source and current source inverters which are having the following disadvantages. Since the Voltage source inverter is a buck converter, the obtainable output voltage is limited below the input line voltage. Voltage sags can interrupt the system and shut down critical loads and processes. Inrush and harmonic current from diode rectifier can pollute the line. Low power factor is another issue of the traditional system. Also performance and reliability are compromised by the V-source inverter structure.

Even current source inverters cannot be a better option because it's a boost converter. Both traditional inverters are disadvantageous in terms of reliability, cost, power factor etc.,.

This Impedance source employs a unique LC-Network in the DC link and an input capacitor on the ac side of the diode rectifier. By controlling the shoot through duty cycle, it can produce any desired output ac voltage even greater than the line voltage. It provides ride-through capability during voltage sags, reduces line harmonics, improves power factor, reliability and extends output voltage range.

ஆய்வுச்சுருக்கம்

சாதாரண மேசைக் கணினி முதல் மெயின் ஃபிரேம் கணினி வரை பல டேட்டா பிராஸஸிங் நிறுவதல்களில் தவிர்க்க இயலாத பகுதியாகிவிட்ட தடைப்படா மின் அளிப்பானின், மூன்று நிலை நேர்திசை மின்னோட்ட மாற்றிக்கான ஒரு இம்பிடன்ஸ் மூலமும் அதற்கான கட்டுப்பாட்டு முறையும் இச்செயல் திட்டத்தில் வடிவமைக்கப்பட்டு உருவாக்கப்பட்டுள்ளன.

இந்த புதிய வடிவமைப்பு பின்வரும் குறைபாடுகளை கொண்டுள்ள, ஏற்கனவே உபயோகத்தில் இருக்கும் மின்னழுத்த மூல மற்றும் மின்னோட்ட மூல நேர்திசை மின்மாற்றிகளுக்கு சிறந்த மாற்றாக அமைகிறது. மின்னழுத்த மூல மின்மாற்றியானது குறைக்கும் மின்மாற்றியாதலால் பெறக்கூடிய வெளியீடு மின்னழுத்தமானது உள்ளீடு மின்னழுத்தத்திற்கும் குறைவாக கட்டுப்படுத்தப்படுகிறது. டையோடு மின்னழுத்த மாற்றியிலிருந்து வரும் இன்ரஷ் மற்றும் ஹாட்மோனிக் மின்னோட்டமானது உள்ளீடு மின்னழுத்தத்தை இடையூறு செய்யக் கூடும். ஏற்கனவே உபயோகத்திலுள்ள மின்மாற்றிகளில் உள்ள மற்றொரு குறை அவற்றின் குறைவான பவர் ஃபேக்டர் ஆகும். செயலாற்றல் மற்றும் நம்பகத்தன்மை ஆகியவையும் இவற்றில் விடுபட்டுள்ள அம்சங்களாகும்.

உள்ளீடு மின்னழுத்தத்தை கூட்டும் திறன் மட்டுமே கொண்டுள்ள மின்மாற்றியாக இருப்பதனால், மின்னோட்ட மூல மின்மாற்றியும் கூட இதற்கு சிறந்த மாற்றாக இருக்க முடியாது. உபயோகத்திலுள்ள இரண்டு மின்மாற்றிகளுமே நம்பகத்தன்மை, விலை, பவர் ஃபேக்டர் ஆகியவற்றை பொறுத்தமட்டில் குறைபாடு உள்ளவையாகவே இருக்கின்றன.

இந்த இம்பிடன்ஸ் மூலமானது ஒரு தனித்தன்மைமிக்க எல்.சி. அமைப்பை இதன் டி.சி. இணைப்பிலும், ஒரு உள்ளீடு மின்தேக்கியை டையோடு மாறுதிசை மின்னோட்ட மாற்றியின் ஏ.சி. பக்கத்திலும் இருத்தி உள்ளது. ஷூட் த்ரூ டியூட்டி சைக்கிளை கட்டுப்படுத்துவதன் மூலமாக, விரும்பும் எந்த வெளியீடு மின்னழுத்தத்தையும், உள்ளீடு மின்னழுத்தத்தை காட்டிலும் அதிகமான மின்னழுத்தத்தை கூட பெற முடியும். இந்த அமைப்பு உள்ளீடு மின்னழுத்தத்தில் திடீர் தொய்வு ஏற்படும் போது அதை சமாளிக்கும் திறனைக் கொண்டுள்ளதுடன், பவர் ஃபேக்டரையும், நம்பகத்தன்மையையும் அதிகரிக்கிறது. மேலும் வெளியீடு மின்னழுத்தத்தின் அளவின்மையும் விரிவாக்கப்படும்.

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LIST OF SYMBOLS AND ABBREVIATIONS

S.No	SYMBOL/ABBREVIATION	DESCRIPTION
1.	V_{c1}	Voltage in capacitor C1
2.	V_{c2}	Voltage in capacitor C2
3.	V_{L1}	Voltage induced in inductor L1
4.	V_{L2}	Voltage induced in inductor L2
5.	V_d	DC voltage from rectifier
6.	V_i	Voltage to inverter
7.	V_o	Output Voltage
8.	M, m	Modulation index
9.	B	Boost factor
10.	B_b	Buck boos factor
11.	V_s	Supply Voltage
12.	f_c	Carrier frequency
13.	f_0	Output frequency
14.	A_c	Amplitude of carrier wave
15.	A_r	Amplitude of reference wave
16.	mf	Frequency modulation ratio
17.	μH	Micro Henry (Unit of inductance)
18.	μF	Micro Farad (unit of capacitance)
19.	$V_{o(t)}$	Instantaneous output voltage
20.	δ	Pulse width
21.	P	Number of Pulses
22.	ZSI	Impedance Source Inverter
23.	CSI	Current Source Inverter
24.	VSI	Voltage Source Inverter
25.	DC	Direct Current
26.	AC	Alternating Current
27.	$MOSFET$	Metal Oxide Semi Conductor Field Effect Transistor
28.	$IGBT$	Insulated Gate Bipolar Junction

S.No	SYMBOL/ABBREVIATION	DESCRIPTION
29.	<i>LCD</i>	Liquid Crystal Display
30.	<i>UPS</i>	Uninterruptible Power Supply
31.	<i>EMI</i>	Electro Magnetic Interference
32.	<i>PWM</i>	Pulse Width Modulation
33.	<i>ADC</i>	Analog to Digital Converter

CHAPTER 1

INTRODUCTION

1.1 GENERAL

An Inverter is a circuit which converts a DC input into an AC output. Traditionally there are two inverters available. They are voltage source inverter and current source inverter. Each inverter has six switches in the main circuit. These switches are power switches with anti-parallel diodes. These diodes are to provide bidirectional current flow and reverse voltage blocking capability.

Traditional inverters having following limitations

- They can be operated either as a Buck or a Boost inverter and cannot be operated as a buck-boost inverter.
- Their output voltage range is limited to either greater or smaller than the input voltage.
- Their main circuit is not inter changeable. In other words the voltage source inverter can not be used as the current source inverter and vice versa.
- They are vulnerable to EMI noise which affects their reliability.

The above limitations can be rectified by an impedance source inverter and we can get higher efficiency. This concept can be applied for all AC to DC, AC to AC, DC to DC, DC to AC power conversions.

1.2 OBJECTIVE

The Primary Objective of this project is to implement an impedance source to the three phase inverter for UPS applications. This inverter can buck as well as boost the input voltage, minimize the component count, increase the efficiency and reduce the cost.

This project focuses on the development of an impedance source inverter system and control for uninterruptible power supply applications (UPS) which have become an indispensable element of many data processing installations, from desktop PCs to mainframe computer systems.

This system employs a unique LC-Network in the DC link and an input capacitor on the ac side of the diode rectifier front end. By controlling the shoot through duty cycle it can produce any desired output ac voltage even greater than the line voltage. It provides ride-through capability during voltage sags, reduces line harmonics, improves power factor and reliability and extends output voltage range.

Methodology

- The Impedance source Inverter circuit was simulated using MATLAB Simulink tool and the desired voltage and current outputs for nominal input voltage and voltage with 50% sag were obtained.
- The hardware for Impedance source Inverter was implemented and the outputs were verified with simulation results. For generating pulses to trigger the inverter switches, PWM technique is adopted and controlled by PIC Microcontroller.

1.3 ORGANISATION

This thesis has been organized into seven chapters.

Chapter 1 gives introduction to Inverters and the objective of this project and the way the various chapters are organized

Chapter 2 focuses on the traditional inverters and their disadvantages.

Chapter 3 explains the impedance source inverter, its advantages and how this can be implemented in UPS

Chapter 4 provides the analysis and design of this impedance network.

Chapter 5 shows the Matlab simulation circuit of the Impedance source inverter and the output waveforms.

Chapter 6 describes the hardware implementation of the impedance source inverter

Chapter 7 concludes the project with recommendations for future work

CHAPTER 2

INVERTER

2.1 TRADITIONAL INVERTERS

Traditional inverters are voltage source inverter and current source inverter. Voltage source inverter is the one which the dc source has small or negligible impedance. In other words a voltage source inverter has stiff dc source voltage at its input terminals. The switching device can be a conventional MOSFET, thyristor or a power transistor.

A current source inverter is fed with adjustable dc current source. In current source inverter output current waves are not affected by the load.

2.2 VOLTAGE SOURCE INVERTER [VSI]

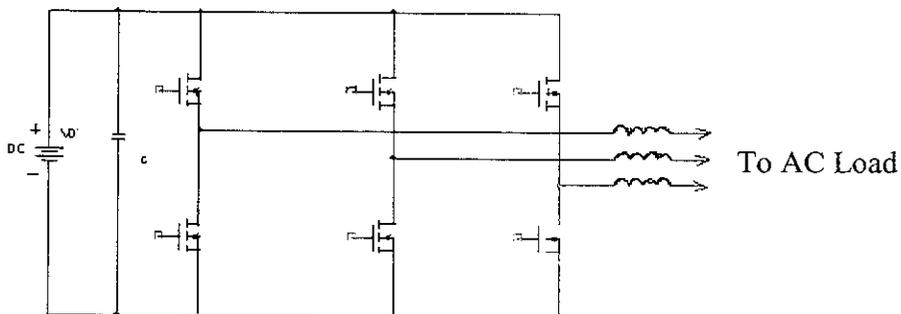


Figure 2.1 Voltage Source Inverter

Figure 2.1 shows the traditional three-phase voltage-source inverter structure. A dc voltage source supported by a relatively large capacitor feeds the main inverter circuit, a three-phase bridge. The dc voltage source can be a battery, fuel-cell stack or a diode rectifier.

Six switches are used in the main circuit; each is traditionally composed of a power transistor and an anti parallel diode to provide bidirectional current flow and unidirectional voltage blocking capability.

The V-source inverter is widely used however; it has the following conceptual limitations.

2.2.1 Limitations Of Voltage Source Inverter

The V-source inverter is a buck (step down) inverter for dc-to-ac power conversion. For applications where over drive is desirable and the available dc voltage is limited, an additional dc-dc boost (step up) stage is needed to obtain a desired ac output. The additional power converter stage increases system cost and lowers efficiency.

The upper and lower devices of each phase leg cannot be gated on simultaneously either by purpose or by EMI noise. Otherwise, a shoot-through would occur and destroy the devices[2]. The shoot-through problem by electromagnetic interference (EMI) noise's mis gating-on is a major killer to the inverter's reliability. Dead time to block both upper and lower devices has to be provided in the V-source inverter, which causes waveform distortion, etc. An output *LC* filter is needed for providing a sinusoidal voltage compared with the current-source inverter, which causes additional power loss and control complexity.

Voltage sags can interrupt an the system and shutdown critical loads and processes. Over 90% of power quality related problems are from momentary voltage sags of 10–50% below nominal Voltage[3]. The dc capacitor in VSI is a relatively small energy storage element, which cannot hold dc voltage above the operable level under such voltage sags. Lack of ride-through capacity is a serious problem for sensitive loads .

The ASD(Adjustable speed drives) industry provides options using fly back converter or boost converter with energy storage or diode rectifier to achieve ride-through; however, these options come with penalties of cost, size/weight, and complexity.

Inrush and harmonic current from the diode rectifier can pollute the line. Low power factor is another issue of the traditional inverters.

2.3 CURRENT SOURCE INVERTER [CSI]

Figure 2.2 shows the traditional three-phase current-source inverter structure. A dc current source feeds the main converter circuit, a three-phase Bridge. The dc current source can be a relatively large dc inductor fed by a voltage source such as a battery, fuel-cell stack, diode rectifier, or thyristor converter.

Six switches are used in the main circuit; each is traditionally composed of a semiconductor switching device with reverse block capability such as a gate-turn-off thyristor (GTO) and SCR or a power transistor with a series diode to provide unidirectional current flow and bidirectional voltage blocking.

However, the I_c -source inverter has the following conceptual and theoretical barriers and limitations.

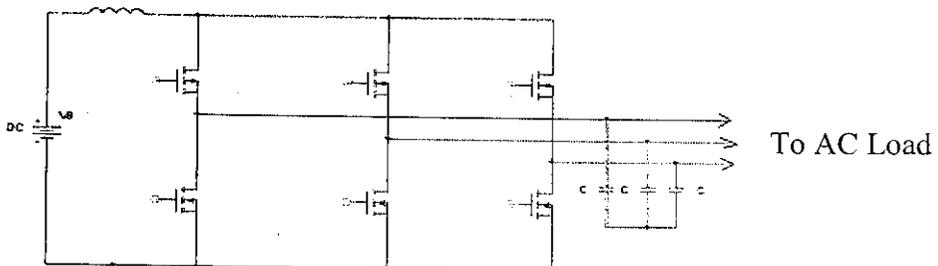


Figure 2.2 Current Source Inverter

2.3.1 Limitations Of Current Source Inverter

The ac output voltage has to be greater than the original dc voltage that feeds the dc inductor or the dc voltage produced is always smaller than the ac input voltage.

For applications where a wide voltage range is desirable, an additional dc–dc boost stage is needed. The additional power conversion stage increases system cost and lowers efficiency.

At least one of the upper devices and one of the lower devices have to be gated on and maintained on at any time. Otherwise, an open circuit of the dc inductor would occur and destroy the devices. The open-circuit problem by EMI noise's mis gating-off is a major concern of the converter's reliability[2]. Overlap time for safe current commutation is needed in the I-source converter, which also causes waveform distortion, etc.

The main switches of the I-source inverter have to block reverse voltage that requires a series diode to be used in combination with high-speed and high-performance transistors such as insulated gate bipolar transistors (IGBTs). This prevents the direct use of low-cost and high-performance IGBT modules .In addition, both the V-source inverter and the I-source inverter have the following common limitations.

2.4 LIMITATIONS OF TRADITIONAL INVERTERS

Their obtainable output voltage range is limited to either greater or smaller than the input voltage .Their main circuits cannot be interchangeable. In other Words, neither the V-source inverter main circuit can be used for the I-source inverter, nor vice versa. They are vulnerable to EMI noise.

2.5 COMPARISON OF VSI AND CSI

TABLE 2.1

COMPARISON OF VOLTAGE & CURRENT SOURCE INVERTERS

S.NO	CURRENT SOURCE INVERTER	VOITAGE SOURCE INVERTER
1	A inductor is used in the dc link the source impedance is high. It provides constant current	A capacitor is used in the dc link, it provides constant voltage source
2	A current source inverter is capable of withstanding short circuit across any two of its output terminals. Hence momentary short circuit on load and short circuit of switches are acceptable	A VSI is more dangerous situation as the parallel capacitor feeds more powering to the fault.
3	It is used only buck or boost operation inverter	It is also used in only buck or boost operation
4	The main circuits cannot be interchanged.	The main circuit cannot interchanged
5	It is affected by the EMI	It is effected by the EMI

CHAPTER 3

IMPEDANCE SOURCE INVERTER

3.1.IMPEDANCE SOURCE INVERTER

This is an inverter which is supplied by an Impedance source. In voltage source inverter the stiff dc supply is provided by a battery in parallel with a capacitor. In current source inverter the constant direct current is provided by a battery in series with an inductor. But in Impedance Source Inverter the DC source is provided by the cross combination of both Capacitors and Inductors

3.2 ADVANTAGES OF THE IMPEDANCE SOURCE NETWORK

- The impedance source inverter concept can be applied in all ac-ac, dc-dc, ac-dc, dc-ac power conversion.
- The output voltage range not limited.
- The impedance source inverter is used as a buck- boost inverter.
- The impedance source inverter does not affect the electromagnetic interference noise.
- The impedance source inverter cost is low.
- The impedance source inverter provides the buck- boost function by two stage power conversion

3.3 UNINTERRUPTIBLE POWER SUPPLY

The AC power supplies are commonly used as standby sources for critical loads and in applications where normal AC supplies are not available. The standby power supplies are also known as uninterruptible power supply(UPS) system

The block diagram of UPS is shown in figure 3.1. The load is normally supplied from the ac main supply and the rectifier maintains the full charge of the battery. If the supply fails , the load is switched to the output of the inverter, which then takes over the main supply. Here the inverter is either voltage source inverter or current source inverter.

This inverter part can be replaced with this new Impedance Source Inverter which is more advantageous than the other two traditional inverters.

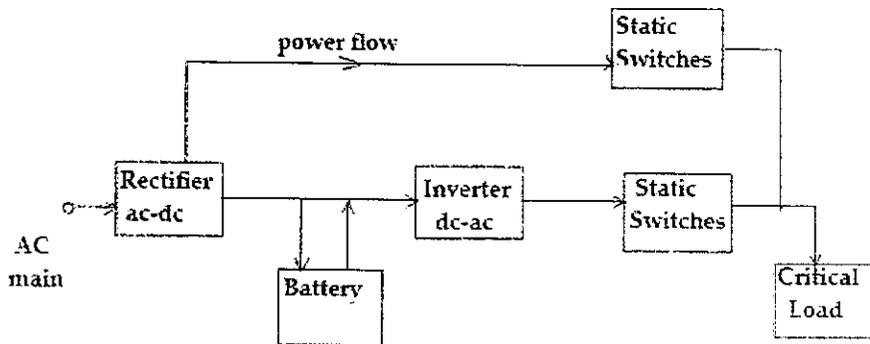


Figure 3.1 UPS Block diagram

The two configurations commonly used in UPS are given below.

- 1) Load normally connected to ac main supply.
- 2) Load normally connected to inverter

In the first case the inverter runs only during the time when the supply failure occurs. Where as in the second case inverter operates continuously and its output is connected to the load. There is no need for breaking the supply in the event of supply failure.

In either case this new type of inverter can perform well without shutting down the critical loads during voltage sags.

3.4. BLOCK DIAGRAM OF IMPEDENCE SOURCE INVERTER

To overcome the limitations of the traditional V-source and I-source inverter, this thesis deals an impedance-source inverter [1] and its control method for implementing dc-to-ac power conversion. This thesis also deals with how to overcome the limitations of voltage source inverter and current source inverter.

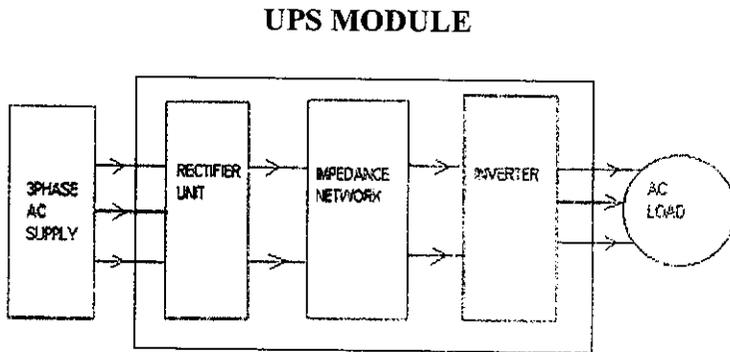


Figure 3.2 Block diagram of Impedance Source Inverter

The proposed impedance source inverter block diagram is shown in figure 3.2. It consists of a voltage source from the rectifier supply, an impedance network, a three-phase inverter, and an AC load. AC voltage is rectified to DC voltage by the rectifier. In the rectified output DC voltage is fed to the impedance network.

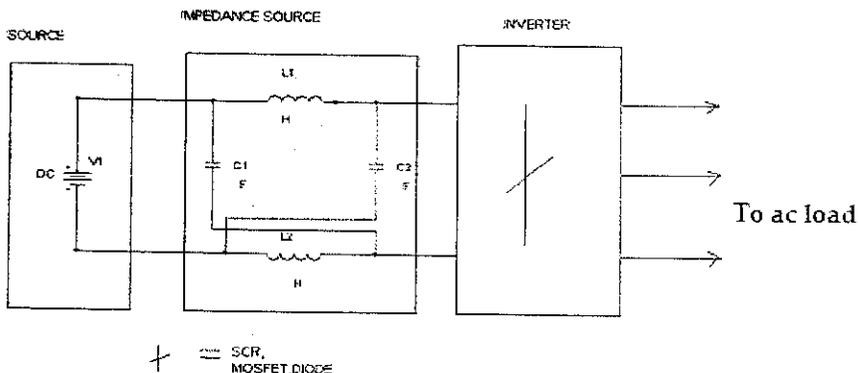


Figure 3.3 Impedance Source Inverter

Figure 3.3 show the proposed impedance source inverter diagram. It employs a unique impedance network to couple the inverter main circuit to the power source and load for providing unique features that cannot be observed in the traditional Voltage and current source inverter where a capacitor and inductor are used respectively. The impedance source inverter overcomes the above-mentioned conceptual and theoretical barriers.

In Figure.3.3, a two-port network that consists of a split-inductor and capacitors are connected in X shape is employed to provide an impedance source coupling the inverter to the dc source .The dc source can be either a voltage or a current source. Therefore, the dc source can be a battery, diode rectifier, thyristor converter, fuel cell. Switches used in the inverter can be a combination of switching devices and diodes.

3.5. THREE PHASE IMPEDANCE SOURCE INVERTER

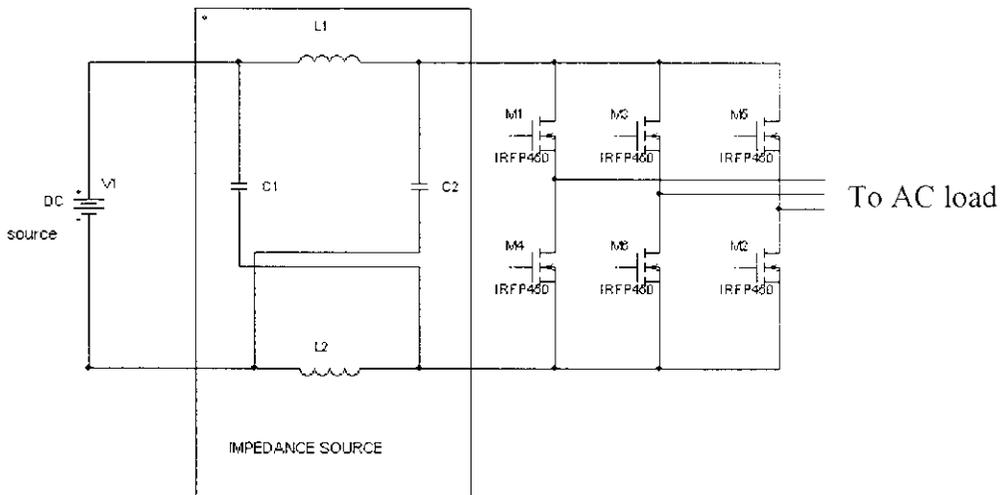


Figure 3.4 Three Phase Impedance Source Inverter

Figure 3.4 show the three-phase impedance source inverter configuration. The inductance can be provided through a split inductor or two separate inductors. The impedance concept [1] can be applied to all dc-to-ac power conversion. To

describe the operating principle and control, this thesis focuses on an application example of the impedance-source inverter .

3.6 IMPEDANCE SOURCE INVERTER FOR UPS

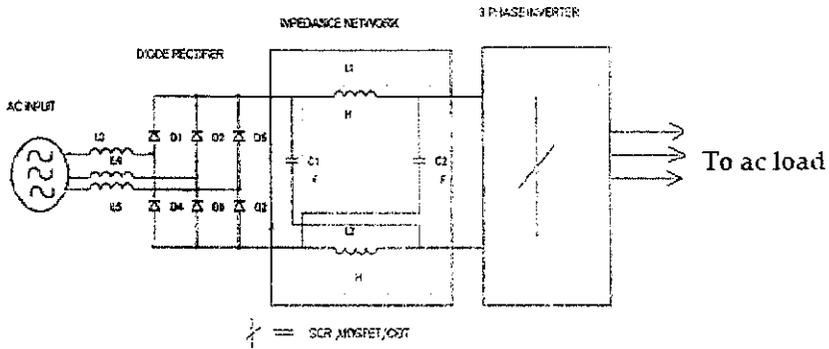


Figure 3.5 Impedance Source Inverter for UPS

The proposed impedance source inverter for UPS is shown in Figure.3.5 which can directly produce an AC voltage greater and less than the DC input voltage.

CHAPTER 4

ANALYSIS AND DESIGN OF THE IMPEDANCE NETWORK

4.1 EQUIVALENT CIRCUIT, OPERATING PRINCIPLE, AND CONTROL

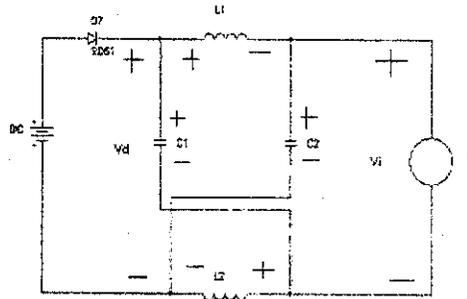


Figure 4.1 Equivalent Circuit of Impedance Source Inverter

The unique feature of the impedance-source inverter is that the output ac voltage can be any value between zero to infinity regardless of the DC voltage. That is, the Impedance-source inverter is a buck–boost inverter that has a wide range of obtainable voltage. The traditional Voltage and current source inverters cannot provide such feature[6] . To describe the operating principle and control of the impedance-source inverter in Figure 4.1, let us briefly examine the impedance-source inverter structure.

The three-phase impedance-source inverter bridge has nine permissible switching states unlike the traditional three-phase Voltage source inverter that has eight[9]. The traditional three-phase Voltage source inverter has six active vectors when the dc voltage is impressed across the load and two zero vectors when the load terminals are shorted through either the lower or upper three devices, respectively. However, the three-phase impedance-source inverter bridge has one extra zero state.

When the load terminals are shorted through both the upper and lower devices of any one phase leg any two phase legs, or all three phase legs .This shoot-through zero state is forbidden in the traditional Voltage source inverter because it would

We call this third zero state the shoot-through zero state, which can be generated by seven different ways: shoot-through via any one phase leg, combinations of any two phase legs, and all three phase legs. The impedance-source network makes the shoot-through zero state possible.

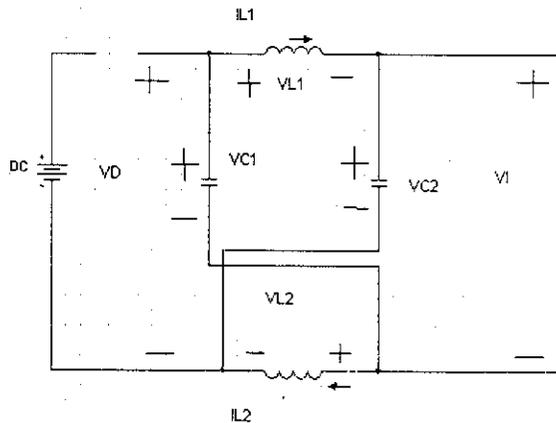


Figure 4.2 Equivalent circuit of the impedance-source inverter viewed from the dc link.

The inverter bridge is equivalent to a short circuit when the inverter bridge is in the shoot-through zero state, as shown in Figure 4.1, whereas the inverter bridge becomes an equivalent current source as shown in Figure 4.2.

When in one of the six active states. Note that the inverter bridge can be also represented by a current source with zero value (i.e., an open circuit) when it is in one of the two traditional zero states. Therefore, Figure 4.2 shows the equivalent circuit of the impedance-source inverter viewed from the dc link when the Inverter Bridge is in one of the eight non shoot-through switching states[6]. All the traditional pulse width-modulation (PWM) schemes can be used to control the impedance-source inverter and their theoretical input-output relationships still hold.

4.2 CIRCUIT ANALYSIS AND OBTAINABLE OUTPUT VOLTAGE

From the impedance–source equivalent circuits we have

$$V_{c1}=V_{c2}=V_c; V_{l1}=V_{l2}=V_l \quad (1)$$

Given the inverter bridge is in the shoot through zero state for an interval of T_0 , during a switch cycle, T and from the equivalent circuit, fig 4.2 one has

$$V_l=V_c; V_d=2V_c; V_i=0; \quad (2)$$

Now consider that the inverter bridge is in one of the eight Non –shoot through states for an interval of T_1 , during the Switching cycle T . From the equivalent circuit

$$V_l=V_o-V_c; V_d=V_o; V_i=V_c-V_l=2V_c-V_o \quad (3)$$

Where V_o is the dc source voltage and $T=T_0+T_1$

The average voltage of the inductors over one switching Period (T) should be zero in steady state, from (2) and (3). We have

$$V_l(av)=[T_0.V_c-T_1(V_o-V_c)]/T=0 \quad (4)$$

$$V_c/V_o = T_1 / (T_1-T_0) \quad (5)$$

Similarly, the average dc-link voltage across the inverter bridge can be found as follows:

$$V_i=V_i(av)=[T_0.0+T_1(2V_c-V_o)]/T=[T_1/(T_1-T_0)]V_o=V_c \quad (6)$$

The peak dc link voltage across the inverter bridge is expressed in equation 3 and it can be rewritten as

$$V_i=V_c-V_l=2V_c-V_o=[T/(T_1-T_0)]V_o=B.V_o \quad (7)$$

Where

$$B=T/(T_1-T_0)=1/[1-2(T_0/T)] \geq 1 \quad (8)$$

B =Boost factor resulting from the shoot through zero state.

The peak dc link voltage V_i is the equivalent dc link voltage of the inverter.

The output peak phase voltage from the inverter can be expressed as

$$V_{ac}=m.(V_i/2) \quad (9)$$

where m is the modulation index.

Substituting equation (7) in equation (9) gives

$$V_{ac} = m \cdot B \cdot (V_o/2) \quad (10)$$

In traditional voltage source PWM inverter, we have the well known relationship $V_{ac} = m \cdot (V_o/2)$. Equation (10) can be modified into

$$V_{ac} = Bb(V_o/2)$$

Where $Bb =$ Buck boost factor

$$Bb = m \cdot B$$

From the above equation the output voltage can be stepped up and stepped down by choosing an appropriate buck-boost factor Bb .

$$Bb = m \cdot B \quad (B \text{ ranges from } 0 \text{ to infinity})$$

The buck-boost factor is determined by the modulation index and boost factor. The boost factor as expressed it can be controlled by duty cycle (i.e., interval ratio) of the shoot-through zero state over the no shoot-through states of the inverter PWM. Note that the shoot-through zero state does not affect the PWM control of the inverter, because it equivalently produce the same zero voltage to the load terminal.

The available shoot through period is limited by the zero-state period that is determined by the modulation index. The impedance source network should require less capacitance and smaller size compared with the traditional Voltage source inverter. Similarly, when the two capacitors are small and approach zero, the impedance source network reduces to two inductors in series and becomes a traditional current source[3]. Therefore, a traditional current source inverter's inductor requirements and physical size is the worst case requirement for the inverter source network.

Considering additional filtering and energy storage by the capacitors, the impedance-source network should require less inductance and smaller size compared with the traditional I-source inverter.

CHAPTER 5

SIMULATION CIRCUIT AND RESULTS OF THE IMPEDANCE SOURCE INVERTER

5.1 MATLAB SIMULINK MODEL FOR IMPEDANCE SOURCE INVERTER

Simulations have been performed to confirm the above analysis. Figure.5.1 shows the main circuit configuration of impedance source inverter for AC drive. The impedance source network parameters are $L1 = L2 = L = 160mH$ and $C1 = C2 = C = 1000\mu F$.

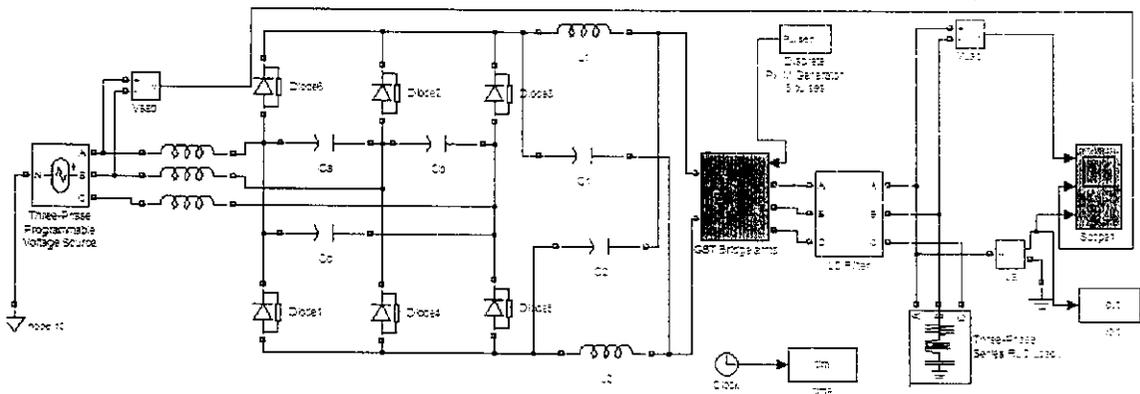


Figure 5.1 Circuit Diagram of Impedance Source Inverter For UPS

5.2 SIMULATED RESULTS FOR NOMINAL INPUT VOLTAGE

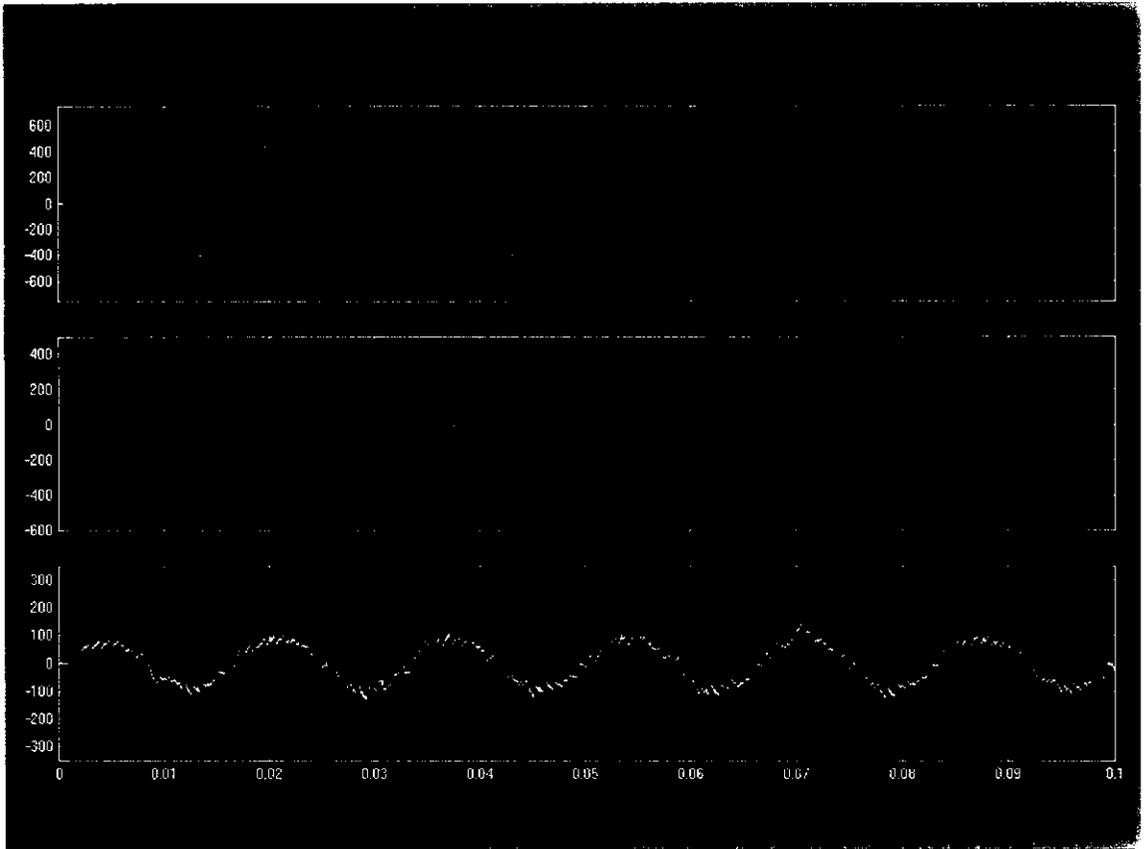


Figure 5.2 Output Voltage, Input Voltage and Output Current Wave forms for nominal input voltage

Figure 5.2 shows the simulated wave forms of output voltage under nominal input voltage, input voltage and output current .

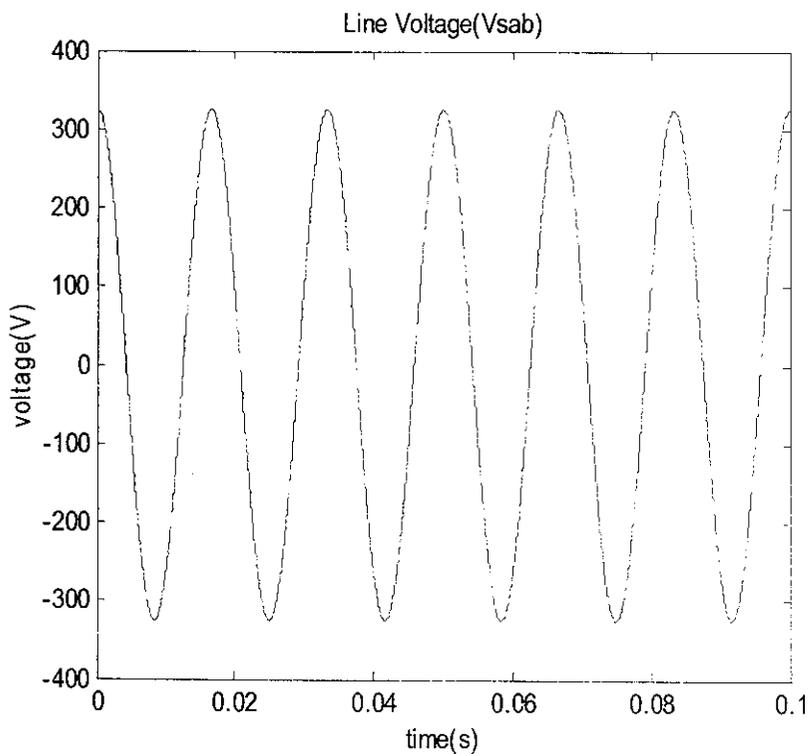


Figure 5.3 Input Voltage Wave form (Nominal input voltage)

Figure shows the input voltage that is 230v nominal AC voltage.

Figure 5.4 and 5.5 are showing the output voltage and current respectively for nominal input voltages. Here we can see that the output voltage can be obtained without any loss in input voltage.

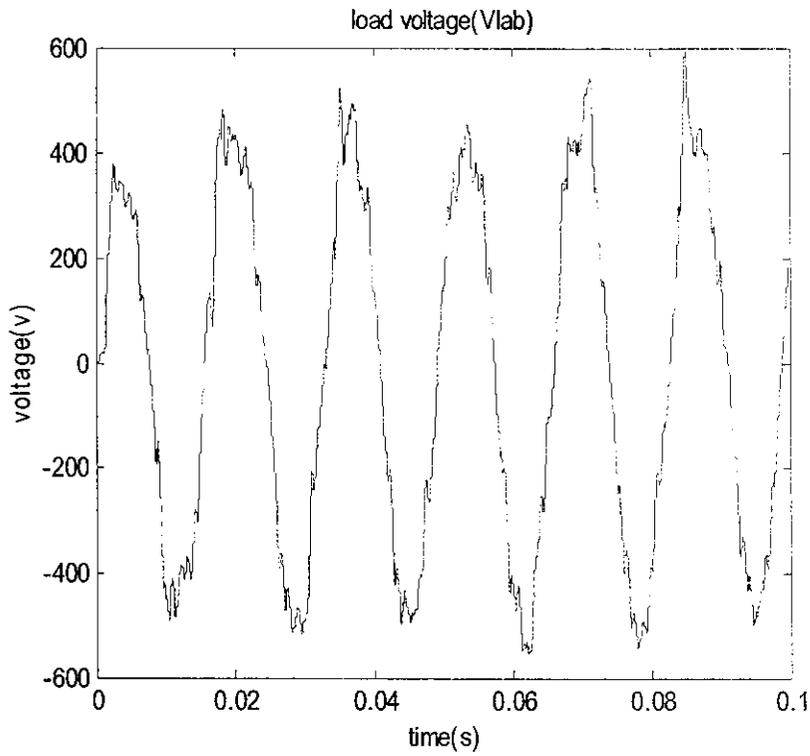


Figure 5.4 Output Voltage Wave form (For Nominal input voltage)

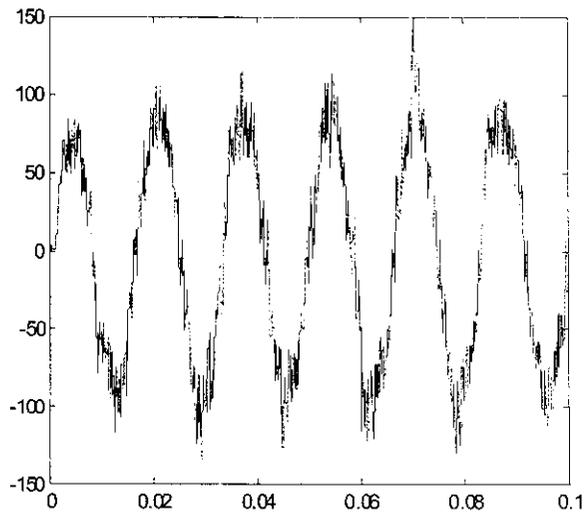


Figure 5.5 Output Current Wave form (For Nominal input voltage)

5.3 SIMULATED RESULTS FOR INPUT WITH 50% VOLTAGE SAG

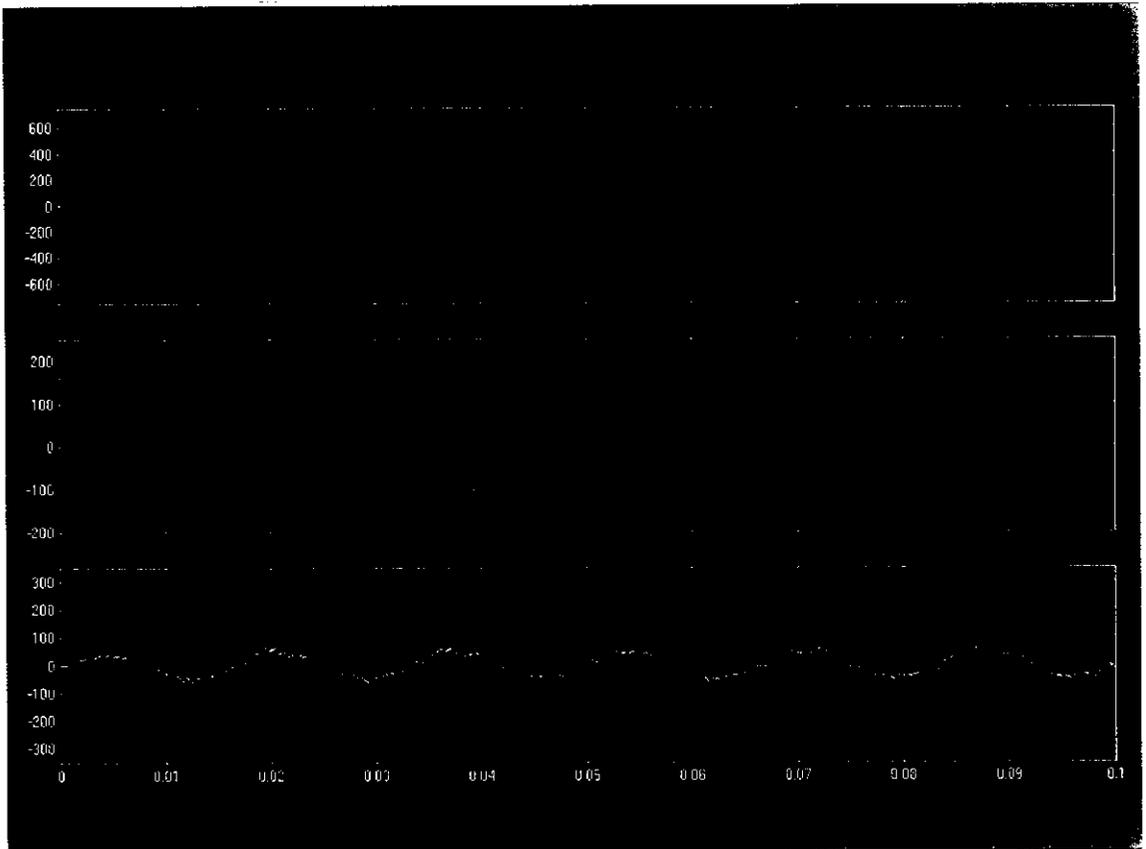


Figure 5.6 Output Voltage, Input Voltage and Output Current Wave forms for 50% sag

Fig 5.6 shows the simulated wave forms for output voltage ,input voltage and output current for 50% sag of nominal voltage that is 115v AC supply

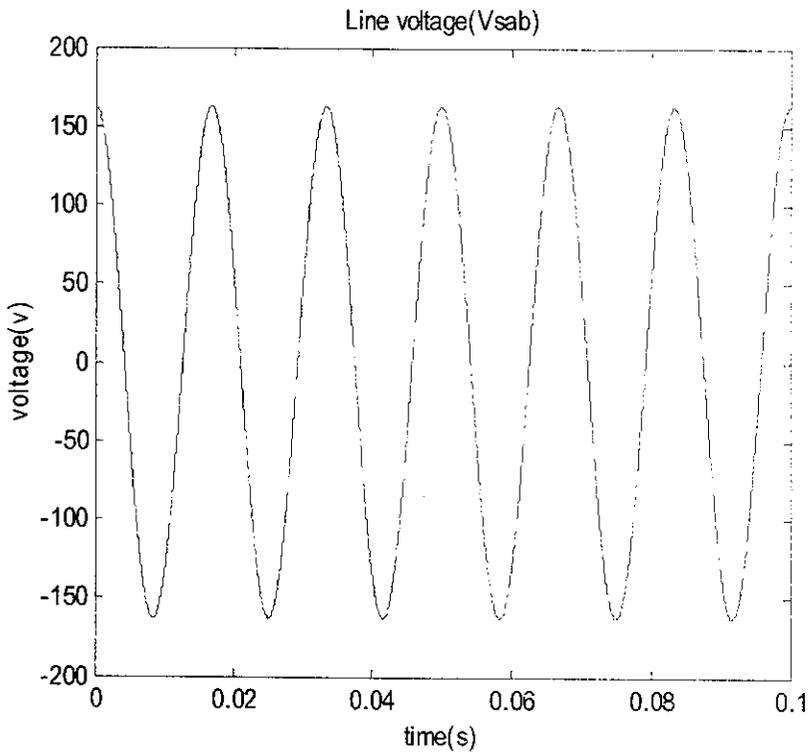


Figure 5.7 Input Voltage waveform with 50% sag of nominal voltage

Figure 5.7 shows the simulated waveform of input voltage which is the 50% of nominal voltage

Figures 5.8 and 5.9 show the output voltage and output current respectively for input voltage with 50% sag of nominal voltage. Thus it shows the ride through capability of Impedance Source Inverter even when the input voltage is not sufficient to give the desired output voltage[4].

The simulation proved the impedance source inverter concept. The voltage in order to maintain the desired output voltage can be achieved by impedance source inverter. The waveforms are consistent with the simulation results

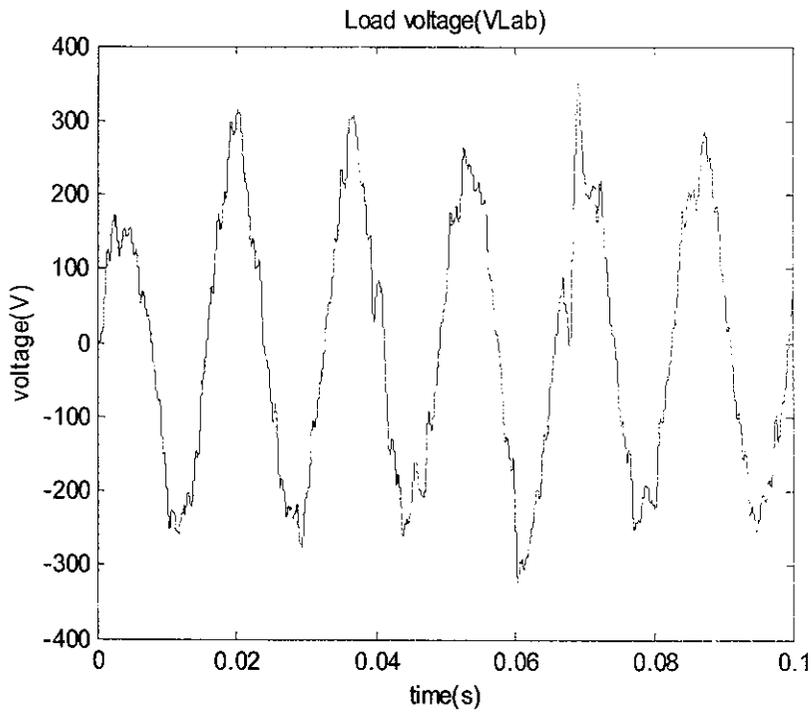


Figure 5.8 Output Voltage Wave forms for 50% sag in input voltage

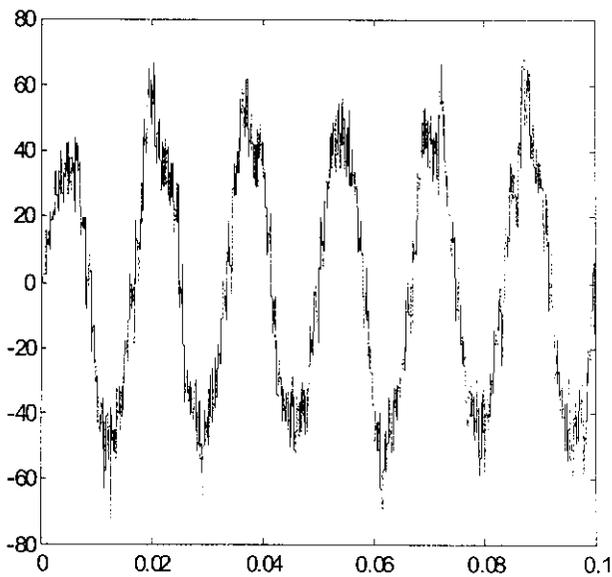


Figure 5.9 Output Current Wave form for 50% sag in Input Voltage

CHAPTER 6

HARDWARE DESCRIPTION

6.1 IMPEDANCE SOURCE INVERTER UPS MODULE

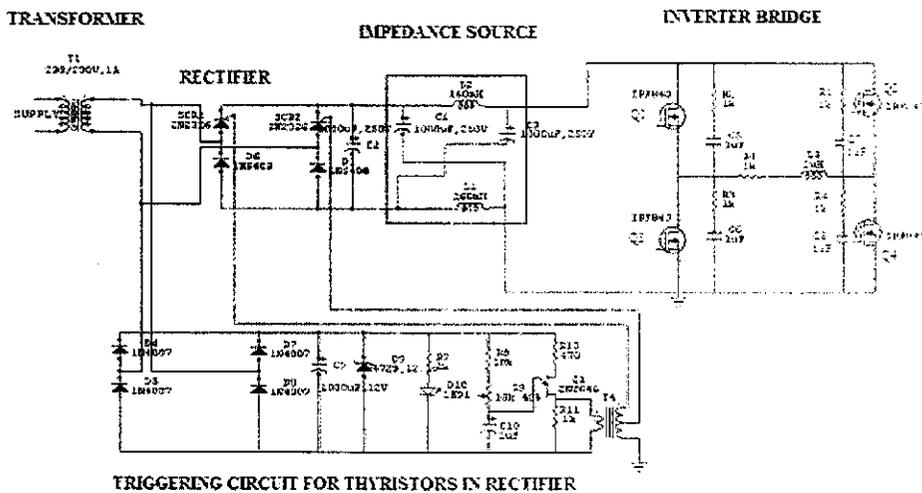


Figure 6.1 Hardware Circuit for Impedance Source Inverter

Figure 6.1 shows the circuit of a single phase impedance source inverter. To minimize the project cost and to reduce the circuit complications, the hardware implementation is done only for a single phase inverter.

The circuit consists of the following six blocks

- Input Transformer
- Rectifier
- Impedance Source
- Inverter Bridge
- Triggering Circuit for Thyristors in Rectifier Bridge
- PWM circuit for inverter switching

6.1.1 Input Transformer

The input transformer is a isolation transformer to isolate the circuit from the input supply surges.

6.1.2 Rectifier

The circuit involves one half controlled rectifier for converting the input ac into dc and the dc output of the rectifier is fed to the next stage via a filtering capacitor .

6.1.3 Impedance Source

In traditional inverters either a capacitor or an inductor is involved in the dc link. In voltage source inverters a capacitor is used where as in the current source inverters an inductor is used. But in this Impedance source inverter both the capacitor and an inductor is involved so that the rectifier output can be boosted as well as bucked as per the requirement. Here the capacitor and the inductor is connected in a manner so as the bridge looks like X . This bridge boosts the rectifier output so that the output of the inverter bridge is maintained as per the requirement.

6.1.4 Inverter Bridge

The circuit involves an single phase inverter which consists four MOSFETs as switching devices. They are named as Q1,Q2,Q3 and Q4.The snubber circuit has resistors and capacitors for protecting the bridge from over voltages and over current.The load used here involves resistor and An inductor. During the positive half cycle , MOSFETs Q1 and Q4 are conducting and MOSFETs Q3 and Q2 conducts during the negative half cycle.

6.1.5 Triggering Circuit For Thyristors In Rectifier Bridge

The thyristors involved in the rectifier bridge are triggered by a special circuit.By controlling this circuit the rectifier output can be adjusted to any desired

6.1.6 PWM Circuit For Inverter Switching

The inverter switches(MOSFETs) are triggered by the PWM circuit which is shown in figure 6.2.Here for generation of PWM pulses a SG2535 IC is used. The technique used for generating PWM pulse is single pulse width modulation technique.The amplitude of output pulses from this PWM generator is not enough to trigger the MOSFETs. So the output voltage is amplified by the two ULN 4002 ICs which are also eliminating the boot strap problem which is existing in all bridge inverters.

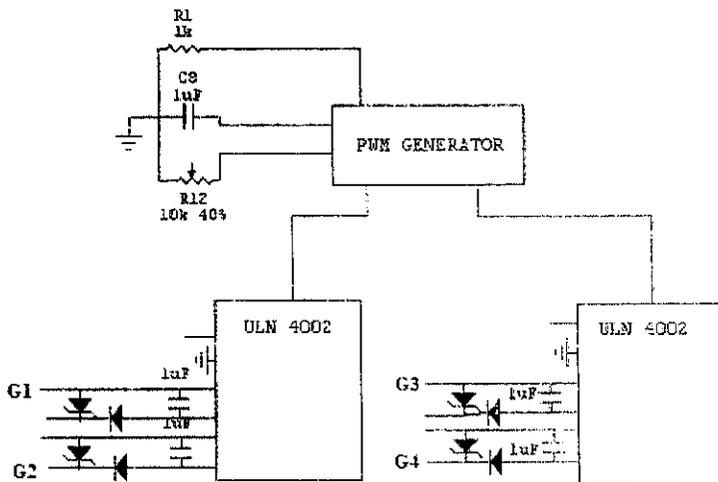


Figure 6.2 PWM Circuit for inverter switching

6.2 PULSE WIDTH MODULATION

6.2.1 Voltage Control of Inverters:

In many industrial applications, it is often required to control the output voltage of inverters to cope with the variations of dc input voltages, for voltage regulation of inverters, and for the constant volts/frequency control requirement.

There are various techniques to vary the inverter gain. The most efficient method of controlling the gain is to incorporate pulse-width-modulation (PWM)

The commonly used techniques are:

- ❖ Single-pulse-width modulation
- ❖ Multiple-pulse-width modulation
- ❖ Sinusoidal pulse-width modulation
- ❖ Modified sinusoidal pulse-width modulation
- ❖ Phase-displacement control

6.2.2 Single-Pulse-Width Modulation

In single-pulse-width modulation control, there is only one pulse per half-cycle and the width of the pulse is varied to control the inverter output voltage. Comparing a rectangular reference signal of amplitude, A_r , generates the gating signals. The frequency of the reference signal determines the fundamental frequency of output voltage. By varying A_r from 0 to A_c , the pulse width, δ , can be varied from 0 to 180° . The ratio of A_r to A_c is the Control variable and defined as the amplitude modulation index. The amplitude modulation index or simply modulation index is given below.

$$M = A_r / A_c$$

The RMS output voltage can be found from

$$V_o = [2/2\pi \int_{(\pi-\delta)/2}^{(\pi+\delta)/2} \int_{(\pi-\delta)/2}^{(\pi-\delta)/2} 2V^2 \sin^2(\omega t) dt]^{1/2} = V_s \sqrt{\delta / \pi}$$

The Fourier series of output voltage yields

$$V_o(t) = \sum_{n=1,3,5,\dots} 4V_s / n\pi \sin n\delta / 2 \sin n\omega t$$

The harmonic content can be reduced by using several pulses in each half-cycle of output voltage. The generation of gating signals for turning on and off of IGBT is done by comparing a reference signal with a triangular carrier wave. The frequency of reference signal sets the output frequency, f_o , and the carrier frequency, f_c , determines the number of pulses per half-cycle, p . The modulation index controls the output voltage. This type of modulation is also known as uniform pulse-width

The number of pulses per half-cycle is found from

$$P = fc/2fo = mf/2$$

Where $mf = fc/fo$ is defined as the frequency modulation ratio.

The variation of modulation index M from 0 to 1 varies the pulse width from 0 to π/p and the output voltage from 0 to V_s . the output voltage for single-phase bridge inverters is shown in the figure.

If δ is the width of each pulse, the rms output voltage can be found from

$$V_o(t) = \left[\sum_{n=1,3,5..}^{\delta} 2p \int_{\pi}^{\delta} (\pi/p + \delta) / 2V^2 d(\omega t) \right]^{1/2} = V_s \sqrt{p\delta / \pi}$$

The general form of a Fourier series for the instantaneous output voltage is

$$V_o(t) = \sum_{n=1,3,5}^{\delta} B_n \sin n\alpha t$$

The coefficient B_n can be determined by considering a pair of pulses such that the positive pulse of duration δ starts at $\omega t = \pi + \alpha$. The effects of all pulses can be combined together to obtain the effective output voltage.

6.3 PIC MICROCONTROLLER

16f877A PIC Microcontroller is used for controlling the width of the pulses from pwm generator, by fixing either the frequency or voltage so that the MOSFETs are turned ON and OFF in the desired sequence

6.3.1 The need for micro controller based PWM generation

- ❖ Micro controller has inbuilt functions such as timer, ADC, PWM, oscillator which reduce the hardware components used.
- ❖ PWM technique used enables the reduction of harmonics
- ❖ Wide variation in speed since frequency is used as control parameter.
- ❖ Digital circuits used employ a faster response.
- ❖ Automatic speed control is achieved since no manual parts all involved.
- ❖ The Micro controller IC Chip senses the input speed requirement and gives the output in favor of the input.
- ❖ No external commutation circuits are required.

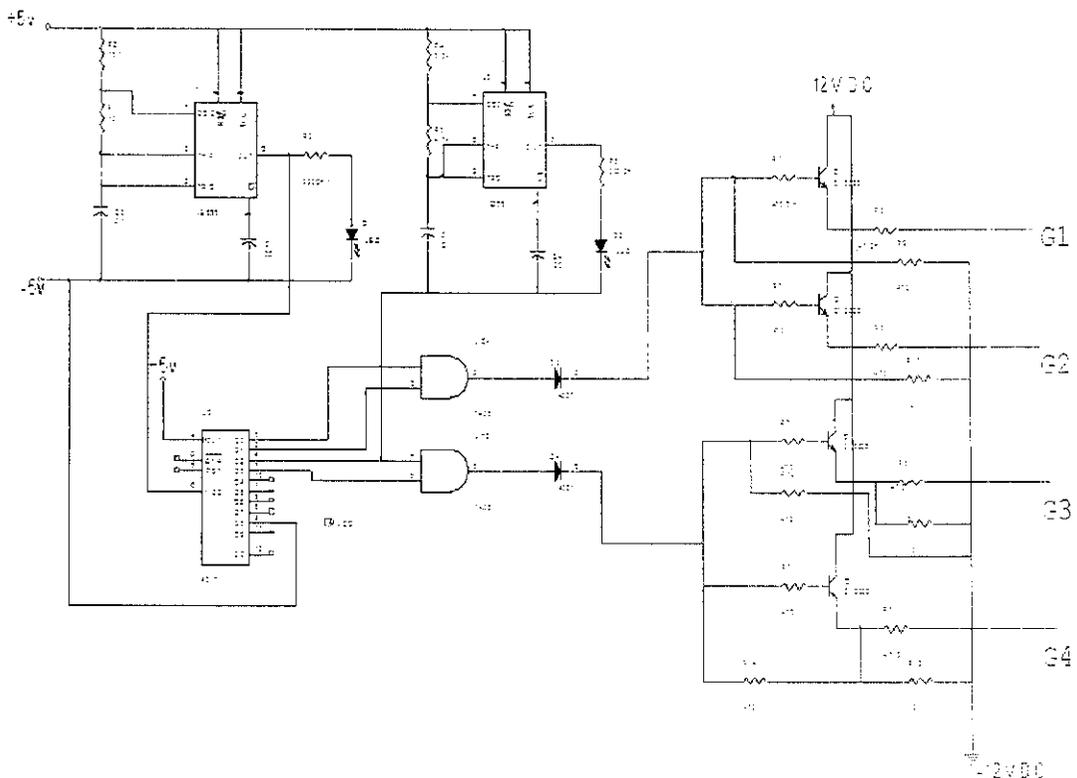


Figure 6.3 shows the complete triggering circuit for the single phase impedance source inverter. The outputs G1, G2, G3 and G4 are the gate pulses applied to the MOSFET switches. The sequence of switching is controlled by the microcontroller. The coding for that control is given in appendix B.

6.3.2 Core Features

- ❖ High-performance RISC CPU
- ❖ Only 35 single word instructions to learn
- ❖ Operating speed: DC - 20 MHz clock input
DC - 200 ns instruction cycle
- ❖ Up to 8K x 14 words of Flash Program Memory,
Up to 368 x 8 bytes of Data Memory (RAM)
Up to 256 x 8 bytes of EEPROM data memory
- ❖ Interrupt capability (up to 14 internal/external
- ❖ Eight level deep hardware stack
- ❖ Direct, indirect, and relative addressing modes
- ❖ Power-on Reset (POR)
- ❖ Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- ❖ Watchdog Timer (WDT) with its own on-chip RC Oscillator for reliable operation
- ❖ Programmable code-protection
- ❖ Power saving SLEEP mode
- ❖ Selectable oscillator options
- ❖ In-Circuit Serial Programming (ICSP) via two pins
- ❖ Only single 5V source needed for programming capability
- ❖ In-Circuit Debugging via two pins
- ❖ Wide operating voltage range: 2.5V to 5.5V
- ❖ High Sink/Source Current: 25 mA
- ❖ Commercial and Industrial temperature ranges
- ❖ Low-power consumption:
< 2 mA typical @ 5V, 4 MHz
20mA typical @ 3V, 32 kHz

6.3.3 Memory Organization

The organization of memory in PIC 16F877 is shown in the following table.

TABLE-6.1 MEMORY OF PIC 16F877

DEVICE	PROGRAM FLASH	DATA MEMORY	DATA EEPROM
PIC 16F877	8K	368 Bytes	256 Bytes

6.3.4 Program Memory Organisation

The PIC16f877 devices have a 13-bit program counter capable of addressing 8K *14 words of FLASH program memory. Accessing a location above the physically implemented address will cause a wraparound.

The RESET vector is at 0000h and the interrupt vector is at 0004h.

6.3.5 Data Memory Organisation

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the special functions Registers. Bits RP1 (STATUS<6>) and RP0 (STATUS<5>) are the bank selected bits.

TABLE 6.2 BANK SELECTION

RP1:RP0	Banks
00	0
01	1
10	2
11	3

Each bank extends up to 7Fh (1238 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM.

All implemented banks contain special function registers. Some frequently used special function registers from one bank may be mirrored in another bank for code reduction and quicker access.

6.3.6 Peripheral Features

- ❖ Timer0: 8-bit timer/counter with 8-bit prescaler
- ❖ Timer1: 16-bit timer/counter with prescaler
- ❖ Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- ❖ Two Capture, Compare, PWM modules
 - Capture is 16-bit, max resolution is 12.5 ns,
 - Compare is 16-bit, max resolution is 200 ns,
 - PWM max. resolution is 10-bit
- ❖ 10-bit multi-channel Analog-to-Digital converter
- ❖ Synchronous Serial Port (SSP) with SPI. (Master Mode) and I2C. (Master/Slave)
- ❖ USART/SCI with 9-bit address detection.
- ❖ Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls

These are all some of the important features of the peripherals available in PIC16F77A Microcontroller. The next Chapter gives the Architecture and pin details of the controller.

6.3.8 16F877A PIC Microcontroller Pin Diagram

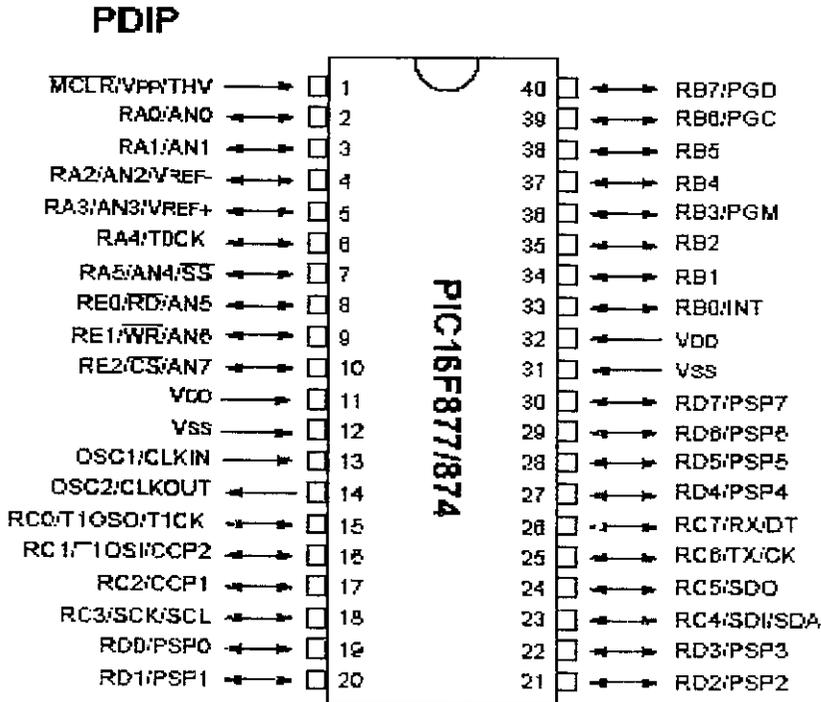


Figure 6.5. Pin diagram of PIC 16F877 Microcontroller

Figure 6.5 shows the pin out diagram of the PIC 16F877 Microcontroller. It is a 40 pin dual inline package(DIP) IC. It has five input / output ports named as Port A, Port B, Port C, Port D and Port E .

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin. The detailed description of the ports are given in Appendix A. Figure 20 gives the pin diagram of the PIC 16F877A Microcontroller

6.3.9 PIC Circuit For Impedance Source Inverter

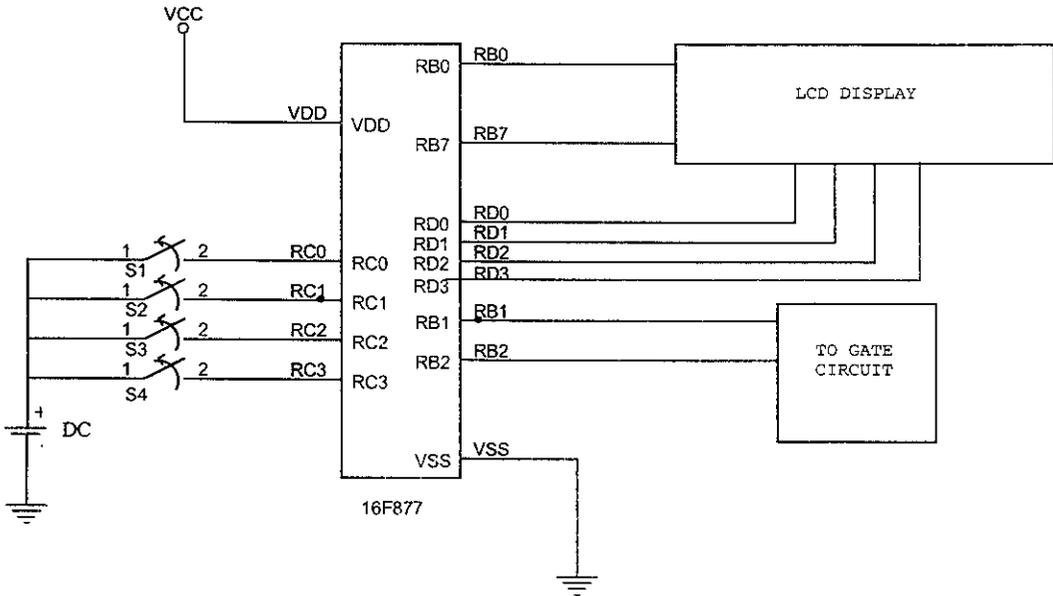


Figure 6.6 PIC circuit for triggering MOSFETs of Impedance source inverter

Figure 6.6 shows the circuit which triggers the switches (MOSFET) of Impedance source inverter. Here Port B and Port D are used as output ports. Port B output controls the gates of the MOSFETs. Port D outputs are given to the LCD display, which is used to display which MOSFETs are conducting. Port C is the input port.

6.4 LCD DISPLAY

Liquid crystal displays (LCD) have materials which combine the properties of both liquids and crystals. Rather than having a melting point, they have a temperature range within which the molecules are almost as mobile as they would be in a liquid, but are grouped together in an ordered form similar to a crystal.

An LCD consists of two glass panels, with the liquid crystal material sandwiched in between them. The inner surface of the glass plates are coated with transparent electrodes which define the character, symbols or patterns to be displayed

polymeric layers are present in between the electrodes and the liquid crystal, which makes the liquid crystal molecules to maintain a defined orientation angle.

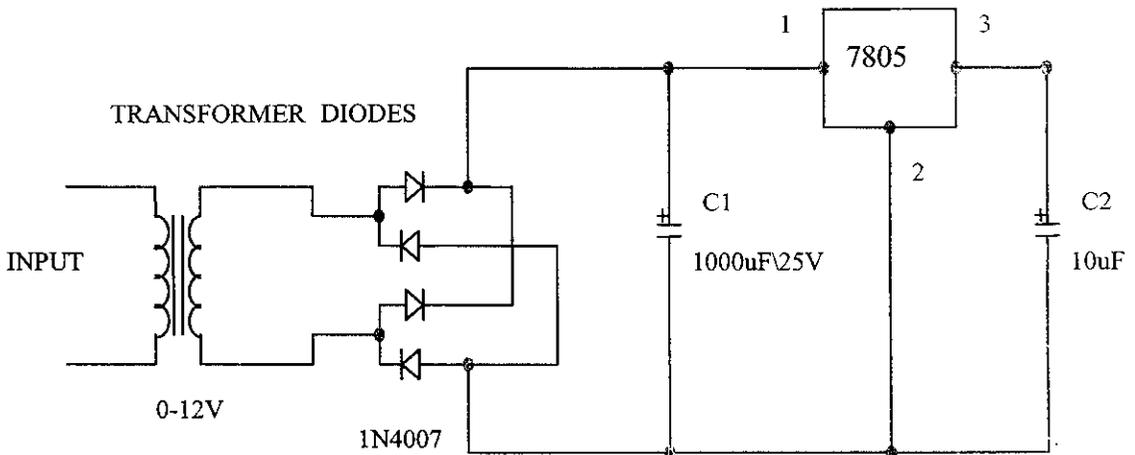


Figure 6.7 LCD Display

Polarizers are pasted outside the two glass panels. These polarizers would rotate the light rays passing through them to a definite angle, in a particular direction. When the LCD is in the off state, light rays are rotated by the two polarizers and the liquid crystal, such that the light rays come out of the LCD without any orientation, and hence the LCD appears transparent.

When sufficient voltage is applied to the electrodes, the liquid crystal molecules would be aligned in a specific direction. The light rays passing through the LCD would be rotated by the polarizers, which would result in activating / highlighting the desired characters.

The LCD's are lightweight with only a few millimeters thickness. Since the LCD's consume less power, they are compatible with low power electronic circuits, and can be powered for long durations.

The LCD doesn't generate light and so light is needed to read the display. By using backlighting, reading is possible in the dark. The LCD's have long life and a wide operating temperature range. Changing the display size or the layout size is

The LCDs are used exclusively in watches, calculators and measuring instruments are the simple seven-segment displays, having a limited amount of numeric data.

The recent advances in technology have resulted in better legibility, more information displaying capability and a wider temperature range. These have resulted in the LCDs being extensively used in telecommunications and entertainment electronics.

The LCDs have even started replacing the cathode ray tubes (CRTs) used for the display of text and graphics, and also in small TV applications.

6.4.1 RCM2034R

The RCM2034R is a reflective TN type liquid crystal module with a built-in controller / driver LSI and a display capacitor of 16 characters in one line.

6.4.2 Features

- 1) Wide viewing angle and high contrast.
- 2) 5_7 dot character matrix with cursor.
- 3) Interfaces with 4-bit or 8-bit MPUs.
- 4) Displays up to 226 characters and special symbols.
- 5) Custom character patterns are displayed with the character RAM.
- 6) Abundant instruction set including clear display, cursor on /off, and character blinking
- 7) Compact and light weight for easy assembly to the host instrument.
- 8) Operable on single 5 V power supply.
- 9) Low power consumption.

The hardware setup for impedance source inverter is implemented. For different input voltages, the outputs are obtained and tabulated. Same test is done in

6.5 HARDWARE RESULTS

The new impedance source inverter for UPS application is designed and implemented. The hardware is tested with various input voltages to the impedance network and the output voltages are obtained and tabulated.

TABLE 6.3 HARDWARE RESULTS OF IMPEDANCE SOURCE INVERTER

S.No	Rectifier output voltage (V)	Impedance source voltage (V)	Inverter output voltage (V)
1.	90	390	200
2.	110	410	210
3.	130	420	215
4.	140	450	220
5.	200	465	230

CHAPTER 7

CONCLUSIONS & RECOMMENDATION FOR FUTURE WORK

7.1 CONCLUSION

- ❖ A new type of inverter for UPS application has been presented.
- ❖ The Impedance source inverter is also suited for fuel cell application and AC electrical drives.
- ❖ The new Impedance source inverter system provides ride through capability during voltage sags.
- ❖ It improves power factor and reliability.
- ❖ Extends output voltage range
- ❖ It incorporates single stage power conversion, and doesn't need any additional components and energy storage. Hence component cost is reduced to a greater extent

The impedance source technology can be applied to the entire spectrum of power conversion.

7.2 RECOMMENDATION FOR FUTURE WORK

The voltage and current source inverters cannot be operated in shoot through mode. In voltage source inverter the incoming MOSFETs should be turned on, only after the outgoing MOSFETs are turned off completely. Otherwise the devices would be damaged. This introduces a delay in switching and therefore we get a pulsating output waveform.

In current source inverter, the incoming MOSFETs should be turned on, before the outgoing pair is completely turned off. This operation introduces a overlap in switching and hence we get a pulsating output waveform.

In impedance source inverter we are getting a smooth waveform, because shoot through mode is possible. This would be helpful for carrying out the following projects.

- Design of impedance source inverter for torque pulsation free induction motor drives
- Design of impedance source inverter for torque pulsation free synchronous motor drives

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APPENDIX A

16F877 PIC MICROCONTROLLER CODING & DETAILS

SOFTWARE CODE

```
#include<pic.h>

#define RS RD0
#define RW RD1
#define EN RD2

void enable();
void busyclick();
void lcd_init();
void delaylcd();
void delaylcd1();
void display(unsigned char);
void cursor_loc(unsigned char);
void display_string(unsigned char const*);

void delay1s( );
void delay20( );
void res( );
void res1( );

unsigned char const title[]=" Z - SOURCE INV ";
unsigned char const vol1[]="Volt 1%";
unsigned char const vol2[]="Volt 2%";
unsigned char const vol3[]="Volt 3%";
unsigned char const vol4[]="Volt 4%";
unsigned char const vol5[]="Volt 5%";
```

```
unsigned char const fre1[]="Freq 1%";
unsigned char const fre2[]="Freq 2%";
unsigned char const fre3[]="Freq 3%";
unsigned char const fre4[]="Freq 4%";
unsigned char const fre5[]="Freq 5%";

unsigned int pin=0,s=0,q=0,p=0,k=0,h=0,h1=0;
```

```
void main()
```

```
{
    ADCON1=0X06;
    TRISB=TRISC=TRISD=0;

    TRISA=0X07;
    PORTA =PORTB =PORTC =PORTD = 0;
```

```
    pin=s=q=0;
    delay1s();
    lcd_init();
    delay1s();
    cursor_loc(0x81);
    display_string(title);
    cursor_loc(0xCC);
    display_string("OFF");
```

```
while(1)
```

```
{

    if(RA0==1)
        {
            h++;
```

```

{
    h=0;
}

switch(h)
{
    case 0:
        delay1s();
        cursor_loc(0xCC);
        display_string("      ");
        cursor_loc(0xCC);
        display_string("OFF");
        h1=0;
        RA3=0;
        break;

    case 1:
        delay1s();
        cursor_loc(0xCC);
        display_string("      ");
        cursor_loc(0xCC);
        display_string("ON");
        h1=1;
        RA3=1;
        break;
}
}

```

```
while(RA1==1)
```

```

{
    k++;
    if(k>=6)
{

```

```
}
```

```
switch(k)
```

```
{
```

```
case 1:
```

```
    res();
```

```
    RA4=1;
```

```
    cursor_loc(0xc0);
```

```
    display_string(vol1);
```

```
    break;
```

```
case 2:
```

```
    res();
```

```
    RA5=1;
```

```
    cursor_loc(0xc0);
```

```
    display_string(vol2);
```

```
    break;
```

```
case 3:
```

```
    res();
```

```
    RC0=1;
```

```
    cursor_loc(0xc0);
```

```
    display_string(vol3);
```

```
    break;
```

```
case 4:
```

```
    res();
```

```
    RC1=1;
```

```
    cursor_loc(0xc0);
```

```
    display_string(vol4);
```

```
    break;
```

```
case 5:
```

```
    res();
```

```
    RC2=1;
```

```
    cursor_loc(0xc0);
```

```
        break;
    }
while(RA2==1)
{
    p++;
    if(p>=6)
    {
        p=1;
    }
    switch(p)
    {
        case 1:
            res1();
            RC3=1;
            cursor_loc(0xc0);
            display_string(fre1);
            break;
        case 2:
            res1();
            RC4=1;
            cursor_loc(0xc0);
            display_string(fre2);
            break;
        case 3:
            res1();
            RC5=1;
            cursor_loc(0xc0);
            display_string(fre3);
            break;
        case 4:
            res1();
            RC6=1;
            cursor_loc(0xc0);
```

```

        break;
    case 5:
        res1();
        RC7=1;
        cursor_loc(0xc0);
        display_string(fre5);
    }
}
}
}
}
}
}
}
}

```

```

void res()
{
    delay1s();
    RA4=RA5=RC0=RC1=RC2=0;
}

```

```

void res1()
{
    delay1s();
    RC3=RC4=RC5=RC6=RC7=0;
}

```

```

void delay20()
{
    unsigned int i=0;
    for(i=0;i<=4000;i++);
}

void delay1s()
{
    unsigned int j=0;
    for(j=0;j<=65000;j++);
}
}

```

LCD DISPLAY

```
void enable()
{
    EN=1;
    asm("NOP");
    asm("NOP");
    asm("NOP");
    asm("NOP");
    asm("NOP");
    asm("NOP");
    asm("NOP");
    asm("NOP");
    asm("NOP");
    EN=0;
}
```

```
void busycheck()
{
    EN=0;
    TRISB=0x80;
    RS=0;
    RW=1;
    EN=1;
    while(RB7);
    EN=0;
    RW=0;
    RS=1;
    TRISB=0;
}
```

```
void delaylcd()
{
    unsigned int k=0;
    for(k=0;k<4000;k++);
}
```

```
void delaylcd1()
{
    unsigned int k=0;

    for(k=0;k<3000;k++);
}
```

```
void lcd_init()
{

    PORTB=PORTD=0;
    delaylcd1();
    PORTB=0x38;
    enable();

    delaylcd();
    PORTB=0x38;
    enable();

    delaylcd();
    PORTB=0x38;
    enable();

    delaylcd1();
    PORTB=0x01;
    enable();
```

```
delaylcd1();  
PORTB=0x06;  
enable();
```

```
delaylcd1();  
PORTB=0x0e;  
enable();
```

```
RS=0;  
PORTB=0x80;  
enable();  
delaylcd1();  
RS=1;
```

```
}
```

```
void cursor_loc(unsigned char p1)
```

```
{
```

```
RS=0;  
PORTB=p1;  
enable();  
busycheck();  
delaylcd1();  
RS=1;
```

```
}
```

```
void display_string(unsigned char const *a1)
```

```
{
```

```
    unsigned char i=0;
```



```
{  
    PORTB=*a1;  
    enable();  
    busycheck();  
    a1++;  
    i++;  
  
}  
}
```

```
void display( char dat)
```

```
{  
    RS=1;  
    PORTB=dat;  
    enable();  
    busycheck();  
  
}
```

16F877 PIC MICROCONTROLLER

PIN OUT DESCRIPTION

The image shows a table with a grid of approximately 10 columns and 20 rows. The text within the table is extremely faint and difficult to read due to heavy noise and low contrast. However, the layout suggests a standard pin out description table with columns for pin number, pin name, and a brief description of the pin's function.

I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

PORTA and the TRISA Register

PORTA is a 6-bit wide bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (=1) will make the corresponding PORTA pin an input, i.e., put the corresponding output driver in a Hi-impedance mode. Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output, i.e., put the contents of the output latch on the selected pin.

Reading the PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore a write to a port implies that the port pins are read; this value is modified, and then written to the port data latch. Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers. Other PORTA pins are multiplexed with analog inputs and analog VREF input. The operation of each pin is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register1).

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

PORT A Function

Name	Bit#	Buffer	Function
RA0/AN0	bit0	TTL	Input/output or analog input
RA1/AN1	bit1	TTL	Input/output or analog input
RA2/AN2	bit2	TTL	Input/output or analog input
RA3/AN3/VREF	bit3	TTL	Input/output or analog input or VREF
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0 Output is open drain type
RA5/SS/AN4	bit5	TTL	Input/output or slave select input for synchronous serial port or analog input

PORTB and the TRISB Register

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input, i.e., put the corresponding output driver in a hi-impedance mode.

Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output, i.e., put the contents of the output latch on the selected pin. Three pins of PORTB are multiplexed with the Low Voltage Programming function; RB3/PGM, RB6/PGC and RB7/PGD. The alternate functions of these pins are described in the Special Features Section. Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>). This interrupt can wake the

device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

- a) Any read or write of PORTB. This will end the mismatch condition.
- b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared. The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature. This interrupt on mismatch feature, together with software configurable pull-ups on these four pins, allow easy interface to a keypad and make it possible for wake-up on key depression

Port B Functions

Name	Bit#	Buffer	Function
RB0/INT	bit0	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3/PGM	bit3	TTL	Input/output pin or programming pin in LVP mode. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6/PGC	bit6	TTL/ST ⁽²⁾	Input/output pin (with interrupt on change) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming clock.
RB7/PGD	bit7	TTL/ST ⁽²⁾	Input/output pin (with interrupt on change) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

PORT C and the TRISC Register

PORTC is an 8-bit wide bi-directional port. The corresponding data direction register is TRISC. Setting a TRISC bit (=1) will make the corresponding PORTC pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISC bit (=0) will make the corresponding PORTC pin an output, i.e., put the contents of the output latch on the selected pin. PORTC is multiplexed with several peripheral functions (Table-3.5). PORTC pins have Schmitt Trigger input buffers.

When the I2C module is enabled, the PORTC (3:4) pins can be configured with normal I2C levels or with SMBUS levels by using the CKE bit (SSPSTAT <6>).

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify write instructions (BSF, BCF, XORWF) with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

Port C Functions

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input
RC1/T1OSI/CCP2	bit1	ST	Input/output port pin or Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I ² C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I ² C mode).
RC5/SDO	bit5	ST	Input/output port pin or Synchronous Serial Port data output
RC6/TX/CK	bit6	ST	Input/output port pin or USART Asynchronous Transmit or Synchronous Clock
RC7/RX/DT	bit7	ST	Input/output port pin or USART Asynchronous Receive or Synchronous Data

Legend: ST = Schmitt Trigger input

PORT D and TRISD Registers

This section is not applicable to the 28-pin devices. PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

PORTD can be configured as an 8-bit wide microprocessor Port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

Port D Functions

Name	Bit#	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit0
RD1/PSP1	bit1	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit1
RD2/PSP2	bit2	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit2
RD3/PSP3	bit3	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit3
RD4/PSP4	bit4	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit4
RD5/PSP5	bit5	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit5
RD6/PSP6	bit6	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit6
RD7/PSP7	bit7	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit7

Legend: ST = Schmitt Trigger input TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffer when in Parallel Slave Port Mode.

PORTE and TRISE Register

PORTE has three pins RE0/RD/AN5, RE1/WR/AN6 and RE2/CS/AN7, which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers.

The PORTE pins become control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make sure that the TRISE<2:0> bits are set (pins are configured as digital inputs). Ensure ADCON1 is configured for digital I/O. In this mode the input buffers are TTL.

PORTE pins are multiplexed with analog inputs. When selected as an analog input, these pins will read as '0's. TRISE controls the direction of the RE pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.

Port E Functions

Name	Bit#	Buffer Type	Function
RE0/RD/AN5	bit0	ST/TTL ⁽¹⁾	Input/output port pin or read control input in parallel slave port mode or analog input: RD 1 = Not a read operation 0 = Read operation. Reads PORTD register (if chip selected)
RE1/WR/AN6	bit1	ST/TTL ⁽¹⁾	Input/output port pin or write control input in parallel slave port mode or analog input: WR 1 = Not a write operation 0 = Write operation. Writes PORTD register (if chip selected)
RE2/CS/AN7	bit2	ST/TTL ⁽¹⁾	Input/output port pin or chip select control input in parallel slave port mode or analog input: CS 1 = Device is not selected 0 = Device is selected

Legend: ST = Schmitt Trigger input TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port Mode.

Instruction Set Summary

Each PIC 16f877 instruction is a 14-bit word, divided into an OPCODE which specifies the instruction type and one or more operand which further specify the operation of the instruction. The PIC16F877 instruction set summary in table 12 lists byte-oriented, bit-oriented, and literal and control operations. Table 11 shows the opcode Field descriptions.

For byte-oriented instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction. The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the w register. If 'd' is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, ‘b’ represents a bit field designator which selects the number of the bit affected by the operation, which ‘f’ represents the address of the file in which the bits is located.

For literal and control operations, ‘k’ represents an eight or eleven bit constant or literal value.

Opcode Field Descriptions

Field	Description
f	Register file address (0x00 to 0x7F)
w	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W. d = 1: store result in file register f. Default is d = 1
PC	Program Counter
\overline{TO}	Time-out bit
\overline{PD}	Power-down bit

The instruction set is highly orthogonal and is grouped into three basic categories:

- Byte-oriented operations
- Bit-oriented operations
- Literal and control operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 ms. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 ms.

16F877 INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	14-Bit Opcode			Status Affected	Notes		
			MSb	LSb					
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		
NOP	-	No Operation	1	00	0000	0xxx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1(2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1(2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDI	-	Clear Watchdog Timer	1	00	0000	0110	0100	TOPD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	TOPD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

- 2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.
- 3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.