Digital Storage Attachment to General Purpose Oscilloscope

P-184

Project Report

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Digital Storage Attachment to General Purpose Oscilloscope

has been submitted by

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In partial fulfilment for the award of Degree of

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Internal Examiner .... External Examiner ....

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SYNOPSIS

This project outlines the design and fabrication of a basic form of a low cost Digital storage front-end attachment to a general purpose oscilloscope. This enhances the capabilities of the oscilloscope to analyze transient events which are non-repetitive.The front-end unit is based on a INTEL 8085 micro-processor trainer with the interfacing of necessary A/D and D/A conversion circuits and trigger circuits. The necessary software for the proper functioning of the unit is also developed.

CONTENTS

INTRODUCTION

CHAPTER 1

INTRODUCTION

The cathode ray oscilloscope is probably the most versatile tool for the development of electronic circuits and systems.It is widely used in servicing of all types of electronic equipments. While it is capable of displaying waveforms of events that take place over periods of micro seconds to seconds, it has a number of limitations. First, the accuracy of measurements obtainable through oscilloscope is of the order of +3% only. Then it can only display on the screen as a stationary waveform if the event is a periodic one. The non-periodic events will produce a trace on the screen which will appear for a fraction of a second and then disappear.

For analysing such events either we have to make a photographic record of the waveform appearing on the screen or we have to use specially developed storage type of oscilloscopes. The photographic recording of the waveform and analysing it could be quite irksome to the user since the time taken to process the film might take several hours to days depending on the facilities available. Whereas the storage type oscilloscope produce a image due to the event on the screen as long as the power supply is turned on and facilitates the analysis of the electronic circuit without any delays,the cost of the storage type of oscilloscope is very high and is not within the reach of all service personnel of electronic equipments. With the advent of VLSI technology development of microprocessor based systems are cheaper and any dedicated system could be realized for a total cost of a few thousand rupees only. The subsequent chapters of the project outlines the design and fabrication of a microprocessor based front end digital storage attachment to a general purpose oscilloscope in its basic form and it could be easily modified to provide all the facilities available in a sophisticated digital storage oscilloscope.

PRINCIPLE OF OPERATION

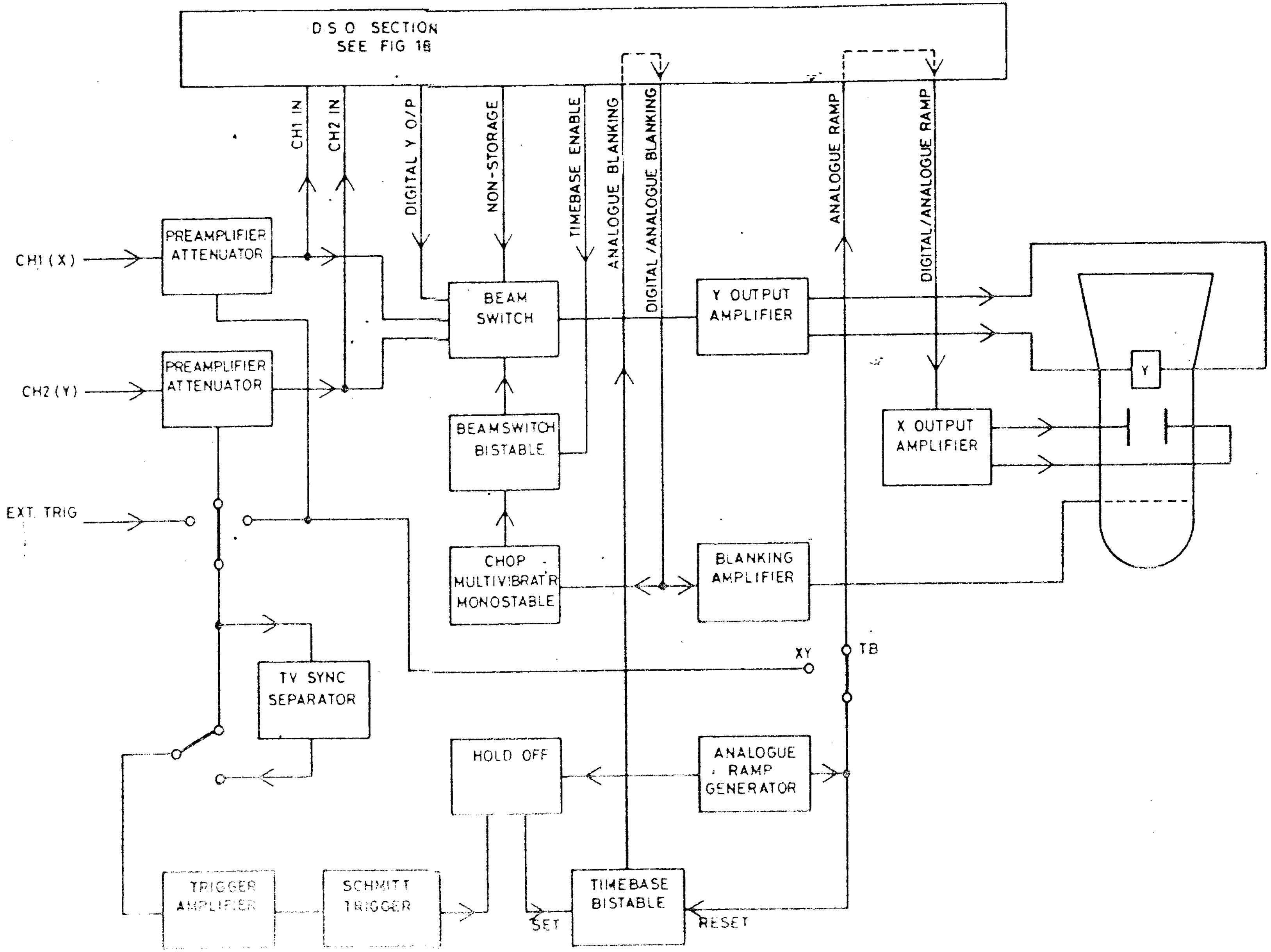
CHAPTER 2

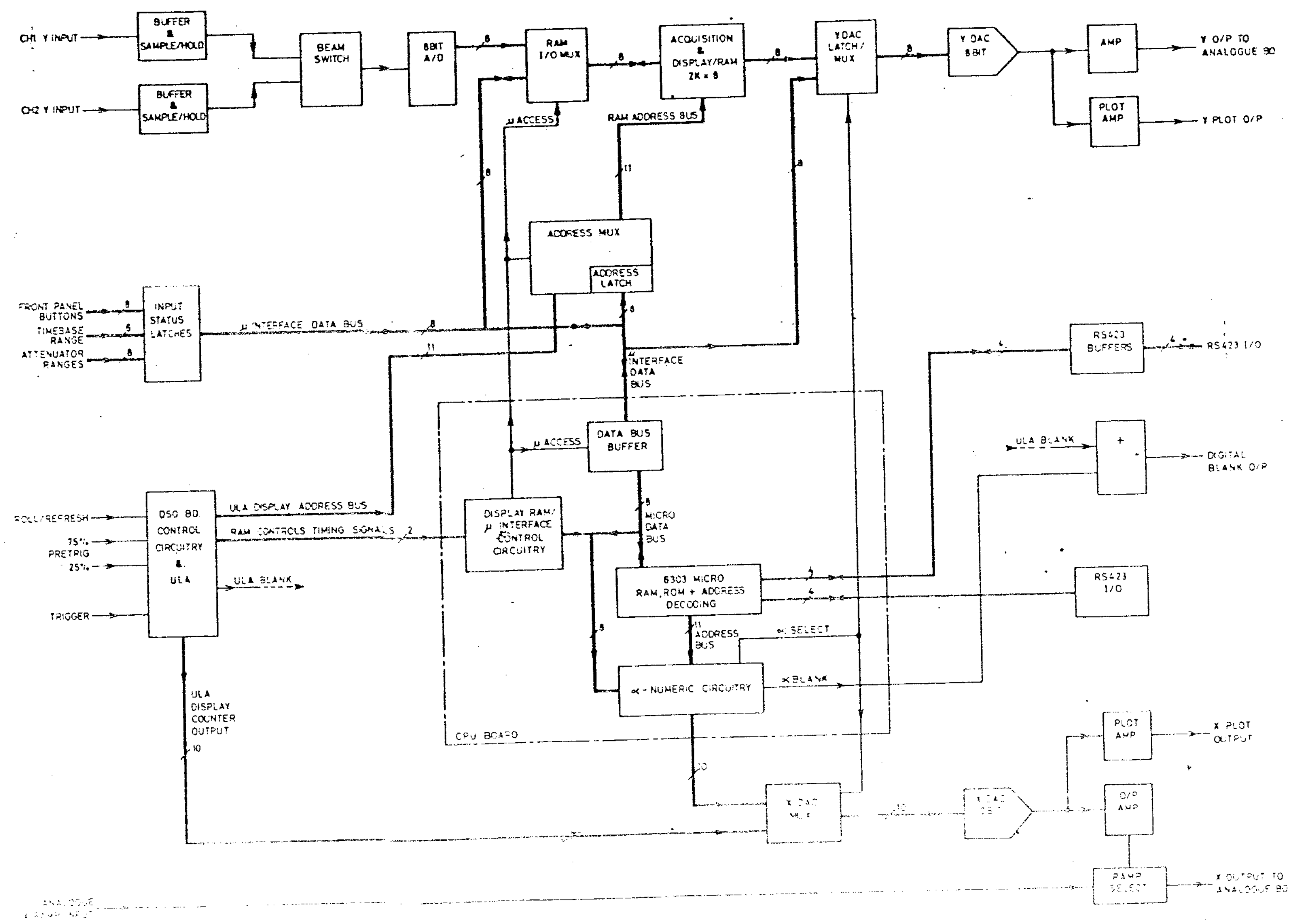
PRINCIPLE OF OPERATION

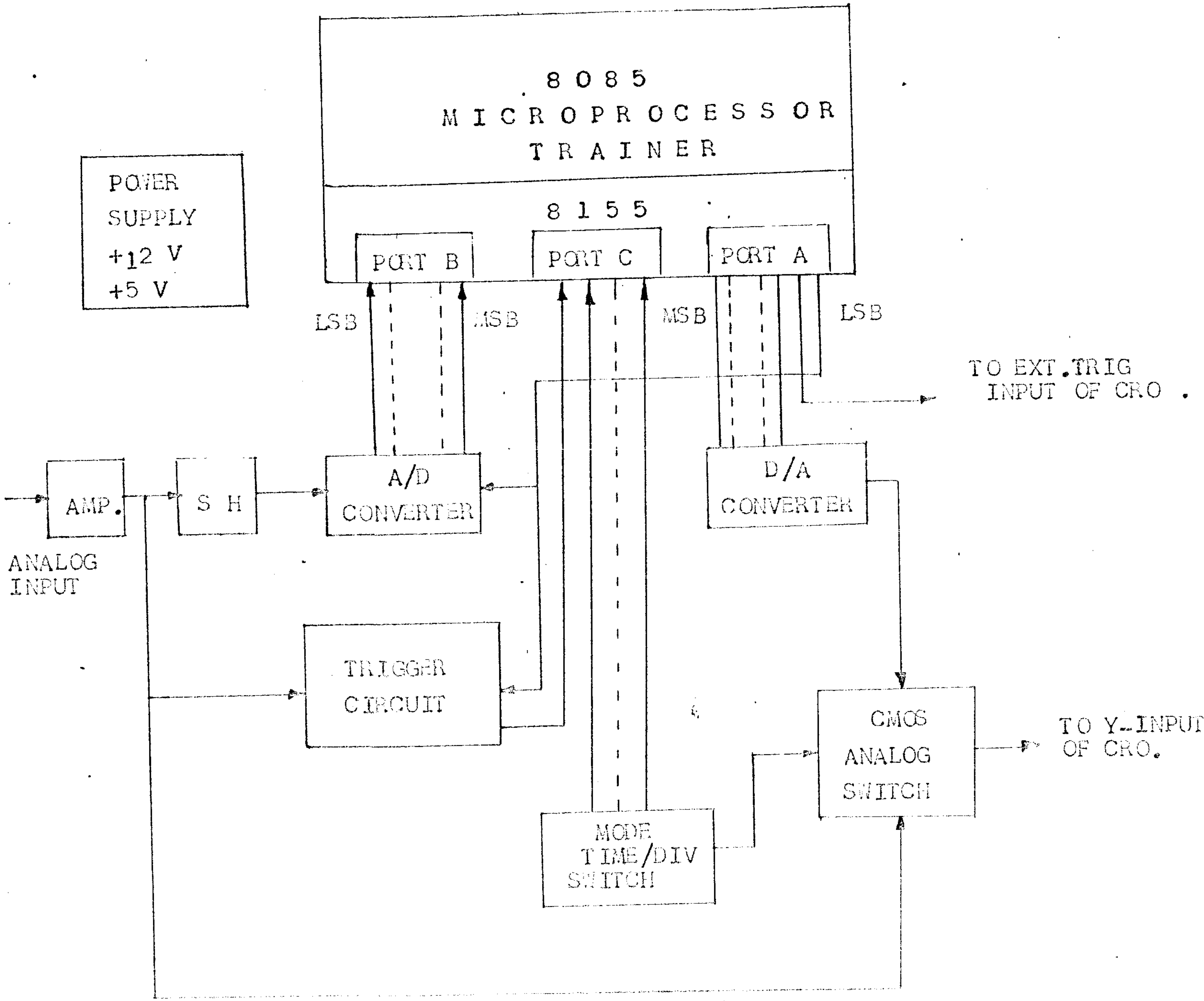
Two types of storage oscilloscope are available. The earlier version is based on a special type of cathode ray tube which can store the information written on the screen of the scope by storing the information as charges retained by the bi-stable action of the mosaic of dots on the fluorescent screen. This type of oscilloscope can retain the stored image as long as the supply is on and if a permanent record of the waveform is required a photograph of the same has to be taken. such oscilloscope are known as analog storage oscilloscopes.

The present day oscilloscopes are of the digital storage type. They sample the input waveforms at close intersects and convert the data into digital form and stores them in consequtive memory locations. Then they are outputed in the same sequence and converted into analog form and displayed on the screen of a normal oscilloscope repeatedly to produce a flicker free image on the screen. The sampling, analog to digital conversion, storing of digital data, outputting the digital data and conversion back to analog form are controlled by a microprocessor clocked by a quartz controlled oscillator. The schematic diagram of a typical digital storage oscilloscope is shown in Figs. 2.1 and 2.2. Since the analog signal is converted into digital form it is possible to provide suitable output to digital plotter to produce a hard copy output.

The proposed front end digital storage attachment to oscilloscope is based on INTEL 8085 microprocessor trainer. ADC 0804, which is an 8 bit A/D converter with a typical conversion time of 100 micro seconds is used to convert the analog input into digital form. Since no multiplexing is done only a single trace can be stored through a port in the memory of trainer as 1024 x 8 bit word in the user RAM area. The stored data is outputted through a port to DAC 0806 D/A converter. The sampling rate, storage mode, trigger armed condition, trigger instant are fed to the processor through another port. The unit can store transients of 100 milliseconds/ 200 milliseconds durations and could be further extended by a factor of 5 through switches on the front panel. The outputs from the unit to the CRO are analog signal, which could be either from the input in the NORMAL MODE or from the D/A converter in STORAGE MODE and a synchronizing pulse for triggering the time base of the CRO through EXT.TRIG.INPUT. The schematic block diagram with the varios switch selectable controls are shown in Fig 2.3.


D S O SECTION
SEE FIG 1B
CH1 IN
CH2 IN
DIGITAL Y O/P
NON-STORAGE
TIMEBASE ENABLE
ANALOGUE BLANKING
DIGITAL /ANALOGUE BLANKING
ANALOGUE RAMP
DIGITAL/ANALOGUE RAMP
CH1 (X)
CH2 (Y)
EXT. TRIG
PREAMPLIFIER ATTENUATOR
PREAMPLIFIER ATTENUATOR
BEAM SWITCH
BEAMSWITCH BISTABLE
CHOP - MULTIVIBRAT'R MONOSTABLE
Y OUTPUT AMPLIFIER
X OUTPUT AMPLIFIER
BLANKING AMPLIFIER
Y
XY
TB
TV SYNC SEPARATOR
HOLD OFF
ANALOGUE RAMP GENERATOR
TRIGGER AMPLIFIER
SCHMITT TRIGGER
TIMEBASE BISTABLE
SET
RESET
DIAGRAM


CH1 Y INPUT
CH2 Y INPUT
BUFFER & SAMPLE/HOLD
BUFFER & SAMPLE/HOLD
BEAM SWITCH
8BIT A/D
RAM I/O MUX
ACQUISITION & DISPLAY/RAM 2K x 8
YDAC LATCH/ MUX
Y DAC 8BIT
AMP
PLOT AMP
Y O/P TO ANALOGUE BD
Y PLOT O/P
μ ACCESS
RAM ADDRESS BUS
ADDRESS MUX
ADDRESS LATCH
FRONT PANEL BUTTONS
TIMEBASE RANGE
ATTENUATOR RANGES
INPUT STATUS LATCHES
μ INTERFACE DATA BUS
μ INTERFACE DATA BUS
RS423 BUFFERS
RS423 I/O
ULA BLANK
DIGITAL BLANK O/P
DATA BUS BUFFER
μ ACCESS
ROLL/REFRESH
75%
PRETRIG
25%
TRIGGER
DSO BD CONTROL CIRCUITRY & ULA
ULA DISPLAY ADDRESS BUS
RAM CONTROLS TIMING SIGNALS
ULA BLANK
DISPLAY RAM/ μ INTERFACE CONTROL CIRCUITRY
MICRO DATA BUS
6303 MICRO RAM, ROM + ADDRESS DECODING
RS423 I/O
ADDRESS BUS
∝ SELECT
∝ BLANK
∝ - NUMERIC CIRCUITRY
ULA DISPLAY COUNTER OUTPUT
CPU BOARD
PLOT AMP
X PLOT OUTPUT
O/P AMP
X OUTPUT TO ANALOGUE BD


8085
MICROPROCESSOR
TRAINER
8155
PORT B
PORT C
PORT A
POWER
SUPPLY
+12 V
+5 V
LSB
MSB
MSB
LSB
TO EXT.TRIG
INPUT OF CRO.
AMP.
S H
A/D
CONVERTER
D/A
CONVERTER
ANALOG
INPUT
TRIGGER
CIRCUIT
CMOS
ANALOG
SWITCH
TO Y-INPUT
OF CRO.
MODE
TIME/DIV
SWITCH

DESIGN OF HARDWARE

CHAPTER 3

DESIGN OF HARDWARE

The hardware of the digital storage unit consists of four sections. They are A/D converter section, D/A converter section, mode select and trigger select and microprocessor trainer.The first three sections mentioned above are interfaced to a 8085 microprocessor trainer kit through the three ports of a 8155 programmable pheripheral interface chip available on the trainer. The sampled and digitized data input is given to port B. Mode select, trigger armed,triggered and time base selection inputs are given to port C. Port A is used for outputting the stored data to D/A converter and also the trigger flip-flop reset and synchronizing pulse outputs.

3.1 A/D CONVERTER:

The A/D converter shown in Fig.3.1 is based on ADC 0804 8 bit converter with a conversion time of typically 100 microseconds. It is preceded by LF 398A sample and hold circuit and an input unity gain buffer amplifier LM

741. Provision is made in the input amplifier for D.C balance adjusment through 10k potentiometer.

The ADC chip is a microprocessor compatible one which could be interfaced directly to the microprocessor buses.But in this scheme the output and the control signals are interfaced through the ports of the 8155 chip available in the trainer. The input voltage of the ADC is 0 to +5 Volts with Vcc at +5 volts and Vref/2 at 2.5 volts. In order to accomodate bipolar input of +10 V a resistor network is connected at the input by 3 resistors as shown in the circuit. It could be seen by the principle of superposition for a +10 V change at the output of S & H circuit the actual change at the Vin+ terminal of the A/D converter is only 0 to +5 V. The chip is enabled by always connecting the CS pin to ground. The WRITE (start conversion) and READ [data latching] is done by a single pulse from the processor which updates the digital data at the falling edge and starts the next conversion at the rising edge of the pulse.This pulse is outputed at the sampling rate required. The inverted version of the WR-RD pulse is given to the control input of the S & H chip.The data is sampled at the high level of the pulse and held at low level for the conversion.The 100 ohms potentiometer in the potential divider for Vref/2 supply is used for full scale adjustment of the ADC. With the analog input at 0 V the digital output is adjusted to be 7F HEX. The ADC chip is self-clocked by an R-C circuit at approximately 1 MHZ so that the maximum conversion time will be about 80 micro seconds.

3.2 D/A CONVERTER :

The D/A converter circuit shown in Fig. 3.2 is based on DAC 0806 8 bit converter with 6 bit accuracy. The stored digital data is fed to the converter through the 6 most significant bits of port A of 8155. The other two bits are used to send out reset pulses to the flip-flop and the external synchronizing pulses to the time base of the oscilloscope. The unipolar output of the DAC chip (0 to 5 V) is level shifted and amplified to provide a bi-polar analog signal (+10 V) corresponding to the analog input of the digital storage unit. A CMOS switch CD 4066 enables the mode selection NORMAL/STORED MODE by switching the analog signals to CRO.

3.3 TRIGGER CIRCUIT :

This circuit is shown in Fig. 3.3. The analog signal at the output of the input buffer amplifier is compared with the tigger level(variable from +10 V to -10 V) through a 10k potentiometer at the front panel. An unity gain inverter is provided to select the slope at which triggering takes place. A sharp +Ve tigger pulse is formed by the R-C high pass filter with the diode. The STORAGE/NORMAL MODE is set by a switch with S-R flip-flop to debounce the contacts and the command signal is given to the processor through the bit 2 of port C. TRIGGER ARMED and TRIGGER instant signals are generated by the J-K flip-flops and fed to the processor through bit 1 & 0 of port C. The TIME/DIV and MULTIPLIER signals which determine the sample rate is set by switches on the front panel and fed through bits 3 & 4 of port C. The complete circuit diagram excluding the microprocessor trainer is shown in Fig. 3.4.

3.4 MICROPROCESSOR TRAINER KIT:

The microprocessor trainer is based on INTEL 8085 CPU at 3.072 clock rate. It has 22 parallel I/O lines (PORTS of 8155). The three circuit sections described above are interfaced through the lines. The circuit diagram of the trainer and the specifications of the systems are given in the APPENDIX. Also given in the

APPENDIX are the pin details and the relevant electrical characteristics of the I.C.s used in the hard ware.

A power supply (Fig. 3.5) is built into the unit to provide the necessary +12 V and +5 V for the analog and digital circuits using three terminal I.C. regulators.

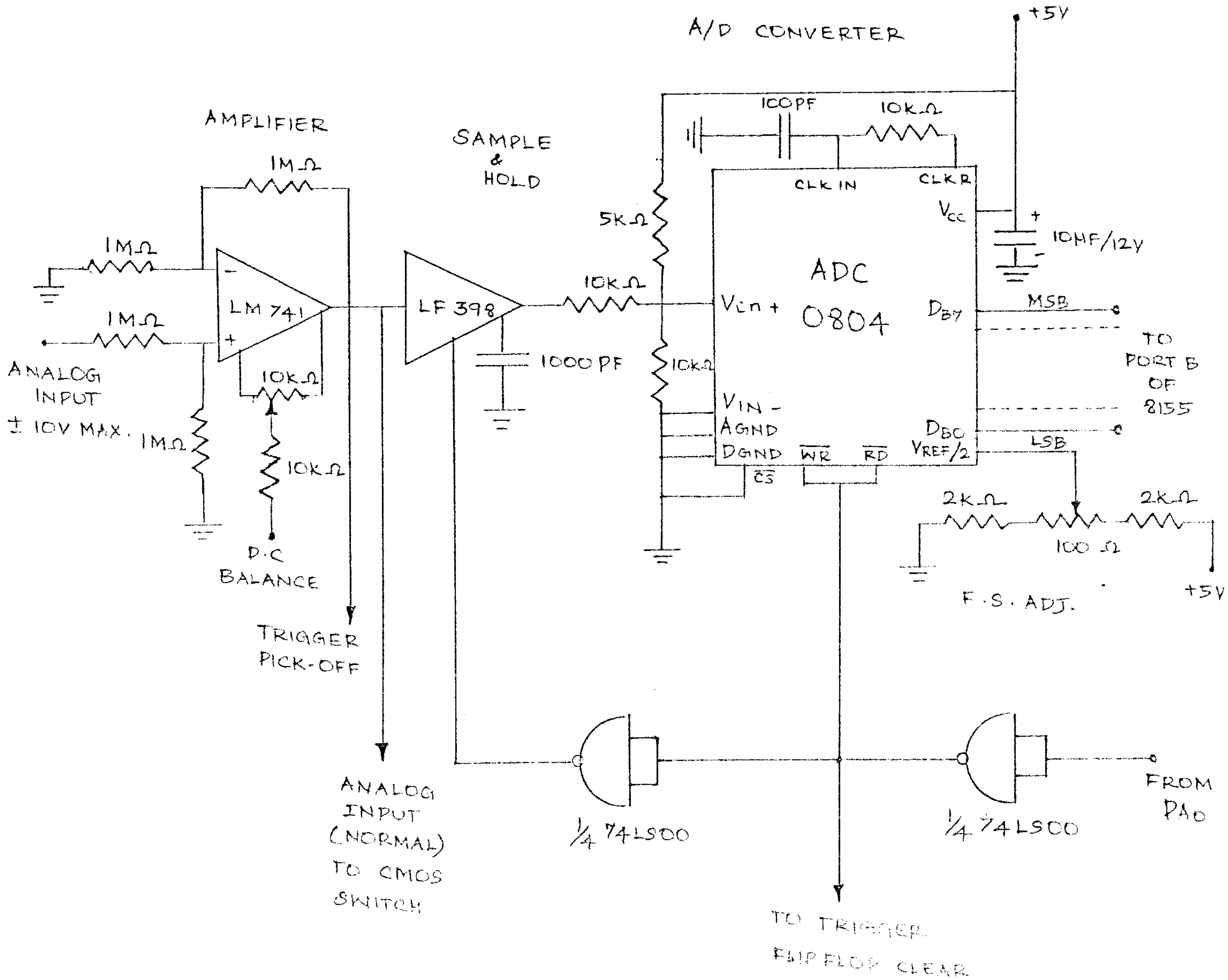


Fig 3.1 A/D CONVERTER CIRCUIT.

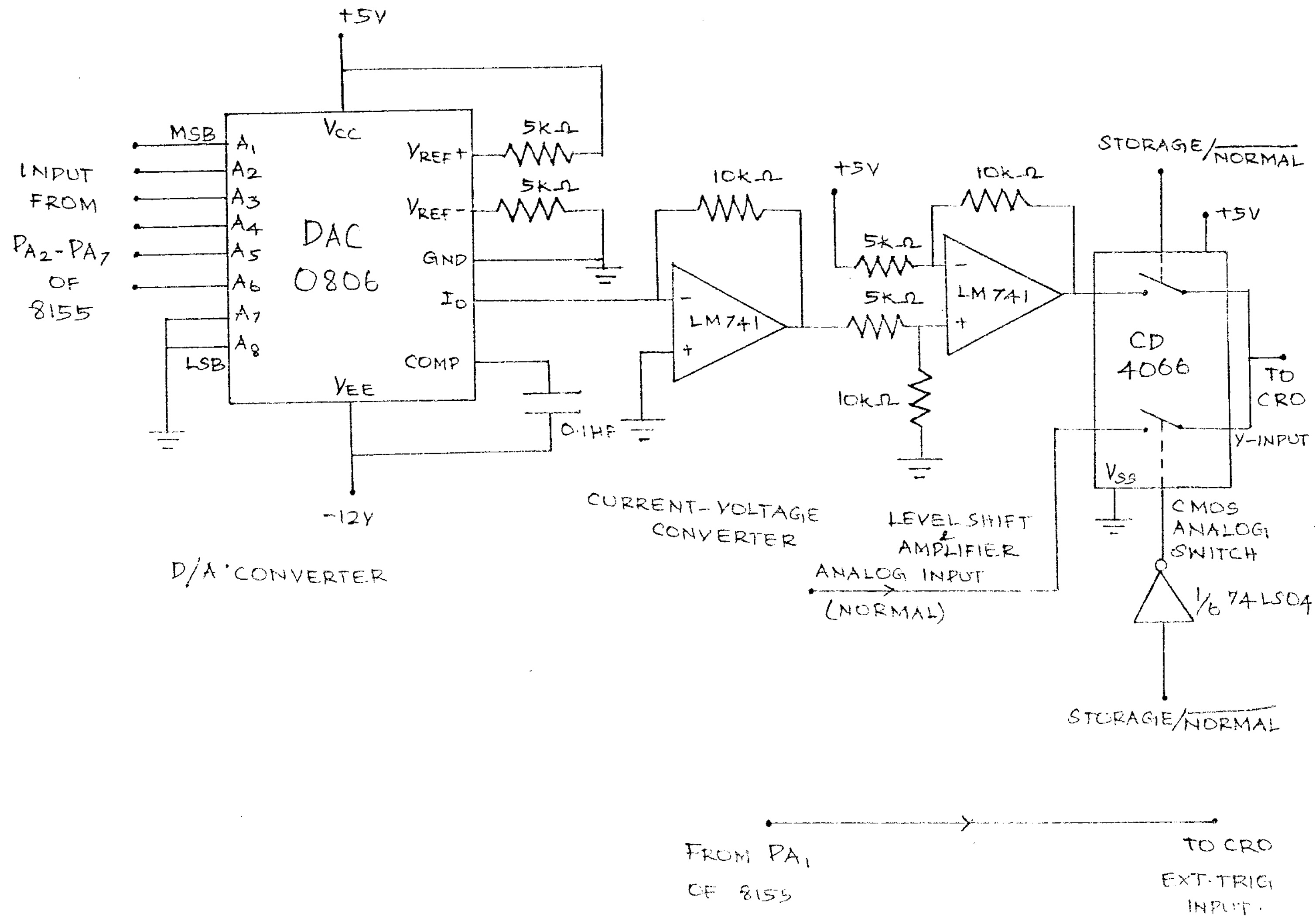


Fig 3.2 D/A CONVERTER CIRCUIT

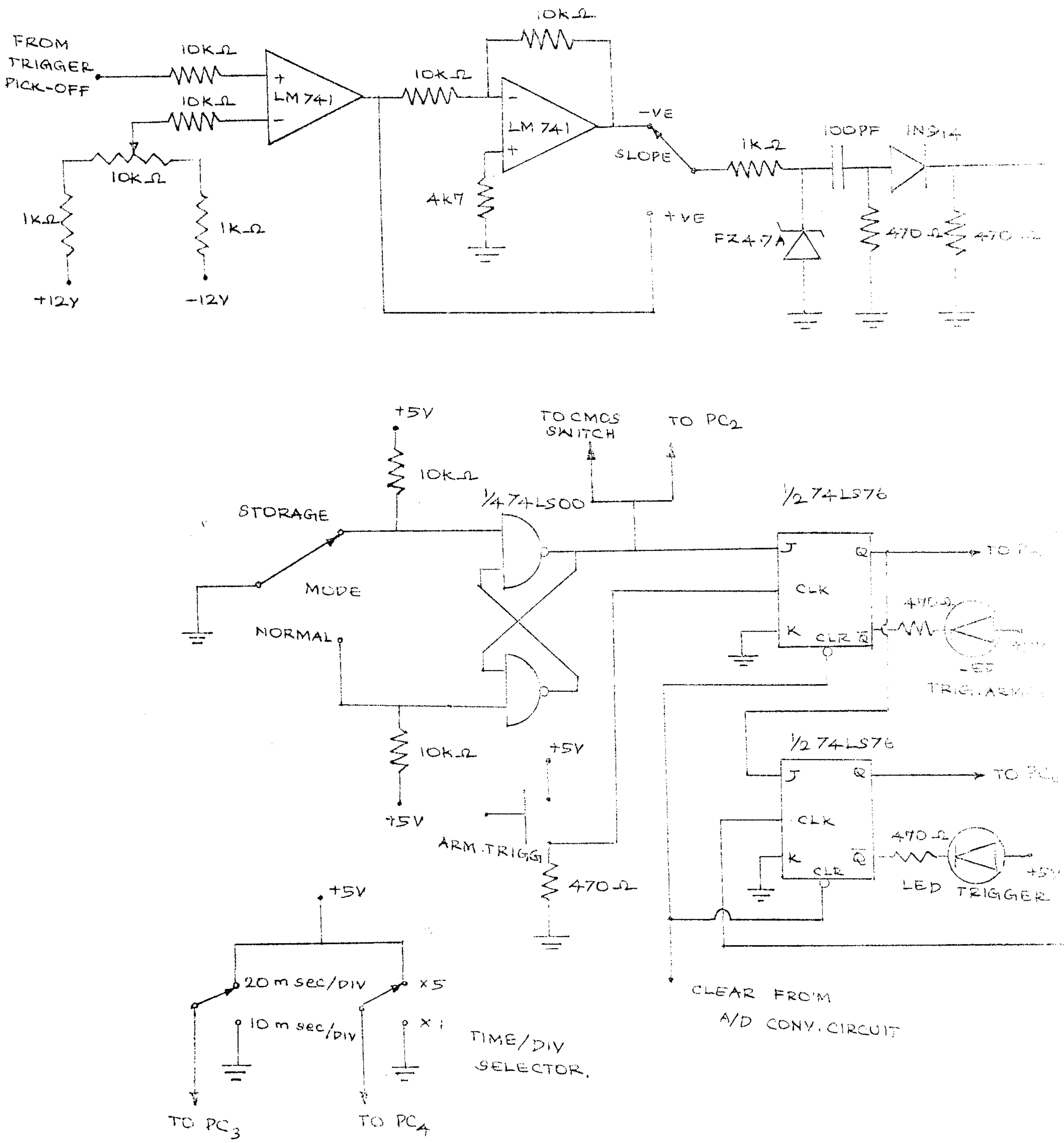


Fig 3.3. TRIGGER CIRCUIT & CONTROL SWITCHES.

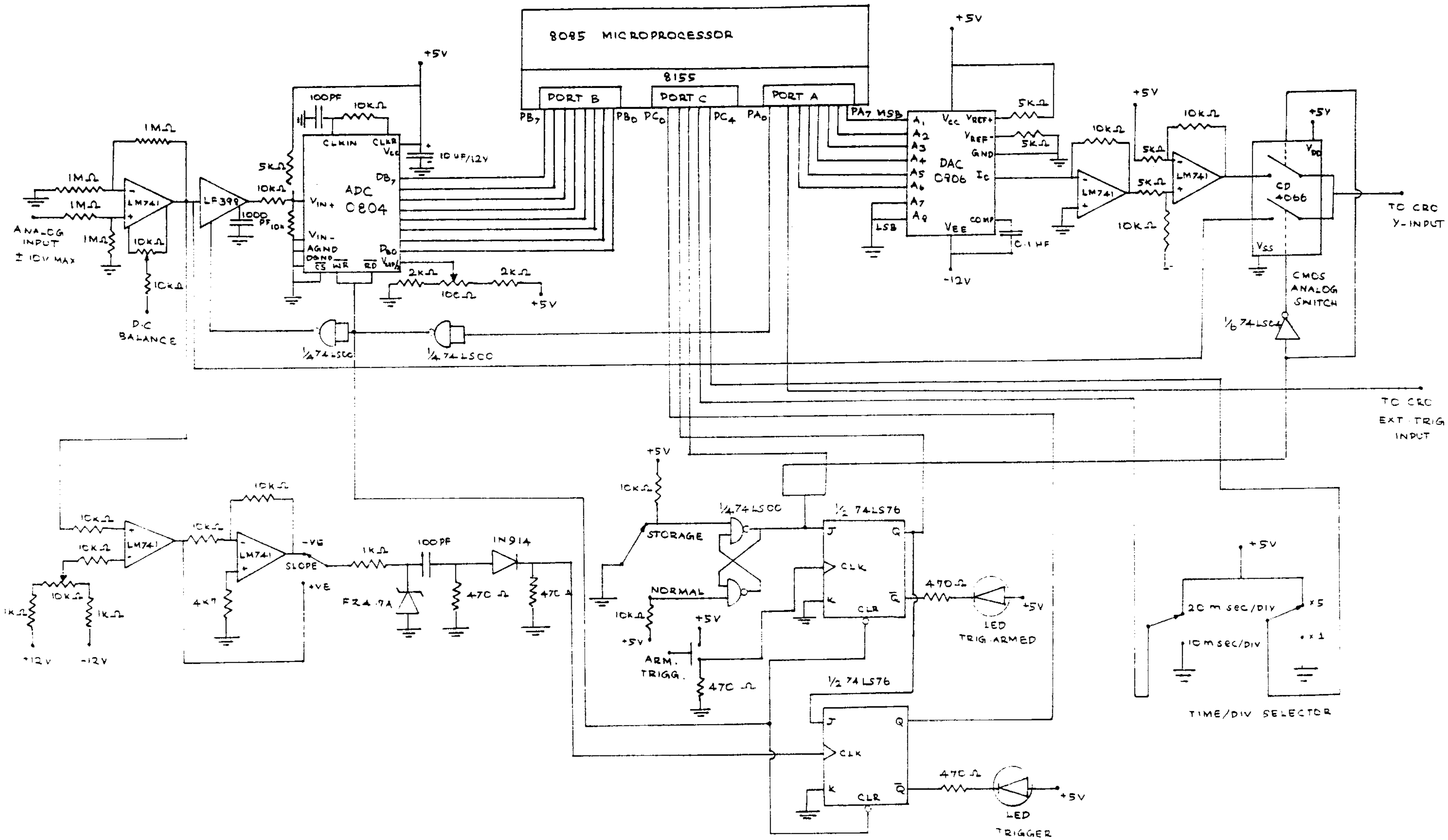


Fig. 3.4. CIRCUIT DIAGRAM OF DIGITAL STORAGE ATTACHMENT.

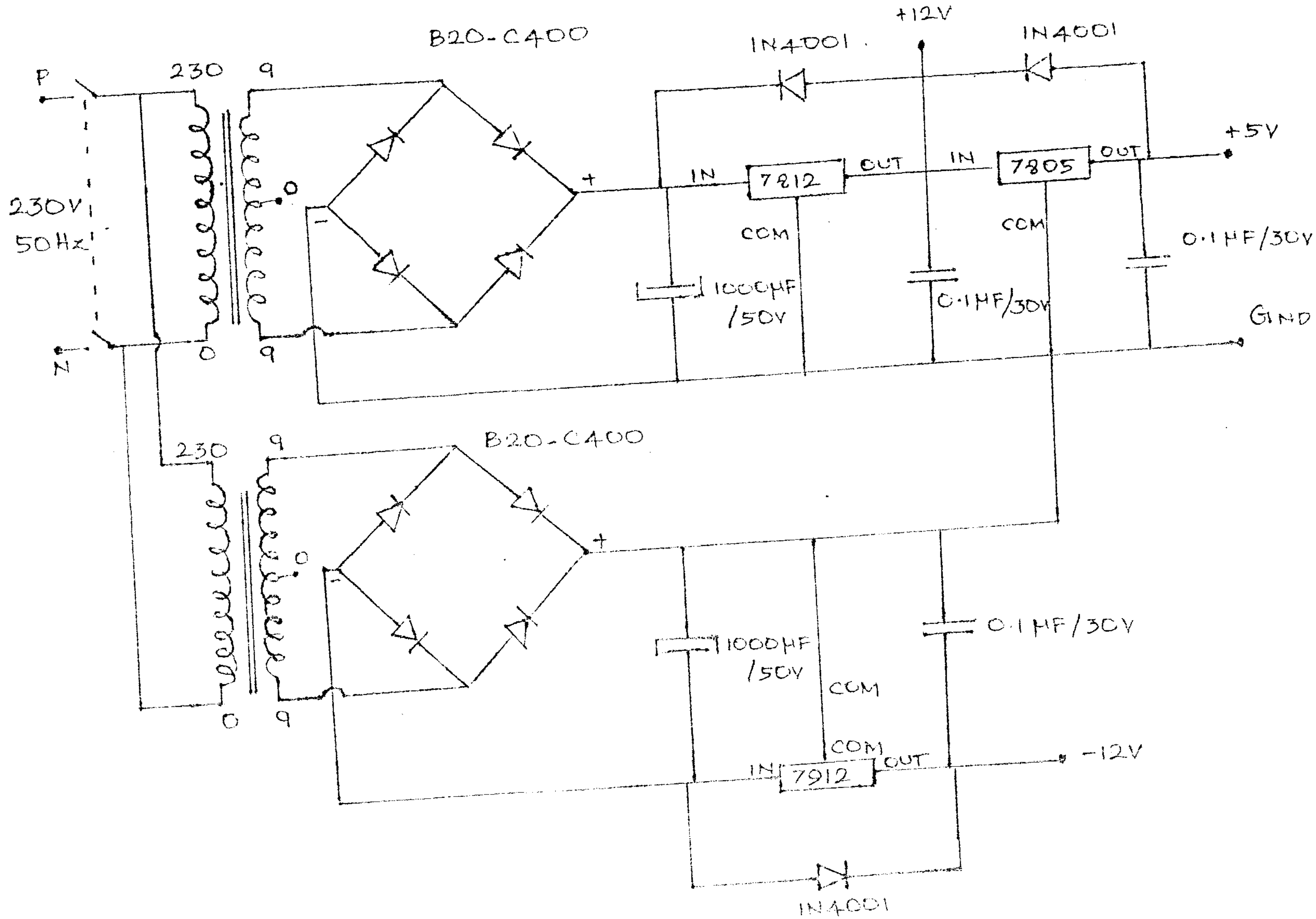


FIG. 3.5 POWER SUPPLY UNIT

DESIGN OF SOFTWARE

CHAPTER 4

DESIGN OF SOFTWARE

The algorithm of the program of the digital storage unit is shown in Fig. 4.1 and Fig. 4.2 as a flow chart. The processor intially configures the ports of 8155 with port A as output port and port B and port C as output ports. Then it reads the input from port C and checks whether the bit 2 is set to '1' level to find out the MODE. If the switch is in STORAGE MODE, the bit 2 of port C will be set to '1'through de-bouncing circuits.

If in STORAGE MODE , the processor will output the stored digital information (1024x8 bit words) from RAM sequentially at 50 microseconds intervals to port A.The time delay is generated through the software as a delay sub-routine. The output is converted in to analog form and given to the Y-input of the oscilloscope reproducing the stored wave form in about 50 milliseconds. Thus repeatedly tracing the waveform at 20 hertz will produce a flicker free trace. At the end of each cycle it checks whether the MODE SELECT is in

STORED MODE and also checks whether TRIGGER ARMED and TRIGGER flip-flop's are set to '1' which is an indication for refreshing the stored wave. On checking the above stored bits 1 & 0 of port C, the program calls a sub-routine for REFRESHING.

The processor generates through software sampling pulses of duration slightly in excess of a input read operation, which enables the sample and hold circuit, latches the previous converted data of A/D converter to its output latches at the rising edge and starts the new conversion at the falling edge. The processor also reads the data in the latches through port A and stores in the RAM. This is repeated 1024 times at sample rates of 10 kHz/5 kHz /2 kHz /1 kHz detemined by the delay routines for storing transients of 100 m secs/ 200 m secs/ 500 m secs /1sec depending on the switch setting on the front panel and are read through bit 3 & 4 of port C. At the end of the routine (after storing 1024 sampled values in consecutive locations in the RAM) the processor displays the new stored waveform until the MODE switch is changed to " NORMAL MODE" or another REFRESH signal is recieved.

While outputting the first word stored in RAM the processor sends out a SYNC. pulse through the LSB of of port A so that it can trigger the time base of the oscilloscope through the EXT.TRIGG. INPUT to synchronise the waveform and the timebase. The processor while refreshing sends out a pulse through bit 1 of port A to reset the TRIGGER circuit flip-flop's. Two states of STORAGE MODE, TRIGGER ARMED & TRIGGER signals are checked at the begining of each cyclic time of the processor while REFRESHING or displaying the waveform stored in the memory. The program is listed in Appendix.

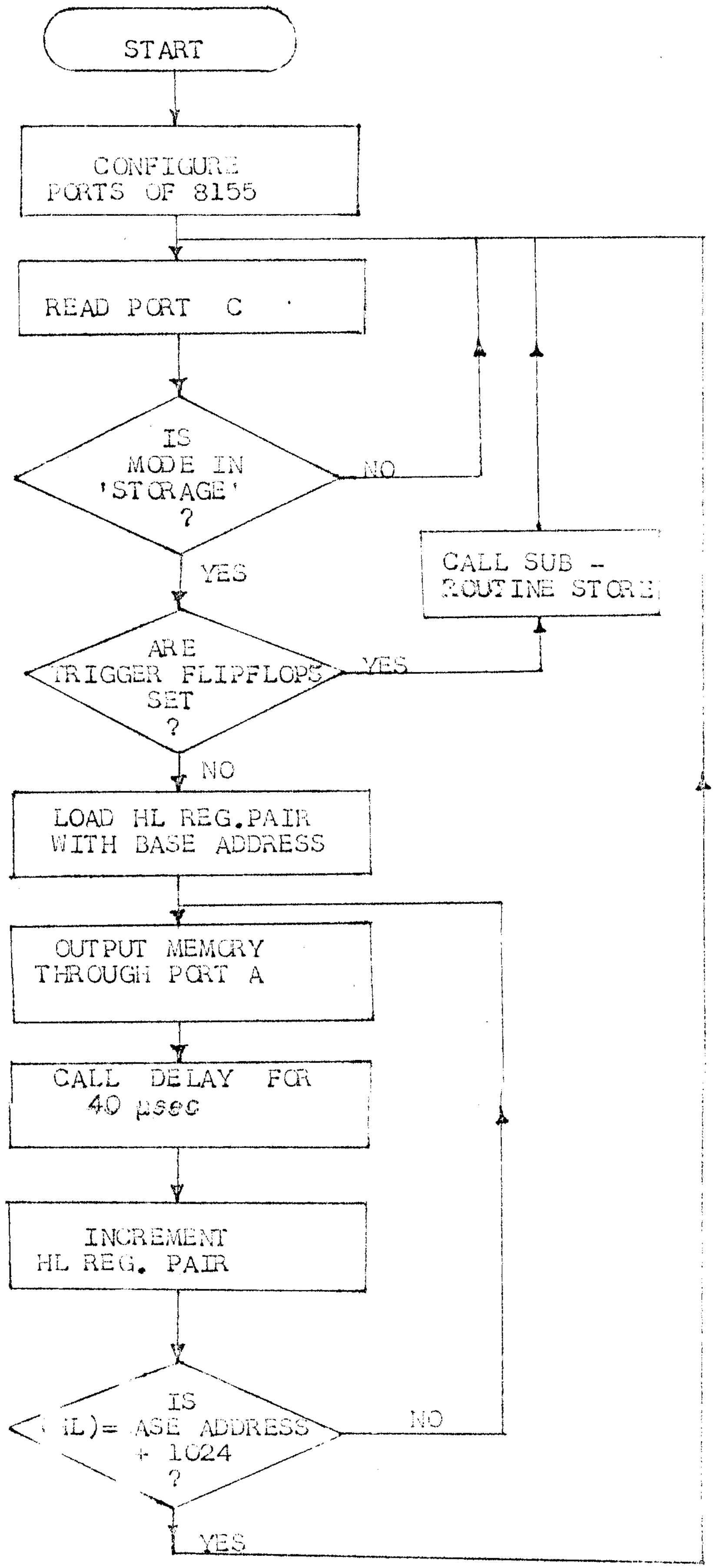


Fig. 1. MAIN PROGRAM.

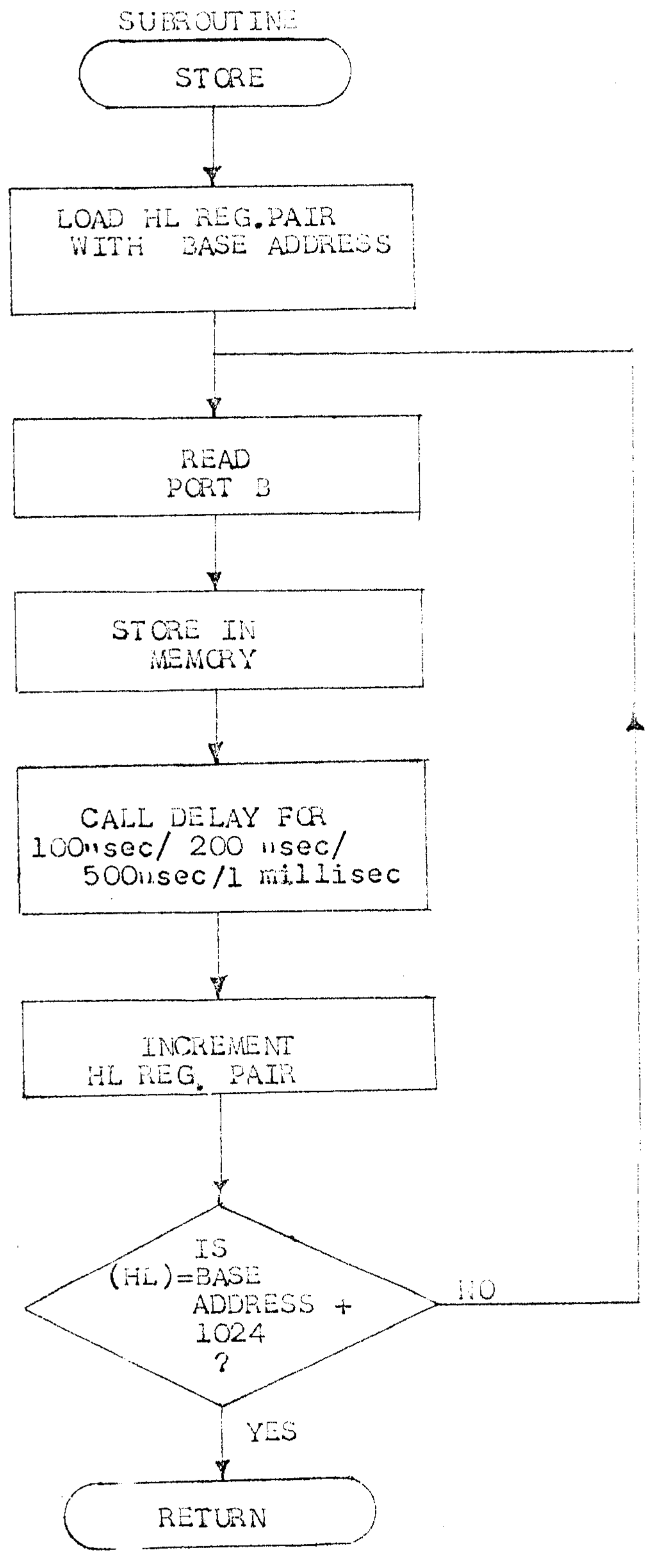


Fig. 4.2 'STORE' SUBROUTINE

TEST RESULTS

CHAPTER 5

TEST RESULTS

The assembled instrument is tested for D.C. transient, A.C. transient and repetitive waveforms. The circuit diagrams for the above tests are shown in Figs. 5.1 to 5.3. The waveforms are photographed and shown in Figs. 5.4 to 5.6. It may be noted from the waveforms photographed, that the instrument is capable of displaying the A.C. and D.C. transients accurately.

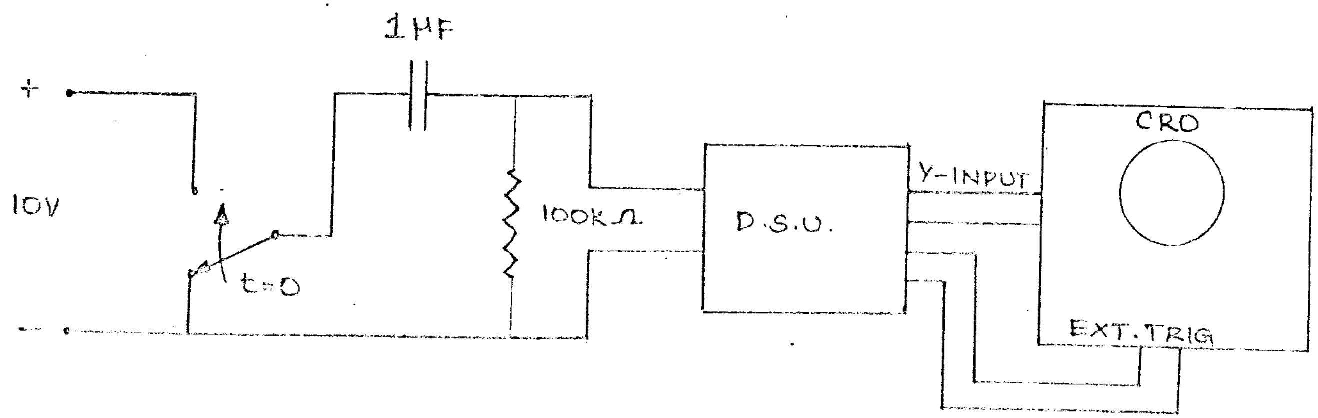


Fig.5.1. TEST SETUP FOR D.C. TRANSIENTS.

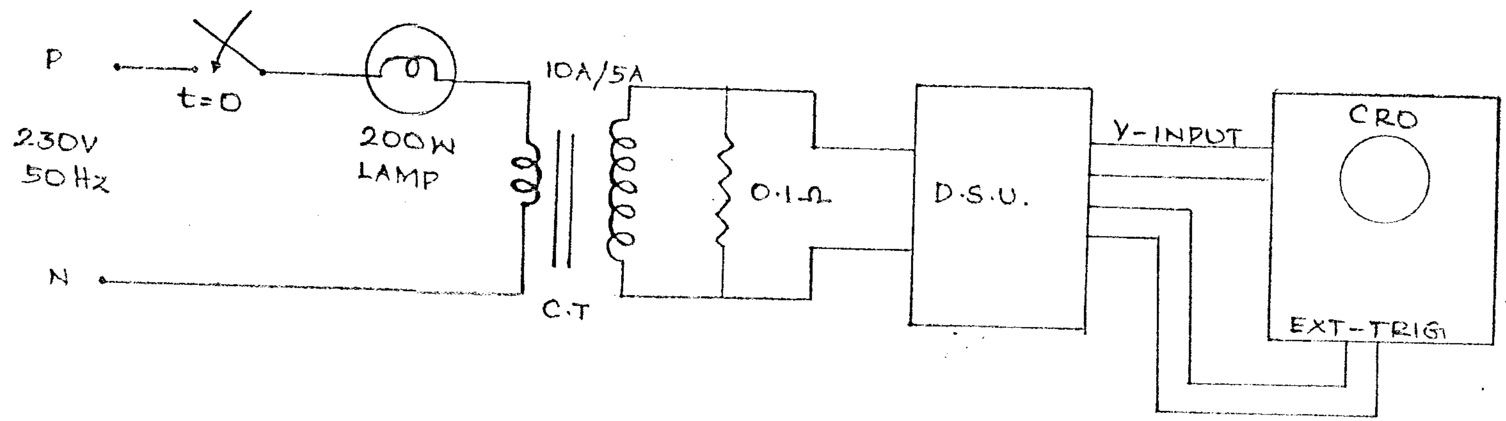


Fig. 5.2. TEST SETUP FOR A.C. TRANSIENTS

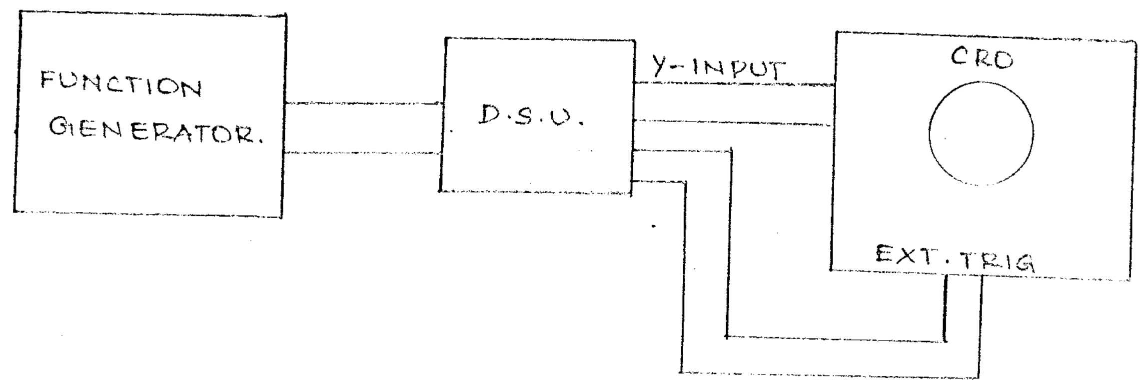


Fig. 5.3. TEST SETUP FOR REPETITIVE WAVEFORMS.

CHAPTER 6

CONCLUSION

The circuit of a Digital storage unit was designed, assembled on a PCB and tested. It is found to work satisfactorily. The total cost of the unit is approximately Rs 2000/=.

There is lot of scope for improving the unit.

* By use of high speed 'FLASH' type A/D converters the unit can store fast transients also.

* By incorporating multiplexing circuits and de-multiplexing circuits, multiple trace storage and display is possible.

* Incorporating additional pre-amplifiers and caliberated attenuators at the input,the input sensitivity (volts/div) can be enhanced in the 1-2-5 sequence of conventional oscilloscope input.

* ROLL & PRETRIGGER MODES of the storage can be implemented through software.

A commercially viabile unit having all the features mentioned above can be fabricated for a total cost of less than Rs 5000/=.

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3. JACOB MILLMAN, "MICROELECTRONICS, DIGITAL AND ANALOG CIRCUITS AND SYSTEMS", McGRAW - HILL BOOK COMPANY, INTERNATIONAL STUDENT EDITION.

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7. "INTEL 8085A USER MANUAL", JAN. 1981.

PROGRAM LISTING

PROGRAM LISTING

MAIN PROGRAM

ADDR	CODE	LABLE	MNEMONICS	COMMENTS
2000	3E		MVI A, 41	;CONFIGURE PORTS A- OUTPUT B&C -INPUT
2001	41			
2002	D3		OUT 10	
2003	10		LXI H,2C00	;BASE ADDRESS FOR STORAGE AREA
2004	21			
2005	00			
2006	2C			
2007	3E	REPEAT1:	MVI A,80	
2008	80			;CLEAR STORAGE AREA
2009	77		MOV M,A	
200A	00		NOP	
200B	23		INX H	
200C	7C		MOV A,H	
200D	FE		CPI 30	
200E	30			
200F	C2		JNZ REPEAT 1	
2010	07			
2011	20			
2012	DB	SCAN:	IN 13	
2013	13			
2014	5F		MOV E,A	;SAVE CONTROL STATUS WORD
2015	E6		ANI 07	;MASK TIME/DIV
2016	07			
2017	FE		CPI 07	
2018	07			
2019	CC		CZ STORE	;CALL "STORE" SUB -ROUTINE
201A	80			
201B	20			
201C	E6		ANI 60	;MASK TRIGGER BIT
201D	06			
201E	FE		CPI 60	;CHECK FOR TRIGGER ARMED
201F	06			
2020	CA		JZ SCAN	;JUMP TO SCAN
2021	12			
2022	20			
2023	E6		ANI 04	;MASK TRIGGER ARMED BIT
2024	04			
2025	CA		JZ SCAN	;CHECK FOR MODE
2026	12			
2027	20			
2028	3E	TRACE:	MVI A,12	
2029	12			
202A	D3		OUT 11	;OUTPUT SYNC.PULSE
202B	11			
202C	00		NOP	
202D	AF		XRA A	;CLEAR ACC.
202E	D3		OUT 11	;TERMINATE SYNC. PULSE

```
202F  11
2030  21                 LXIH,2C00        ;BASE ADRESS  OF
2031  00                                   STORAGE
2032  2C
2033  7E    DISPLAY:     MOV A,M
2034  E6                 ANI FC           ;MASK A1 & A0
2035  FC
2036  D3                 OUT 11           ;OUT DATA TO  DAC
2037  11
2038  23                 INX H            ;NEXT  DATA
2039  7C                 MOV A,H
203A  FE                 CPI 30           ;CHECK FOR COMPLETION
203B  30                                   (1024  DATA)
203C  CA                 JZ TRACE
203D  28
203E  20
203F  DB                 IN 13
2040  13
2041  5F                 MOV E,A          ;CONTROL STATUS IN  R
2042  E6                 ANI 07           ;MASK TIME/DIV BITS
2043  07
2044  FE                 CPI  07
2045  07
2046  CC                 CZ  STORE        ;CALL "STORE"  SUB-
2047  80                                   ROUTINE
2048  20
2049  E6                 ANI  60          ;MASK  TRIGGER  BIT
204A  06
204B  FE                 CPI  60          ;CHECK FOR TRIGGER
204C  06
204D  CA                 JZ ERASE         ;CLEAR OUTPUT
204E  5D
204F  20
2050  E6                 ANI 04           ;MASK TRIGGER BIT
2051  04
2052  00                 NOP
2053  00                 NOP
2054  00                 NOP
2055  00                 NOP
2056  00                 NOP
2057  00                 NOP
2058  00                 NOP
2059  00                 NOP
205A  C2                 JNZ  DISPLAY     ;CHECK FOR MODE
205B  33
205C  20
205D  3E    ERASE:       MVI A,80         ;CLEAR  PORT A
205E  80
205F  D3                 OUT  11
2060  11
2061  C3                 JMP  SCAN
2062  12
2063  20
```

"STORE SUB-ROUTINE"

```
2080  3E            MVI A,80       ;CLEAR OUTPUT
2081  80
2082  D3            OUT 11
2083  11
2084  7B            MOV  A,E       ;CONTROL  STATUS
2085  E6            ANI  18        ;MASK  TRIGGER  BITS
2086  18                            & MODE  BIT
2087  5F            MOV E,A        ;SAVE TIME/DIV IN E
2088  16            MVID,21
2089  21
208A  21            LXI H 2C00     ;BASE  ADDRESS
208B  00
208C  2C
208D  EB            XCHG           ;COUNT  TABLE ADDRESS
208E  4E            MOV C,M        ;DELAY  COUNT IN C
208F  EB            XCGH
2090  41  REPEAT2:  MOV B,C        ;WR/RD PULSE
2092  81
2093  D3            OUT 11
2094  11
2095  00            NOP
2096  00            NOP
2097  00            NOP
2098  00            NOP
2099  DE            IN  12         ;READ ADC
209A  12
209B  77            MOV M,A        ;STORE DATA
209C  3E            MOV A,80
209D  80
209E  D3            OUT 11         ;TERMINATE  WR/RD
209F  11                            PULSE
20A0  23            INX  H         ;NEXT DATA
20A1  76            MOV  A,H
20A2  FE            CPI 30         ;CHECK FOR
20A3  30                            COMPLETION
20A4  C8            R2             ;RETURN TO SCAN
20A5  05  REPEAT3:  DCRB           ;DELAY
20A6  C2            JNZ REPEAT3
20A7  A5
20A8  20
20A9  00            NOP
20AA  00            NOP
20AB  C3            JMP REPEAT 2
20AC  90
20AD  20
20AE
20AF
```

DATA IN COUNT TABLE

2100	0E	100 MICRO SECONDS
2108	24	200 MICRO SECONDS
2110	66	500 MICRO SECONDS
2118	D4	1000 MICROSECONDS

MICROPROCESSOR TRAINER KIT DETAILS

MICRO-85 SPECIFICATIONS

HARDWARE SPECIFICATIONS

1.CPU (Central Processing Unit)
Intel 8085 CPU at 3.072 MHz clock rate.

2.ROM (Read Only Memory)
A 4KB EPROM (2732) providing the powerful system software to use Micro-85 in minimum and maximum configurations.

Address : 0000 - 0FFF

3.RAM (Random Access Memory)
*2 Static RAM 6116, total 4 K bytes.

*Expandable to 16 K bytes using 8 K x 8 RAM (6264)

Address : 2000 - 2FFF for 4 K bytes
: 3000 - 3FFF

: 2000 - 3FFF for 16 K bytes
: 6000 - 7FFF

4.Input/Output :
Parrallel : 22 lines (One 8155)
I/O Address : 10 - 13 (Hex)
Serial : RS 232 C (8251)
Baud rate selectable form 300 to 9600 baud
Timer : One programmable channel Timer (8155)
Port Address :10 - 13 (Hex)
: Three programmable channel Timers (8253)
(Channel 0 is used as baud rate clock generator for 8251)
Port Address : F0-F5(Hex)

5.Display :
6 digit,0.3",7- segment green/yellow LED Display for ease of operation.

6.Keyboard
21 Keys including function keys and hexadecimal keys.

7.Speaker and Speaker Interface. (optional)
A. 2.25" diameter speaker is provided for user's expansion.

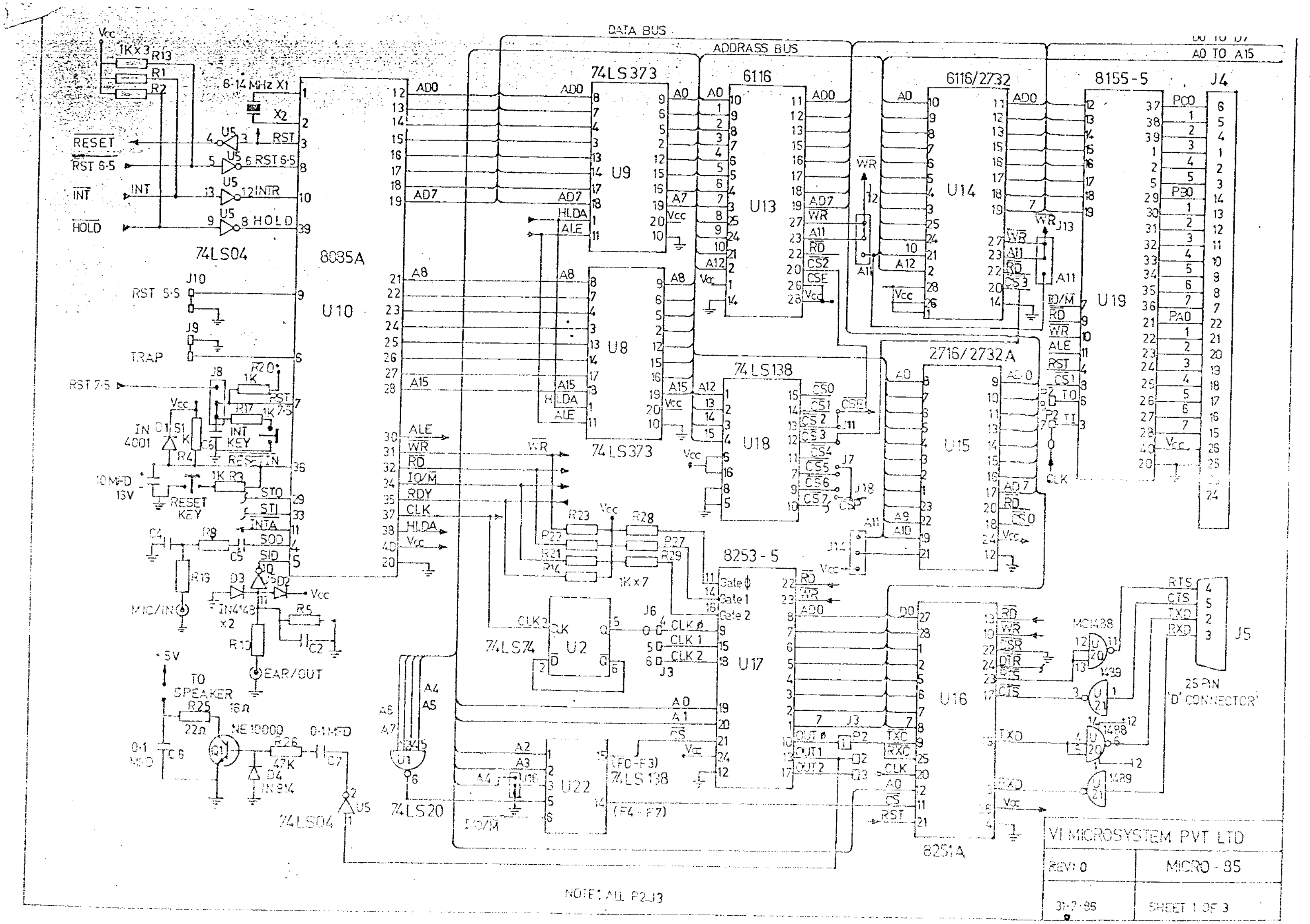
8.Audio tape Interface.

9.System power consumption.

+ 5 V : 550 ma
+ 12 V : 200 ma
- 12 V : 100 ma

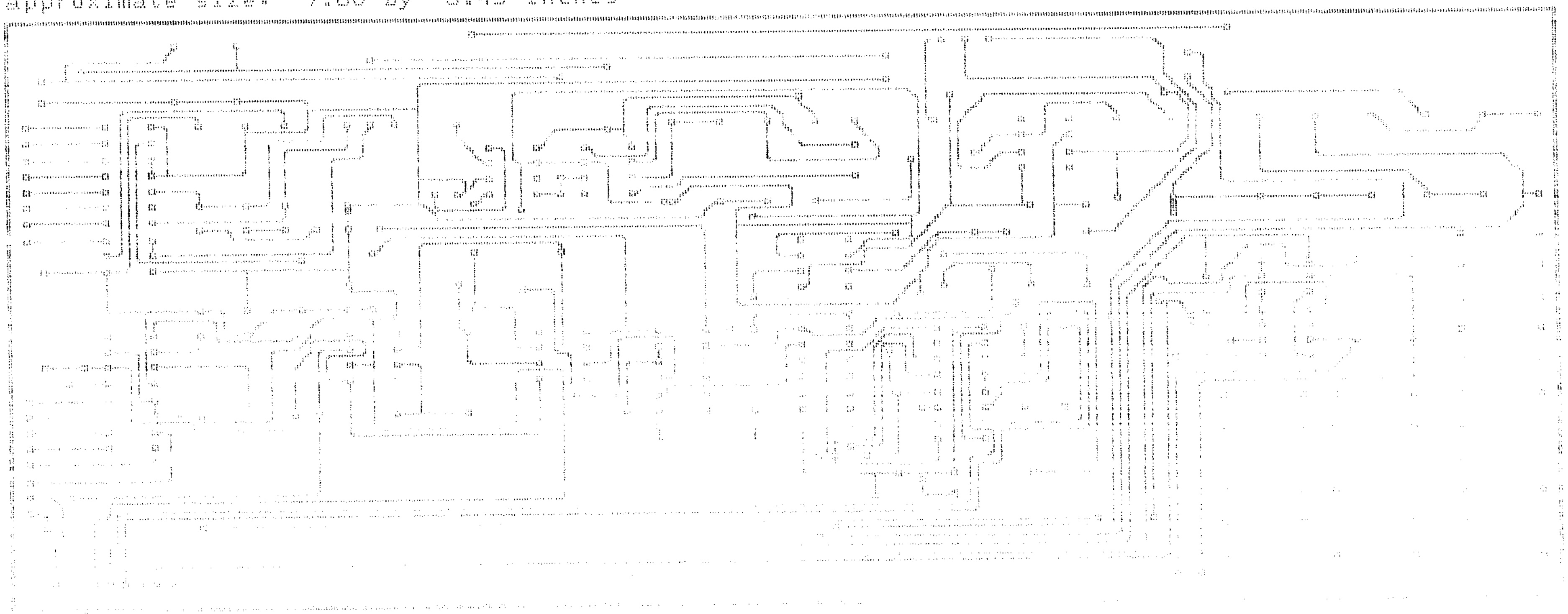
Parallel I/O port connector J4 pin assignments

Pin	Function	Pin	Function
1	Port PC bit 3	14	Port PB bit 0
2	Port PC bit 4	15	Port PA bit 7
3	Port PC bit 5	16	Port PA bit 6
4	Port PC bit 2	17	Port PA bit 5
5	Port PC bit 1	18	Port PA bit 4
6	Port PC bit 0	19	Port PA bit 3
7	Port PB bit 7	20	Port PA bit 2
8	Port PB bit 6	21	Port PA bit 1
9	Port PB bit 5	22	Port PA bit 0
10	Port PB bit 4	23	No connection
11	Port PB bit 3	24	No connection
12	Port PB bit 2	25	Ground
13	Port PB bit 1	26	+5 Volt


DATA BUS
ADDRASS BUS
D0 TO D7
A0 TO A15
8085A
U10
74LS04
74LS373
U9
U8
6116
U13
6116/2732
U14
2716/2732A
U15
8155-5
U19
J4
74LS138
U18
8253-5
U17
74LS74
U2
U22
74LS20
U16
8251A
J5
25 PIN
'D' CONNECTOR
MIC/IN
EAR/OUT
TO SPEAKER
RESET KEY
INT KEY
6·14 MHz X1
NOTE: ALL P2-J3
VI MICROSYSTEM PVT LTD
REV: 0
MICRO - 85
31-7-86
SHEET 1 OF 3

PCB LAYOUT

1X checkplot   27 Mar 1993   04:20:46
proj
v1.2 r3 holes: 390   solder side
approximate size: 9.60 by 3.45 inches



I.C DETAILS

National Semiconductor Corporation

LM741/LM741A/LM741C/LM741E Operational Amplifier

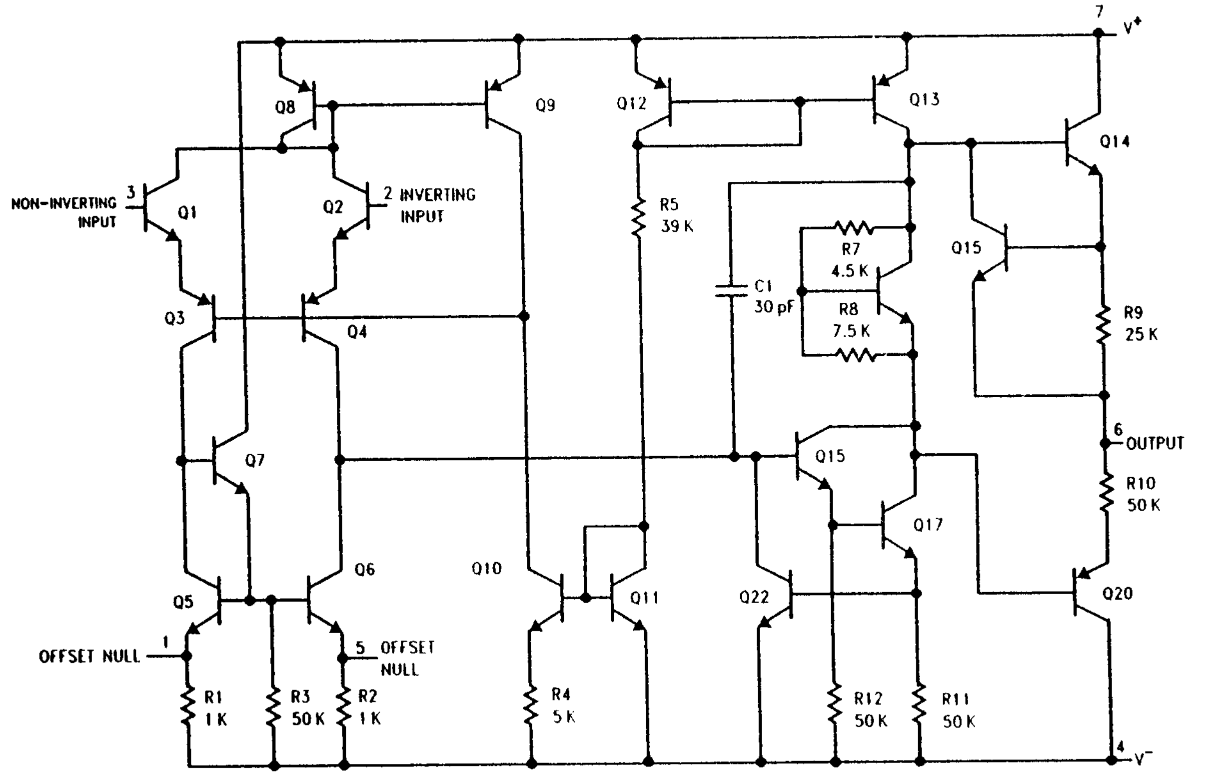
General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

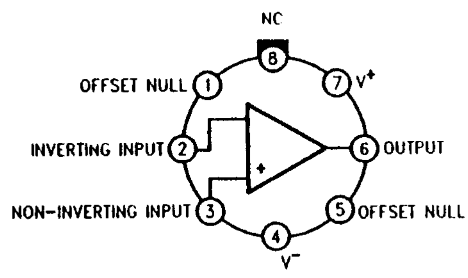
The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Schematic and Connection Diagrams (Top Views)



TL/H/9341–1

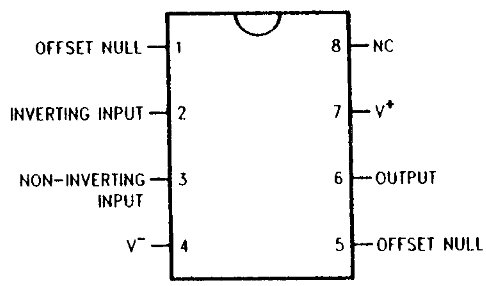
Metal Can Package



TL/H/9341–2

Order Number LM741H, LM741AH, LM741CH or LM741EH
See NS Package Number H08C

Dual-In-Line or S.O. Package



TL/H/9341–3

Order Number LM741CJ, LM741CM, LM741CN or LM741EN
See NS Package Number J08A, M08A or N08E

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \geq 10\ k\Omega$	±16									V
	$R_L \geq 2\ k\Omega$	±15									V
	$V_S = \pm 15V$										
	$R_L \geq 10\ k\Omega$				±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$				±10	±13		±10	±13		V
Output Short Circuit Current	$T_A = 25°C$	10	25	35		25			25		mA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
Common-Mode Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
	$R_S \leq 10\ k\Omega, V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \leq 50\ k\Omega, V_{CM} = \pm 12V$	80	95								dB
Supply Voltage Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \leq 50\Omega$	86	96								dB
	$R_S \leq 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		μs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 4)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/μs
Supply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM741A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741E	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			150							mW
	$T_A = T_{AMAX}$			150							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 1: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	TO-5 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100°C/W	100°C/W	150°C/W	195°C/W
θ_{jC} (Junction to Case)	N/A	N/A	80°C/W	N/A

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Unless otherwise specified, these specifications apply for $V_S = \pm 15V$, −55°C ≤ T_A ≤ +125°C (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0°C ≤ T_A ≤ +70°C.

Note 4: Calculated value from: BW (MHz) = 0.35/Rise Time(μs).

Note 5: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 5)

	LM741A	LM741E	LM741	LM741C
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1)	500 mW	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V	±30V
Input Voltage (Note 2)	±15V	±15V	±15V	±15V
Output Short Circuit Duration	Indefinite	Indefinite	Indefinite	Indefinite
Operating Temperature Range	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	100°C	150°C	100°C
Soldering Information				
N-Package (10 seconds)	260°C	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C	300°C
M-Package				
Vapor Phase (60 seconds)	215°C	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C	215°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 3)

Parameter	Conditions	LM741A/LM741E Min	LM741A/LM741E Typ	LM741A/LM741E Max	LM741 Min	LM741 Typ	LM741 Max	LM741C Min	LM741C Typ	LM741C Max	Uni
Input Offset Voltage	$T_A = 25°C$ $R_S \le 10\ k\Omega$					1.0	5.0		2.0	6.0	m
	$R_S \le 50\Omega$		0.8	3.0							m
	$T_{AMIN} \le T_A \le T_{AMAX}$ $R_S \le 50\Omega$			4.0							m
	$R_S \le 10\ k\Omega$						6.0			7.5	m
Average Input Offset Voltage Drift				15							μV/
Input Offset Voltage Adjustment Range	$T_A = 25°C, V_S = \pm 20V$	±10				±15			±15		m
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	n
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	n
Average Input Offset Current Drift				0.5							nA
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	n
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	μ
Input Resistance	$T_A = 25°C, V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		M
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5									M
Input Voltage Range	$T_A = 25°C$							±12	±13		
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					
Large Signal Voltage Gain	$T_A = 25°C, R_L \ge 2\ k\Omega$ $V_S = \pm 20V, V_O = \pm 15V$	50									V
	$V_S = \pm 15V, V_O = \pm 10V$				50	200		20	200		V
	$T_{AMIN} \le T_A \le T_{AMAX}$, $R_L \ge 2\ k\Omega$, $V_S = \pm 20V, V_O = \pm 15V$	32									V
	$V_S = \pm 15V, V_O = \pm 10V$				25			15			V
	$V_S = \pm 5V, V_O = \pm 2V$	10									V

National Semiconductor Corporation

LM78XX Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expanded to make the LM78XX series of regulators easy to use and mininize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

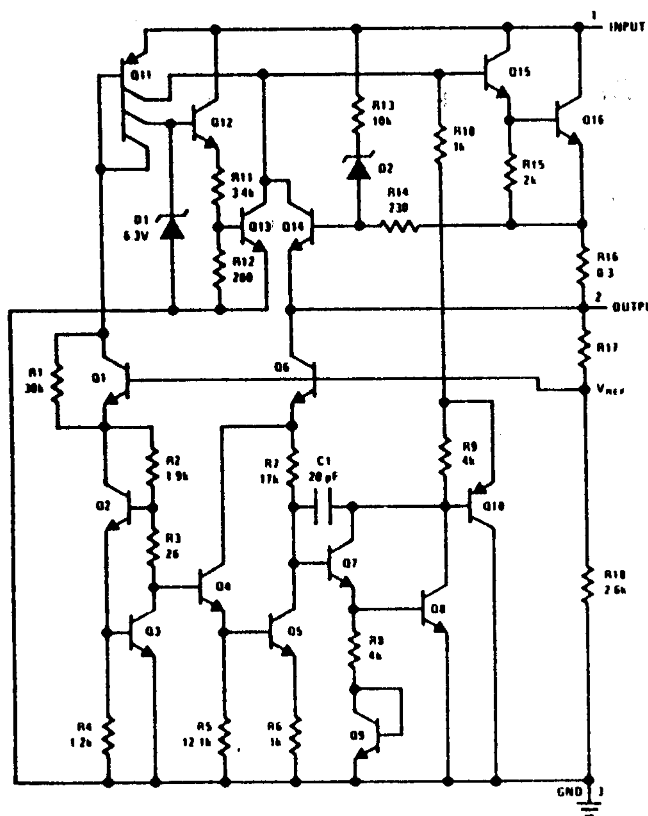
Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

Voltage Range

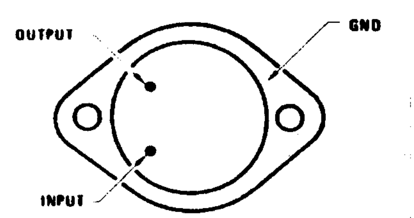
LM7805C	5V
LM7812C	12V
LM7815C	15V

Schematic and Connection Diagrams



TL/H/7746-1

Metal Can Package
TO-3 (K)
Aluminum

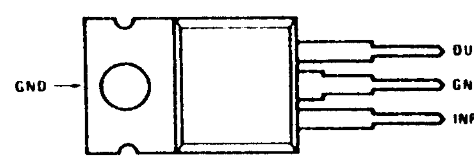


TL/H/7746-2

Bottom View

Order Number LM7805CK, LM7812CK or LM7815CK
See NS Package Number KC02A

Plastic Package
TO-220 (T)



TL/H/7746-3

Top View

Order Number LM7805CT, LM7812CT or LM7815CT
See NS Package Number T03B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage (V_O = 5V, 12V and 15V)	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range (T_A)	0°C to +70°C
Maximum Junction Temperature	
(K Package)	150°C
(T Package)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
TO-3 Package K	300°C
TO-220 Package T	230°C

Electrical Characteristics LM78XXC (Note 2) 0°C ≤ T_j ≤ 125°C unless otherwise noted.

Output Voltage				5V			12V			15V			Units
Input Voltage (unless otherwise noted)				10V			19V			23V			
Symbol	Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	T_j = 25°C, 5 mA ≤ I_O ≤ 1A		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A		4.75		5.25	11.4		12.6	14.25		15.75	V
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)			V
ΔV_O	Line Regulation	I_O = 500 mA	T_j = 25°C		3	50		4	120		4	150	mV
			ΔV_{IN}	(7 ≤ V_{IN} ≤ 25)			14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
			0°C ≤ T_j ≤ +125°C			50			120			150	mV
			ΔV_{IN}	(8 ≤ V_{IN} ≤ 20)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			V
		I_O ≤ 1A	T_j = 25°C			50			120			150	mV
			ΔV_{IN}	(7.5 ≤ V_{IN} ≤ 20)			(14.6 ≤ V_{IN} ≤ 27)			(17.7 ≤ V_{IN} ≤ 30)			V
			0°C ≤ T_j ≤ +125°C			25			60			75	mV
			ΔV_{IN}	(8 ≤ V_{IN} ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			V
ΔV_O	Load Regulation	T_j = 25°C	5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150	mV
			250 mA ≤ I_O ≤ 750 mA			25			60			75	mV
		5 mA ≤ I_O ≤ 1A, 0°C ≤ T_j ≤ +125°C				50			120			150	mV
I_Q	Quiescent Current	I_O ≤ 1A	T_j = 25°C			8			8			8	mA
			0°C ≤ T_j ≤ +125°C			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A				0.5			0.5			0.5	mA
		T_j = 25°C, I_O ≤ 1A				1.0			1.0			1.0	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			V
		I_O ≤ 500 mA, 0°C ≤ T_j ≤ +125°C				1.0			1.0			1.0	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
V_N	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40			75			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	I_O ≤ 1A, T_j = 25°C or	62	80		55	72		54	70		dB
			I_O ≤ 500 mA, 0°C ≤ T_j ≤ +125°C	62			55			54			dB
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			V
R_O	Dropout Voltage	T_j = 25°C, I_{OUT} = 1A			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz			8			18			19		mΩ
	Short-Circuit Current	T_j = 25°C			2.1			1.5			1.2		A
	Peak Output Current	T_j = 25°C			2.4			2.4			2.4		A
	Average TC of V_{OUT}	0°C ≤ T_j ≤ +125°C, I_O = 5 mA			0.6			1.5			1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	T_j = 25°C, I_O ≤ 1A			7.5		14.6			17.7			V

Note 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

Note 2: All characteristics are measured with capacitor across the input of 0.22 μF, and a capacitor across the output of 0.1μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

National Semiconductor Corporation

LM79XX Series 3-Terminal Negative Regulators

General Description

The LM79XX series of 3-terminal regulators is available with fixed output voltages of −5V, −12V, and −15V. These devices need only one external component—a compensation capacitor at the output. The LM79XX series is packaged in the TO-220 power package and is capable of supplying 1.5A of output current.

These regulators employ internal current limiting safe area protection and thermal shutdown for protection against virtually all overload conditions.

Low ground pin current of the LM79XX series allows output voltage to be easily boosted above the preset value with a resistor divider. The low quiescent current drain of these devices with a specified maximum change with line and load ensures good regulation in the voltage boosted mode.

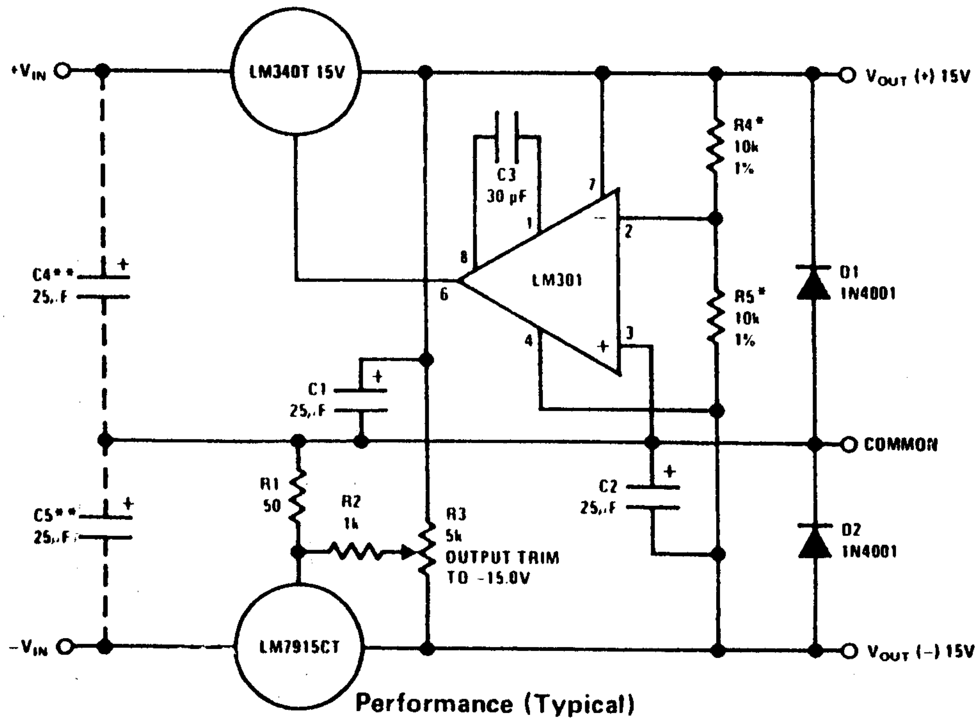
For applications requiring other voltages, see LM137 data sheet.

Features

- Thermal, short circuit and safe area protection
- High ripple rejection
- 1.5A output current
- 4% preset output voltage

Typical Applications

± 15V, 1 Amp Tracking Regulators



Performance (Typical)

TL/H/7340-1

	(−15)	(+15)
Load Regulation at $\Delta I_L = 1A$	40 mV	2 mV
Output Ripple, $C_{IN} = 3000\ \mu F$, $I_L = 1A$	100 μVrms	100 μVrms
Temperature Stability	50 mV	50 mV
Output Noise 10 Hz ≤ f ≤ 10 kHz	150 μVrms	150 μVrms

*Resistor tolerance of R4 and R5 determine matching of (+) and (−) outputs.

**Necessary only if raw supply filter capacitors are more than 3" from regulators.

Electrical Characteristics (Continued) Conditions unless otherwise noted: I_{OUT} = 500 mA, C_{IN} = 2.2 μF, C_{OUT} = 1 μF, 0°C ≤ T_J ≤ +125°C, Power Dissipation = 1.5W.

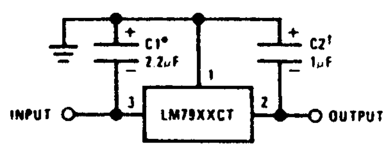
Part Number			LM7912C			LM7915C			Units
Output Voltage			12V			15V			
Input Voltage (unless otherwise specified)			−19V			−23V			
Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	T_J = 25°C 5 mA ≤ I_{OUT} ≤ 1A, P ≤ 15W	−11.5 −11.4 (−27 ≤ V_{IN} ≤ −14.5)	−12.0	−12.5 −12.6	−14.4 −14.25 (−30 ≤ V_{IN} ≤ −17.5)	−15.0	−15.6 −15.75	V V V
ΔV_O	Line Regulation	T_J = 25°C, (Note 2)	(−30 ≤ V_{IN} ≤ −14.5) −22 ≤ V_{IN} ≤ −16)	5 3	80 30	(−30 ≤ V_{IN} ≤ −17.5) (−26 ≤ V_{IN} ≤ −20)	5 3	100 50	mV V mV V
ΔV_O	Load Regulation	T_J = 25°C, (Note 2) 5 mA ≤ I_{OUT} ≤ 1.5A 250 mA ≤ I_{OUT} ≤ 750 mA		15 15 5	200 200 75		15 15 5	200 200 75	mV mV mV
I_Q	Quiescent Current	T_J = 25°C		1.5	3		1.5	3	mA
ΔI_Q	Quiescent Current Change	With Line With Load, 5 mA ≤ I_{OUT} ≤ 1A	(−30 ≤ V_{IN} ≤ −14.5)		0.5 0.5	(−30 ≤ V_{IN} ≤ −17.5)		0.5 0.5	mA V mA
V_n	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 Hz		300			375		μV
	Ripple Rejection	f = 120 Hz	54 (−25 ≤ V_{IN} ≤ −15)	70		54 (−30 ≤ V_{IN} ≤ −17.5)	70		dB V
	Dropout Voltage	T_J = 25°C, I_{OUT} = 1A		1.1			1.1		V
I_{OMAX}	Peak Output Current	T_J = 25°C		2.2			2.2		A
	Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0 C ≤ T_J ≤ 100°C		−0.8			−1.0		mV/°C

Note 1: For calculations of junction temperature rise due to power dissipation, thermal resistance junction to ambient (θ_{JA}) is 50°C/W (no heat sink) and 5°C/W (infinite heat sink).

Note 2: Regulation is measured at a constant junction temperature by pulse testing with a low duty cycle. Changes in output voltage due to heating effects must be taken into account.

Typical Applications (Continued)

Fixed Regulator



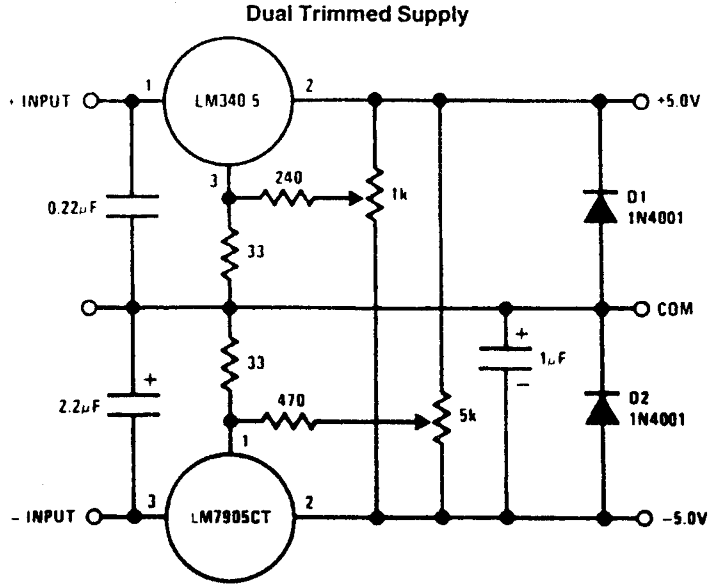
TL/H/7340-3

*Required if regulator is separated from filter capacitor by more than 3". For value given, capacitor must be solid tantalum. 25 μF aluminum electrolytic may be substituted.

†Required for stability. For value given, capacitor must be solid tantalum. 25 μF aluminum electrolytic may be substituted. Values given may be increased without limit.

For output capacitance in excess of 100 μF, a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

Dual Trimmed Supply



TL/H/7340-4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage	
(V_o = 5V)	−35V
(V_o = 12V and 15V)	−40V
Input-Output Differential	
(V_o = 5V)	25V
(V_o = 12V and 15V)	30V
Power Dissipation (Note 1)	Internally Limited
Operating Junction Temperature Range	0°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	230°C

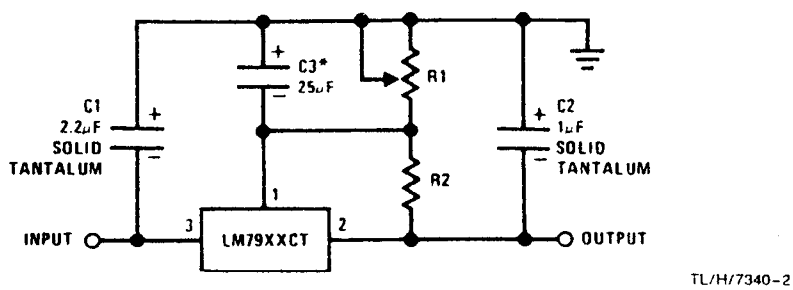
Electrical Characteristics

Conditions unless otherwise noted: I_{OUT} = 500 mA, C_{IN} = 2.2 μF, C_{OUT} = 1 μF, 0°C ≤ T_J ≤ +125°C, Power Dissipation ≤ 1.5W.

Part Number			LM7905C			Units
Output Voltage			5V			
Input Voltage (unless otherwise specified)			−10V			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	
V_O	Output Voltage	T_J = 25°C	−4.8	−5.0	−5.2	V
		5 mA ≤ I_{OUT} ≤ 1A,	−4.75		−5.25	V
		P ≤ 15W		(−20 ≤ V_{IN} ≤ −7)		V
ΔV_O	Line Regulation	T_J = 25°C, (Note 2)		8	50	mV
				(−25 ≤ V_{IN} ≤ −7)		V
				2	15	mV
				(−12 ≤ V_{IN} ≤ −8)		V
ΔV_O	Load Regulation	T_J = 25°C, (Note 2)				mV
		5 mA ≤ I_{OUT} ≤ 1.5A		15	100	mV
		250 mA ≤ I_{OUT} ≤ 750 mA		5	50	mV
I_Q	Quiescent Current	T_J = 25°C		1	2	mA
ΔI_Q	Quiescent Current Change	With Line			0.5	mA
				(−25 ≤ V_{IN} ≤ −7)		V
		With Load, 5 mA ≤ I_{OUT} ≤ 1A			0.5	mA
V_n	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 Hz		125		μV
	Ripple Rejection	f = 120 Hz	54	66		dB
				(−18 ≤ V_{IN} ≤ −8)		V
	Dropout Voltage	T_J = 25°C, I_{OUT} = 1A		1.1		V
I_{OMAX}	Peak Output Current	T_J = 25°C		2.2		A
	Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0 C ≤ T_J ≤ 100°C		0.4		mV/°C

Typical Applications (Continued)

Variable Output



TL/H/7340-2

*Improves transient response and ripple rejection. Do not increase beyond 50 μF.

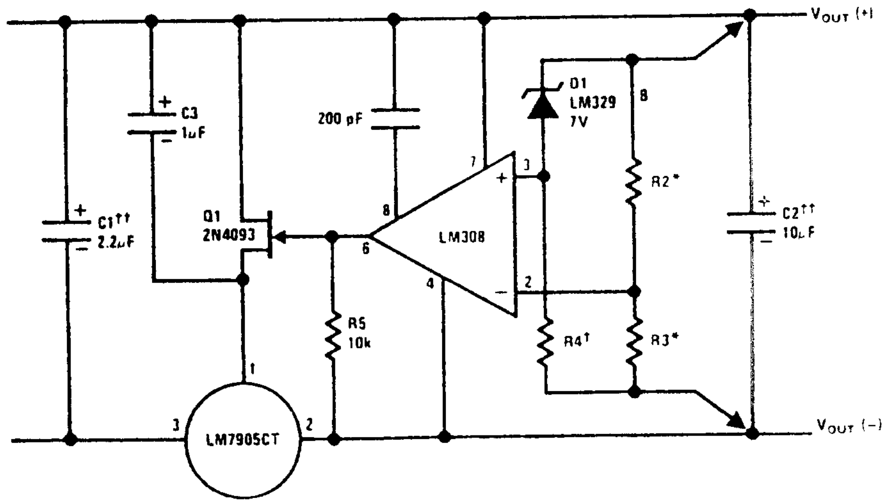
$$V_{OUT} = V_{SET}\left(\frac{R1 + R2}{R2}\right)$$

Select R2 as follows:

LM7905CT	300Ω
LM7912CT	750Ω
LM7915CT	1k

Typical Applications (Continued)

High Stability 1 Amp Regulator



TL/H/7340-5

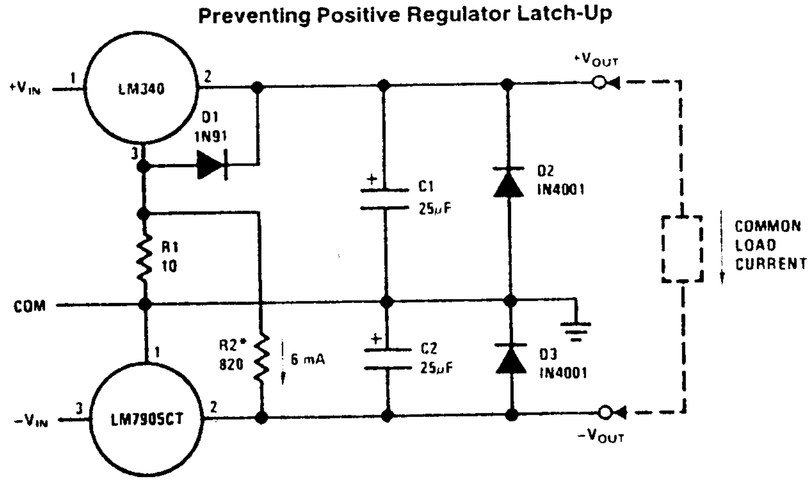
Load and line regulation < 0.01% temperature stability ≤ 0.2%

†Determine Zener current

††Solid tantalum

*Select resistors to set output voltage. 2 ppm/°C tracking suggested

Preventing Positive Regulator Latch-Up

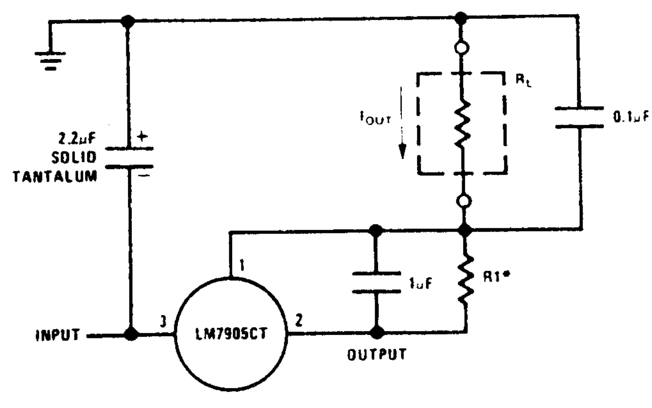


TL/H/7340-6

R1 and D1 allow the positive regulator to "start-up" when $+V_{IN}$ is delayed relative to $-V_{IN}$ and a heavy load is drawn between the outputs. Without R1 and D1, most three-terminal regulators will not start with heavy (0.1 A-1A) load current flowing to the negative regulator, even though the positive output is clamped by D2.

*R2 is optional. Ground pin current from the positive regulator flowing through R1 will increase $+V_{OUT} \approx 60$ mV if R2 is omitted.

Current Source

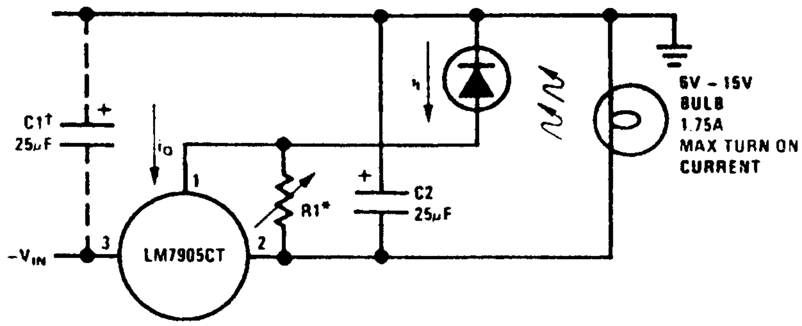


$^*I_{OUT} = 1\text{ mA} + \frac{5V}{R1}$

TL/H/7340-7

Typical Applications (Continued)

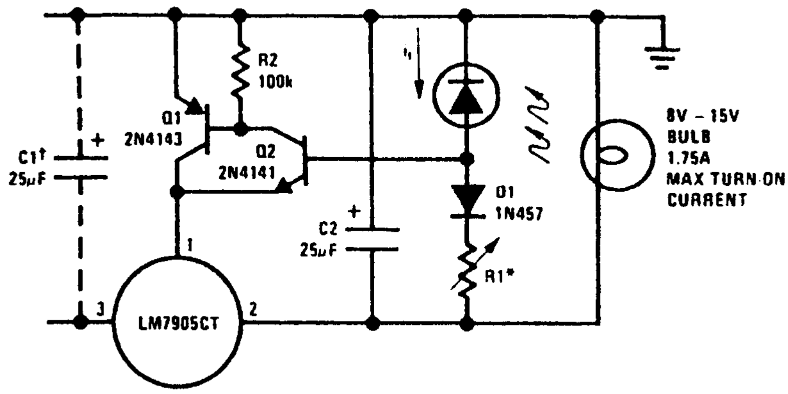
Light Controllers Using Silicon Photo Cells



TL/H/7340-8

*Lamp brightness increase until $i_l = i_O$ (≈ 1 mA) + 5V/R1.

†Necessary only if raw supply filter capacitor is more than 2" from LM7905CT



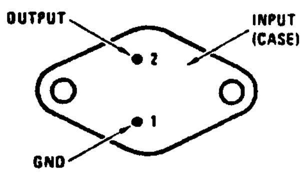
TL/H/7340-9

*Lamp brightness increases until i_l = 5V/R1 (I_l can be set as low as 1 µA)

†Necessary only if raw supply filter capacitor is more than 2" from LM7905CT

Connection Diagrams

TO-3 Package



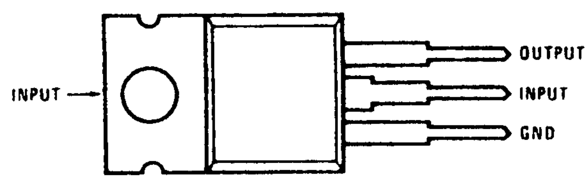
TL/H/7340-10

Bottom View

Order Number LM7905CK, LM7912CK or LM7915CK

See NS Package Number KC02A

TO-220 Package



TL/H/7340-11

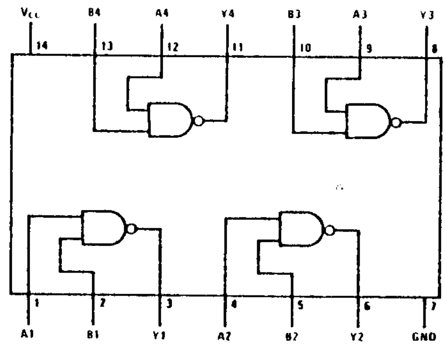
Top View

Order Number LM7905CT, LM7912CT or LM7915CT

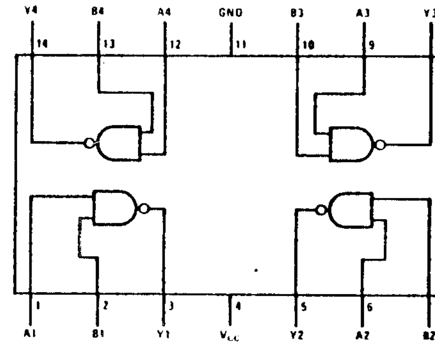
See NS Package Number TO3B

00 Quad 2-Input NAND Gates

$Y = \overline{AB}$



5400/7400(J), (N); 54H00/74H00(J), (N); 54L00/74L00(J), (N); 54LS00/74LS00(J),(N),(W); 74S00(N)

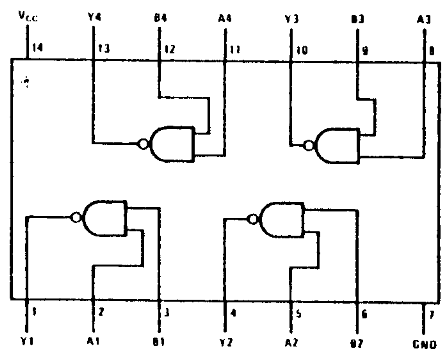


5400/7400(W); 54L00/74L00(W)

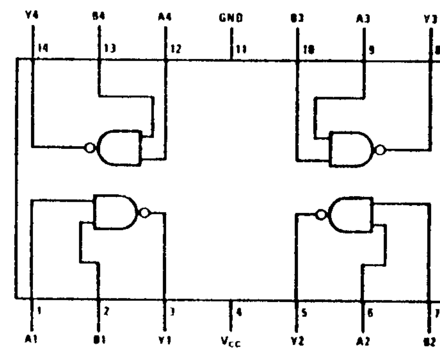
See page 1-36 for electrical tables.

01 Quad 2-Input NAND Gates with Open-Collector Outputs

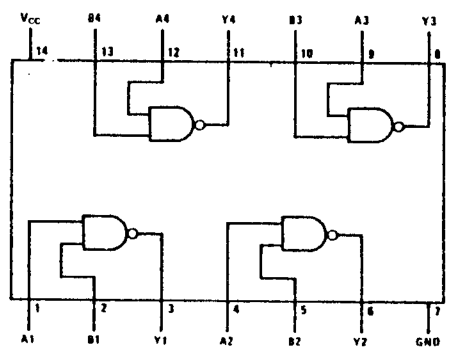
$Y = \overline{AB}$



5401/7401(J), (N); 54LS01/74LS01(J), (N), (W)



5401/7401(W); 54L01/74L01(W)

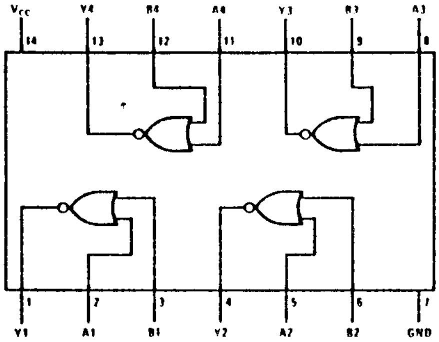


54H01/74H01(J), (N)

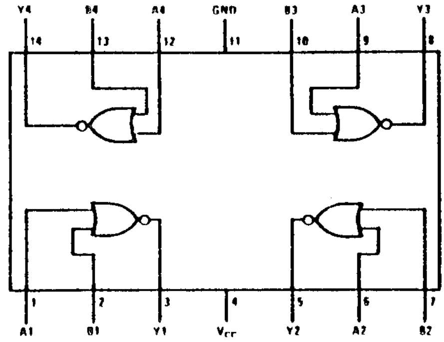
See page 1-38 for electrical tables.

02 Quad 2-Input NOR Gates

$Y = \overline{A+B}$



5402/7402(J), (N); 54L02/74L02(J), (N); 54LS02/74LS02(J), (N), (W); 74S02(N)

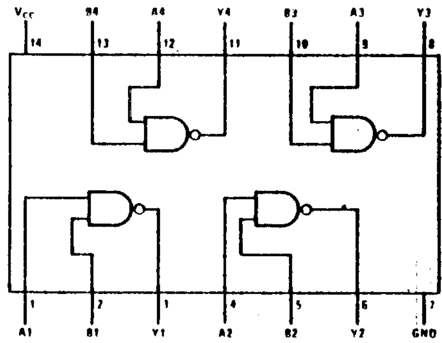


5402/7402(W); 54L02/74L02(W)

See page 1-40 for electrical tables.

03 Quad 2-Input NAND Gates with Open-Collector Outputs

$Y = \overline{AB}$

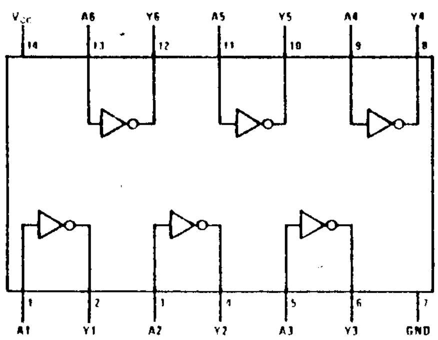


5403/7403(J), (N); 54L03/74L03(J), (N); 54LS03/74LS03(J), (N), (W); 74S03(N)

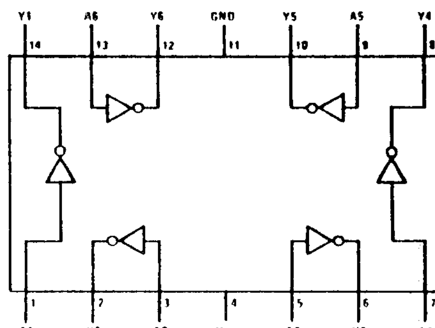
See page 1-38 for electrical tables.

04 Hex Inverters

$Y = \overline{A}$



5404/7404(J), (N); 54H04/74H04(J), (N); 54L04/74L04(J), (N), 54LS04/74LS04(J),(N),(W); 74S04(N)



5404/7404(W); 54L04/74L04(W)

See page 1-36 for electrical tables.

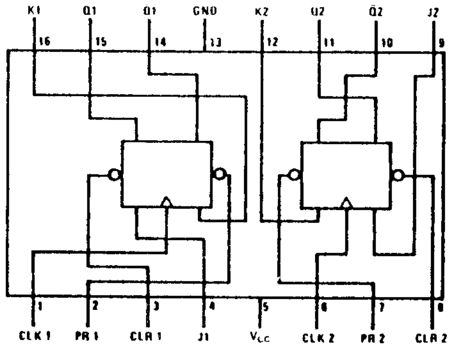
76 Dual J-K Flip-Flops with Preset and Clear

TRUTH TABLE
76, H76

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓	L	L	Q0	Q̄0
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	

TRUTH TABLE
LS76

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	Q̄0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	Q̄0



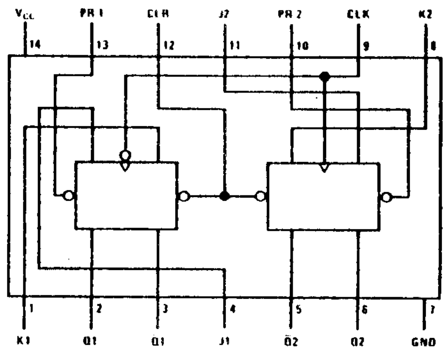
5476/7476(J), (N), (W); 54H76/74H76(J), (N);
54LS76/74LS76(J), (N), (W)

See page 1-62 (76), 1-64 (H76), 1-68 (LS76) for electrical tables.

78 Dual J-K Flip-Flops with Preset, Common Clear, and Common Clock

TRUTH TABLE
H78, L78

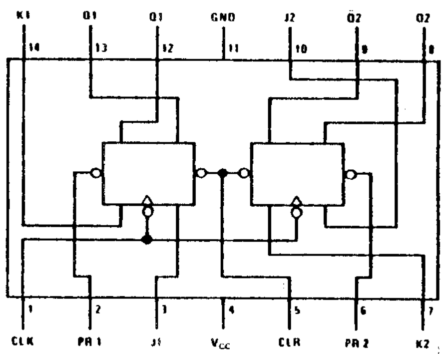
INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓	L	L	Q0	Q̄0
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	



54H78/74H78(J),(N)

TRUTH TABLE
LS78

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	Q̄0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	Q̄0



54L78/74L78(J), (N), (W);
54LS78/74LS78(J), (N), (W)

See page 1-64 (H78), 1-66 (L78), 1-68 (LS78) for electrical tables.

Notes: ⊓ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.

Q0 = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

National Semiconductor Corporation

Sample and Hold Selection Guide

	LF198A	LF398A	LF198	LF398	LF298	Units
Accuracy Gain/Offset Error	0.01	0.01	0.02	0.02	0.02	% Max
Offset Voltage	2	3	5	10	5	mV Max
Droop Rate (25°C) C_S = 1000 pF C_S = 10000 pF	30 3	30 3	30 3	30 3	30 3	mV/sec
Acquisition Time (25°C) C_S = 1000 pF C_S = 10000 pF	4 20	4 20	4 20	4 20	4 20	μs
Aperture Time (25°C)	25	25	25	25	25	[illegible]
Temperature Range	−55 to +125	0 to +70	−55 to +125	0 to +70	−25 to +[illegible]	[illegible]
Comment	Low Drift	Low Drift	General Purpose	General Purpose	Low Drift	

National Semiconductor Corporation

LF198/LF298/LF398, LF198A/LF398A Monolithic Sample and Hold Circuits

General Description

The LF198/LF298/LF398 are monolithic sample and hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 μF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

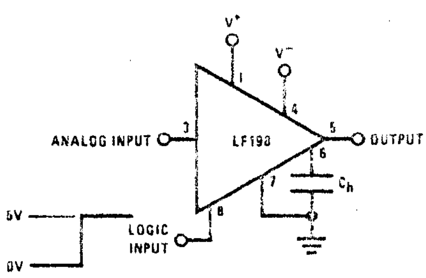
Features

- Operates from ±5V to ±18V supplies
- Less than 10 μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at C_h = 0.01 μF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

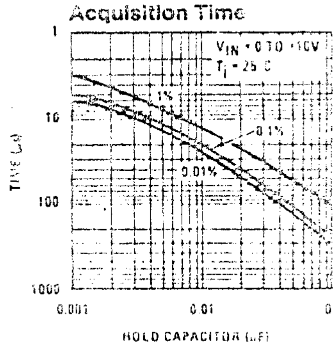
Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies. It is available in an 8-lead TO-5 package.

An "A" version is available with tightened electrical specifications.

Typical Connection and Performance Curve

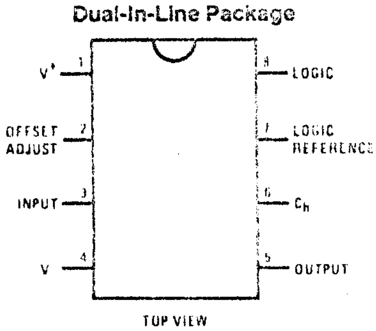


Acquisition Time



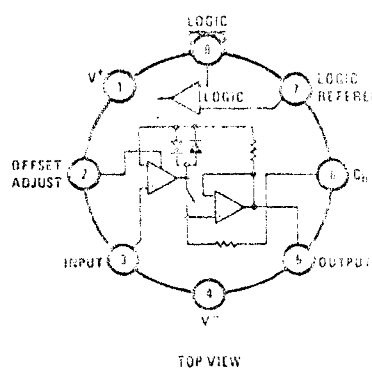
Connection Diagrams

Dual-In-Line Package



Order Number LF398N or LF398AN
See NS Package Number N08E

Metal Can Package



Order Number LF198H, LF298H, LF398H, LF198AH or LF398AH
See NS Package Number H08C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Package Limitation) (Note 1)	500 mW
Operating Ambient Temperature Range	
LF198/LF198A	−55°C to +125°C
LF298	−25°C to +85°C
LF398/LF398A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Input Voltage	Equal to Supply V[illegible]
Logic To Logic Reference Differential Voltage (Note 2)	[illegible]
Output Short Circuit Duration	[illegible]
Hold Capacitor Short Circuit Duration	[illegible]
Lead Temperature (Soldering, 10 seconds)	[illegible]

Thermal Resistance (θ_{JA}) (typicals)

H package 215°C/W (Board mount in still air)

85°C/W (Board mount in 400LF/min air [illegible])

N package 115°C/W

θ_{JC} (typical) 20°C/W

Electrical Characteristics (Note 3)

Parameter	Conditions	LF198/LF298			LF398			[illegible]
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage, (Note 6)	T_j = 25°C Full Temperature Range		1	3 5		2	7 10	[illegible]
Input Bias Current, (Note 6)	T_j = 25°C Full Temperature Range		5	25 75		10	50 100	[illegible]
Input Impedance	T_j = 25°C		10^{10}			10^{10}		[illegible]
Gain Error	T_j = 25°C, R_L = 10k Full Temperature Range		0.002	0.005 0.02		0.004	0.01 0.02	[illegible]
Feedthrough Attenuation Ratio at 1 kHz	T_j = 25°C, C_h = 0.01 μF	86	96		80	90		[illegible]
Output Impedance	T_j = 25°C, "HOLD" mode Full Temperature Range		0.5	2 4		0.5	4 6	[illegible]
"HOLD" Step, (Note 4)	T_j = 25°C, C_h = 0.01 μF, V_{OUT} = 0		0.5	2.0		1.0	2.5	[illegible]
Supply Current, (Note 6)	$T_j \geq$ 25°C		4.5	5.5		4.5	6.5	[illegible]
Logic and Logic Reference Input Current	T_j = 25°C		2	10		2	10	[illegible]
Leakage Current into Hold Capacitor (Note 6)	T_j = 25°C, (Note 5) Hold Mode		30	100		30	200	[illegible]
Acquisition Time to 0.1%	ΔV_{OUT} = 10V, C_h = 1000 pF C_h = 0.01 μF		4 20			4 20		[illegible]
Hold Capacitor Charging Current	$V_{IN} - V_{OUT}$ = 2V		5			5		[illegible]
Supply Voltage Rejection Ratio	V_{OUT} = 0	80	110		80	110		[illegible]
Differential Logic Threshold	T_j = 25°C	0.8	1.4	2.4	0.8	1.4	2.4	[illegible]

Electrical Characteristics (Continued) (Note 3)

Parameter	Conditions	LF198A			LF398A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage, (Note 6)	$T_j = 25°C$ Full Temperature Range		1	1 2		2	2 3	mV mV
Input Bias Current, (Note 6)	$T_j = 25°C$ Full Temperature Range		5	25 75		10	25 50	nA nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k$ Full Temperature Range		0.002	0.005 0.01		0.004	0.005 0.01	% %
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\ \mu F$	86	96		86	96		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode Full Temperature Range		0.5	1 4		0.5	1 6	Ω Ω
"HOLD" Step, (Note 4)	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	1		1.0	1	mV
Supply Current, (Note 6)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	$T_j = 25°C$, (Note 5) Hold Mode		30	100		30	100	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000\ pF$ $C_h = 0.01\ \mu F$		4 20	6 25		4 20	6 25	μs μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	90	110		90	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Note 1: The maximum junction temperature of the LF198/LF198A is 150°C, for the LF298, 115°C, and for the LF398/LF398A, 100°C. When operating at elevated ambient temperature, the power dissipation must be derated based on a thermal resistance (θ_{jA}) of 150°C/W.

Note 2: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 3: Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, [illegible] and $R_L = 10\ k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

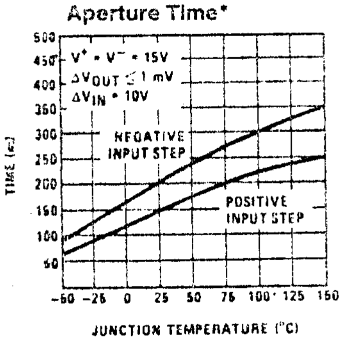
Note 4: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional [illegible] step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated [illegible] be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 6: These parameters guaranteed over a supply voltage range of ± 5 to ± 18V, and an input range of $-V_S + 3.5V \leq V_{IN} \leq +V_S - 3.5V$.

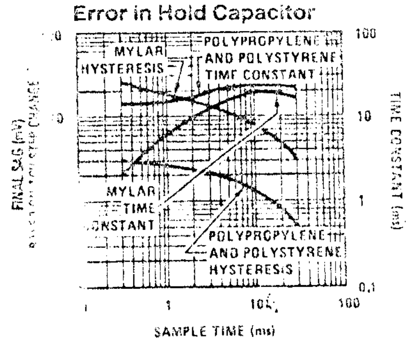
Typical Performance Characteristics

Aperture Time*

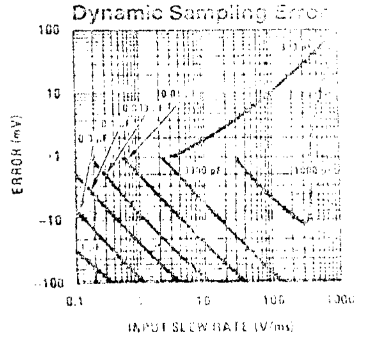


*See Definition of Terms

Dielectric Absorption Error in Hold Capacitor

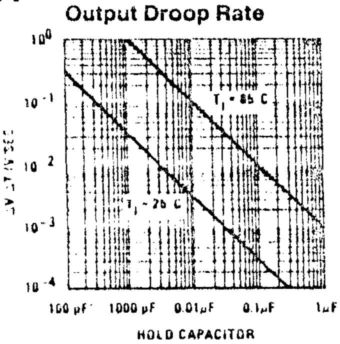


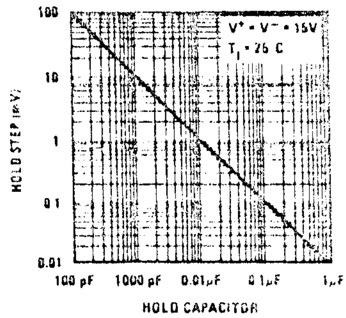
Dynamic Sampling Error

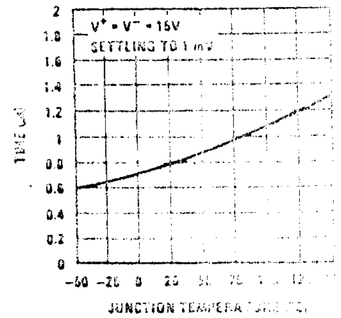


TL/H/5692

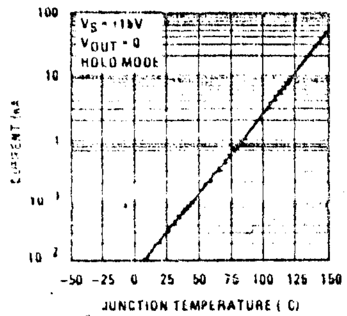
Typical Performance Characteristics (Continued)

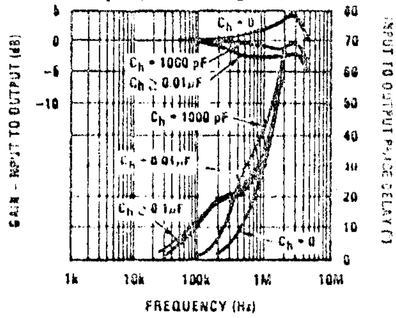
Output Droop Rate


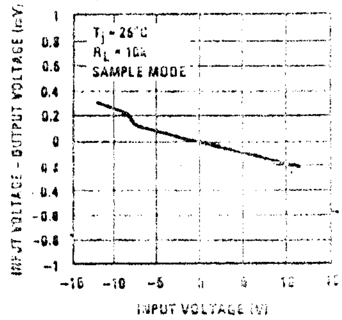
Hold Step


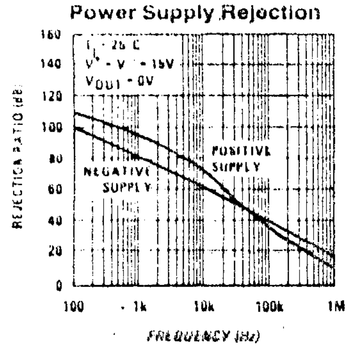
"Hold" Settling Time*


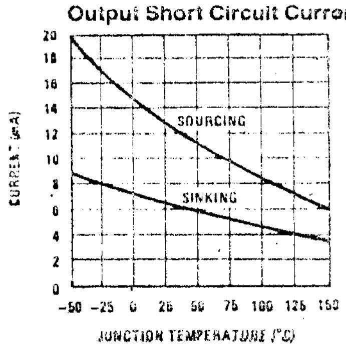
*See definition

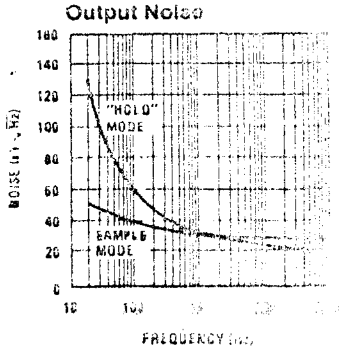
Leakage Current into Hold Capacitor


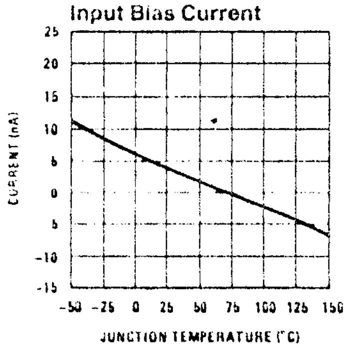
Phase and Gain (Input to Output, Small Signal)


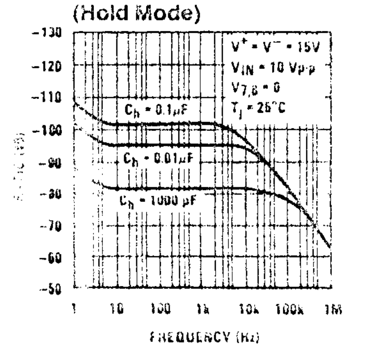
Gain Error


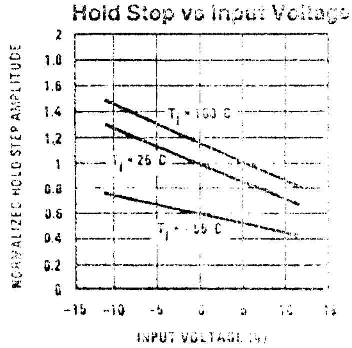
Power Supply Rejection


Output Short Circuit Current


Output Noise


Input Bias Current


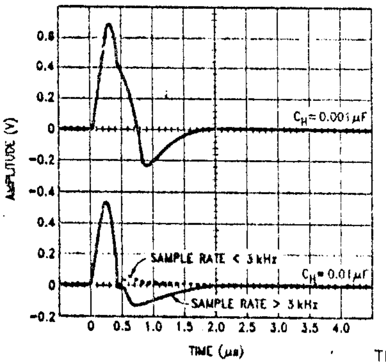
Feedthrough Rejection Ratio (Hold Mode)


Hold Step vs Input Voltage


TL/H/5692-

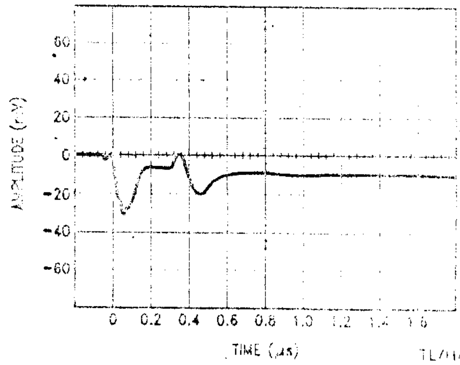
Typical Performance Characteristics (Continued)

Output Transient at Start of Sample Mode



TL/H/5692-12

Output Transient at Start of Hold Mode

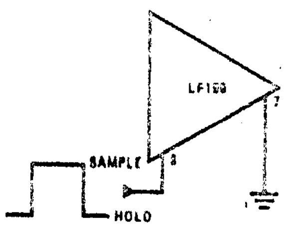


TL/H/5692-13

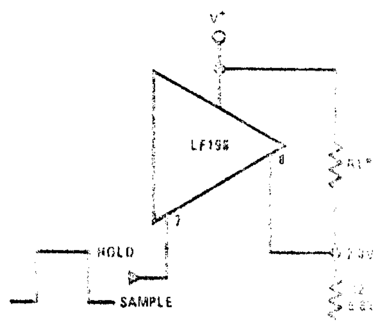
Logic Input Configurations

TTL & CMOS

3V ≤ V_L (Hi State) ≤ 7V



Threshold = 1.4V

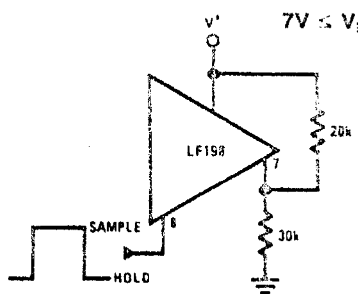


Threshold = 1.4V

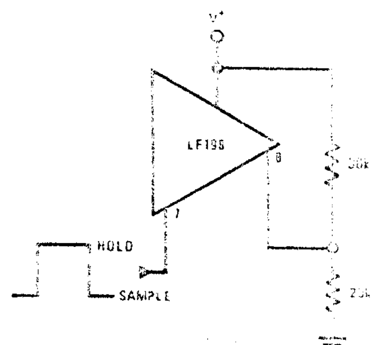
*Select for 2.8V at pin 8

CMOS

7V ≤ V_L (Hi State) ≤ 15V

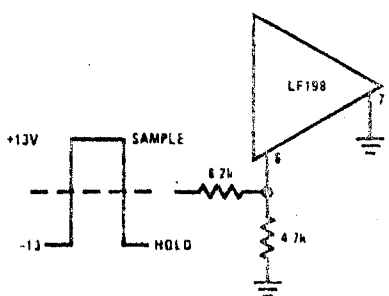


Threshold = 0.6 (V+) + 1.4V

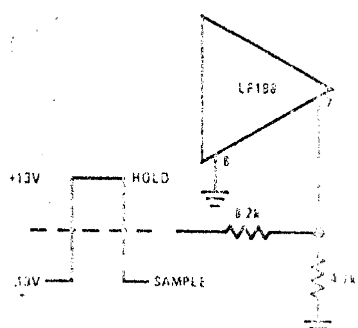


Threshold = 0.6 (V+) − 1.4V

Op Amp Drive



Threshold ≈ +4V



Threshold ≈ −4V

National Semiconductor Corporation

ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

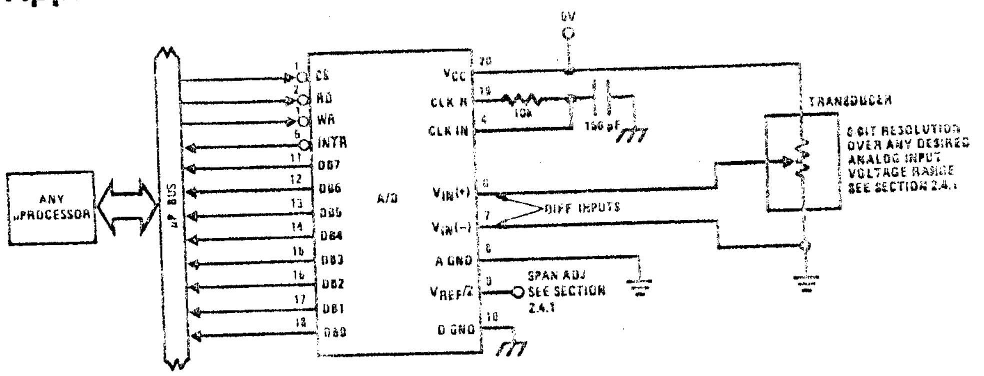
Features

- Compatible with 8080 µP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

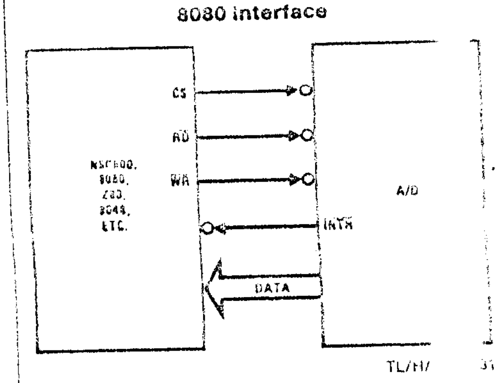
- Resolution 8 bits
- Total error ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time 100 µs

Typical Applications



TL/H/5671-1

8080 Interface



TL/H/ 31

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC}+0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LJ	$-55°C \le T_A \le +125°C$
ADC0801/02/03/04LCJ	$-40°C \le T_A \le +85°C$
ADC0801/02/03/05LCN	$-40°C \le T_A \le +85°C$
ADC0804LCN	$0°C \le T_A \le +70°C$
ADC0802/03/04LCV	$0°C \le T_A \le +70°C$
ADC0802/03/04LCWM	$0°C \le T_A \le +70°C$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±1/4	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$=2.500 V_{DC}			±1/2	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±1/2	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$=2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			±1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±1/8	LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC} ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/16	±1/8	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC} and T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK}=640 kHz (Note 6)	103		114	µs
T_C	Conversion Time	(Note 5, 6)	66		73	1/f_{CLK}
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC}=5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$=0 V_{DC}, f_{CLK}=640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$=0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = 5V_{DC} and $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 4.75 V_{DC}			0.8	[illegible]
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN} = 5 V_{DC}		0.005	1	[illegible]
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN} = 0 V_{DC}	−1	−0.005		[illegible]
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T−	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	[illegible]
V_H	CLK IN (Pin 4) Hysteresis (V_T+)−(V_T−)		0.6	1.3	2.0	[illegible]
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O = 360 µA, V_{CC} = 4.75 V_{DC}			0.4	[illegible]
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O = −360 µA, V_{CC} = 4.75 V_{DC}	2.4			[illegible]
DATA OUTPUTS AND INTR						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs INTR Output	 I_{OUT} = 1.6 mA, V_{CC} = 4.75 V_{DC} I_{OUT} = 1.0 mA, V_{CC} = 4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O = −360 µA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O = −10 µA, V_{CC} = 4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT} = 0 V_{DC} V_{OUT} = 5 V_{DC}	−3		 3	µADC µADC
I_{SOURCE}		V_{OUT} Short to Gnd, T_A = 25°C	4.5	6		[illegible]
I_{SINK}		V_{OUT} Short to V_{CC}, T_A = 25°C	9.0	16		[illegible]
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/[illegible]5 ADC0804LCN/LCV/LCW[illegible]	f_{CLK} = 640 kHz, V_{REF}/2 = NC, T_A = 25°C and $\overline{CS}$ = 5V		 1.1 1.9	 1.8 2.5	[illegible]

Note 1: Absolute Maximum Ratings indicate limits be[illegible] ond which damage to the device may occur. DC and AC electrical specifications do not apply wh[illegible] the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to [illegible], unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, [illegible]m V_{CC} [illegible] Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \ge V_{IN}(+)$ the digital [illegible]put cod[illegible] will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will conduct for analog input voltages one di[illegible] drop b[illegible] w ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} [illegible] as high level analog inputs (5V) can cau[illegible] this inpu[illegible] ode to conduct—especially at elevated temperatures, and cause errors for analog inputs [illegible] spec allows 50 mV forward bias of eith[illegible] diode. T[illegible] means that as long as the analog V_{IN} does not exceed the supply voltage by more than [illegible] code will be correct. To achieve an abs[illegible] to 0 V_{DC} 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over [illegible] variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} [illegible] 640 kH[illegible] higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle [illegible] extended so long as the minimum cloc[illegible] gh time [illegible] val or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pu[illegible] up to 8 [illegible] periods may be required before the internal clock phases are proper to start the conversion pro[illegible] start request is internally latched, see [illegible]re 2 an[illegible] tion 2.0.

Note 7: The $\overline{CS}$ input is assumed to b[illegible] the W[illegible] be input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width [illegible] the converter in a reset mode and the [illegible] of con[illegible] on is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

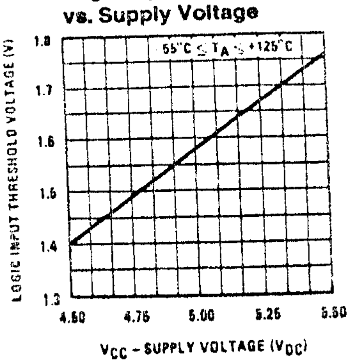
Note 8: None of these A/Ds requires [illegible] ro adjus[illegible] section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

Note 9: The V_{REF}/2 pin is the center p[illegible] of a tw[illegible] tor divider connected from V_{CC} to ground. Each resistor is 2.2k, except for the ADC0804LCJ [illegible] resistor is 16k. Total ladder input resis[illegible] is the [illegible] of the two equal resistors.

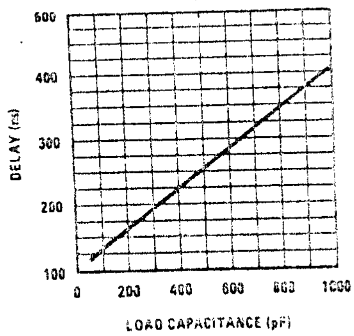
Note 10: Human body model, 100 pF [illegible] harged [illegible] 1.5 kΩ resistor.

Typical Performance Characteristics

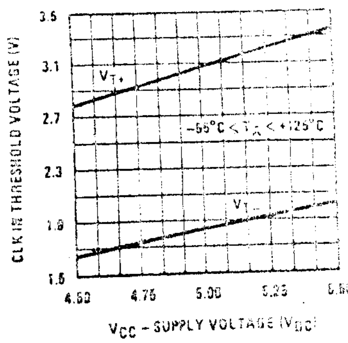
Logic Input Threshold Voltage vs. Supply Voltage



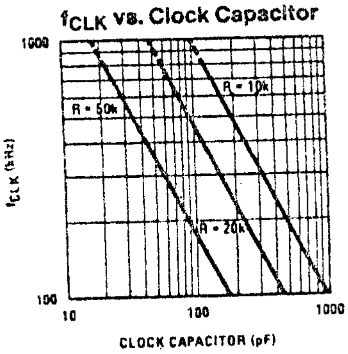
Delay From Falling Edge of RD to Output Data Valid vs. Load Capacitance



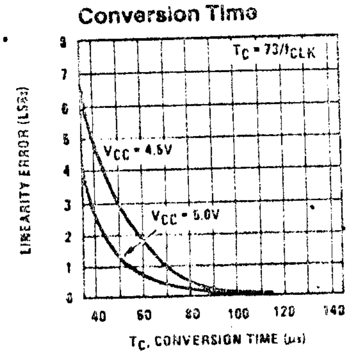
CLK IN Schmitt Trip Levels vs. Supply Voltage



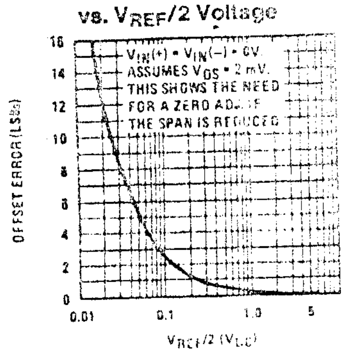
fCLK vs. Clock Capacitor



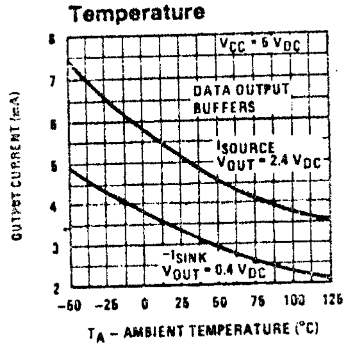
Full-Scale Error vs Conversion Time



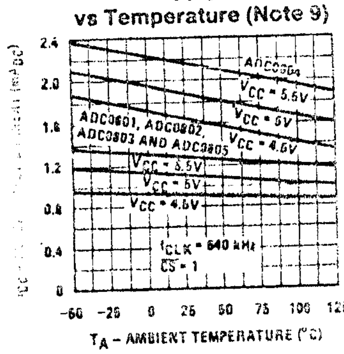
Effect of Unadjusted Offset Error vs. VREF/2 Voltage



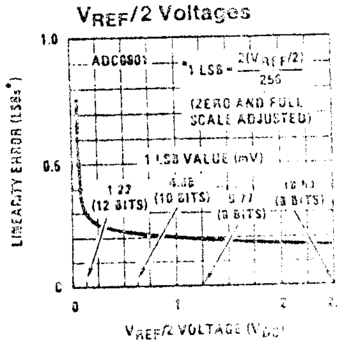
Output Current vs Temperature



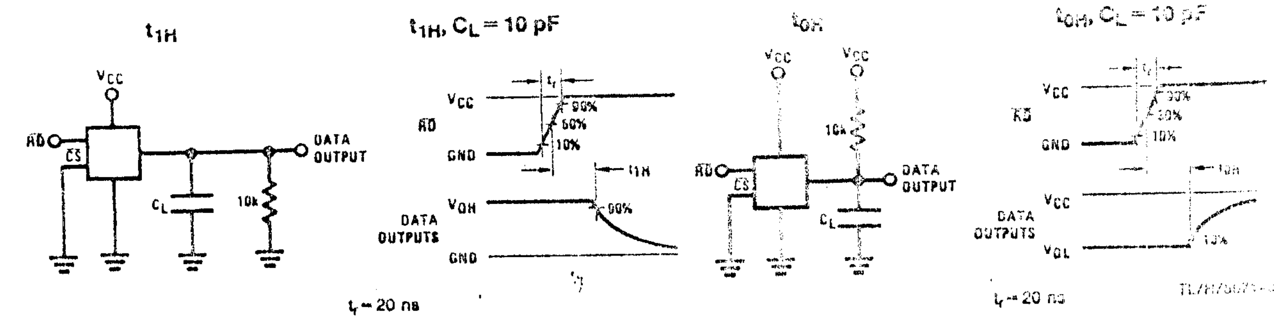
Power Supply Current vs Temperature (Note 9)



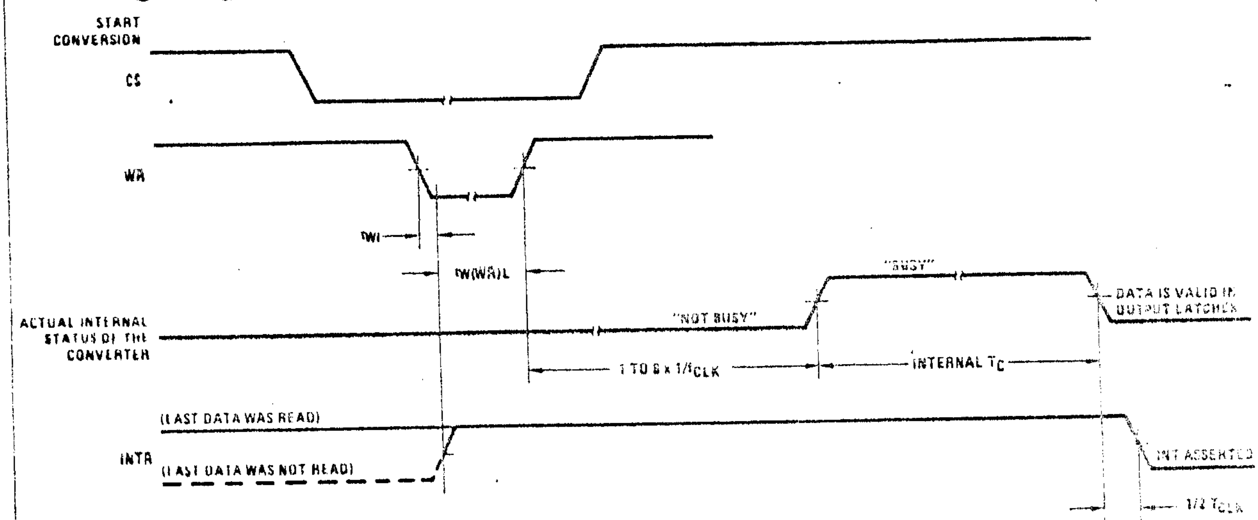
Linearity Error at Low VREF/2 Voltages



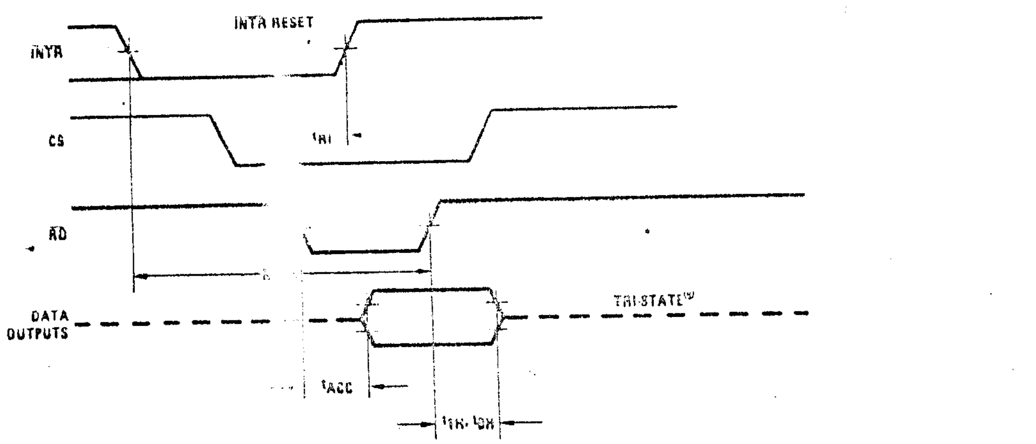
TRI-STATE Test Circuits and Waveforms



Timing Diagrams (All timing is measured from the 50% voltage points)



Output Enable and Reset INTR



Note: Read strobe must occur k periods ($3/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

National Semiconductor Corporation

DAC0808, DAC0807, DAC0806 8-Bit D/A Converters

General Description

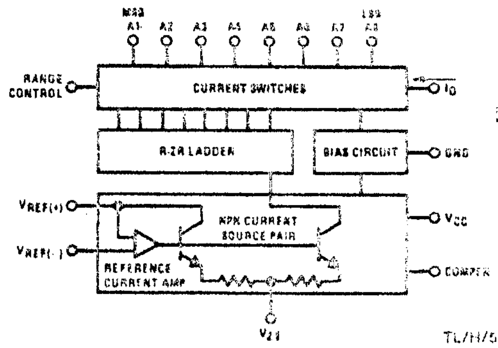
The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

Features

- Relative accuracy: ±0.19% error maximum (DAC0808)
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

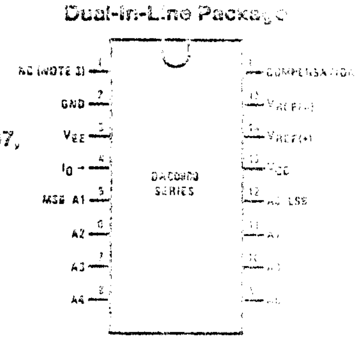
Block and Connection Diagrams



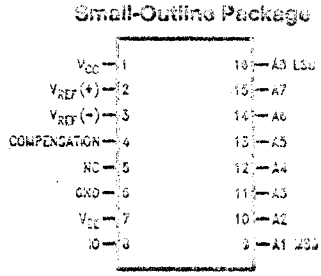
TL/H/5687-1

Order Number DAC0808, DAC0807, or DAC0806 See NS Package Number J16A, M16A or N16A

Dual-In-Line Package



Small-Outline Package



TL/H/5687-13

Top View

Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS				
		J PACKAGE (J16A)*		N PACKAGE (N16A)*		SO PACKAGE (M16A)
8-bit	$-55°C \leq T_A \leq +125°C$	DAC0808LJ	MC1508L8			
8-bit	$0°C \leq T_A \leq +75°C$	DAC0808LCJ	MC1408L8	DAC0808LCN	MC1408P8	DAC0808LCM
7-bit	$0°C \leq T_A \leq +75°C$	DAC0807LCJ	MC1408L7	DAC0807LCN	MC1408P7	DAC0807LCM
6-bit	$0°C \leq T_A \leq +75°C$	DAC0806LCJ	MC1408L6	DAC0806LCN	MC1408P6	DAC0806LCM

*Note. Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage	
V_{CC}	$+18\ V_{DC}$
V_{EE}	$-18\ V_{DC}$
Digital Input Voltage, V5–V12	$-10\ V_{DC}$ to $+18\ V_{DC}$
Applied Output Voltage, V_O	$-11\ V_{DC}$ to $+18\ V_{DC}$
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Note 3)	1000 mW
ESD Susceptibility (Note 4)	TBD
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC0808L	$-55°C \le T_A \le +125°C$
DAC0808LC Series	$0 \le T_A \le +75°C$

Electrical Characteristics

($V_{CC} = 5V$, $V_{EE} = -15\ V_{DC}$, $V_{REF}/R14 = 2$ mA, DAC0808: $T_A = -55°C$ to $+125°C$, DAC0808C, DAC0807C, DAC0806C, $T_A = 0°C$ to $+75°C$, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	(*Figure 4*)				
	DAC0808L (LM1508-8), DAC0808LC (LM1408-8)				±0.19	%
	DAC0807LC (LM1408-7), (Note 5)				±0.39	%
	DAC0806LC (LM1408-6), (Note 5)				±0.78	%
	Settling Time to Within ½ LSB (Includes t_{PLH})	$T_A = 25°C$ (Note 6), (*Figure 5*)		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	$T_A = 25°C$, (*Figure 5*)		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	(*Figure 3*)				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	(*Figure 3*)				
	High Level	$V_{IH} = 5V$		0	0.040	mA
	Low Level	$V_{IL} = 0.8V$		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	(*Figure 3*)		−1	−3	μA
	Output Current Range	(*Figure 3*)				
		$V_{EE} = -5V$	0	2.0	2.1	mA
		$V_{EE} = -15V$, $T_A = 25°C$	0	2.0	4.2	mA
I_O	Output Current	$V_{REF} = 2.000V$, $R14 = 1000\Omega$, (*Figure 3*)	1.9	1.99	2.1	mA
	Output Current, All Bits Low	(*Figure 3*)		0	4	μA
	Output Voltage Compliance (Note 2)	$E_r \le 0.19\%$, $T_A = 25°C$				
	$V_{EE} = -5V$, $I_{REF} = 1$ mA				−0.55, +0.4	V_{DC}
	V_{EE} Below −10V				−5.0, +0.4	V_{DC}

Electrical Characteristics (Continued)

($V_{CC} = 5V$, $V_{EE} = -15\ V_{DC}$, $V_{REF}/R14 = 2$ mA, DAC0808: $T_A = -55°C$ to $+125°C$, DAC0808C, DAC0807C, DAC0806C, $T_A = 0°C$ to $+75°C$, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SRI_{REF}	Reference Current Slew Rate	*(Figure 6)*	4	8		mA/μs
	Output Current Power Supply Sensitivity	$-5V \le V_{EE} \le -16.5V$		0.05	2.7	μA/V
I_{CC} I_{EE}	Power Supply Current (All Bits Low)	*(Figure 3)*		2.3 −4.3	22 −13	mA mA
V_{CC} V_{EE}	Power Supply Voltage Range	$T_A = 25°C$, *(Figure 3)*	4.5 −4.5	5.0 −15	5.5 −16.5	V_{DC} V_{DC}
	Power Dissipation All Bits Low All Bits High	 $V_{CC} = 5V, V_{EE} = -5V$ $V_{CC} = 5V, V_{EE} = -15V$ $V_{CC} = 15V, V_{EE} = -5V$ $V_{CC} = 15V, V_{EE} = -15V$		 33 106 90 160	 170 305	 mW mW mW mW

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: Range control is not required.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maixmum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the dual-in-line J package when the board mounted is 100°C/W. For the dual-in-line N package, this number increases to 175°C/W and for the small outline M package this number is 100°C/W.

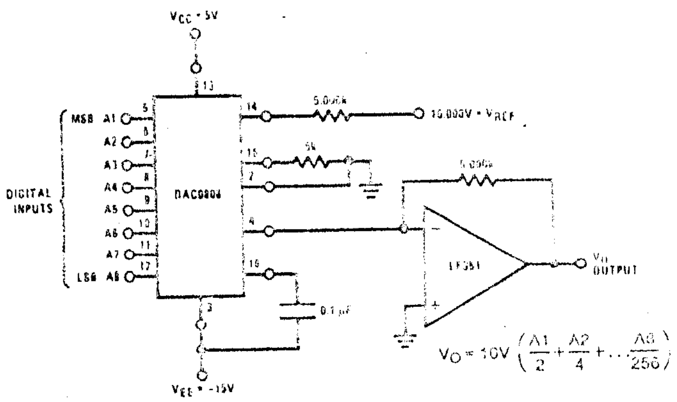
Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: All current switches are tested to guarantee at least 50% of rated current.

Note 6: All bits switched.

Note 7: Pin-out numbers for the DAL080X represent the dual-in-line package. The small outline package pinout differs from the dual-in-line package.

Typical Application



$V_O = 10V\left(\frac{A1}{2} + \frac{A2}{4} + \ldots \frac{A8}{256}\right)$

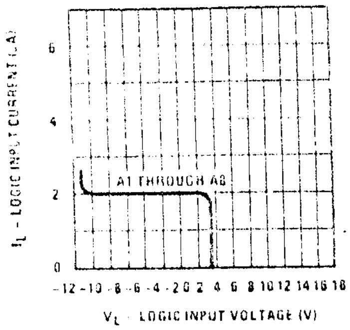
TL/H/5687-5

FIGURE 1. +10V Output Digital to Analog Converter (Note 7)

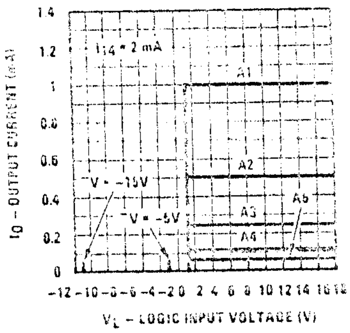
Typical Performance Characteristics

$V_{CC} = 5V$, $V_{EE} = -15V$, $T_A = 25°C$, unless otherwise noted

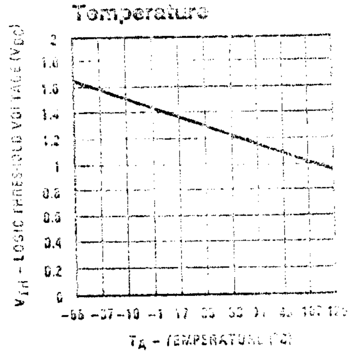
Logic Input Current vs Input Voltage



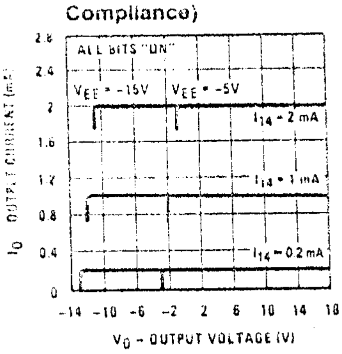
Bit Transfer Characteristics



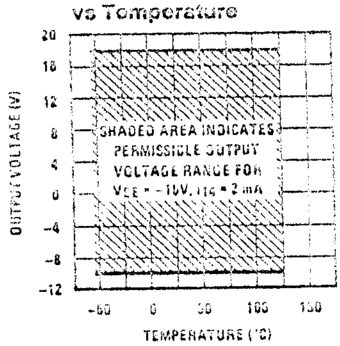
Logic Threshold Voltage vs Temperature



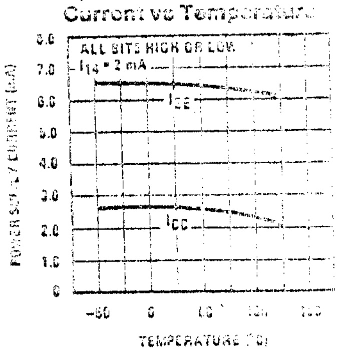
Output Current vs Output Voltage (Output Voltage Compliance)



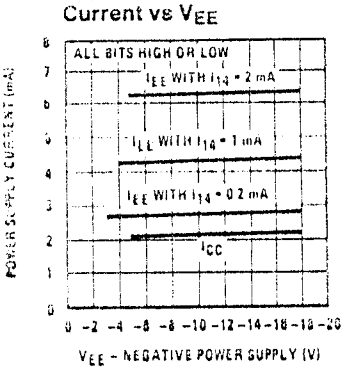
Output Voltage Compliance vs Temperature



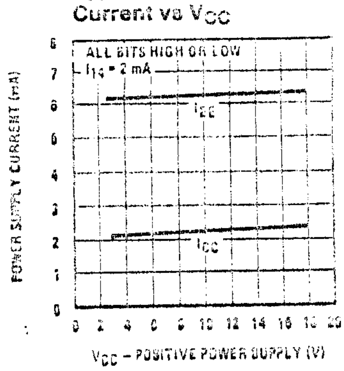
Typical Power Supply Current vs Temperature



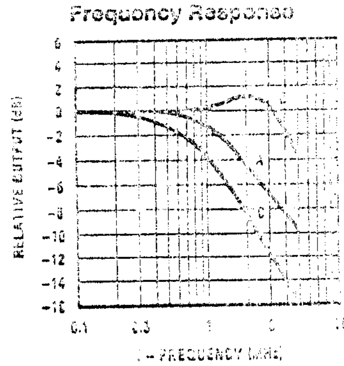
Typical Power Supply Current vs V_{EE}



Typical Power Supply Current vs V_{CC}



Reference Input Frequency Response



TL/H/5687-6

Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}; $R_L = 50Ω$, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1 V above ground.

Curve B: Small Signal Bandwidth Method of *Figure 7*, $R_L = 250Ω$, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp, $R_L = 50Ω$), $R_S = 50Ω$, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

National Semiconductor Corporation

CD4066BM/CD4066BC Quad Bilateral Switch

General Description

The CD4066BM/CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BM/CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Wide range of digital and analog switching — ±7.5 V_{PEAK}
- "ON" resistance for 15V operation — 80Ω
- Matched "ON" resistance over 15V signal input — ΔR_{ON} = 5Ω (typ.)
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio — 65 dB (typ.) @ f_{is} = 10 kHz, R_L = 10 kΩ
- High degree linearity — 0.1% distortion (typ.) @ f_{is} = 1 kHz, V_{in} = 5V_{p-p}, V_{DD} − V_{SS} = 10V, R_L = 10 kΩ

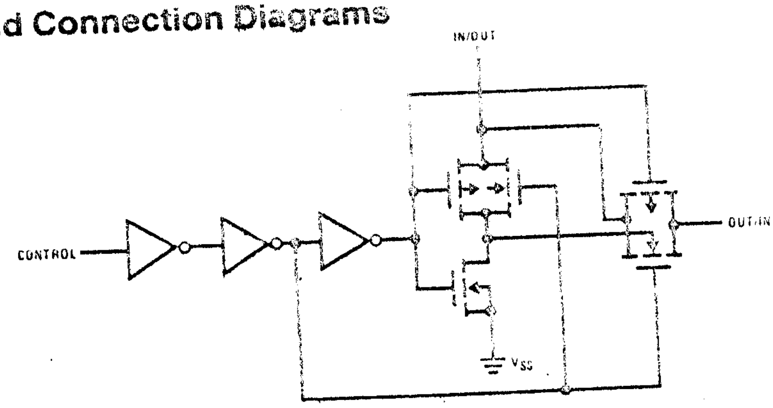
High degree linearity
High degree linearity

- Extremely low "OFF" switch leakage — 0.1 nA (typ.) @ $V_{DD} - V_{SS}$ = 10V, T_A = 25°C
- Extremely high control input impedance — 10^{12}Ω (typ.)
- Low crosstalk between switches — −50 dB (typ.) @ f_{is} = 0.9 MHz, R_L = 1 kΩ
- Frequency response, switch "ON" — 40 MHz (typ.)

Applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal-gain

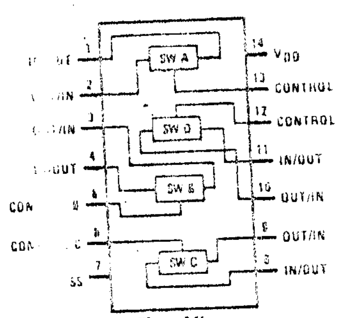
Schematic and Connection Diagrams



Dual-In-Line Package

Cavity Dual-In-Line Package (J)
Order Number CD4066BMJ or CD4066BCJ
See NS Package Number J14A

Molded Dual-In-Line Package (N)
Order Number CD4066BMN or CD4066BCN
See NS Package Number N14A



Top View

Small Outline Package (M)
Order Number CD4066BCM
See NS Package Number M14A

TL/F/5665-1