LANE DEPARTURE WARNING SYSTEM

A PROJECT REPORT

Submitted by

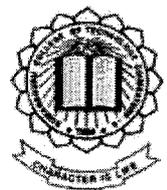|	
DEEPIKA.S	**71203106011**
DHIVYA.A	**71203106012**
PRIYADARSINI.L	**71203106038**
SURYAPRABHA.S	**71203106055**

in partial fulfillment for the award of the degree

of

BACHELOR OF ENGINEERING

IN

KUMARAGURU COLLEGE OF TECHNOLOGY, COIMBATORE

ANNA UNIVERSITY:: CHENNAI 600 025

**APRIL 2007**

ANNA UNIVERSITY :: CHENNAI 600 025

BONAFIDE CERTIFICATE

Certified that this project report **"LANE DEPARTURE WARNING SYSTEM"** is the bonafide work of **"DEEPIKA.S, DHIVYA.A, PRIYADARSINI.L, SURYAPRABHA.S"** who carried out the project work under my supervision.

SIGNATURE

Mrs.Rajeshwari Mariappan
HEAD OF THE DEPARTMENT

Electronics & Communication
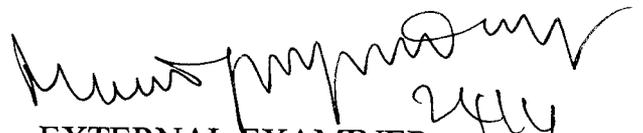Engineering
Kumaraguru College of Technology,
Coimbatore 641006.
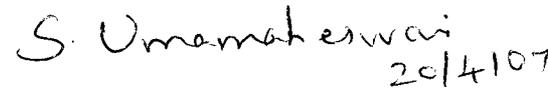
SIGNATURE

Mrs.S.Umamaheswari
SUPERVISOR

Sr.Lecturer
Electronics & Communication
Engineering
Kumaraguru College of Technology,
Coimbatore 641006.

Submitted for university exam held on ...24-.4-.2007....

INTERNAL EXAMINER

EXTERNAL EXAMINER

PL/TRG/PROJ/2007
17-04-2007

PROJECT COMPLETION CERTIFICATE

We are pleased to issue this certificate in the process of operationalising our "Industry- Institute Interaction Synergy" drive.

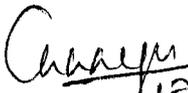|		
Name	:	S. Suryaprabha
		S. Deepika
		L. Priyadarsini
		A. Dhivya
Institution	:	Kumaraguru College of Technology Coimbatore-641 006
Qualification	:	B E (Electronics & Communication)
Project Title	:	"Lane Departure Warning System "
Project Duration	:	Jan'07 to April'07
Department	:	Synoro Technologies
Performance/ Conduct	:	Good

For Pricol Limited,

Chhaya
Sr. Officer -//HR

ACKNOWLEDGEMENT

We would like to thank our respected principal **Dr.Joseph.V Thanikal, M.E., Ph.D., PDF., CEPIT.,** for providing an enthusiastic atmosphere to work in our college.

We would like to thank our beloved Head of the Department, **Dr.Rajeswari Mariappan,** for her constant support and encouragement throughout the entire course.

We take privilege to thank **Mr.R.Krishna Murthi,** VP Electronics **PRICOL Limited,** Coimbatore for giving us the opportunity to work on this project. We would also like to thank **Mr.M.Suresh,** Project Co-ordinator, Synoro Technologies, R&D Division of PRICOL Limited, Coimbatore for guiding us throughout our project.

We would like to thank our project guide, **Mrs.S.Umamaheswari,** for her guidance and valuable advice without whom this project would not have been completed.

We extend our gratitude to our project coordinator, **Prof.K.Ramprakash,** for his continuous support during the course of our project.

Last but not least, we would also like to thank all the staff members of our department.

ABSTRACT

In this fast moving world everyone have a vehicle of their own. As a result there is an increase in the day-to-day traffic and an increase in the number of accidents. The major causes of these accidents are lane departures. Vehicles wander out of the lane due to the following reasons: driver lost in a cell phone conversation, distraction by screaming children in the vehicle, drowsiness at the end of a long day and drunkenness at the end of a long night.

Lane Departure Warning System is a driver assistance system which will alert the driver of any unintentional lane departures. Such systems must extract information of the lane boundaries ahead of the vehicle and the vehicle position within the lane.

Hence our main objective is to process the real time input to extract the details mentioned above and to give a warning, if necessary. For this purpose the simulation is done in MATLAB 7.0, which will be converted to C code and implemented in hardware. The hardware processor used here is Blackfin 561 due to its benefits like high performance, low power consumption, ease of use and code compatible capabilities.

TABLE OF CONTENTS

LIST OF FIGURES

1. INTRODUCTION

Road and lane departures are the primary cause of accidents, especially on National Highways. For example, on U.S. highways 70% of the accidents are due to lane departures. Lane departures can be due to various reasons like drowsy drivers, drivers handling of cell phones and various other distractions. Lane departure warning system (LDWS) will alert the driver in such situations.

1.1 What is our project?

Lane departure warning system (LDWS) has been developed for driver assistance applications. This project was done at Synoro Technologies, R&D division of PRICOL Limited, Coimbatore. The hardware consists of a camera that captures the road image as a video. This video is taken as input and processed by the blackfin561 DSP processor. The entire process is written in the form of a   C-code and ported to the DSP processor. Before going for the real-time software, the same process is simulated in MATLAB version 7.0 concentrating on Digital Image Processing.

Our objective is to develop software for supporting the lane departure warning system hardware. For this purpose we take a sample video and convert the video into a series of bitmap images. These images are processed in MATLAB to extract the lane information.

Fig 1.1 Simplified Block Diagram

| CAMERA | → | PROCESSOR | → | BUZZER |

1.2 Initial products

The first production of LDWS was available in North America which was the system jointly developed by Valeo and Iteris for Nissan Motors and is fitted to their 2005 Infiniti FX and 2006 M45 vehicles. In Europe Citroën first offered LDWS on their 2005 C4 and C5 models, and now also on their C6 model .

1.3 Installation and cost

Some LDWS may be installed directly as an aftermarket accessory, while other LDWS are installed when the vehicles are manufactured. As technology advances, new features and components may be added to these systems. The costs of LDWS vary greatly depending on the number of units wanted, technology used and make.

2. APPROACH 1

2.1 Overview

The road image is captured through a camera. This camera is fixed at the centre of the vehicle behind the rear view mirror facing the road. This road image will serve as the input through which the lane information is extracted. First the colour image is converted to gray image. From the gray image the edges are detected. The resulting edge image is segmented to find the intended lane. The angle between the lane markings and the horizontal axis is determined. These angle values will be compared with standard threshold values. Based on the comparison a warning will be generated if the angle values deviate from the threshold values.

2.2 Algorithm

Step1: Image Capturing

The image captured from the camera is read in as input.

- Function used: imread()
- Function description:

A = imread(filename,fmt) reads a grayscale or color image from the file specified by the string filename, where the string fmt specifies the format of the file. If the file is not in the current directory or in a directory in the MATLAB path, specify the full pathname of the location on your system. If imread cannot find a file named filename, it looks for a file named filename.fmt.

Step 2: Image Pre-processing

All image processing functions in MATLAB 7.0 use double precision values. Hence the pixel values of the input image are first converted to double precision values.

- Function used: im2double()
- Function description:

I2 = im2double(I) converts the intensity image I to double precision, rescaling the data if necessary. im2double takes an image as input, and returns an image of class double. If the input image is of class double, the output image is identical to it. If the input image is of class logical, uint8, or uint16, im2double returns the equivalent image of class double, rescaling or offsetting the data as necessary.

In order to simplify the process the colour image is converted to gray scale image.

- Function used: rgb2gray()

- Function description:

I = rgb2gray(RGB) converts the true-color image RGB to the grayscale intensity image I. rgb2gray converts RGB images to grayscale by eliminating the hue and saturation information while retaining the luminance.

Step 3: Edge Detection

The edges in the gray image are detected using canny filter

- Function used: edge()

- Function description:

Edge takes an intensity image I as its input, and returns a binary image BW of the same size as I, with 1's where the function finds edges in I and 0's elsewhere. Edge supports six different edge-finding methods. One such method used here is Canny edge detection. The Canny method finds edges by looking for local maxima of the gradient of I. The gradient is calculated using the derivative of a Gaussian filter. The method uses two thresholds, to detect strong and weak edges, and includes the weak edges in the output only if they are connected to strong edges. This method is therefore less likely than the others to be fooled by noise, and more likely to detect true weak edges.

BW = edge(I,'canny',thresh) specifies sensitivity thresholds for the Canny method. Thresh is a two-element vector in which the first element is the low threshold, and the second element is the high threshold. If you specify a scalar for thresh, this value is used for the high threshold and

5

0.4*thresh is used for the low threshold. If you do not specify thresh, or if thresh is empty ([]), edge chooses low and high values automatically.

Step 4: Image segmentation

The edge image is further processed to segment the intended lane. The intended lane is converted to 0s i.e. to black and the area outside the lane is converted to 1s i.e. to white.

- No built-in functions are used here

Step 5: Angle Determination

From the segmented image the angle of the lane markings are determined. Two points on the lane marking are chosen and the angle is calculated.

- the angles are found using available trigonometric functions
- Function used: atand()
- Function description:

Y = atand(X) is the inverse tangent, expressed in degrees, of the elements of X.

Step 6: Decision Making

Analysing the available samples, a standard threshold value is fixed. The calculated angle values will be compared with the standard threshold values and a warning will be generated, if there is a deviation.

- No built-in functions are used here.

The images displayed are:

1) input colour image

2) gray image

3) edge image

4) segmented image

These images are displayed as a series of outputs.

- Function used: imshow()

- Function description:

imshow(BW) displays the binary image BW. imshow displays pixels with the value 0 (zero) as black and pixels with the value 1 as white.

imshow(RGB) displays the true-color image RGB.

From the segmented binary image, the angle of the lane markings is determined as follows

- two points on the lane markings are selected

- the distance between co-ordinates of the two points are calculated

- this distance gives the length of the adjacent and opposite sides of a right-angled triangle

- the angle is found using the inverse tangent formulae

These angles are compared with the standard threshold values and if there is a deviation a warning will be given.

2.3 Flowchart

Fig 2.1 Flowchart for approach 1

```
        ┌─────────────────────────┐
        │    IMAGE CAPTURING      │◄──────────┐
        └─────────────────────────┘           │
                    │                          │
                    ▼                          │
        ┌─────────────────────────┐           │
        │  BINARISING THE IMAGE   │           │
        └─────────────────────────┘           │
                    │                          │
                    ▼                          │
        ┌─────────────────────────┐           │
        │     EDGE DETECTION      │           │
        └─────────────────────────┘           │
                    │                          │
                    ▼                          │
        ┌─────────────────────────┐           │
        │   IMAGE SEGMENTATION    │           │
        └─────────────────────────┘           │
                    │                          │
                    ▼                          │
        ┌─────────────────────────┐           │
        │   ANGLE DETERMINATION   │           │
        └─────────────────────────┘           │
                    │                          │
                    ▼                    NO    │
                  ╱   ╲  ────────────────────►─┘
                ╱ IF ANGLE>╲
                ╲ THRESHOLD ╱
                  ╲   ╱
                    │ YES
                    ▼
        ┌─────────────────────────┐
        │   WARNING WILL BE        │
        │     GENERATED            │
        └─────────────────────────┘
```

8
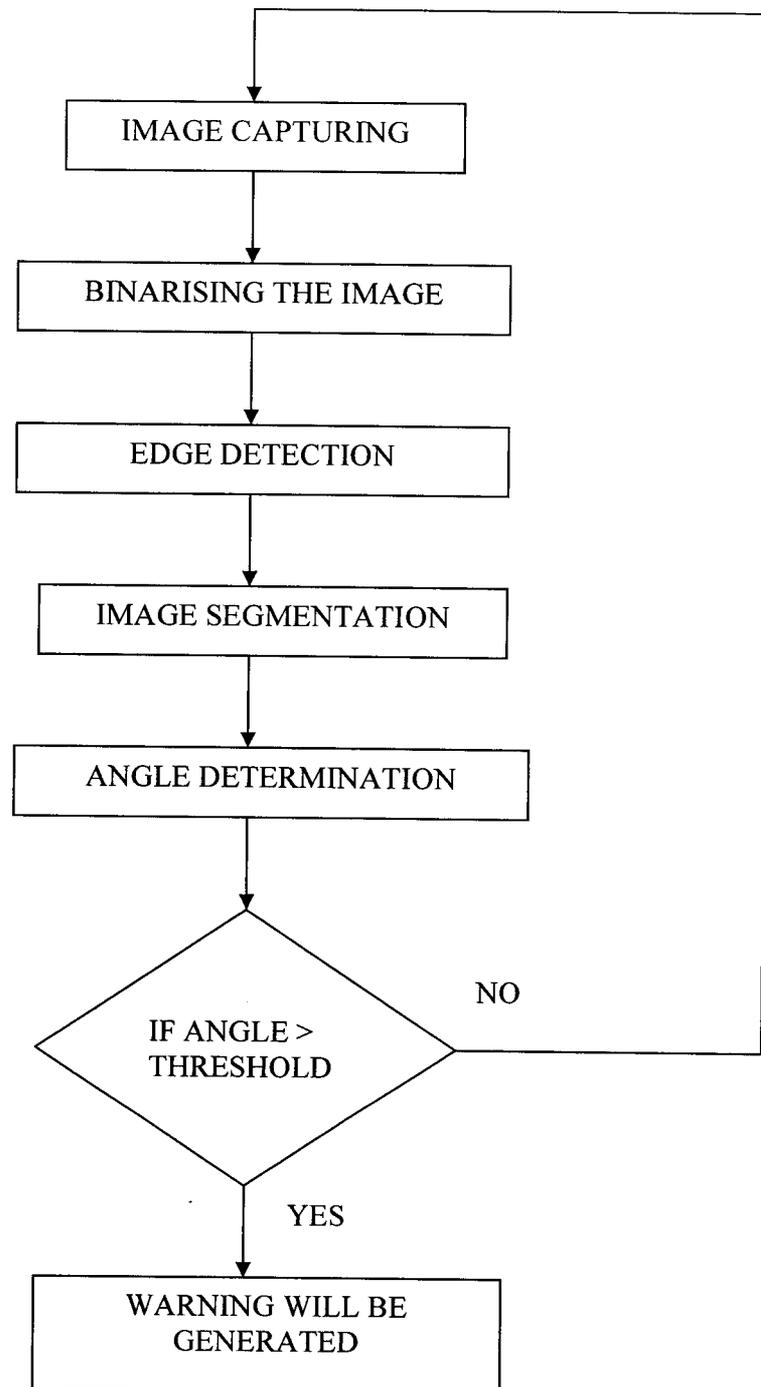
2.4 Sample outputs

2.4.1 Sample 1

a) Input colour image
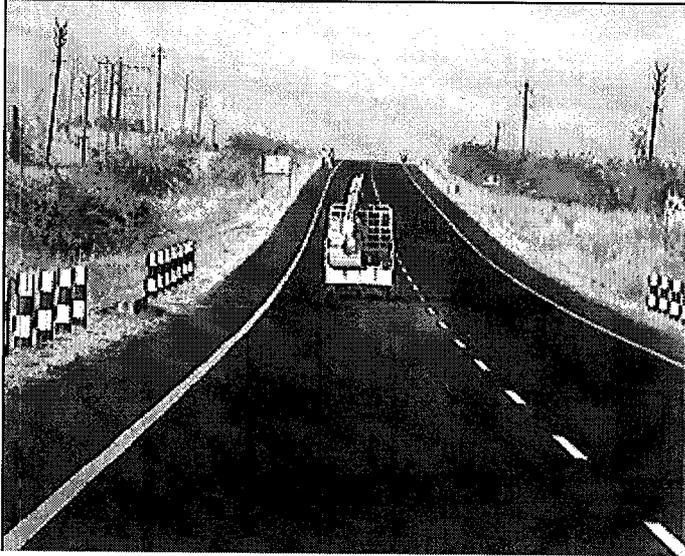
b) Gray image

gray image

c) Edge image
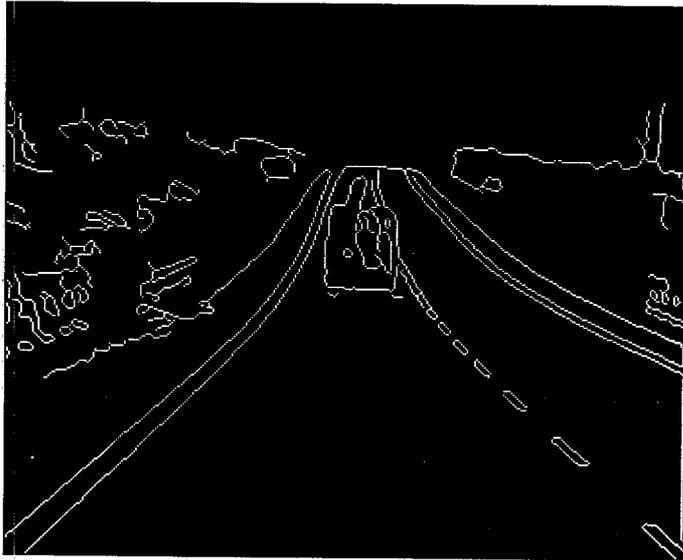
edge image

d) Segmented image

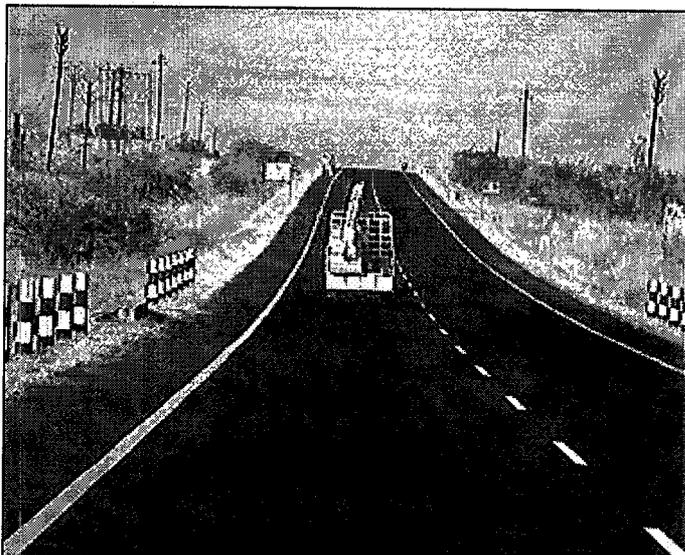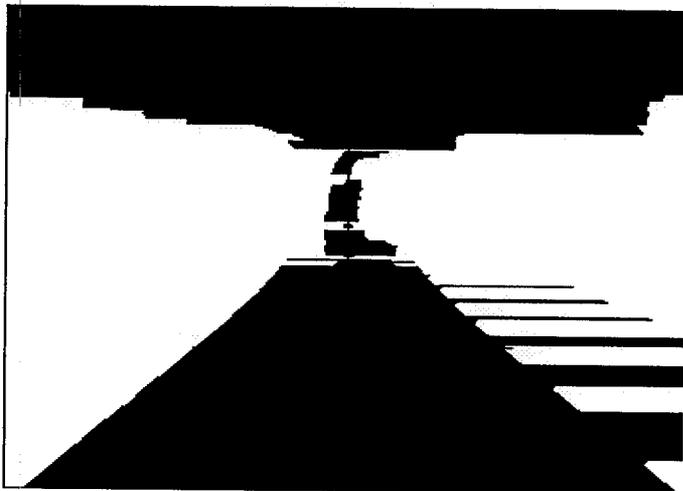binary image

2.4.2 Sample 2

a) Input colour image
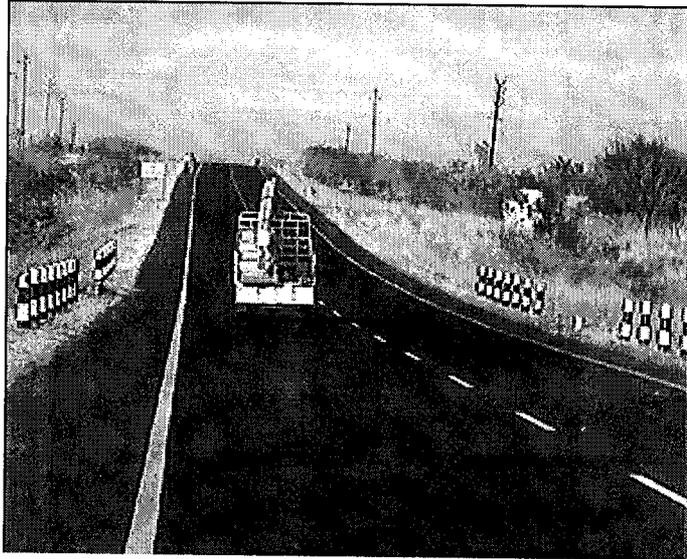
b) Gray image

gray image
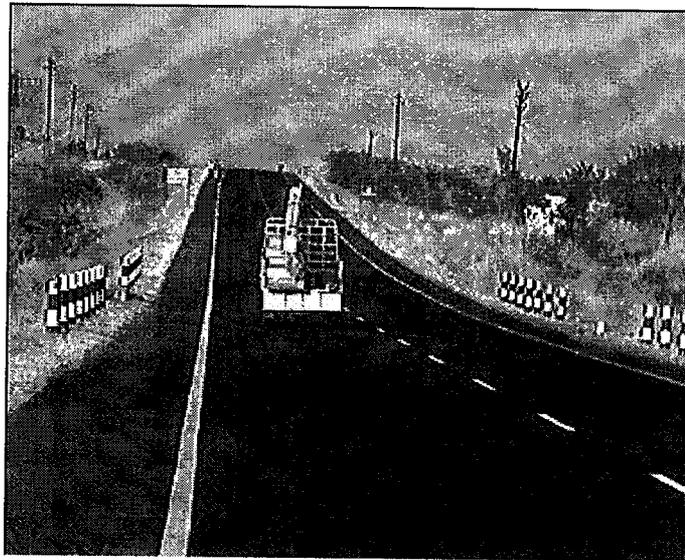
c) Edge image

edge image

d) Segmented image

binary image

2.5 Drawbacks

The above approach has been tested on many samples and we found few drawbacks which are listed below.

- In order to find the angle of the lane markings, the entire image has to be processed sequentially. For this purpose we use a series of MATLAB built-in functions.
- Presence of noise signals in the image may lead to false warnings.
- The presence of shadows and various other small objects can cause errors in lane detection which will also lead to false warnings.
- The road geometry will affect the angle determination, for example the road curvature will yield in angles greater than the threshold value and hence will give a warning. In reality the vehicle will be inside the lane but a warning will be given due to the angle comparison.
- The implementation in hardware is complicated due to the use of many MATLAB built in functions. Hardware implementation of these functions is complex.

3. APPROACH 2

3.1 Overview

In this approach instead of processing the whole image only few parts of the image are processed to extract the lane information. Six bounding boxes are fixed on the image. These bounding boxes are basically fixed dimension rectangles on fixed positions of the image.

A detailed study has been done on

1) determining the number of rectangles,

2) fixing the position of the rectangles and

3) determining the dimensions of these rectangles.

Based on the study and observation of some sample outputs we came to a conclusion of using three pairs of rectangles.

Once the number of rectangles was determined the next step was to position these rectangles and fix its dimensions. First a detailed mathematical analysis was carried out and the rectangles were fixed with reference to the dimensions of the image and the results were tested on the samples. But these dimensions are subject to change and hence the rectangles were positioned at an offset from the centerline of the **centre image** (i.e. an image taken by positioning the vehicle at the centre of the lane).

Next step is to determine the rectangle dimensions. In order to fix the **left image** (i.e. an image taken by positioning the vehicle at the left edge of the lane) and **right image** (i.e. an image taken by positioning the vehicle at the right edge of the lane) are taken as reference. Based on the sample reference images the dimensions have been fixed.

3.2 Algorithm

Step 1: Image Capturing

The colour image is read in as input and converted to black and white image.

Step 2: Declaration of constants used in the program.

Step 3: Rectangle Generation

The rectangles are generated on the black and white image.

- the rectangles are generated by selecting the pixels on the position of the image and changing the colour of those pixels
- the rectangles are generated in pairs
- here the rectangles will be in white since the road is in a darker shade

Step 4: Lane Detection

The next step is to process the pixels within these rectangles and detect the lane markings.

- the lane markings are detected based on intensity comparisons
- once the lane marking is detected then the colour of those pixels are changed to black

Step 5: Decision Making

Based on the processing done in step 4 the position of the vehicle in the lane is determined.

- if the vehicle is inside the lane then no warning is given
- if the vehicle is very close to the edge of the lane then a visible warning will be given
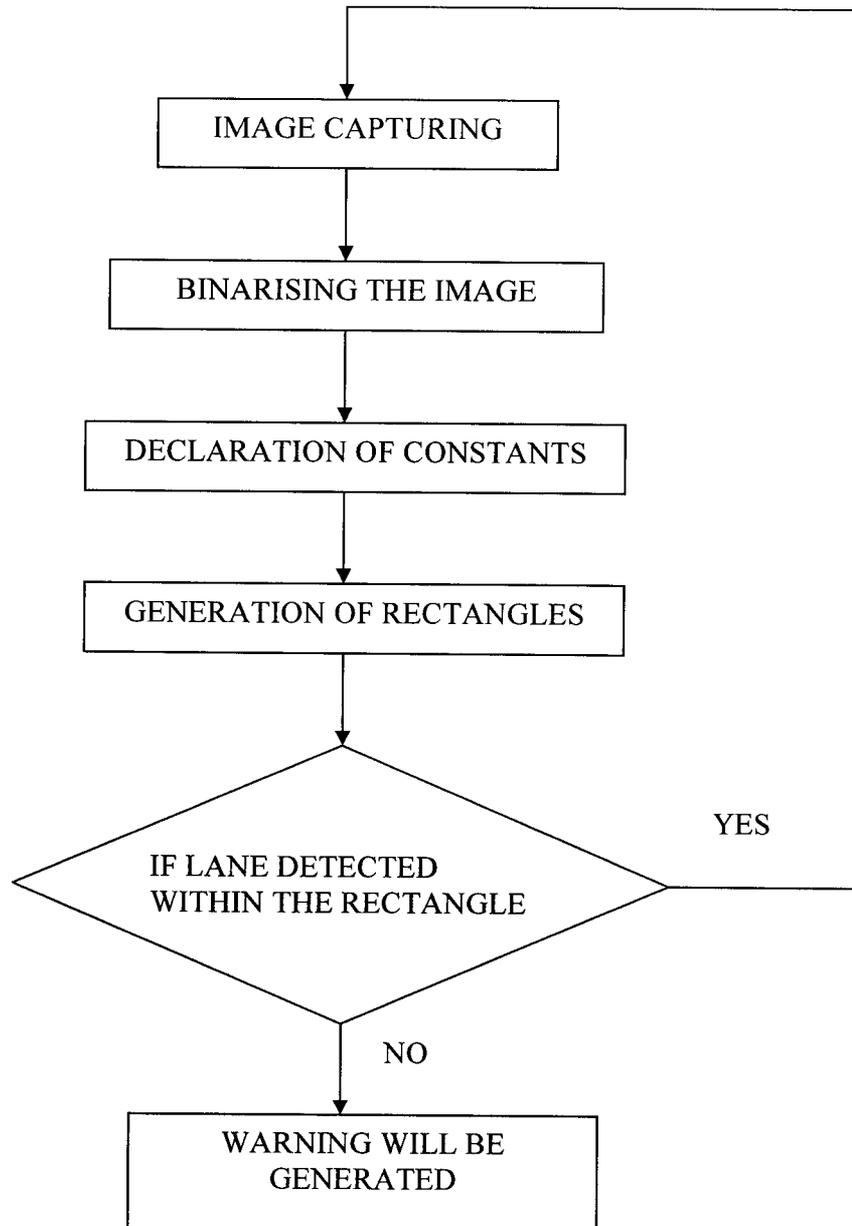
- if the vehicle is on edge of or out of the lane then an audible warning will be given

The images displayed are

1) input (colour) image
2) gray input image
3) image with generated rectangles
4) lane detected image

3.3 Flow chart

Fig 3.1 Flow chart for approach 2

```
                    ┌──────────────────────────┐
                    ▼                          │
          ┌─────────────────────┐             │
          │   IMAGE CAPTURING   │             │
          └─────────────────────┘             │
                    │                          │
                    ▼                          │
        ┌───────────────────────┐             │
        │ BINARISING THE IMAGE  │             │
        └───────────────────────┘             │
                    │                          │
                    ▼                          │
       ┌─────────────────────────┐            │
       │ DECLARATION OF CONSTANTS │           │
       └─────────────────────────┘            │
                    │                          │
                    ▼                          │
      ┌──────────────────────────┐            │
      │ GENERATION OF RECTANGLES │            │
      └──────────────────────────┘            │
                    │                          │
                    ▼                   YES    │
              ◇─────────────◇─────────────────┘
              │ IF LANE DETECTED │
              │ WITHIN THE RECTANGLE │
              ◇─────────────◇
                    │
                    │ NO
                    ▼
          ┌─────────────────────┐
          │  WARNING WILL BE    │
          │    GENERATED        │
          └─────────────────────┘
```
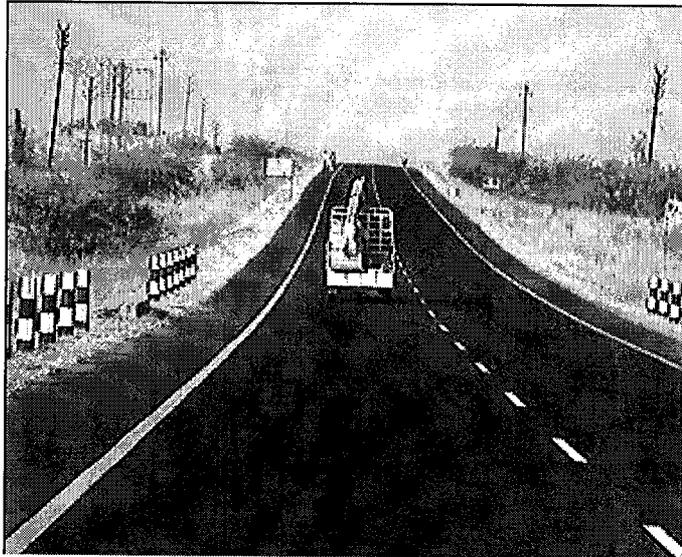
18

3.4 OUTPUT

3.4.1 Reference samples:

In this section let us see the output of the reference samples.

3.4.1.1 centre image

a)   input (colour) image

b)   gray input image

gray image

c)   image with generated rectangles

Image with rectangles

d)   output (lane detected) image

Lane Detected Image

3.4.1.2 left image

a) input (colour) image
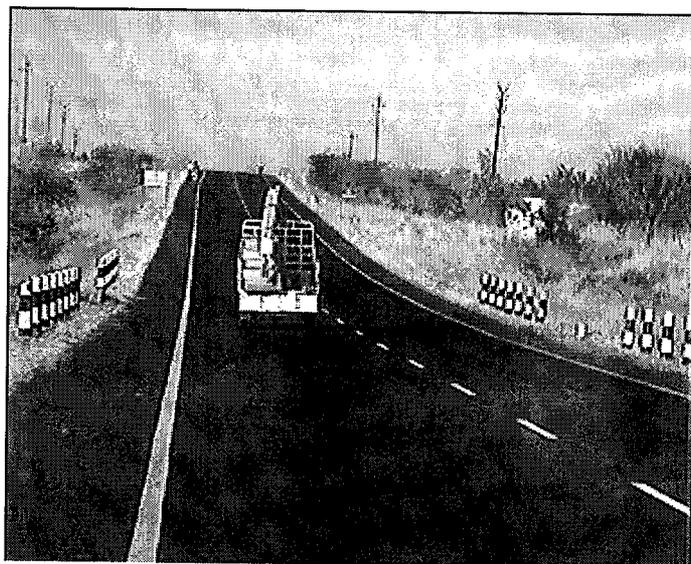
b) gray input image

Gray Image

c) image with generated rectangles

Image with rectangles
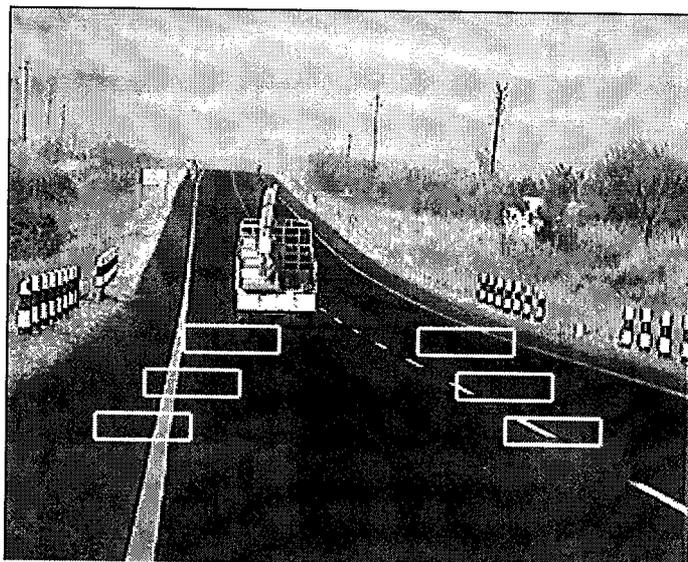
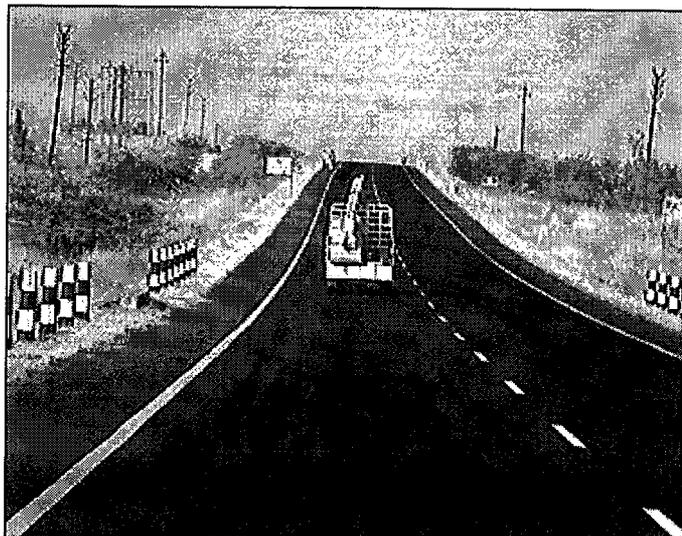d) output (lane detected) image

Lane Detected Image
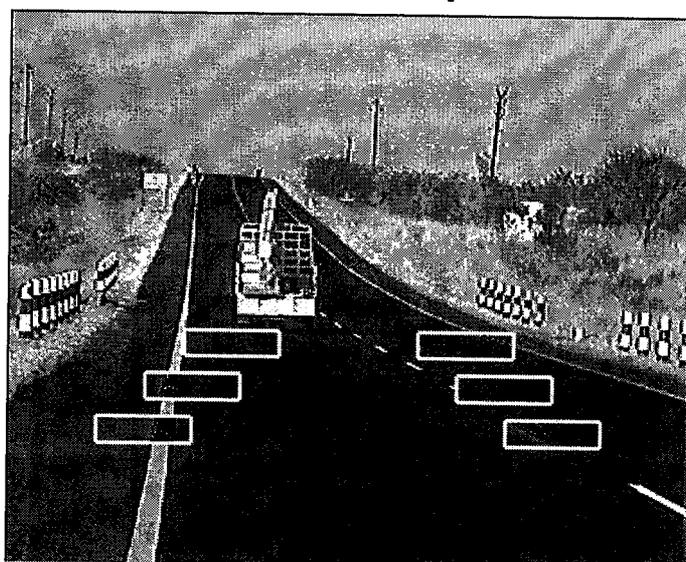
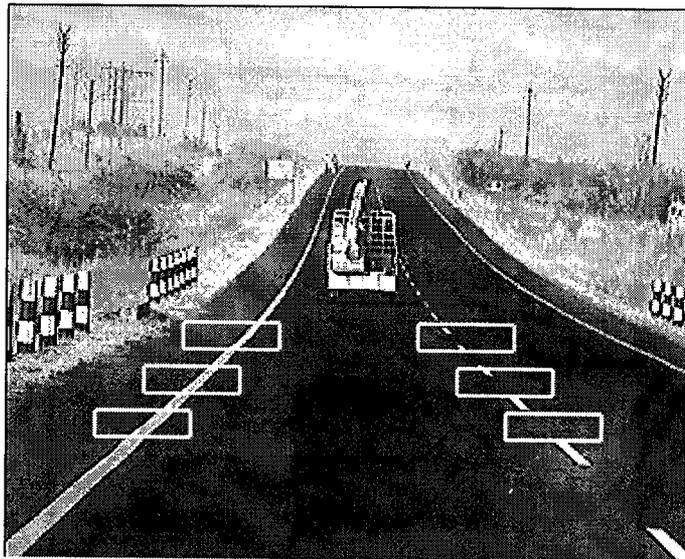## 3.4.1.3 right image

a) input (colour) image
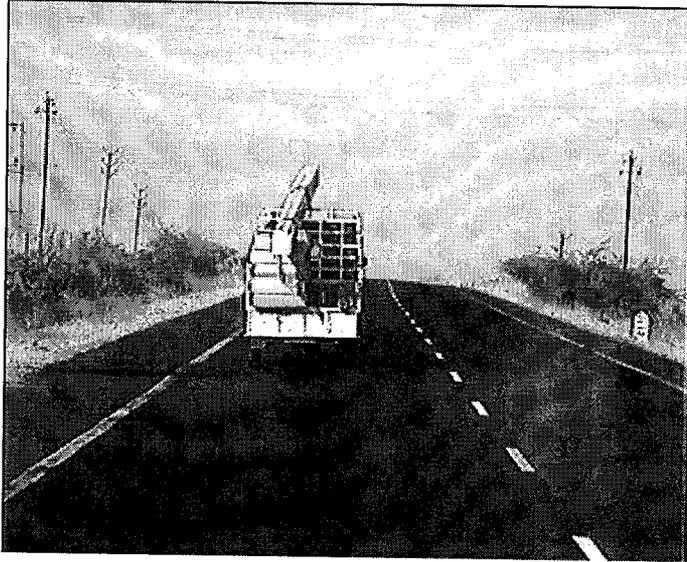
b) gray input image

Gray Image
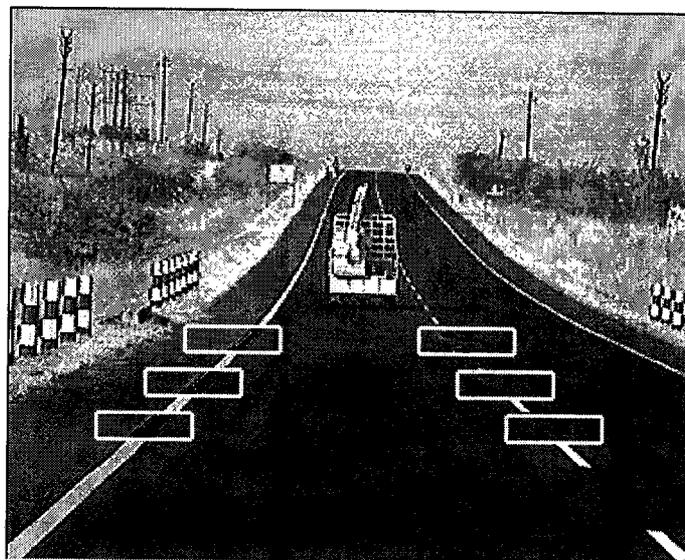
c) image with generated rectangles

Image with rectangles
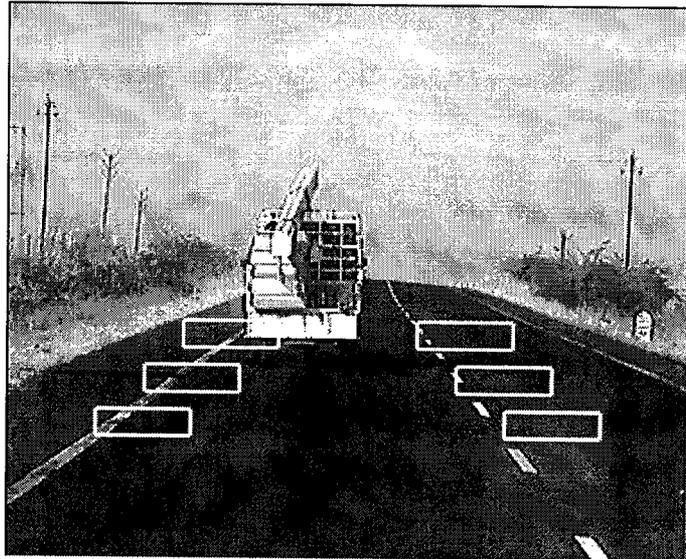
d) output (lane detected) image

Lane Detected Image
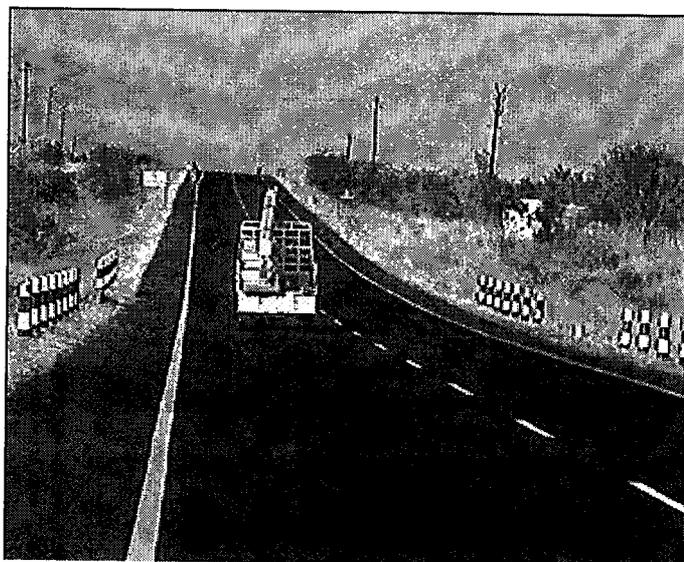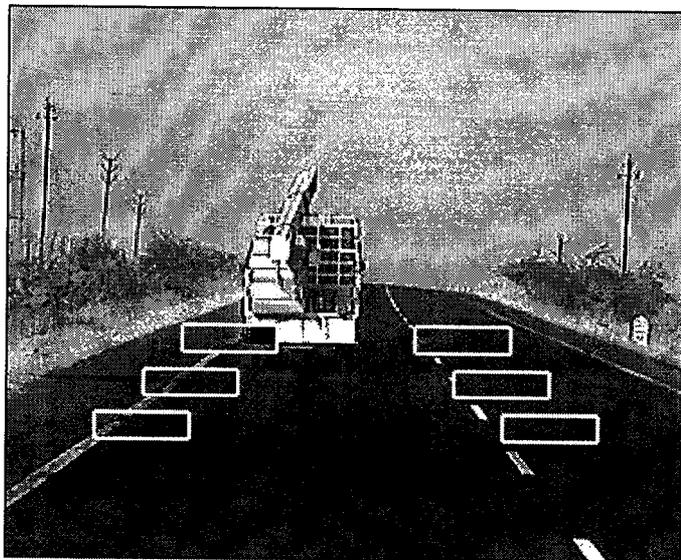
3.4.2 Sample outputs

In this section let us see the output of some actual samples.

3.4.2.1 sample 1

a)   input image
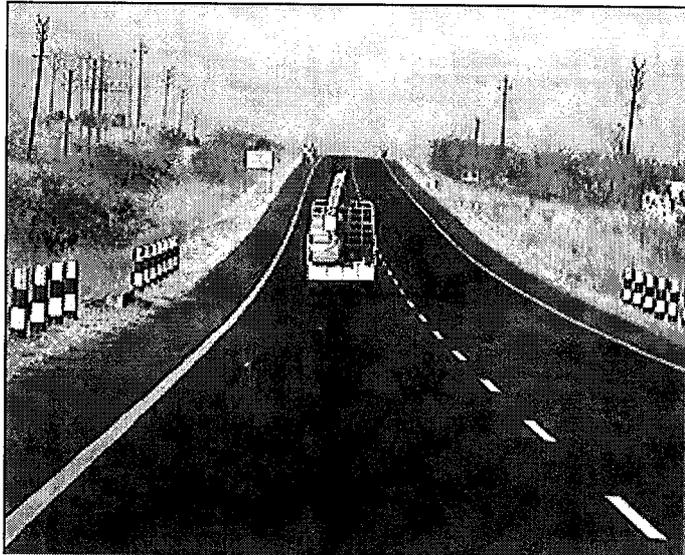
b)   output image

Lane Detected Image
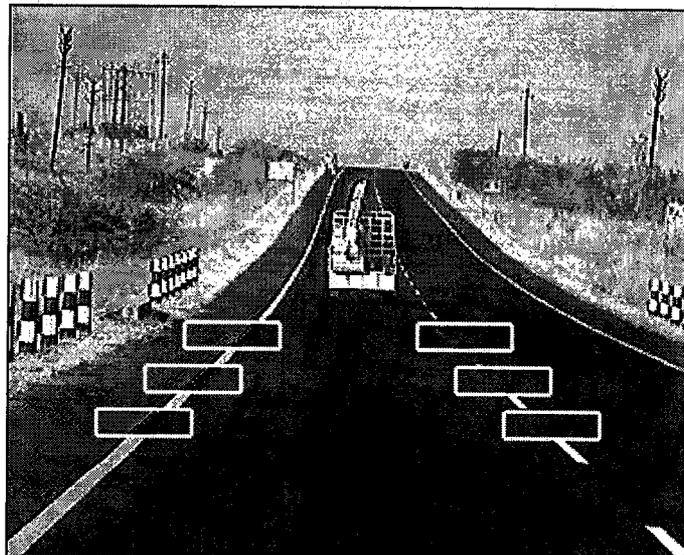
3.4.2.2 Sample 2

a) input image
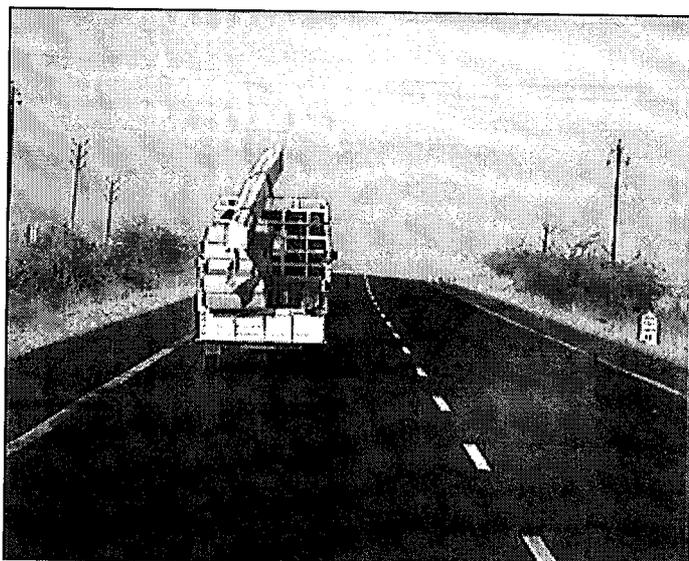
b) output image

Lane Detected Image
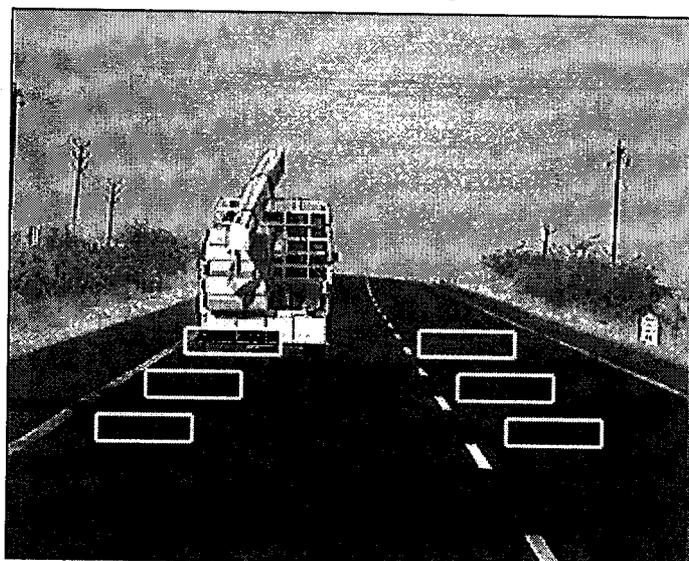
In the above approach the vehicle position is determined by the presence of lane markings within the rectangles.

3.5 Advantages

This approach is more advantages than the previous approach in the following ways

- Previously the entire image has to be processed to determine the position of the vehicle, whereas in this approach only the pixels within the rectangles have to be processed to determine the same.
- The probability of the presence of noise signals, shadows and various other small objects in the rectangles is negligible and hence the false warnings can be minimized to a greater extent.
- The road geometry will not affect the determination of the position of the vehicle.
- Since we have used only few built in functions, the implementation in hardware is simple and easy.

4. HARDWARE

4.1 Architectural Overview

Blackfin Processors are a new breed of 16-32-bit embedded processor designed specifically to meet the computational demands and power constraints of today's embedded audio, video and communications applications. Based on the Micro Signal Architecture (MSA) jointly developed with Intel Corporation, Blackfin Processors combine a 32-bit RISC-like instruction set and dual 16-bit multiply accumulate (MAC) signal processing functionality with the ease-of-use attributes found in general-purpose microcontrollers. This combination of processing attributes enables Blackfin Processors to perform equally well in both signal processing and control processing applications-in many cases deleting the requirement for separate heterogeneous processors. This capability greatly simplifies both the hardware and software design implementation tasks.

Currently, Blackfin Processors offer performance up to 756MHz in single core products. New symmetric multi-processor members of the Blackfin processor family double the performance at the same frequency. The Blackfin Processor family also offers industry leading power consumption performance down to 0.8V. This combination of high performance and low power is essential in meeting the needs of today's and future signal processing applications including broadband wireless, audio/video capable Internet appliances, and mobile communications.

Figure 4-1. ADSP-BF561 Block Diagram
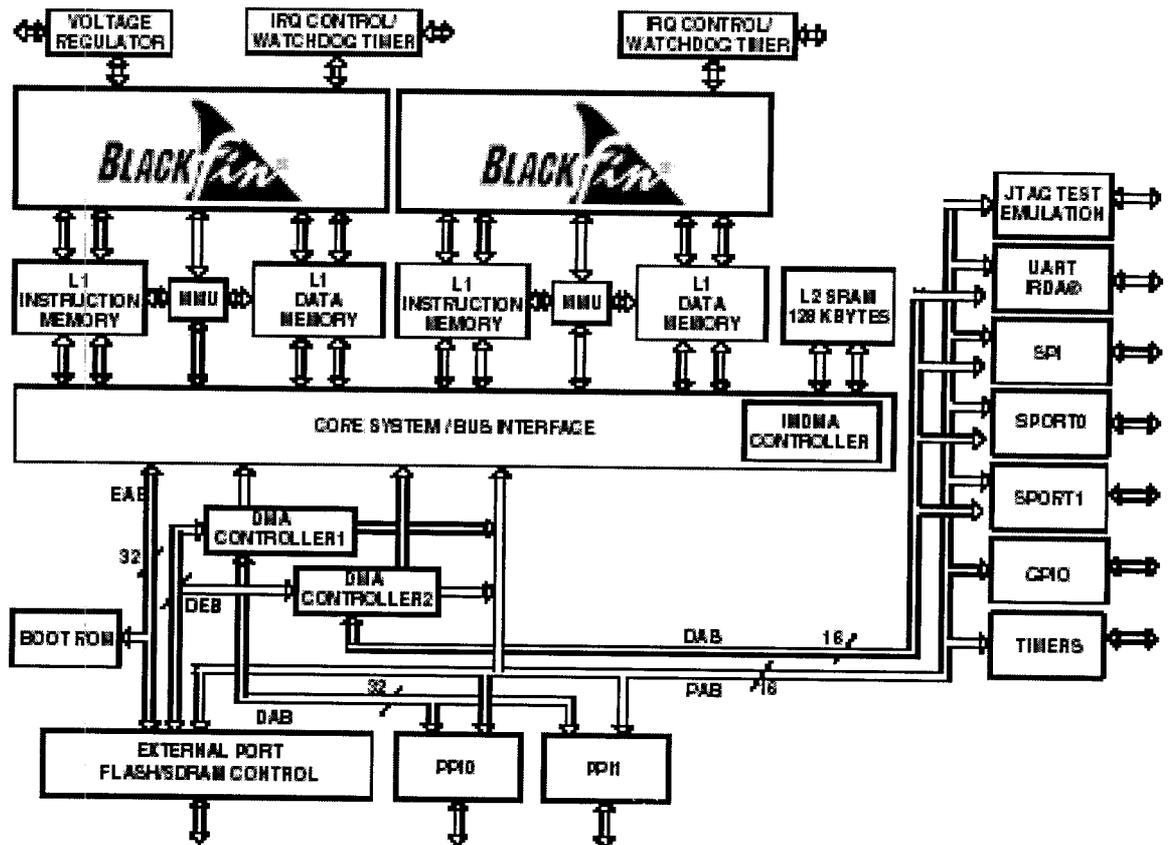
All Blackfin Processors offer fundamental benefits to the system designer which include

- High-performance signal processing and efficient control processing capability enabling a variety of new markets and applications.
- Dynamic Power Management (DPM) enabling the system designer to specifically tailor the device power consumption profile to the end system requirements.
- Easy to use mixed 16-/32-bit Instruction Set Architecture and development tool suite ensuring that product development time is minimized.

4.1.1 High Performance Processor Core

The Blackfin Processor architecture is based upon a 10-stage RISC MCU/DSP pipeline with a mixed 16-/32-bit Instruction Set Architecture designed for optimal code density. Blackfin processors architecture is also fully SIMD compliant and includes instructions for accelerated video and image processing. The architecture is well suited for full signal processing / analytical capabilities while also offering efficient RISC MCU control tasking capabilities - on either a single or dual core device. With the optimal code density and the possibility of little to no code optimization, quicker time to market can be achieved without running into performance headroom barriers seen on other traditional processor.

4.1.2 High Bandwidth DMA Capability

All Blackfin Processors have multiple, independent DMA controllers that support automated data transfers with minimal overhead from the processor core. DMA transfers can occur between the internal memories and any of the many DMA-capable peripherals. Transfers can also occur between the peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller.

4.1.3 Video Instructions

In addition to native support for 8-bit data, the word size common to many pixel-processing algorithms, the Blackfin Processor architecture includes instructions specifically defined to enhance performance in video processing applications. For example, Discrete Cosine Transform (DCT) is supported with an IEEE 1180 rounding operation, while the "SUM ABSOLUTE DIFFERENCE" instruction supports motion estimation algorithms used in video compression algorithms such as MPEG2, MPEG4, and JPEG.

Implementing video compression algorithms in software allows OEMs to adapt to evolving standards and new functional requirements without hardware changes. The enhanced instructions allow Blackfin Processors to be considered in applications previously addressed primarily by ASICs, VLIW media processors or hardwired chipsets. Ultimately, Blackfin Processors will help lower overall system cost while improving the time to market for the end application.

4.1.4 Efficient Control Processing

The Blackfin Processor architecture also offers a variety of benefits most often seen in RISC control processors. These features include a powerful and flexible hierarchical memory architecture, superior code density, and a variety of microcontroller-style peripherals including items such as 10/100 Ethernet MAC, UARTS, SPI, CAN controller, Timers with PWM support, Watchdog Timer, Real-Time Clock, and a glueless synchronous and asynchronous memory controller. All of these features provide the system designer with a great deal of design flexibility while minimizing end system costs.

4.1.5 Hierarchical Memory

Fig 4.2 Hierarchical Memory
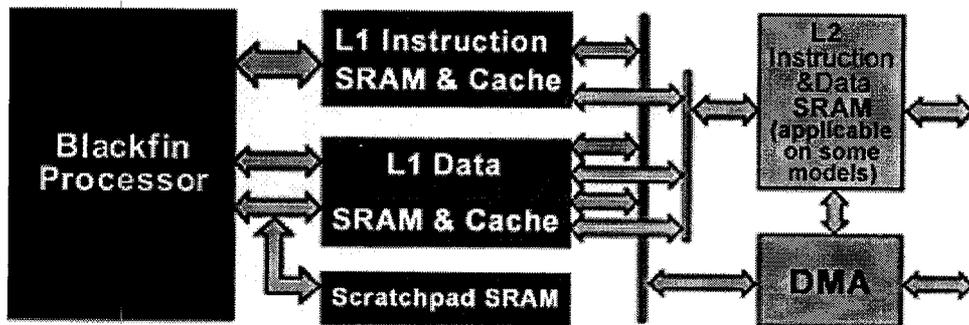
The Blackfin Processor memory architecture provides for both Level 1 (L1) and Level 2 (L2) memory blocks in device implementations. The L1 memory is connected directly to the processor core, runs at full system clock speed, and offers maximum system performance for time critical algorithm

segments. The L2 memory is a larger, bulk memory storage block that offers slightly reduced performance, but still faster than off-chip memory.

The L1 memory structure has been implemented to provide the performance needed for signal processing while offering the programming ease found in general purpose microcontrollers. This is accomplished by allowing the L1 memory to be configured as SRAM, cache, or a combination of both. By supporting both SRAM and cache programming models, system designers can allocate critical real time signal processing data sets that require high bandwidth and low latency into SRAM, while storing more 'soft' real time control / OS tasks in the cache memory.

The Memory Management Unit provides for a memory protection format that, when coupled with the core's User and Supervisor modes, can support a full Real Time Operating System. The RTOS runs in Supervisor mode and partitions blocks of memory and other system resources for the actual application software to run in User mode. Thus, the MMU offers an isolated and secure environment for robust systems and applications.

4.1.6 Superior Code Density

The Blackfin Processor architecture supports multi-length instruction encoding. Very frequently used control-type instructions are encoded as compact 16-bit words, with more mathematically intensive signal processing instructions encoded as 32-bit values. The processor will intermix and link 16-bit control instructions with 32-bit signal processing instructions into 64-bit groups to maximize memory packing. When caching and fetching

33

instructions, the core automatically fully packs the length of the bus because it does not have alignment constraints. When combined, these two features enable Blackfin Processors to deliver code density benchmarks comparable to industry-leading RISC processors.

4.1.7 Dynamic Power Management

All Blackfin Processors employ multiple power saving techniques. Blackfin Processors are based on a gated clock core design that selectively powers down functional units on an instruction-by-instruction basis. Blackfin Processors also support multiple power-down modes for periods where little or no CPU activity is required. Lastly, and probably most importantly, Blackfin Processors support a self-contained dynamic power management scheme whereby the operating frequency AND voltage can be independently manipulated to meet the performance requirements of the algorithm currently being executed. These transitions may occur continually under the control of an RTOS or user firmware. Most Blackfin processors offer on-chip core voltage regulation circuitry as well as operation to as low as 0.8V and are particularly well suited for portable applications requiring extended battery life.

4.1.8 Easy to Use

A single Blackfin Processor can be utilized in many applications previously requiring both a high performance signal processor and a separate efficient control processor. This benefit greatly reduces development time and costs, ultimately enabling end products to get to market sooner. Additionally, a

single set of development tools can be used, which decreases the system designer's initial expenses and learning curve.

4.2 ADSP-BF561 Core Architecture

The ADSP-BF561 has two identical Blackfin cores and each core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit arithmetic logic units (ALUs), four 8-bit video ALUs, and a 40-bit shifter, along with the functional units of each core as shown in Figure 4.2. The computational units process 8-, 16-, or 32-bit data from the register file.

Figure 4-3. Core Architecture of each ADSP-BF561 Core
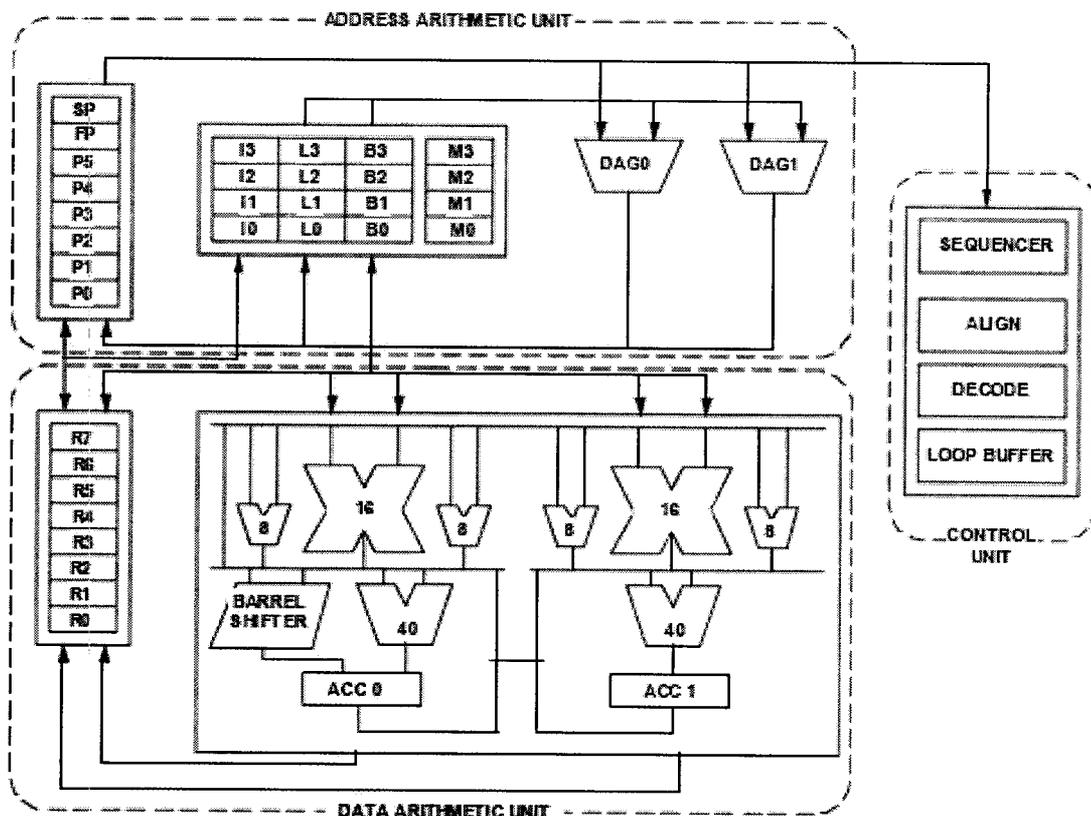
All the functional units of each core are described below.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16- by 16-bit multiply per cycle, with accumulation to a 40-bit result. Signed and unsigned formats, rounding, and saturation is supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. Many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 232 multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions includes byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/ absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions. For some instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). By also using the second ALU, quad 16-bit operations are possible.

The 40-bit shifter can deposit data and perform shifting, rotating, normalization, and extraction operations.

A program sequencer controls the instruction execution flow, including instruction alignment and decoding. For program flow control, the sequencer supports PC-relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that there are no visible pipeline effects when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit Index, Modify, Length, and Base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

Blackfin products support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only, the data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

Multiple L1 memory blocks are provided, which may be configured as a mix of SRAM and cache. The Memory Management Unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The ADSP-BF561 dual cores share an on-chip L2 memory system, which provides high speed SRAM access with somewhat longer latency than the L1 memory banks. The L2 memory is a unified instruction and data memory and can hold any mixture of code and data required by the system design.

The architecture provides three modes of operation: User, Supervisor, and Emulation. User mode has restricted access to a subset of system resources, thus providing a protected software environment. Supervisor and Emulation modes have unrestricted access to the system and core resources.

The Blackfin instruction set is optimized so that 16-bit op-codes represent the most frequently used instructions. Complex DSP instructions are encoded into 32-bit op-codes as multifunction instructions. Blackfin products support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions. This allows the programmer to use many of the core resources in a single instruction cycle.

The ADSP-BF561 assembly language uses an algebraic syntax. The architecture is also optimized for use with a C compiler.

Blackfin Processors include a high performance 16-/32-bit embedded processor core with a 10-stage RISC MCU/DSP pipeline, variable length ISA for optimal code density, and full SIMD support with instructions for accelerated video and multimedia processing. The Blackfin core is described below:

General-purpose register files

- Data register file

- Data types include 8-, 16-, or 32-bit signed or unsigned integer and 16- or 32-bit signed fractional

- 32-bit reads AND two 32-bit writes

- Address register file

- Stack pointer, Frame pointer

Data arithmetic unit

- Two 16-bit MACs

- Two 40-bit ALUs

- Four 8-bit video ALUs

- Single barrel shifter

Address arithmetic unit

- Memory fetches

- Index, length, base, and modify registers

- Circular buffering

Program sequencer unit

- Conditional jumps and subroutine calls

- Nested zero-overhead looping

- Code density

4.2.1 General purpose register files

The Blackfin Processor core includes an 8-entry by 32-bit data register file for general use by the computational units. Supported data types include 8-, 16-, or

32-bit signed or unsigned integer and 16- or 32-bit signed fractional. In every clock cycle, this multiported register file supports two 32-bit reads AND two 32-bit writes. It can also be accessed as a 16-entry by 16-bit data register file.

The address register file provides a general purpose addressing mechanism in addition to supporting circular buffering and stack maintenance. This register file consists of 8 entries and includes a frame pointer and a stack pointer. The frame pointer is useful for subroutine parameter passing, while the stack pointer is useful for storing the return address from subroutine calls.

4.2.2 Data Arithmetic Unit

The Data Arithmetic Unit contains roughly twice the system resources of previous Analog Devices 16-bit architectures. It contains:

- Two 16-bit MACs
- Two 40-bit ALUs
- Four 8-bit video ALUs
- Single barrel shifter

All computational resources can process 8-, 16-, or 32-bit operands from the data register file-R0 through R7. Each register can be accessed as a 32-bit register or a 16-bit register high or low half.

In a single clock cycle, this SIMD architecture can read AND write up to two 32-bit values. However, since the high and low halves of the R0 through R7 registers are individually addressable (Rx, Rx.H, or Rx.L), each computational block can

choose from either two 32-bit input values or four 16-bit input values with no restrictions on input data. The results of the computation can be written back into the register file as either a 32-bit entity or as the high or low 16-bit half of the register. Additionally, the method of accumulation can vary between data paths. For example, A0 could be a constant summation, and A1 could be a constant subtraction. This capability is referred to as 'flexible SIMD'.

Both accumulators are 40 bits in length, providing 8 bits of extended precision. Similar to the general-purpose registers, both accumulators can be accessed in 16-, 32-, or 40-bit increments. The Blackfin architecture also supports a combined add/subtract instruction that can generate two 16-, 32-, or 40-bit results or four 16-bit results. In the case where four 16-bit results are desired, the high and low half results can be interchanged. This is a very powerful capability and significantly improves, for instance, the FFT benchmark results.

4.2.3 Address Arithmetic Unit

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches from memory. The DAGs share a register file that contains four sets of 32-bit index (I), length(L), base(B), and modify(M) registers. There are also eight additional 32-bit address registers—P0 through P5, frame pointer, and stack pointer—that can be used as pointers for general indexing of variables and stack locations.

The four sets of I, L, B, and M registers are useful for implementing circular buffering. Used together, each set of index, length, and base registers can

implement a unique circular buffer in internal or external memory. The Blackfin architecture also supports a variety of addressing modes, including indirect, autoincrement and decrement, indexed, and bit reversed. Last, all address registers are 32 bits in length, supporting the full 4 Gbyte address range of the Blackfin Processor architecture.

4.2.4 Program sequencer unit

The program sequencer controls the flow of instruction execution and supports conditional jumps and subroutine calls, as well as nested zero-overhead looping. A multistage fully interlocked pipeline guarantees code is executed as expected and that all data hazards are hidden from the programmer. This type of pipeline guarantees result accuracy by stalling when necessary to achieve proper results. This greatly simplifies the programming task since the software engineer doesn't have to completely understand pipeline latency issues. On-chip interlocking hardware ensures that operand data is valid at the time of a particular instruction's execution.

The Blackfin architecture supports 16- and 32-bit instruction lengths in addition to limited multi-issue 64-bit instruction packets. This ensures maximum code density by encoding the most frequently used control instructions as compact 16-bit words and the more challenging math operations as 32-bit double words.

4.3 Memory Architecture

The processor architecture structures memory as a single, unified 4 GB address space using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space.

The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low-latency on-chip memory as cache or SRAM, and larger, lower-cost and lower-performance off-chip memory systems. Figure 4.3 shows the memory map for the ADSP-BF561.

Figure 4-4. ADSP-BF561 Internal/External Memory Map

	CORE A MEMORY MAP	CORE B MEMORY MAP

```
0XFFFF FFFF ─►
0XFFE0 0000 ─►
0XFFC0 0000 ─►
0XFFB0 1000 ─►
0XFFB0 0000 ─►
0XFFA1 4000 ─►
0XFFA1 0000 ─►
0XFFA0 4000 ─►
0XFFA0 0000 ─►
0XFF90 8000 ─►
0XFF90 4000 ─►
0XFF90 0000 ─►
0XFF80 8000 ─►
0XFF80 4000 ─►
0XFF80 0000 ─►
0XFF70 1000 ─►
0XFF70 0000 ─►
0XFF61 4000 ─►
0XFF61 0000 ─►
0XFF60 4000 ─►
0XFF60 0000 ─►
0XFF50 8000 ─►
0XFF50 4000 ─►
0XFF50 0000 ─►
0XFF40 8000 ─►
0XFF40 4000 ─►
0XFF40 0000 ─►
0XFEB2 0000 ─►
0XFEB0 0000 ─►
0XEF00 0800 ─►
0XEF00 0000 ─►
0X3000 0000 ─►
0X2C00 0000 ─►
0X2800 0000 ─►
0X2400 0000 ─►
0X2000 0000 ─►
TOP OF LAST ─►
SDRAM PAGE
0X0000 0000 ─►
```

CORE MMR REGISTERS | CORE MMR REGISTERS

SYSTEM MMR REGISTERS

RESERVED

L1 SCRATCHPAD SRAM (4K)

RESERVED

L1 INSTRUCTION SRAM/CACHE (16K)

RESERVED

L1 INSTRUCTION SRAM (16K)

RESERVED

L1 DATA BANK B SRAM/CACHE (16K)

L1 DATA BANK B SRAM (16K)

RESERVED

L1 DATA BANK A SRAM/CACHE (16K)

L1 DATA BANK A SRAM (16K)

RESERVED

L1 SCRATCHPAD SRAM (4K)

RESERVED

L1 INSTRUCTION SRAM/CACHE (16K)

RESERVED

L1 INSTRUCTION SRAM (16K)

RESERVED

L1 DATA BANK B SRAM/CACHE (16K)

L1 DATA BANK B SRAM (16K)

RESERVED

L1 DATA BANK A SRAM/CACHE (16K)

L1 DATA BANK A SRAM (16K)

RESERVED

L2 SRAM (128K)

RESERVED

BOOT ROM (2K)

RESERVED

ASYNC MEMORY BANK 3

ASYNC MEMORY BANK 2

ASYNC MEMORY BANK 1

ASYNC MEMORY BANK 0

RESERVED

SDRAM BANK 3

SDRAM BANK 2

SDRAM BANK 1

SDRAM BANK 0

INTERNAL MEMORY

EXTERNAL MEMORY

44

The memory DMA controller provides high-bandwidth data-movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

4.3.1 Internal Memory

Each core of the ADSP-BF561 has three blocks of on-chip memory that provide high-bandwidth access to the core:

- L1 instruction memory consisting of 32K bytes SRAM, of which 16K bytes can be configured as a four-way set-associative cache. This memory block is accessed at full processor speed.
- L1 data memory, consisting of two banks of 32K bytes each. One bank is always configured as SRAM while the other can be configured as SRAM or a two-way set associative cache.
- 4-Kbyte L1 scratchpad RAM, which runs at the full processor speed but is only accessible as data SRAM and cannot be configured as cache memory.

The ADSP-BF561 dual cores share a low latency, high-bandwidth on-chip Level 2 (L2) memory. It forms an on-chip memory hierarchy with L1 memory and provides much more capacity than L1 memory, but the latency is higher. The on-chip L2 memory is SRAM and can not be configured as cache. On-chip L2 memory is capable of storing both instructions and data.

4.3.2 External Memory

External (off-chip) memory is accessed via the External Bus Interface Unit (EBIU). This 32-bit interface provides a glueless connection to as many as four banks of synchronous DRAM (SDRAM) and as many as four banks of asynchronous memory devices including flash memory, EPROM, ROM, SRAM, and memory-mapped I/O devices.

The PC133-compliant SDRAM controller can be programmed to interface to up to 512 Mbytes of SDRAM.

The asynchronous memory controller can be programmed to control up to four banks of devices. Each bank occupies a 1 Mbyte segment regardless of the size of the devices used, so that these banks are only contiguous if each is fully populated with 1 Mbyte of memory.

4.3.3 I/O Memory Space

Blackfin products do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4 Gbyte address space. These are separated into two smaller blocks: one contains the control MMRs for all core functions and the other contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in Supervisor mode. They appear as reserved space to on-chip peripherals.

4.4 Why Blackfin561 processor?

Traditionally, embedded microcontroller engineers and digital signal processing engineers approached their crafts very differently and very separately. Today, with complex interactions occurring between external events and the application, control and signal processing are fundamentally intertwined.

As processing power keeps increasing, programmable processors have become a critical technology in many high-performance signal processing systems, often in the same application or signal chain as ADI's high-performance analog products.

The combined need for convergent capabilities and ever increasing processing power opens new opportunities for Analog Devices' processor families.

Blackfin® embodies a new breed of 16/32-bit embedded processor with the industry's highest performance and power efficiency for applications where a convergence of capabilities – multi-format audio, video, voice and image processing; multi-mode baseband and packet processing; and real-time security and control processing – are critical. It is this powerful combination of software flexibility and scalability that has gained Blackfin widespread adoption in convergent applications such as digital home entertainment; networked and streaming media; automotive telematics and infotainment; and digital radio and mobile TV.

4.4.1 Blackfin Highlights

- Single instruction-set architecture with processing performance that meets or beats the competition's DSP product range - and provides better power, cost, and memory efficiency

- 16/32-bit architecture enables next generation embedded applications

- Control, signal, and multimedia processing in a single core.

- Performance tunable for signal processing or power consumption through dynamic power management.

- Portfolio of code- and pin-compatible products. Under $5 to 1,500 MIPS - leverages engineering development across a wide range of end products.

- Twice the performance and half the power of competing DSPs*, enabling breakthrough specs and new applications.

- Quickly adopted into thousands of designs, supported by multiple tool chains and operating systems.

- Increases developer productivity

- Minimal optimization required due to powerful software development environment coupled with core performance.

- Extensive third party ecosystem mitigates risk

- Supported by industry-leading development tools, RTOS, software providers, and system integration partners.

5. CONCLUSION

Analyzing the two approaches we conclude that the approach 2 is more efficient than approach 1 due to the advantages explained in section 3.5. The efficiency of the second approach was found to be more than 90% by tests carried on 1000 samples. The second approach should also consider the following aspects: when there are no lane markings on the road, when the lane width varies and when the camera position is altered due to some reasons.

The evolution of the final product, i.e. LANE DEPARTURE WARNING SYSTEM requires intensive testing with real time inputs in order to implement in the hardware. This product will minimize the number of accidents due to lane departures hence saving human life and money.

Hence Lane Departure Warning System will be a proven, reliable product with the potential to become as much a part of overall vehicle safety. Once customers realize the significance of the lane departure problem, this system will become a must-have feature for all vehicles.

APPENDIX

1.MANUFACTURERS

Some of the manufactures are dealt in detail in this section.

1.1 ASSISTWARE TECHNOLOGY

Assistware is dedicated to improving highway safety through a suite of driver assistance aids. In 1999, AssistWare introduced SafeTRAC making it the industry's first commercially available Lane Departure Warning System built on years of research and development. This system combines both lane departure warning and drowsy driving detection. Today, SafeTRAC can be found on commercial truck and passenger vehicles worldwide. Assistware is committed to making the nation's highways a safer place and will continue to introduce new products to support that goal.

1.1.1 About SafeTRAC

SafeTRAC is an on-board electronic warning system that prevents crashes caused by driver drowsiness or distraction. SafeTRAC utilizes a small windshield mounted video camera to monitor the road ahead. It warns the driver if they begin to drift out of their lane without using their turn signal, and also provides a continuous 'score' of their driving performance. The system also detects drowsy or distracted driving by sensing weaving or erratic lane keeping. SafeTRAC has the potential to prevent thousands of highway deaths and save billions of dollars annually by reducing the number

of accidents caused by drowsy, distracted or inattentive driving. As a driver becomes fatigued or distracted, their score drops and SafeTRAC generates an alert recommending that he get rest.

1.1.2 New features and options include

• Flexible packaging − available in on-dash, in-dash and embedded OEM configurations.

• Driver data recorder − monitor short- and long-term driving performance, turn signal usage, number of departures, etc.

• Event video recorder − capture video image of the road ahead just prior to and immediately after an accident.

• 'Silence' feature - enables operator to temporarily disable the unit when in a construction zone, or other area with poor lane markings.

• Enhanced lane tracking algorithms − improve tracking accuracy reducing the already low number of false alarms.

• Password protection − allows fleet management to lockout certain convenience settings (volume, sensitivity, etc.) from being changed by the operator.

• Transportation grade components - ensure reliable operation, and high availability even under the harsh conditions of a commercial truck.

1.2 CITROËN

Citroën is committed to pursuing growth and efficiency through a culture of constant progress. The brand name also stands for quality of both products and services. Citroën has implemented a certified quality system through which it is aiming to identify and satisfy customer expectations even more effectively. The Lane Departure Warning System is a new driving aid that detects unintentional lane departures on motorways and dual carriageways at speeds of 80 kmph and above. The system is triggered automatically when the driver mistakenly allows the vehicle to stray out of lane.

1.2.1 Technology

When the vehicle moves across road markings (white line lane markers) without the indicator being used, infrared sensors behind the front bumper detect the movement and trigger the ECU which warns the driver by means of a vibrating signal on the left or right side of the driver's seat, depending which way the vehicle is drifting. The system is activated by a button on the central console and remains active when the engine is switched off. To detect unintentional lane departures, LDWS uses six infrared sensors which are fitted under the front bumper, three on each side. Each sensor is equipped with an infrared light-emitting diode and a detection cell. Lane departures are detected by variations in the reflections from the infrared beams emitted by the diode onto the road. The sensors can detect white lines as well as the temporary road markings in yellow, red and blue that are used in some European countries. The system identifies lines (continuous and broken) and other road markings such as directional arrows (except non-standard symbols).

1.3 DELPHI FOREWARN LANE DEPARTURE WARNING

Delphi is a leading global supplier of mobile electronics and transportation systems, including powertrain, safety, steering, thermal, and controls & security systems, electrical/electronic architecture, and in-car entertainment technologies. Engineered to meet and exceed the rigorous standards of the automotive industry, Delphi technology is also found in computing, communications, consumer electronics, energy and medical applications.

1.3.1 Description

Delphi forewarn lane departure warning system is a lane tracking system that helps alert drivers when they unintentionally drift out of their intended lane. Using a camera and image processing to detect painted lane markers up to 25 meters ahead of the equipped vehicle, the system determines the vehicle's heading and lateral position in the lane to provide the appropriate warning.

1.3.2 Benefits

• Helps drivers become aware of lane drifting quickly

• Does not report stopped objects along the roadside, reducing false alarms

• Flexible alert configuration based upon OEM requirements including audible, tactile and/or visual driver warnings

• Camera mounted behind the wiped area of the windshield allows driver to maintain a clear line of sight

- Camera can be shared with Delphi Active Night Vision system

1.3.3 Features

Lane change prediction

    b. Estimates lane width and road curvature to accurately determine vehicle heading and lateral position in the lane

    c. Extendable to lane-keeping through integration with electronic power steering and controllable brakes

    d. Helps enhance performance of currently available collision warning systems

- Image processing algorithms
- State estimation techniques to detect and track lane boundaries
- Blocked sensor notification
- Flexible alert configuration including simulated rumble strips, audible tones and hap-tic alerts

1.4 INFINITI

Infiniti developed a new Lane Departure Warning (LDW) system, which alerts drivers of an unintended movement of the vehicle out of a designated traffic lane. The new system utilizes a small camera, speed sensor, an indicator and an audible warning buzzer.

1.4.1 Technology

The Infiniti Lane Departure System recognizes lane markings through the use of a small camera mounted behind the rearview mirror. The camera's signal and the vehicle's speed are sent to the system's advanced microprocessing unit, which combines the information to calculate both the distance between the vehicle and the lane marking and the lateral velocity to the lane marking.

A judgment is then made as to whether the vehicle is moving out of the lane (depending on the distance and lateral velocity to the lane). If it is determined that the vehicle is leaving the lane, both visual (indicator light located on the instrument panel) and audible (buzzer) warning signals are generated, alerting the driver to take corrective action. The system will not operate if the camera can't detect the lane markers or if vehicle's speed is below 45 miles per hour.

1.5 ITERIS

Iteris is the technology leader in systems and sensors that optimize the flow of traffic and enhance driver safety. Iteris has combined outdoor image processing, traffic engineering and information technology to offer a broad range of safety solutions for surface transportation markets around the world. Iteris' product line includes: AutoVue, LDWS; Vantage, Vehicle Detection Systems; and Mil-Lektron, Video Transmission and Isolation products.

1.5.1 Technology

Lane Departure Warning (LDW) system by Iteris is a small, integrated unit consisting of a camera, onboard computer and software that easily attaches to the windshield, dashboard or overhead. It is an important safety and convenience feature that warns motorists if they are drifting out of their lanes. Iteris LDW is programmed to recognize the difference between the road and lane markings. The unit's camera tracks visible lane markings and continually feeds the information directly into the unit's computer, which combines this data with the vehicle's speed. Using image recognition software and Iteris proprietary algorithms, the computer can predict when a vehicle begins to drift towards an unintended lane change. When this occurs, the unit automatically emits the commonly known rumble strip sound, alerting the driver to make a correction.

Iteris LDW is a proven, reliable product with the potential to become as much a part of overall vehicle safety as airbags and ABS brakes. Once consumers realize the significance of the lane departure problem, AutoVue LDWS will become a "must have" feature.

1.6 MOBILEYE

Mobileye is a pioneer in the development of vision systems for intelligent transportation systems (ITS). Its mission is to develop vision systems for accident reduction and driver assistance. These systems work as a "third" eye for the driver. Mobileye has also developed the AWS(Advance Warning System), a vision system for driver assistance for the aftermarket providing lane departure warning, forward collision warning and headway monitoring. Mobileye's lane departure and vehicle detection technologies are also included in Delphi's Advanced Collision Mitigation Systems.

1.6.1 Lane Detection Technology

Lane detection technology detects road markings and provides the system with various measurements related to them. The technology utilizes a sophisticated filtering technique combined with detection and classification algorithms to detect a variety of lane markings including – solid, dashed, Bott's dots, double lane markings etc, under various weather conditions and on various road types (e.g. concrete, asphalt). The technology can identify both white and yellow lane markings, in daytime as well as night time conditions. Given that lane markings are visible; their detection is not hindered by the presence of clutter, shadows, rain, snow or any other disturbance on the road.

Mobileye's Lane Detection algorithms can measure the distance from the wheel to the lane markings, as well as providing a more detailed description of the lane marking, for example the width.

The Lane Detection technology is based upon a three-parameter lane markings model that accounts for lateral position, slope and curvature and has been tested using various sensors and validated by thousands of hours of driving in many countries and conditions.

1.6.2 Application

The core lane detection technology can be used for various applications, principally Lane Departure Warning (LDW), in which the driver is given a warning before unintentionally crossing a lane marking. The implementation is based upon the calculation of lateral speed of the vehicle with respect to the lane marking. The warning mechanism can be tuned for sensitivity, for example, the system can warn only when the vehicle is actually crossing the lane marking or it can give an early warning. The warning can be adapted to the type of road, for example it could provide the driver with more slack in case of narrow roads or allow the driver to "cut" curves. Depending on the system interfaces LDW can provide the driver with various types of warnings (e.g. hepatic or audible). LDW can also be utilized to warn of an unintentional roadway departure or provide Drowsy Driver alerts by monitoring irregular driving patterns associated with drowsiness.

1.7 SIEMENS

Siemens VDO is a leading international automotive supplier of electronics and mechatronics. As a development partner within the automobile industry, we manufacture a comprehensive spectrum of products relating to the drivetrain, engine management electronics and fuel injection. If a truck strays out of its lane, a critical situation can easily arise. Such situations could be prevented by pro.pilot Lane Departure Warning.

1.7.1 Technology

This system helps drivers to stay in lane. A highly dynamic CMOS camera mounted inside the cab, protected from the weather, scans the road up to 50 meters ahead of the vehicle for lane markings and a display on the instrument cluster shows the system status. The system then uses an intelligent algorithm to define a lane and continuously monitors whether the vehicle stays within it.

As soon as the driver seems about to stray out of lane unintentionally, i.e. without indicating, a warning is issued before
- the vehicle enters another lane,
- drives onto the verge or central reservation,
- leaves the road completely.

These warning signals can be individually customized and consist of the same noise as that created by rumble strips, with the volume increasing as the driver gets closer to the edge of the lane. This warning also helps reduce the risk of tire damage caused by deviating from the proper road surface.

This system is programmed to recognize and work with almost all road markings used worldwide, regardless of type and color and is also unaffected by rain and spray. The assistance function is automatically deactivated at speeds below 55 km/h to prevent the driver from being distracted in urban driving conditions where frequent lane changes are necessary.

REFERENCES

1. Rafael C. Gonzalez, Richard E. Woods (2004),"Digital Image Processing",Addison-Wesley Publishing Company, pp.1-15.

2. Rafael C. Gonzalez, Richard E. Woods, Steven L. Eddins (2006),"Digital Image Processing Using MATLAB", Dorling Kindersley (India) Pvt. Ltd.

3. www.analogdevices.com

4. www.mathworks.com

5. www.wikipedia.org

6. ADSP-BF561 Blackfin® Processor Hardware Reference, Revision 1.0, July 2005, Part Number 82-000561-01.