# On-Line UPS for Computers — Microprocessor Based

Project Work 1989



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**AUTHORS**

# S Y N O P S I S

This report discusses the details of uninterruptable power supply, which comprises of a switched mode power supply, transistorised inverter, battery, analog to digital converter and a microprocessor. UPS works in the continuous mode, in which the inverter operates continuously obtaining normal power through an a.c line. The a.c power is transformed to d.c which charges the battery at its appropriate level and powers the d.c / a.c inverter. In the event of failure of power, the battery will continue to supply power to the inverter , ensuring uninterruptible power supply to the load.

To achieve stabilisation the output voltage is stepped down and fed to analog to digital converter , which sends its output signals to the microprocessor. The microprocessor has been programmed to obtain the sine wave of desired amplitude.

# C O N T E N T S

# INTRODUCTION

## NEED FOR SWITCHED MODE POWER SUPPLY :

Electronic equipments which require direct current and voltages for their operation can be met with the use of batteries, but in order to improve the practicability in supplying power a separate circuit called switched mode power supply employing transistors, resistors and capacitors is developed.

## POWER SOURCE TO UPS :

As energy cannot be created, the power supply is fed continuously from an external a.c. or d.c. source. Batteries obtain power through charging and store it electrically by chemical means. These power supplies have transistors in the input circuit which inverts periodically d.c. into a.c. These devices make use of power transformers with various winding configurations depending upon the capacity.

## SIGNIFICANCE OF UPS :

For many modern installations such as telecommunication establishments or computer centers, a power faliure could result in transient disturbances, unstable voltage, dips and surges, brownouts and blackouts which would be disasterous, so the necessity of providing an UPS is increasingly seen as essential specially in computers. High speed data transfer between large capacity disc drives and C.P.U are particularly susceptible and results in corrupted data files, mysterious halts, jobs being suddenly aborted or system going into a loop. Loss of power even for a very short duration can cause real time data to be lost or can affect memories. The new types of semiconductor memories are particularly sensitive to a voltage loss of millisecond duration.

While servo-controlled stabilisers are powerless to prevent these problems, UPS system are fully solid state with a much faster response rate, can handle them besides providing a stable output voltage and frequency (due to incorporation of low pass filters and isolation transformers). UPS though gives a less faster response time and speed of correction besides higher inversion efficiency are particularly suited for high capacity disc drives and for critical load application.

**WORTH IN HAVING UPS ON ON-LINE :**

- It is ideal uninterruptible power supply as inverter operates continuously isolating the load from the surges.
- Doesn't need the use of separate stabilisers which it itself can produce spikes .
- Avoids solid state switches which causes time delay in switching.

**IMPORTANCE OF MICROPROCESSOR :**

Various power inverters use software control with microprocessor to implement the control functions most effectively and effeciently. Following are the advantages with the use of microprocessor.

- With mere change of software, different modulation strategies are possible which cannot be realised with hardware circuits.

- The modulatin index (i.e. the number of pulses per half cycle) can be changed.
- A number of UPS systems can be controlled by time multiplexing.
- Other processor controls can also be combined to the same controller.
- Microprocessor senses the different modes of operation in UPS viz. normal mode, emergency mode, recharge mode, overload, battery discharged and over temperature.
- Realising the sine weighted pulse width modulation is tedious using conventional hardware and also will be costly.

# D E S C R I P T I O N

The system comprises of a SMPS, ADC, battery , microprocessor based inverter and filter. The inverter supplies power to the load. The input a.c voltage is rectified to a d.c voltage in the SMPS and is fed to the inverter simultaneously charging the battery. During the power failure, the inverter continues to output while drawing power from the battery bank.

Uninterruptible power supply is basically of two types.

i) continuous mode type

ii) stand-by mode type

i) In continuous mode , the inverter operates continuously, as the main power supply with the commercial a.c. supply serving as stand by. Fig(2.1) shows this mode of operation.

ii) In stand-by mode , the commercial a.c. supply provides the main power source with the inverter serving as stand-by. Fig(2.2) shows this mode of operation.

The block diagram of the uninterruptible power supply is shown in Fig(2.3). It comprises of a SMPS which charges the battery as well as supplies the required power to the inverter. The line voltage is stepped down to a desired value through a transformer which is further rectified to a d.c. voltage at a required level maintaining a maximum current limit.

The d.c. voltage with the battery in parallel is filtered to reduce the ripple voltage level and fed to the inverter, the inverter provides continuous voltage and frequency stabilised alternative power source to the load, since the output of the UPS is purely isolated from the main line, it not only offers protection from power corruption problems but also maintains a load under blackout condition.

The inverter is basically pulse width modulated using a microprocessor to achieve low harmonic distortion at the a.c. output as well as to obtain the maximum efficiency from the system. Another requirement for the inverters with the depth of modulation without appreciable increase in the lower order harmonics. The PWM scheme which deals with the method of obtaining linear variations of the outpt voltage with the reduced lower order harmonics and without affecting the fundamental component, is done through software control by modifying the PWM pattern by suitably dropping a number of pulses per cycle and changing the depth of modulation so as to avoid any noticeable change in the output voltage.

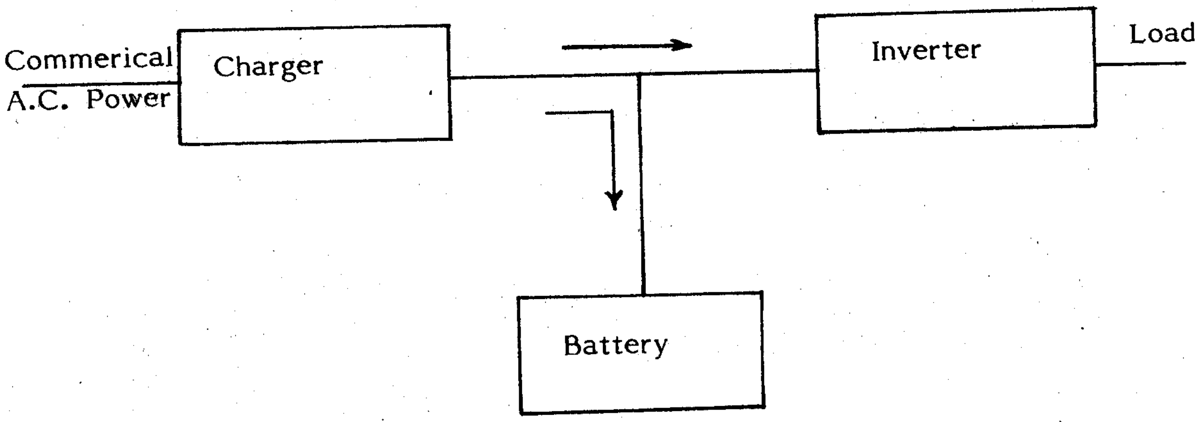



FIG. 2.1(a) NORMAL / RECHARGE

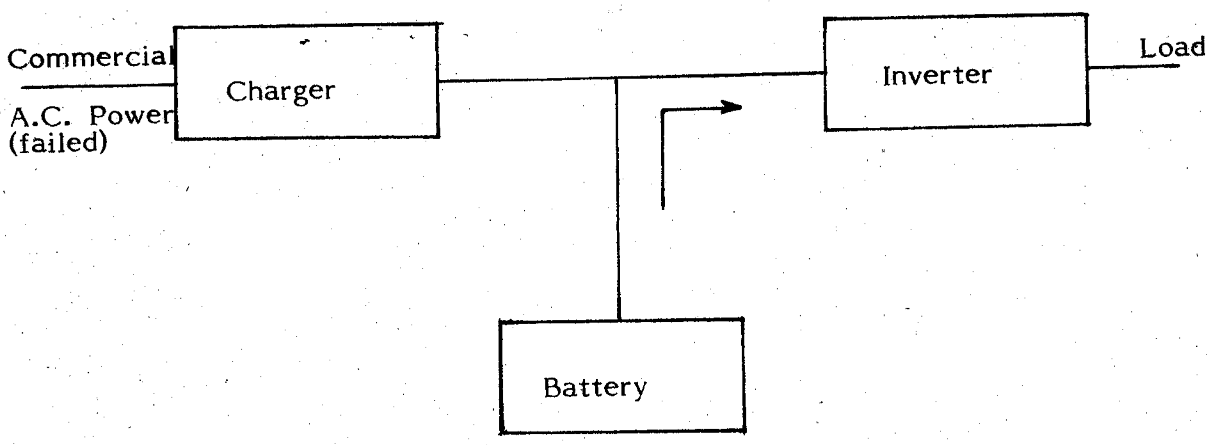



FIG. 2.1(b) EMERGENCY

## 2.1 CONTINUOUS MODE

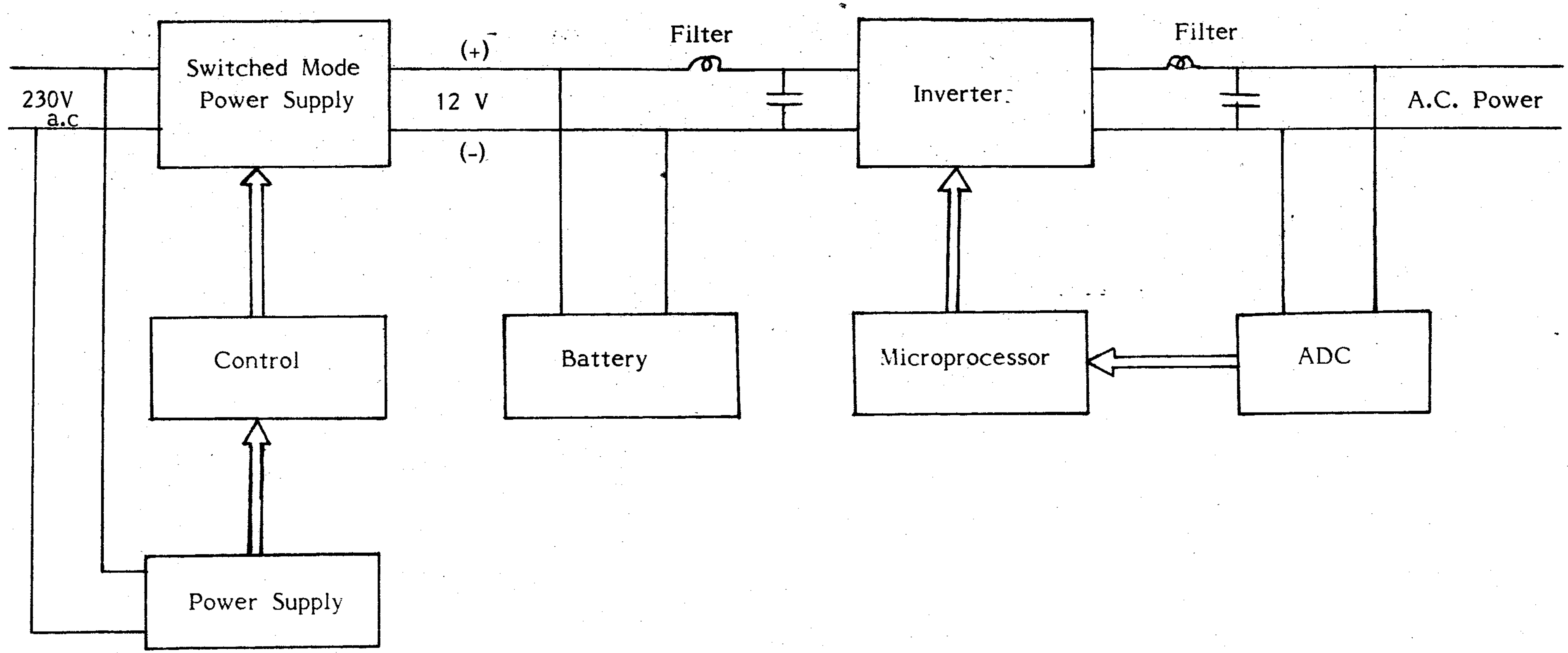



FIG. 2.3 BLOCK DIAGRAM OF U.P.S.

## PRINCIPLES OF OPERATION OF ON-LINE UPS

The typical low power mini UPS system is an ON-LINE system with three modes of operation during which a.c power is supplied to the load. These are 'normal', 'emergency' and 'recharge'. There are also three retriggerable inverter shutdown modes ; 'overload', 'battery discharged' and 'overtemperature'.

### NORMAL MODE:

The critical load is powered by the inverter. The rectifier derives power from the input a.c line and supplies d.c power to the inverter while simultaneously maintaining the battery fully charged.

### EMERGENCY MODE

The critical load is powered by the inverter. The input a.c line has failed, the rectifier is inoperative and the inverter remains within the specified regulation, single harmonic and total harmonic distortion limits during this mode.

RECHARGE MODE

The critical load is powered by the inverter. The input a.c line has returned after a failure and the rectifier has supplied d.c power to the inverter while simultaneously recharging the battery. The rectifier will continue to recharge the battery even with the inverter turned off.

OVERLOAD

The inverter will automatically restart twice after shutting down due to overload. If a third overload shut down occurs, the inverter remains shut down until manually restarted. High inrush-current designs shut down in the presence of sustained overloads greater than 30s with no allowed restart.

BATTERY DISCHARGE

When the battery is supplying power and the reserve(battery) operating time expires, the inverter shuts itself off, the actual operating time being dependent on the output load. When a prolonged power failure results in complete battery discharge and consequent inverter shutdown, designs incorporating automatic inverter restart will automatically resume inverter operation when the a.c input power is restored, manual restart of the inverter is eliminated.

<u>OVER TEMPERATURE</u>

Should the inverter heatsink on which the power semi-conductors are mounted exceed a preset temperature, the inverter will turn itself off. This mode may occur owing to an external obstruction of natural air flow around the enclosure, in which case the user can restart by letting it cool down, after allowing for air flow as described previously. The rectifier operates whenever the input a.c line is present and regardless of the status of the inverter. A replaceable line fuse, located on the front panel, protects the rectifier, and two internal fuses protect the battery and inverter.

# S W I T C H E D   M O D E   P O W E R   S U P P L Y

Electronic equipment require power supplies producing low voltages at large currents, up to 5A. Main electric power is obtained at 220 V, 50 Hz a.c. This has to be converted into low voltage d.c using stepdown transformer and rectifier and ripples are filtered with capacitors and inductors. In order to keep the output voltage constant, one must obtain a higher rectified voltage from the transformer and dissipate the excess power as heat. It means extra power loss and poorer efficiency.

A SMPS, on the otherhand, is highly efficient and operates on entirely different principles. It appeared when fast switching transistors were available at good current capacities. The output voltage of the SMPS is controlled by varying either the duty cycle or frequency, or both, of the signal that turns the switching transistor 'ON' or 'OFF'. By varying the duty cycle or frequency of the switching, one can vary the stored energy in each cycle, and thus control the output voltage. As a switch can only be 'ON' or 'OFF', it either allows energy to pass or stops, but does not dissipate energy in itself. Since, only the energy required to maintain the output voltage at a load current is drawn, there is no dissipation and hence a higher efficiency is obtained. Energy is pumped in discrete lumps, but the output voltage is kept steady by capacitor storage.

| PARAMETER | LINEAR SUPPLY | SMPS |
|---|---|---|
| 1. Efficiency | Less than 50% | More than 50% |
| 2. Static regulation | Quick regulation | Low to regulate |
| 3. Cost | More | Less |
| 4. Size and Weight | More | Less |
| 5. Ripple | Less | More |
| 6. Circuit Complexity | Less Complex | More Complex |

## TYPES

### i. FLYBACK SMPS

Energy is stored entirely in the magnetic flux of the inductor during the ON period of the switch. This energy is emptied into the output voltage circuit when the switch is in the open state. The output voltage depends upon the ratio of the ON to OFF period. The fig(4.1) is the basic circuit for flyback SMPS. When S1 is on the current passes through the primary of the transformer thereby inducing some voltage in the secondary. There is no secondary current because of diode D1 being reverse biased. When S1 opens, voltage across primary reverses thereby D1 gets forward biased thus, the energy stored in primary is transfered to the output capacitor and load. It is the cheapest but its regulation is poor and output ripple is greater. It is used for high voltage requirement.

### ii. FORWARD SMPS

When S1 is in ON position, the Vin voltage is applied at the primary side of the transformer. Voltage is induced, in accordance with the turns ratio, at the secondary. So D1 conducts and energy is supplied to load as well as inductor. When S1 turns 'OFF' the polarity of secondary side reverses and the energy to the load is supplied by inductor and capacitor via diode D2. Output voltage can be fixed by changing the duty cycle for input change. Useful where high voltage is a requirement, because it is not possible to have large inductive chokes at the output.

### iii. PUSH - PULL SMPS

The Push-pull SMPS basically comprises two single ended systems. There are two switching transistors represented by S1 and S2 and both turns ON and OFF alternatively. Voltage across the transistor is equal to supply voltage when it turns OFF. Amount of energy supplied by the choke is lesser as most of time energy to the load is supplied by the primary side. Here, magnetisation is in both directions, so transformer does not saturate. When output power is high, and tight regulation with low ripple is the requirement, then Push-pull SMPS is used. Generally, push-pull SMPS is used where output power is beyond 200 watts. The disadvantage of it is that the driving circuit becomes more complex because of the requirement of two power transistors.

Our unit uses Push-Pull SMPS.

COMPONENTS :

1. Core :

The flux is supported by the magnetic core of the coil. The core material chosen is ferrite as it can work at the frequencies above 15 KHz and has low energy loss due to hysterisis. Core size decides the value of flux which can be supported. Ferrite is usually operated below saturation level.

2. TRANSISTOR :

Used as a switch, a transistor inherently has a fast switch- on time, ample current rating to withstand surges and a high breakdown voltage rating to withstand the peak induced voltage in the coil at switch OFF. Transistors used has very small switching time, comprising turn on delay, rise time and fall times of current.

3. <u>DIODES</u> :

Diodes used are different from the common diffused junction types used at main frequency. Switching diodes with either gold doped junction or the schottky barrier diodes which have metal semi-conductor junctions are employed.

4. <u>CAPACITORS</u> :

Electrolytic capacitors are used for filtering ripples. The frequency of switching is high, of the order of several KHz.

<u>REGULATION</u> :

A switching power supply is regulated essentially by changing either the switch-on period or repetition rate of switching or both when the power is switched on, current is pumped into the coil and induces energy into it. This energy is released to the output via a fast recovery diode into a resevoir electrolytic capacitor. The output voltage across the capacitor is smooth and can drive the d.c load. As load varies, the output voltage drops. This is compensated by increasing the pulse width during which the current increases in the coil. More width means more time for the current to rise to a greater value, causing an increased storage of magnetic energy in each cycle. The IC(SG3524) used has built-in PWM to vary the on time of the series pass transistor.

WORKING

The SMPS works directly on mains, main voltage is rectified with the use of Bridge rectifier and filtered by a LC filter. The unregulated d.c voltage is fed to the centre tap of the ferrite core transformer having two secondaries, with specifications of 12V and 15V respectively operating at 20 KHz. 12V secondary is fed to the inverter and the 15V secondary is fed to the charging circuit simultaneously. Switching of the transistors is done by darlington pairs . Charger transistor is controlled by pulse width modulaion as shown in FIG 4.4 .

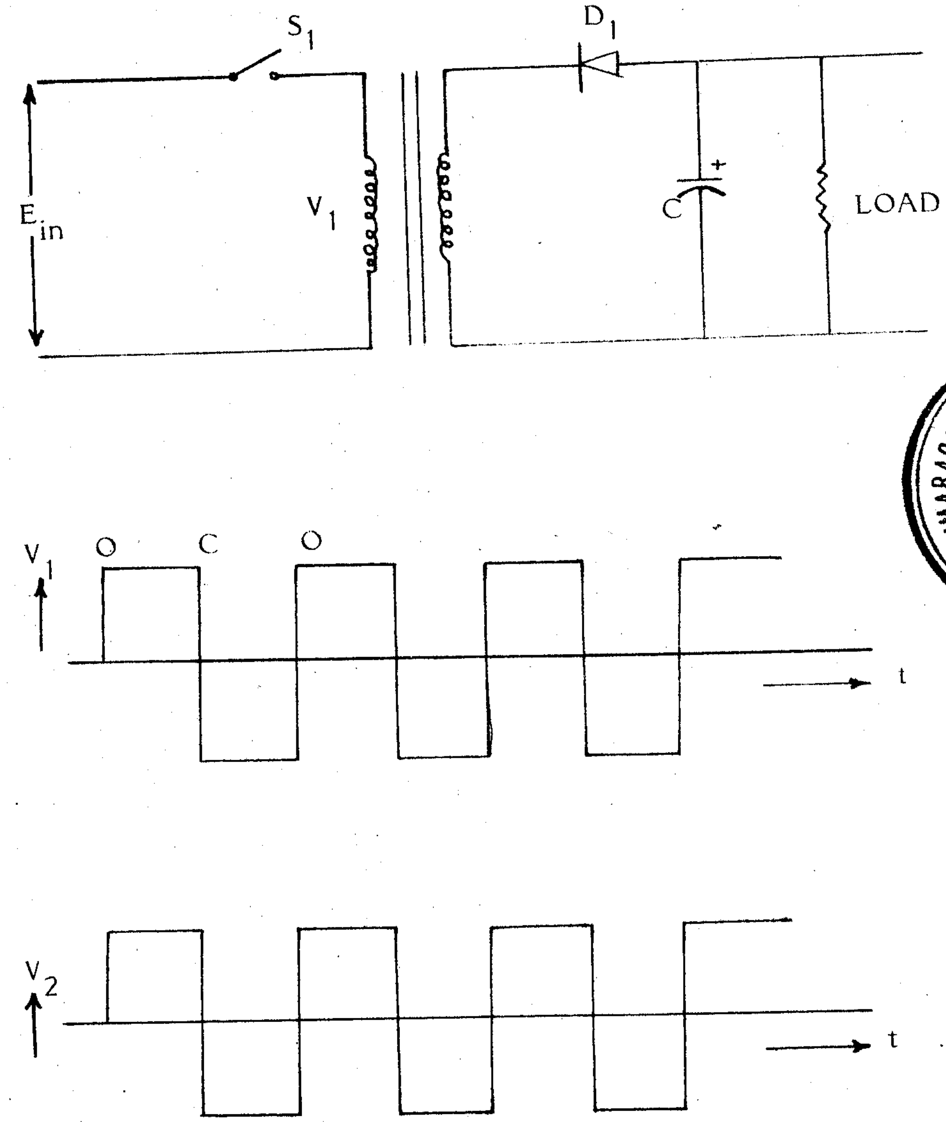



FIG: 4.1 FLYBACK SMPS



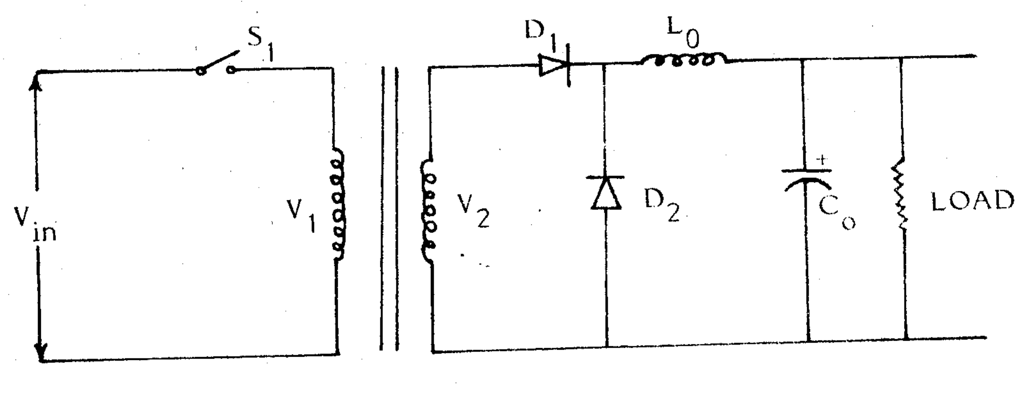
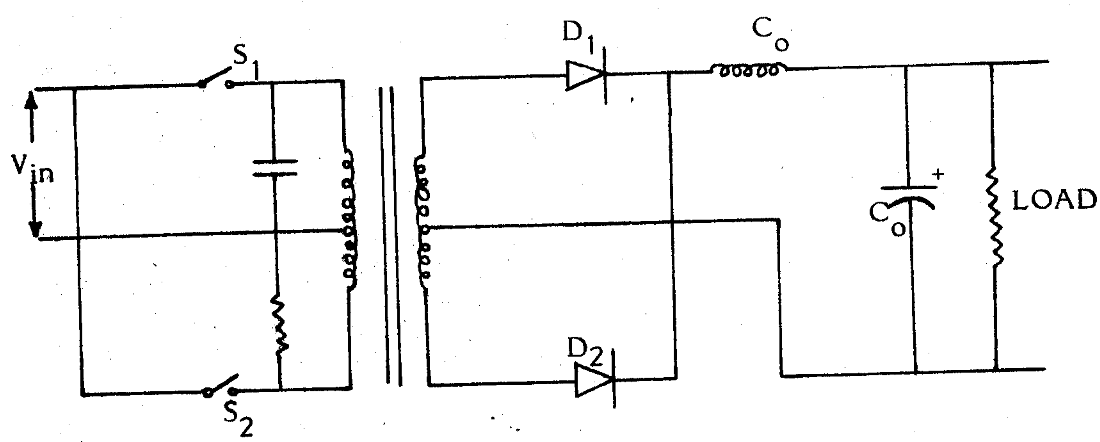



FIG: 4.2 FORWARD SMPS



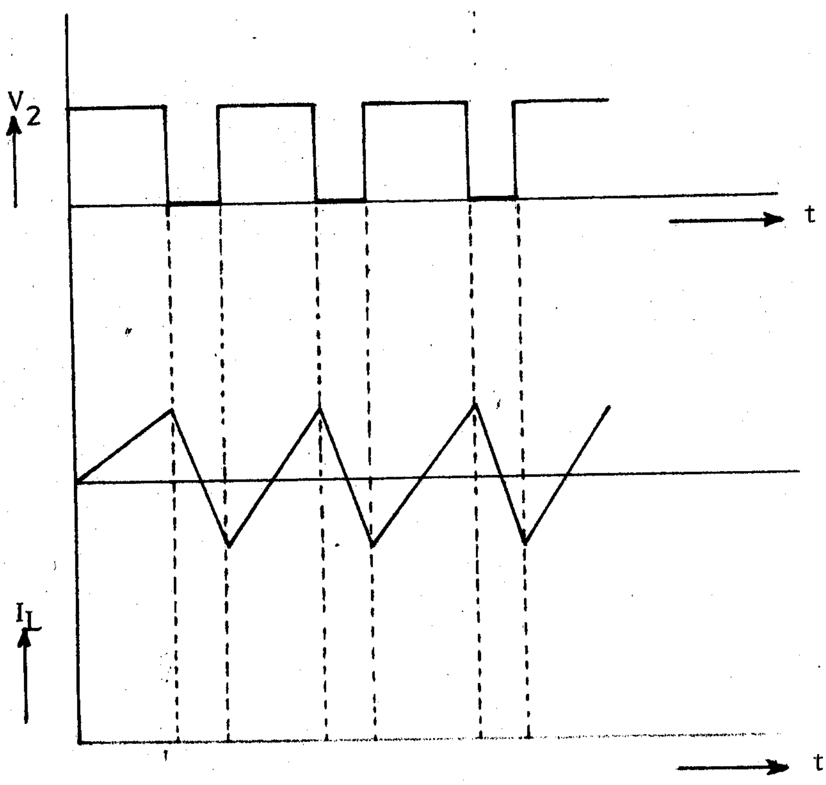
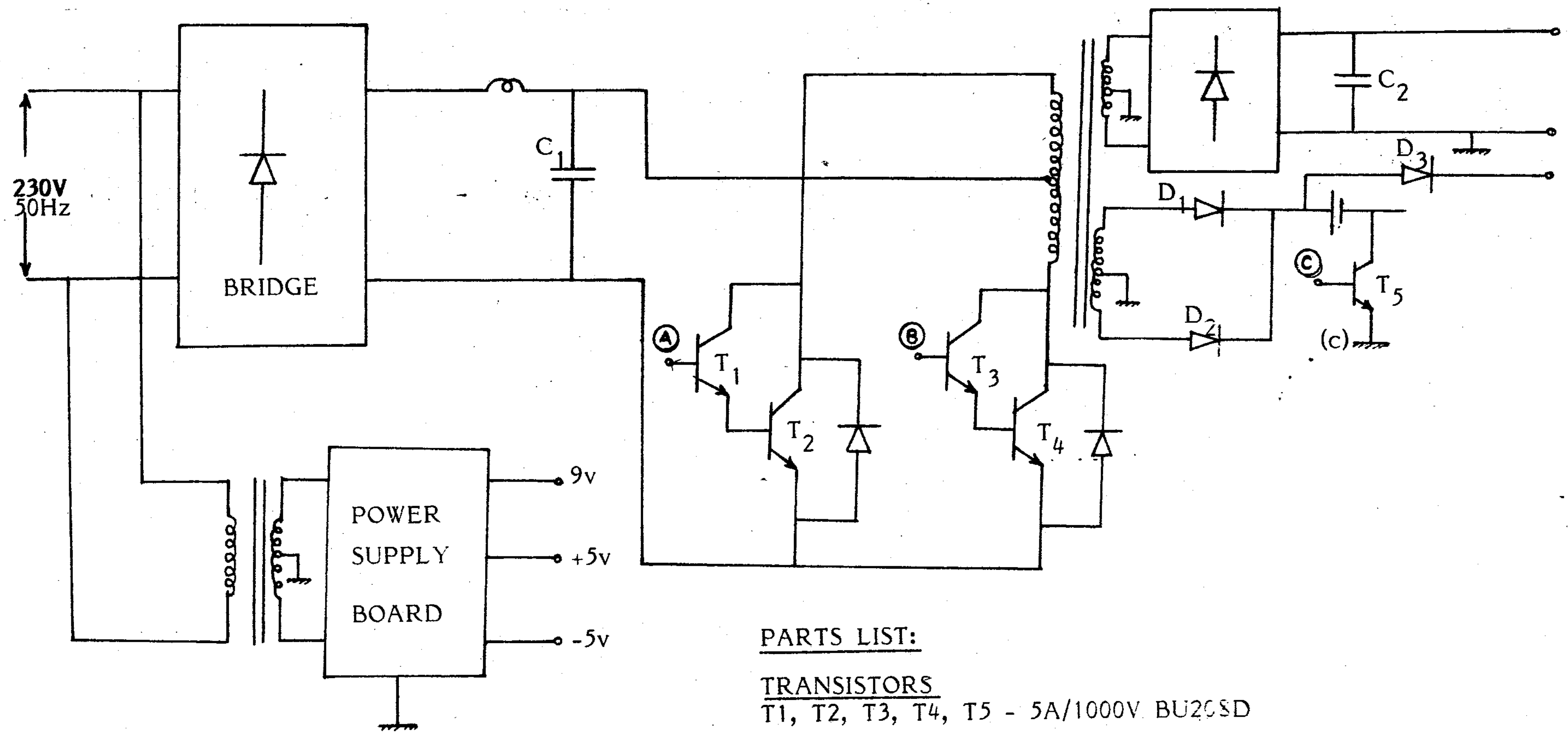




**FIG: 4.3 PUSH-PULL SMPS**




PARTS LIST:

TRANSISTORS
T1, T2, T3, T4, T5 - 5A/1000V BU208D
DIODES
INPUT DIODES - 12A / 800V MS BYW -88 - 1200
OUTPUT DIODES - 35A / 200V D4004
CAPACITOR
$C_1$ - 330 F / 450V
BATTERY - 12V
A, B, C FROM IC3524

**FIG 4.4 SWITCHED MODE POWER SUPPLY CIRCUIT**

# CONTROL CIRCUIT

This SMPS converts an alternating voltage into a stabilised d.c voltage. To achieve this, the input voltage is rectified and periodically connected to the load by a switching transistor, output transformer and filter acting as a d.c to d.c converter. Unlike a series regulator, the SMPS does not incorporate a power-dissipating series control element and is therefore much more efficient. Since, the switching can be effected at ultrasonic frequency, the size and weight of SMPS circuit components, and the losses they introduce, can be minimised. However, although the SMPS is lightweight, compact, and efficient, it must incorporate a complex control circuit capable of performing

i. Generation of drive pulses for the SMPS switching transistor.

ii. Control of the duty factor (pulse duration) of the drive pulses to counteract load variations.

In addition to performing these control functions, the circuit must also protect the supply from hazardous operating conditions by providing.

a. Overvoltage and overload protections.

b. Protection if the supply voltage to the control circuit is too low.

c. Protection in the event of a fault in the feedback circuit.

d. Protection if the core of the output transformer becomes saturated.

The monolithic IC(SG 3524) contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in the 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut down circuitry. This device can be used for switching regulations of either polarities, transformer coupled d.c to d.c converters transformer less voltage doublers and polarity converters, as well as other power control applications.

FEATURES

i. Complete PWM power control circuitry.

ii. Single ended or push-pull outputs.

iii. Line and load regulation of 0.2%.

iv. 1% maximum temperature variation.

v. Total supply current less than 10 mA.

vi. Operation beyond 100 KHz.

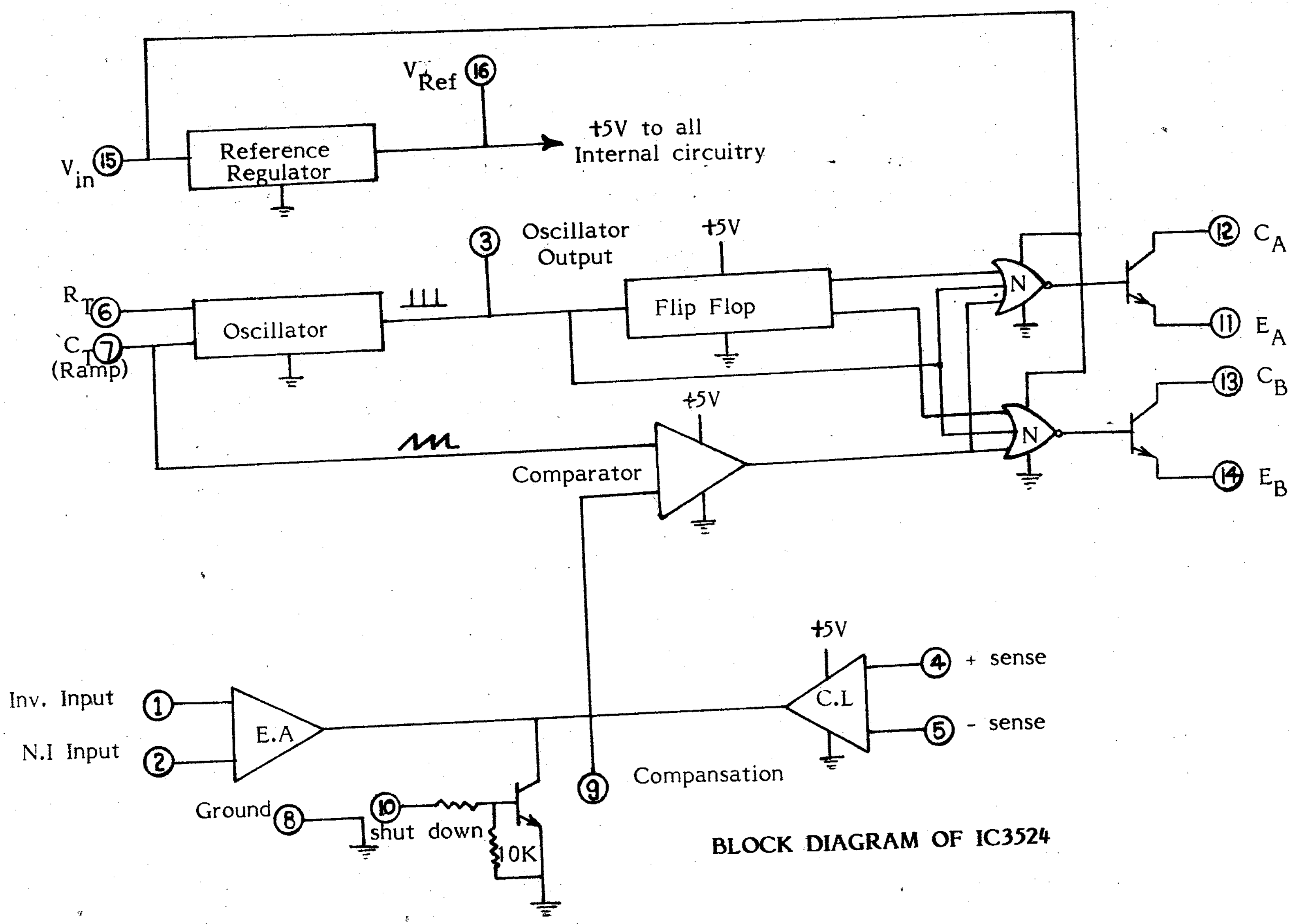
**ABSOLUTE MAXIMUM RATINGS :**

| | | |
|---|---|---|
| Output voltage | ---- | 40 V |
| Output current(each output) | ---- | 100 mA |
| Reference output current | ---- | 50 mA |
| Oscillator charging current | ---- | 5 mA |
| Power dissipation(package limitation) | ---- | 1000 mW |
| Derate above 25 $^{o}$C | ---- | 8mW / $^{o}$C |
| Operating temperature range | ---- | 0 $^{o}$C to +70 $^{o}$C |
| Storage temperature range | ---- | -65 $^{o}$C to +150 $^{o}$C |

## OSCILLATOR DESIGN:

The oscillator period is approximately t=RtCt where t is in microseconds when Rt=Ohms and Ct=microfarads.The oscillator in the IC SG 3524 uses an external resistor( Rt ) to establish a constant charging current into an external capacitor(Ct).The charging current is equal to 3.6 V / Rt and should be kept with in the range of approximately 30 micro amps to 2mA, ie., 1.8 K <Rt<100 K. The range of values for Ct also has limits as the discharge time of Ct determines the pulse width of the oscillator output pulses.Practical values of Ct fall between 0.001 and 1.0 mfd.

The use of FIG 5.3 will allow selection of Rt and Ct for a wide range of operating frequencies.For push-pull applications, the outputs,are separated and the flip-flop divides the frequency such that each output's duty cycle is 0 to 45 % and the overall frequency is half that of the oscillator.




**BLOCK DIAGRAM OF IC3524**

TOP VIEW

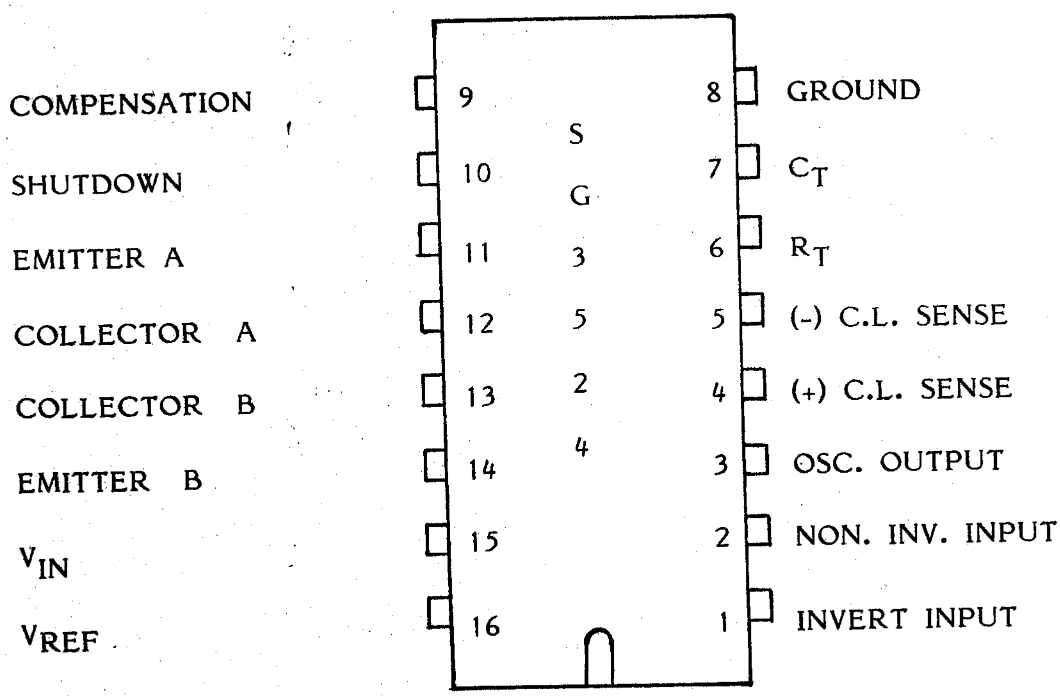



**FIG : 5.2. CONNECTION DIAGRAM**

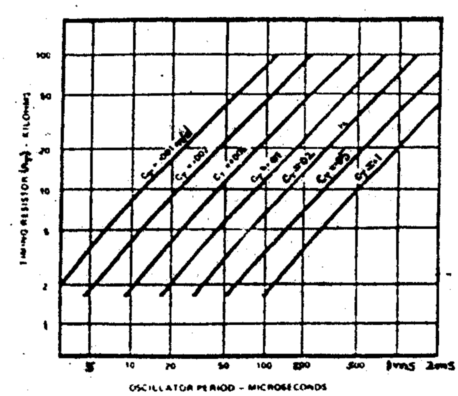
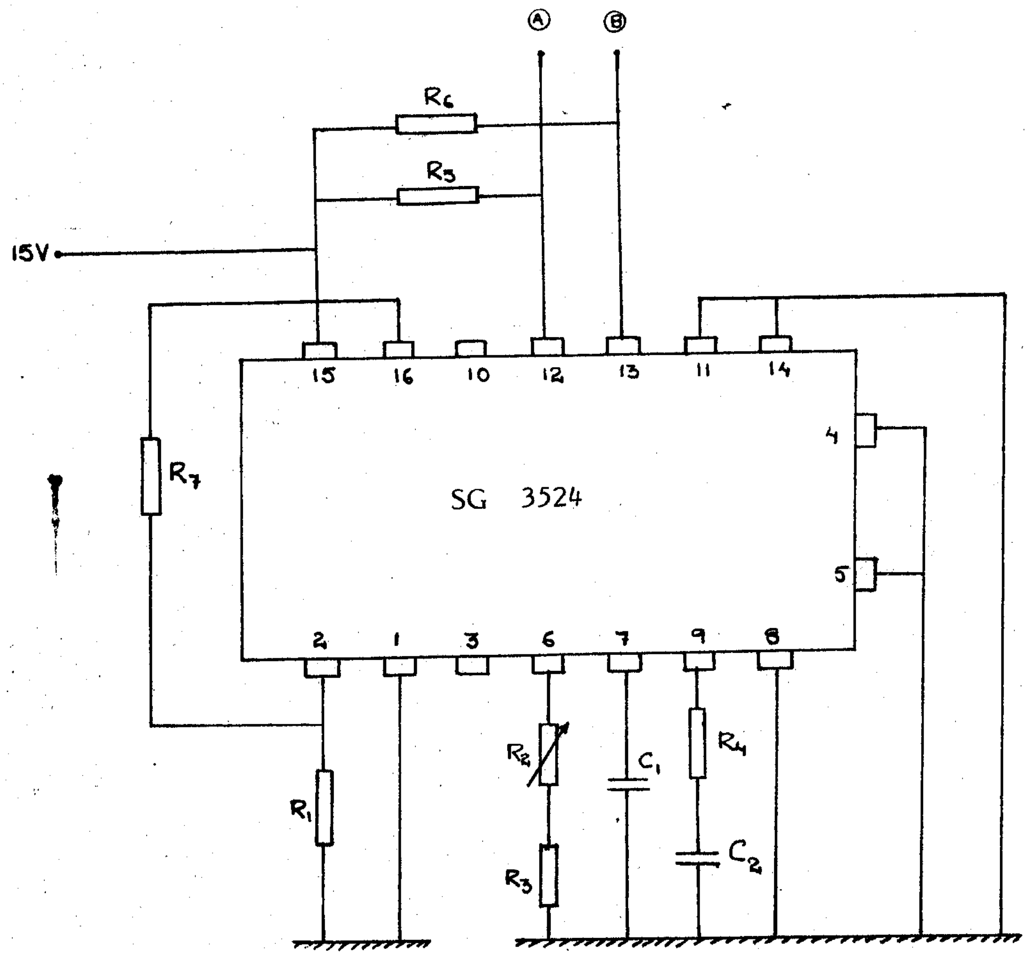



**FIG : 5.3. OSCILLATER DESIGN OF 3524**




**PARTS LIST**

**RESISTORS**

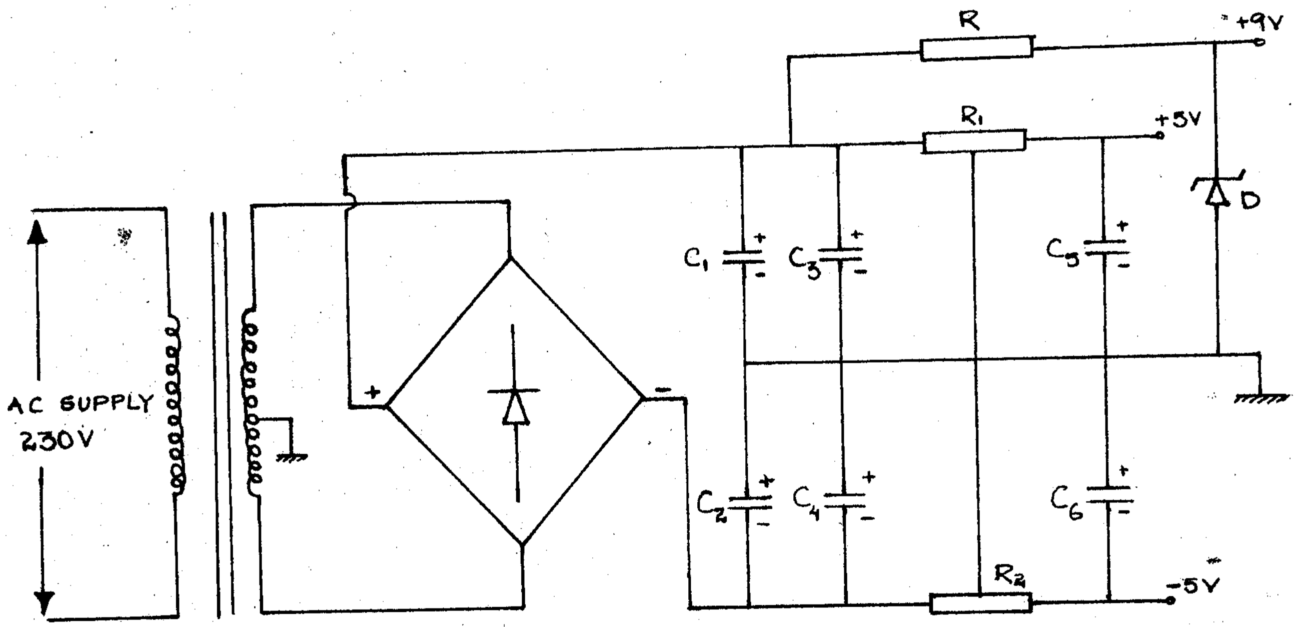
| | | |
|---|---|---|
| $R_1$ | = | 5K |
| $R_2$ | = | 7.2K |
| $R_3$ | = | 1K |
| $R_4$ | = | 20K |
| $R_5$ | = | 1K |
| $R_6$ | = | 1K |
| $R_7$ | = | 5K |

A, B TO SMPS

**CAPACITORS**

| | | |
|---|---|---|
| $C_1$ | = | 0.01MF |
| $C_2$ | = | 0.001MF |

**FIG. 5.4 PUSH - PULL OUTPUT CIRCUIT**




**PARTS LIST**

**CAPACITORS**

| | | |
|---|---|---|
| $C_1$ | - | 2000M/25V |
| $C_2$ | - | 470M/25V |
| $C_3$ | - | 10M/25V |
| $C_4$ | - | 10M/25V |
| $C_5$ | - | 4.7M/16V |
| $C_6$ | - | 4.7M/16V |

**RESISTOR**

R - 330 /2W

**3 PIN REGULATOR**

$R_1$ - 7805

$R_2$ - 7905

**ZENER DIODE**

D - 9.1V / 1W

FIG. 5.5 POWER SUPPLY FOR THE CONTROL UNIT

# I N V E R T E R S

An inverter circuit is used to convert d.c power to a.c power.The conversion can be achieved either by transistors or by SCRs.For low and medium power outputs,transistorised inverters are suitable but for high power outputs SCRs should be used.Our unit uses transistors for the conversion.Transistors have some edge over SCRs regarding the switching speed,simplicity in control circuits,higher efficiency and greater reliablity.This is mainly because of the fact the SCR inverters require extra circuits to turn SCRs off moreover additional complex logic circuits may be required to prevent false triggering and provide proper communication timing.

An inverter system can be considered to have two basic configurations, the driven and self oscillating. The driven type has a seperate timing circuit which feeds into the drive unit controlling the switch turning the output power ON and OFF as shown in FIG 6.1(a). If the load is known and fixed, then a saving can be made by using the self-positive feedback taken from the power output given in the FIG 6.1(b). In both of these configurations the output stage may employ either a single active device-single ended or two devices in a push-pull arrangement.

## PUSH-PULL SELF OSCILLATING CIRCUITS :

An inverter system can be considered to have push-pull self oscillating type when the timing and drive are one using positive feedback taken from the power output. In this configuration the output stage employs two devices in a push-pull arrangement.

For a simple supply to produce an output voltage which is a multiple or sub-multiple of the input a single saturating transformer converter is ideal. The running frequency is independent of loading and can be as high as 50 KHz, without excessive losses in the core. The output voltage regulation will be nearly as good as the input voltage. Although the transistor turn 'ON' dissipation is low the turn 'OFF' dissipation is high and is also independent of loading.

## PUSH - PULL DRIVEN CIRCUITS :

A practical and useful push-pull driven inverter, especially in times of electricity strikes, is one which operates from a 12V battery and provides a 300 watts, 50 Hz supply. The basic output configuration is shown in FIG 6.2. On the primary side each transistors collector will swing from Vce(sat) i.e. approximately earth to twice the maximum battery voltage (33V). Therefore with a safety factor, a device rating of, say, 40 V would be suitable. With 300 W output 240 V the average secondary current is 1.25 A. Assuming an efficiency of 80% the effective required average secondary current is 1.55 A. The transformer's turns ratio must be 20, therefore the primary peak current, which must be switched by each transistor in turn, is approximately 33 A. 33 A, 40 V transistors do exist but they are extremely expensive, therefore the use of lower current transistors in parallel must usually be considered.

The base current drive to the output stage needs to be about 4 A each side and is supplied by a driver and timing circuit shown in block diagram form in FIG 6.3 . The oscillator runs at 100 Hz, i.e. twice the required output frequency, and its output, W, is divided using a bistable /2, so that two complementary outputs, y and z, of 50 Hz with equal mark space ratio are obtained. Waveforms y and z are ac coupled to driver stages so that on start up all power transistors are certain to be 'OFF' until the oscillator is functioning correctly and no damage occurs to them. Using a 3:1 driver transformer, TX, the required secondary current, approximately 4 A, is produced from 1.3 A primary current available. However, the driver transformer employed is a bulky and usually a costly item. Therefore it is worth considering its removal by using the Darlington transistors in place of the discrete transistors to obtain the necessary gain in the system. Darlington transistors have a problem in that their turn off($t_{off}$) is long ($\simeq$10ms). The driver circuit must make account of this, otherwise both sets of output transistors could be 'ON' at the same time. Fig.6.4 shows then block diagram how this is accomplished. As can be seen, it is achieved by inserting a monostable between the oscillators and divide-by-two circuit, and gating its output X, with the y and z complementary outputs to give new waveforms, a and b, to be a.c coupled to the driver stages.

The waveform diagrams show that the period of the monostable (_~10ms) is therefore subtracted from the loading edges of the waveforms a and b applied to the driver stages, thus allowing sufficient time for the 'ON' Darlington transistors to switch 'OFF' before the others turn 'ON'.

SINUSOIDAL- PULSE MODULATED INVERTER :

The pulse modulated inverter has sinusoidal pulse width modulated drive for the Darlington pairs .Though in multiple-pulse modulation ,the output harmonic content is less than that in a single-pulse modulation, the situation can be further improved by using sinusoidal modulation.In this modulation ,the mean output voltage is controlled according to a sine function in every half period as shown in FIG 6.5 .The control circuit is more complicated . The control waveform is achieved by comparing a sine wave of variable amplitude of a particular frequency ' F ' with a triangular wave of fixed amplitude with a much higher frequency ' Fo ' . The triangular wave is reversed in polarity at the end of each half cycle of the output voltage

The ratio of the frequency of the above two waveforms must be an integer ' N '

$$2 * N = Fo / F$$

where N represents the number of voltage pulses per half cycle .

The comparator gives out a pulse when the sinusoidal voltage is greater than the triangular voltage . The output voltage is controlled by altering the amplitude ofthe sine wave with range 0 to Vp ,where Vp is the peak of the triangular voltage.

The output harmonic content is a function of ' N ' and is much less compared with other pulse width modulation . It is observed that if the peak of the sine voltage is less than half the peak of the triangular voltage , harmonics less than 2*N are eliminated . Since the hardware required generating the above sinusoidal pulse modulation is complicated ,microprocessor is used for generating sinusoidal modulated drive(using timer chip 8253 ,PPI 8255 and an oscillator circuit).

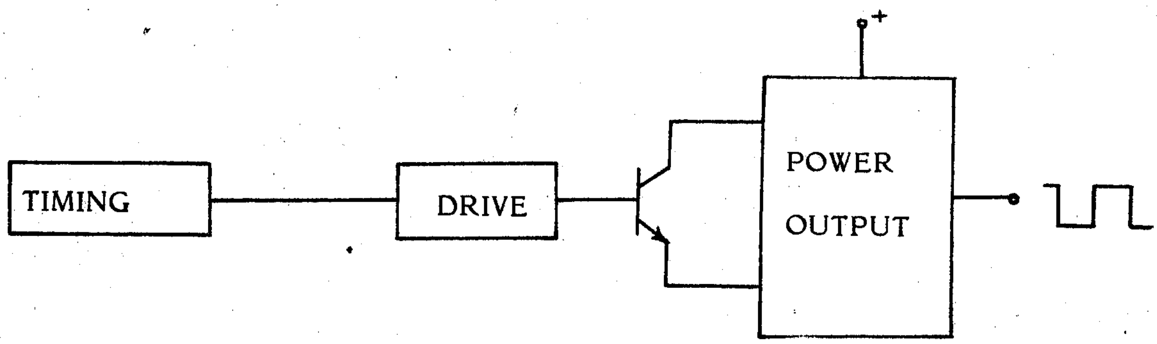



**FIG : 6.1(a) DRIVEN**

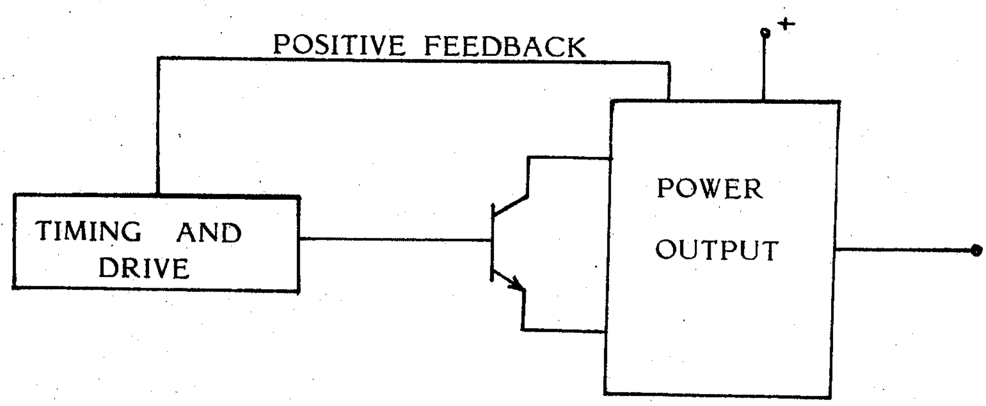



**FIG : 6.1(b) SELF OSCILLATING**

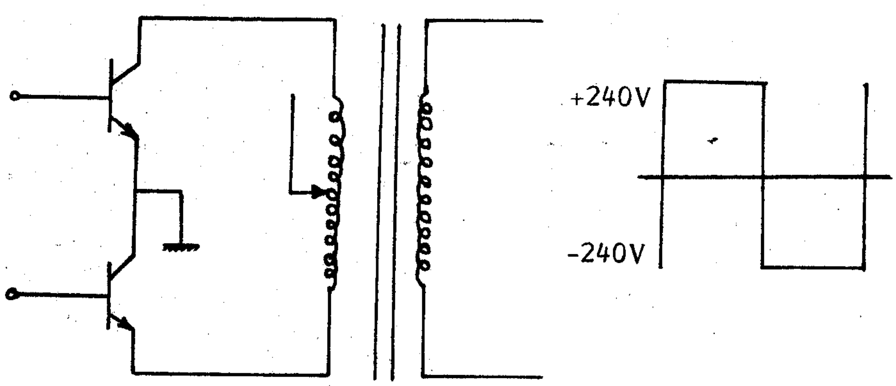



**FIG : 6.2 BASIC OUTPUT CONFIGURATION**

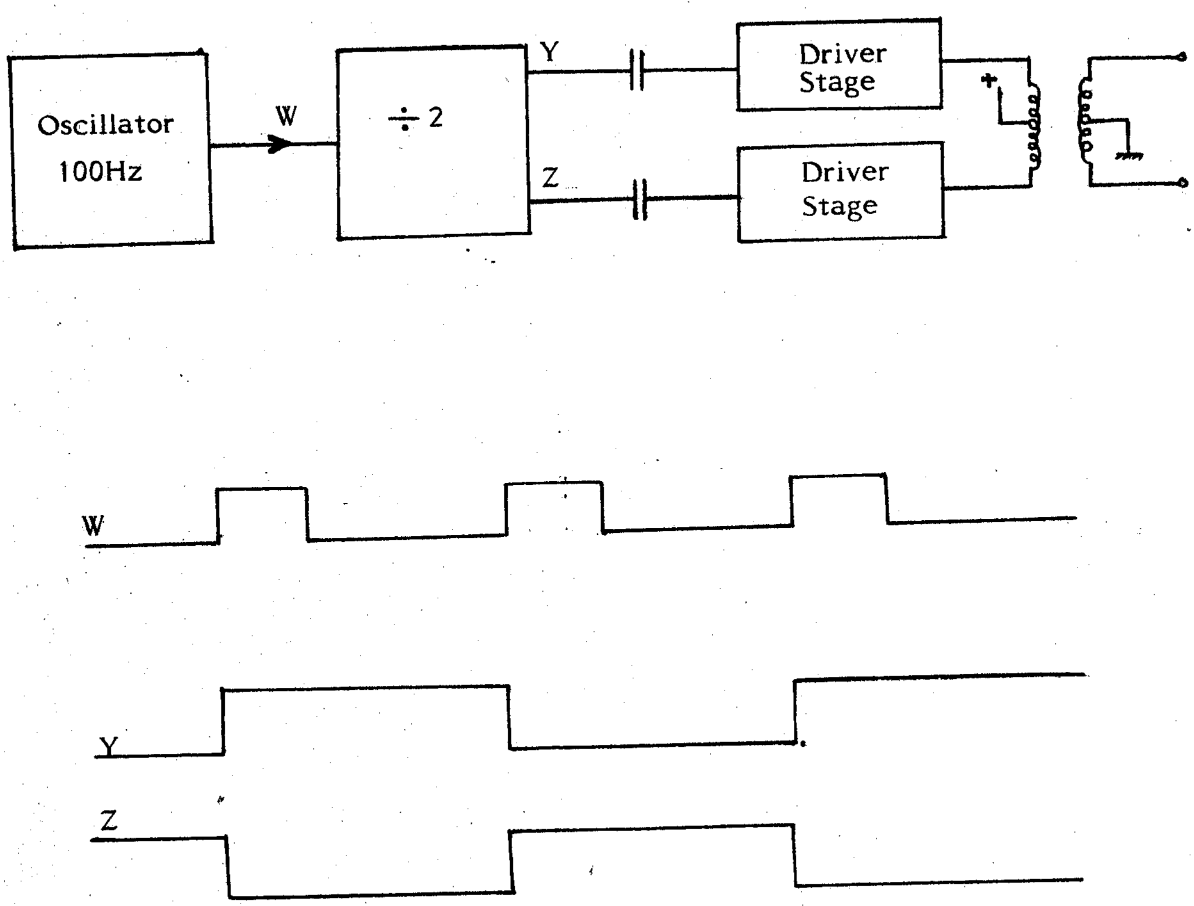



FIG. 6.3 BLOCK DIAGRAM AND DRIVER CIRCUIT

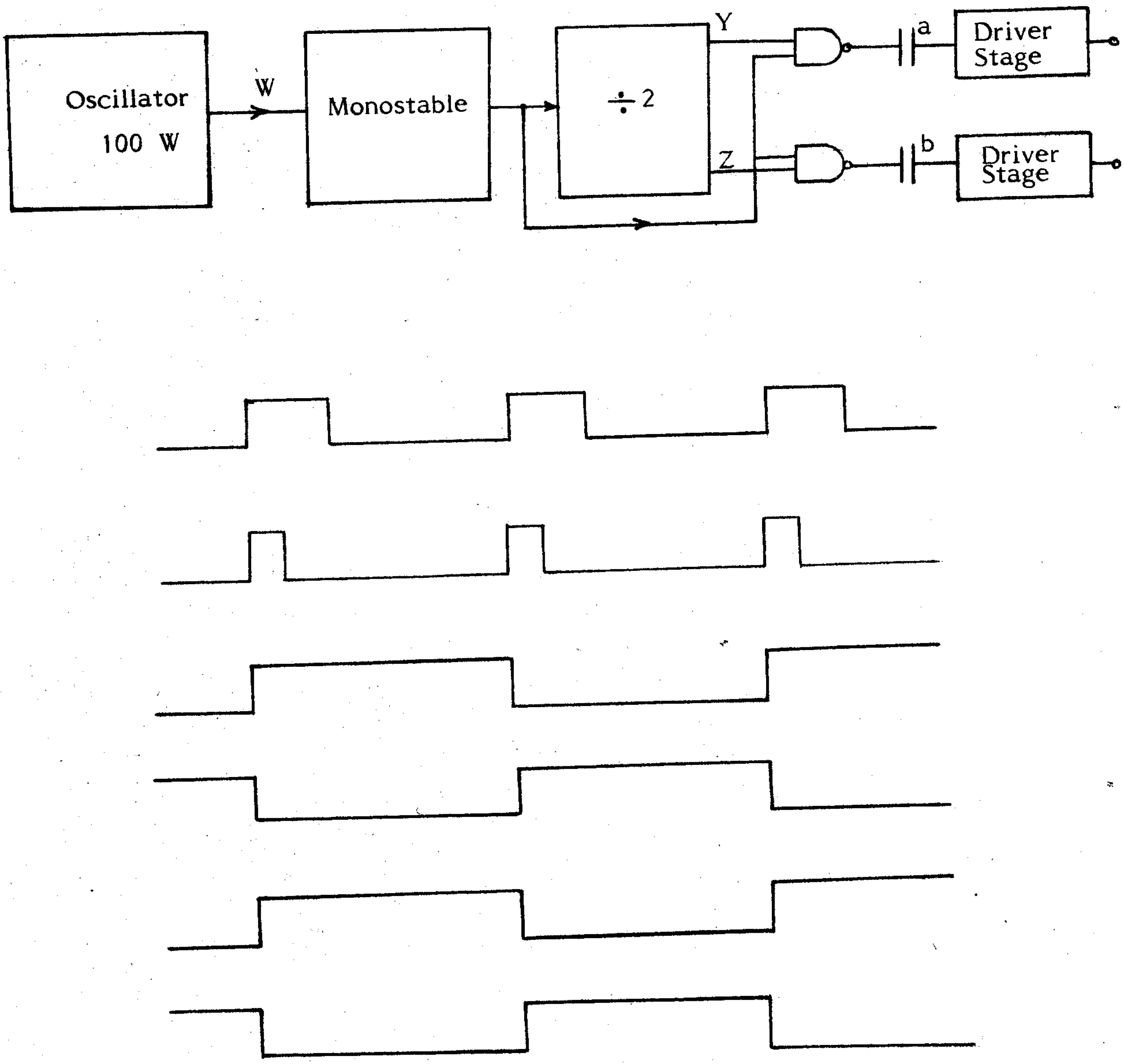



**FIG 6.4 MODIFIED DRIVER CIRCUIT B.D**

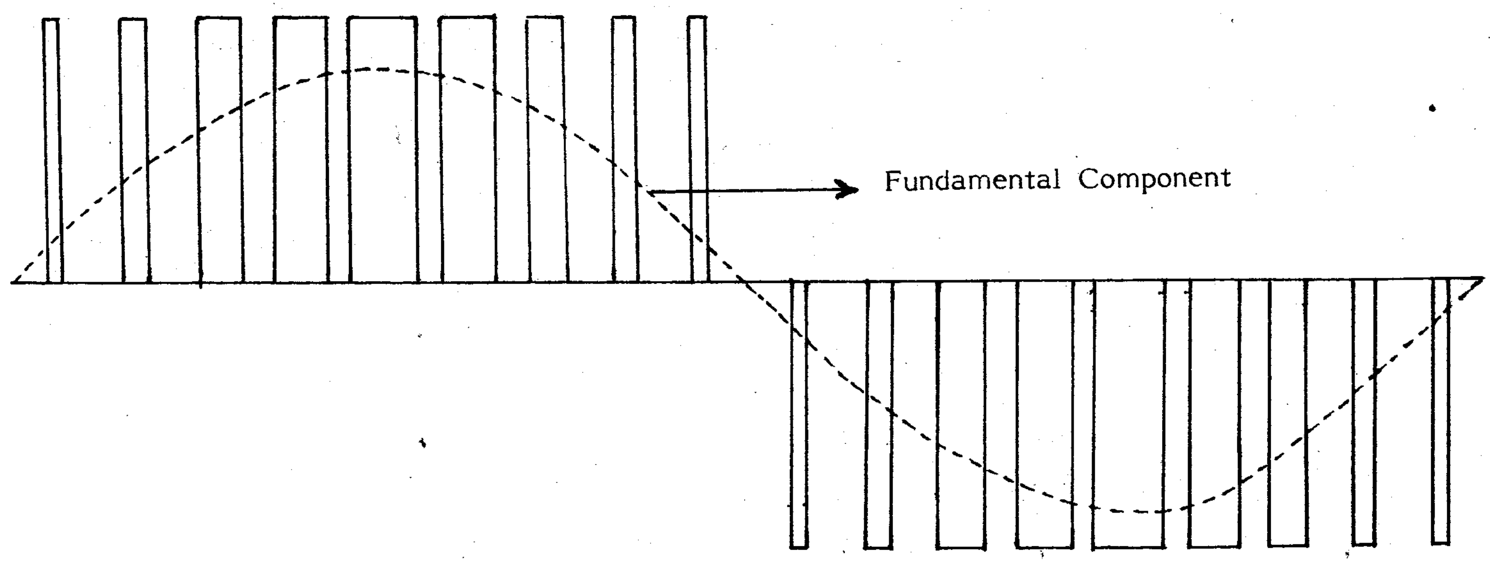
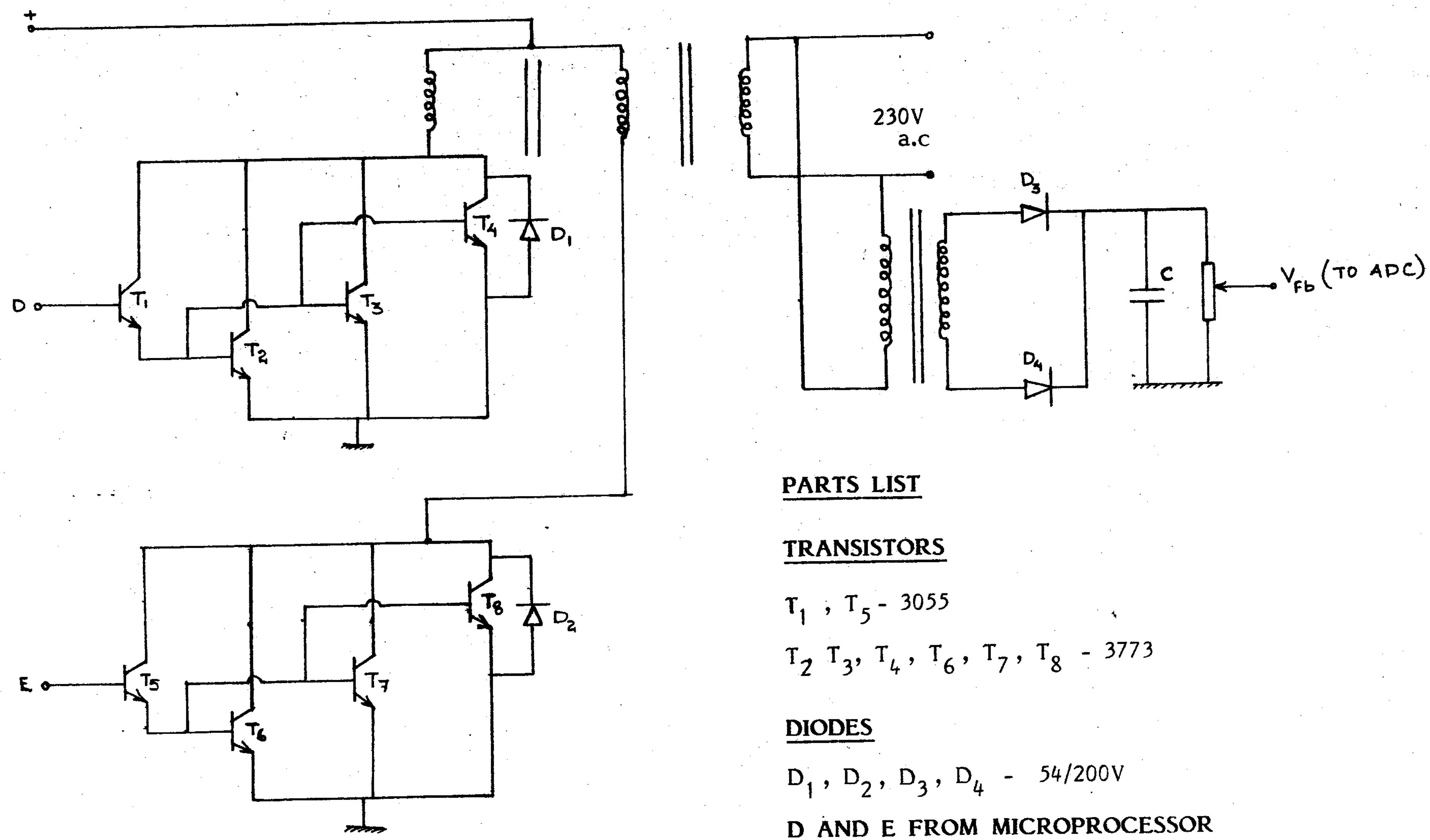



FIG 6.5 OUTPUT VOLTAGE OF INVERTER WITH SPWM




**PARTS LIST**

**TRANSISTORS**

$T_1$ , $T_5$ - 3055

$T_2$ $T_3$, $T_4$, $T_6$, $T_7$, $T_8$ - 3773

**DIODES**

$D_1$, $D_2$, $D_3$, $D_4$ - 54/200V

D AND E FROM MICROPROCESSOR

FIG. 6.6 INVERTER CIRCUIT

# DESIGN

## SMPS TRANSFORMER :

Design of the transformer is based on the equation

E = 4 * flux * frequency * turns

The turns / volt = 1 /( 4 * frequency * flux)

flux = B * A , where B = 0.1 Tesla.

Suitable wire was selected refering to the standard wire gauge cable.

Operating frequency - 20 KHz

Type of transformer - Ferrite core. Type U-60 was used.

## INVERTER TRANSFORMER :

Equation for the design of transformer,

E = 4 * frequency * flux * turns

turns / Volt = 1 / ( 4 * flux * frequency )

flux = B * A , where B = 1.0 Tesla

Suitable wire was selcted refering to the standard wire gauge cable

Operating frequency - 50 Hz

Type of transformer - Dyno grade Si-steel transformer core Type no. 6(GKW)

## SEMICONDUCTORS SELECTION

### SMPS SECTION :

Input Diodes - 12 A / 800 V MS BYW-88-1200, MELTRON

Output Diodes - 35 A / 200 V D4004 USHA Rectifier.

Transistors - 5 A / 1000 V- BU208D ECIL make.

### INVERTER SECTION :

Diodes - 5 A / 200 V

Transistors - 16 A / 60 V - 2N3773 GEC make

All the above semiconductors have been selected refering to the manufacturers data sheets.

# A N A L O G   T O   D I G I T A L   C O N V E R T E R

Analog to digital conversion forms an important aspect of digital data processing.The analog to digital converter is used to change the analog output signals produced by various types of sensors and transducers into equivalent digital signals.These signals would then be in a form suitable for entry into a digital system.ADC is often refered to as an" encoding device" since it encodes signals for entry into a digital system .In many process applications the microprocessors are used to read analog voltages that represent process variables. As the microprocessor can handle only digital signals,the analog variables have to be converted to equivalant digital values which is achieved by the ADC.

This project uses 8-bit ,8 channel ADC which is buit around National Semiconductor's ADC 0809 signal chip ADC.Its maximum speed of conversion is 10 KHz(period is 100 micro seconds).The exteranal requirement for this chip is an external clock of 640 KHz and 5.12 V external reference.The external clock is generated by CD4046 VCO .The external reference is generated using LM 317T voltage regulator.The full scale adjustment can be done using the 10 turn potentiometer P1.The output of ADC has a tristate buffer, thus it can be directly interfaced to the data bus.The CS line from the processor enables the board.The address lines A0,A1 and control lines RD and WR are decoded using decoder 74LS156.We get four select lines for READ of which one is connected to the ADC chip select.There are four select lines for WRITEs of which one line is used for start conversion,and one for Address Latch Enable.

The ADC chip has 8 multiplexed inputs,thus eight variables can be monitered.Any one of the eight channels can be selected by just outputting the channel number to the ADC. The design has been optimized in such a way that it offers high speed,high accuracy,minimal temperature dependence, excellent long time accuracy and repeatability and consumes minimum power.

## SUCCESSIVE APPROXIMATION A/D CONVERTER

The successive approximation A/D converter is one of the most commonly used A/D convertion device which consists of starting with the MSB and succesively trying a ` 1 ' in each bit of D/A decoder.As each bit is tried the output of the D/A decoder is compared against the input analog signal.The D/A output if is large the ` 1 ' is removed from the bit as the process continues and a ` 1 ' is tried in the next MSB.If the analog input signal is larger,the ` 1 ' remains in that bit.At the end of the process the digital word in the D/A decoder is the digital equivalent of the analog voltage.The conversion word rate is limited by the fact that each bit must be successfully tried before the conversion is complete.Thus A/D circuits must respond completely with some time left over before the next step begins.

Its accuracy is a function of the quantisizing error and the errors in the electronic circuitry that is the D/A decoder analog comparator and reference voltage source.Accuracies of better than 0.005 % are possible with this conversion process.Though, it utilizes more electronic parts than some of the other conversion processes,it is often not a serious drawback in view of the availability of present day microcircuits and microcircuit arrays for implementing these functions.

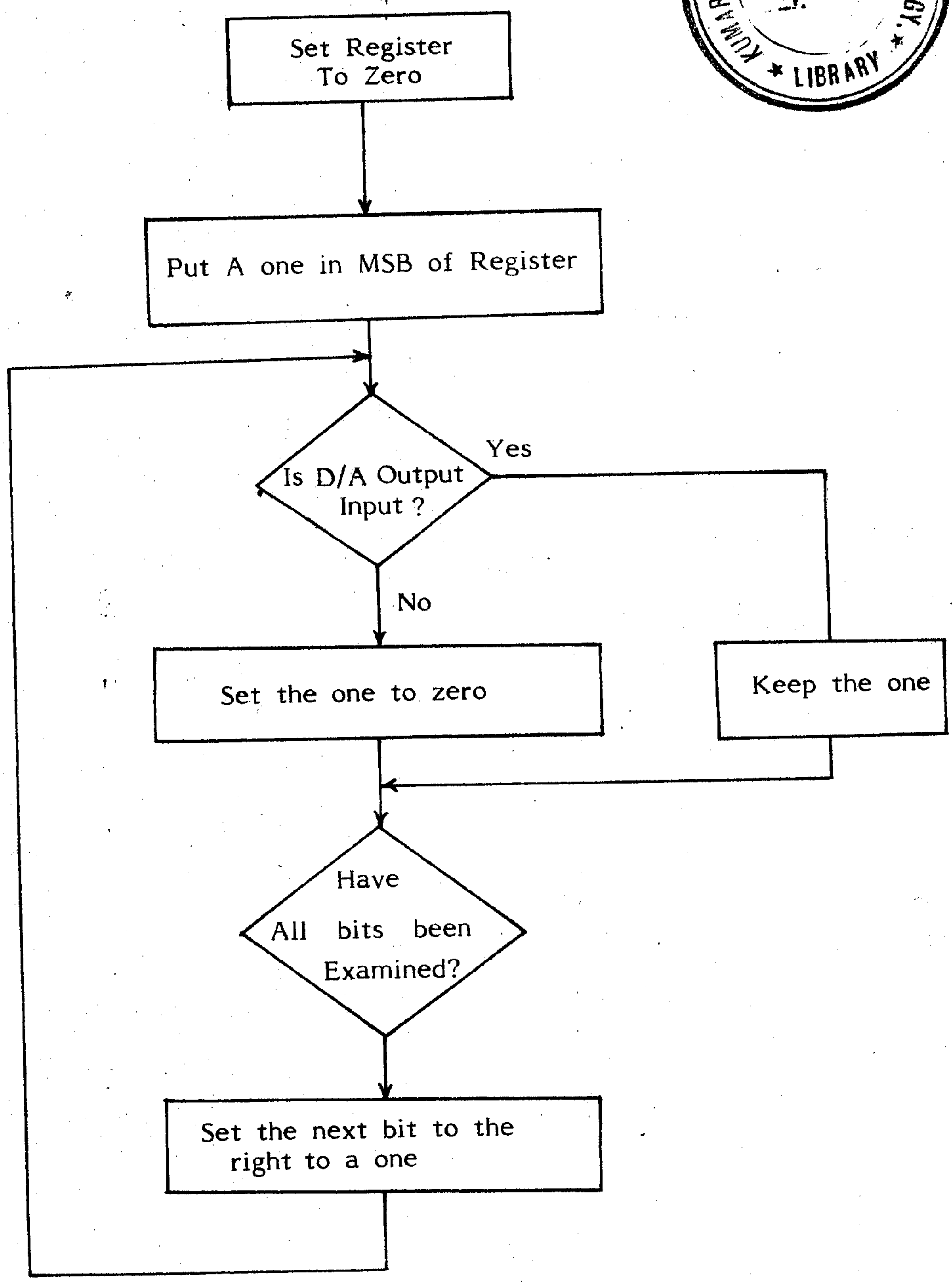



**FIG. 8.1 FLOW DIAGRAM FOR SUCESSIVE APPROXIMATION**

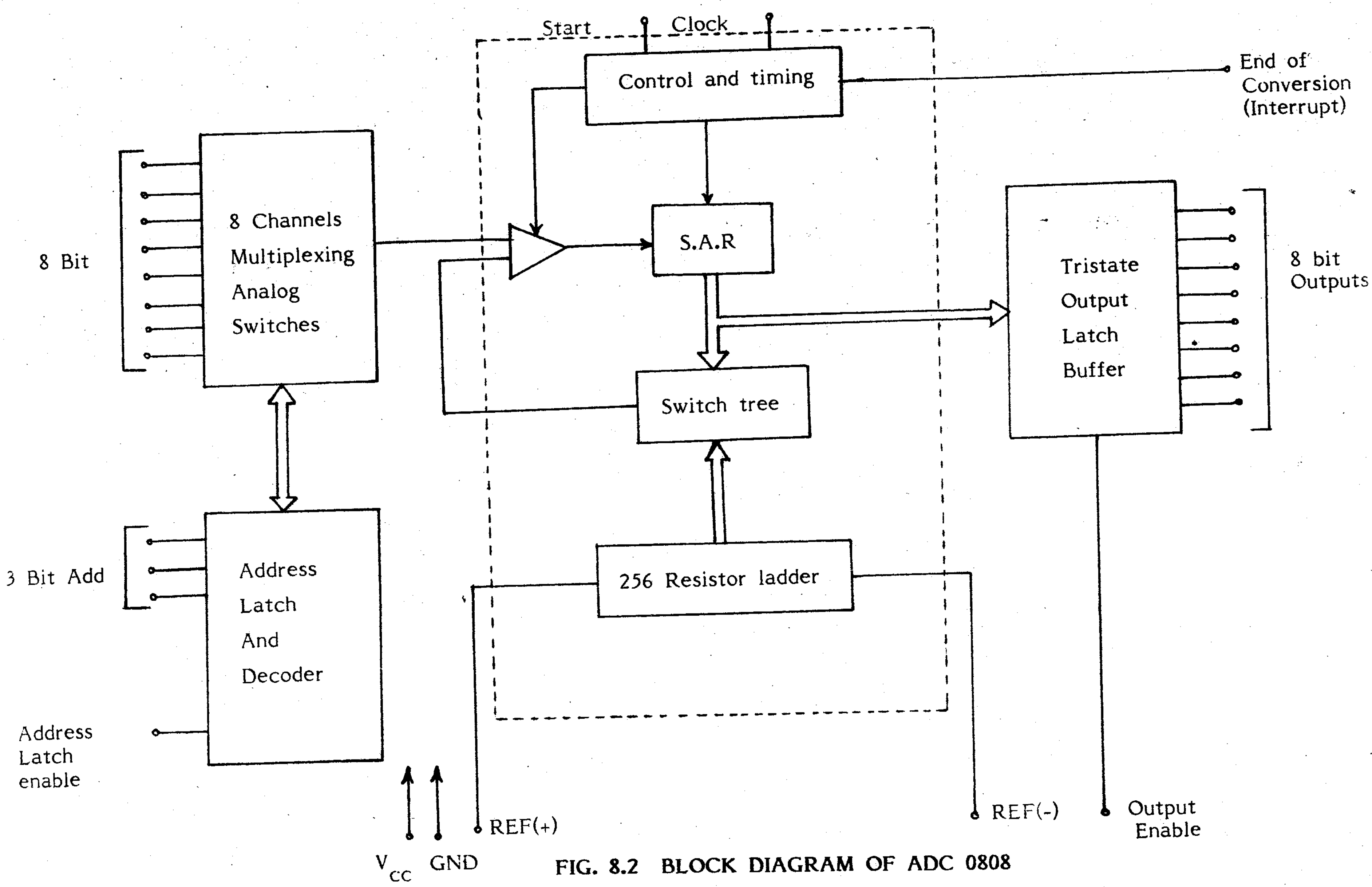



**FIG. 8.2 BLOCK DIAGRAM OF ADC 0808**

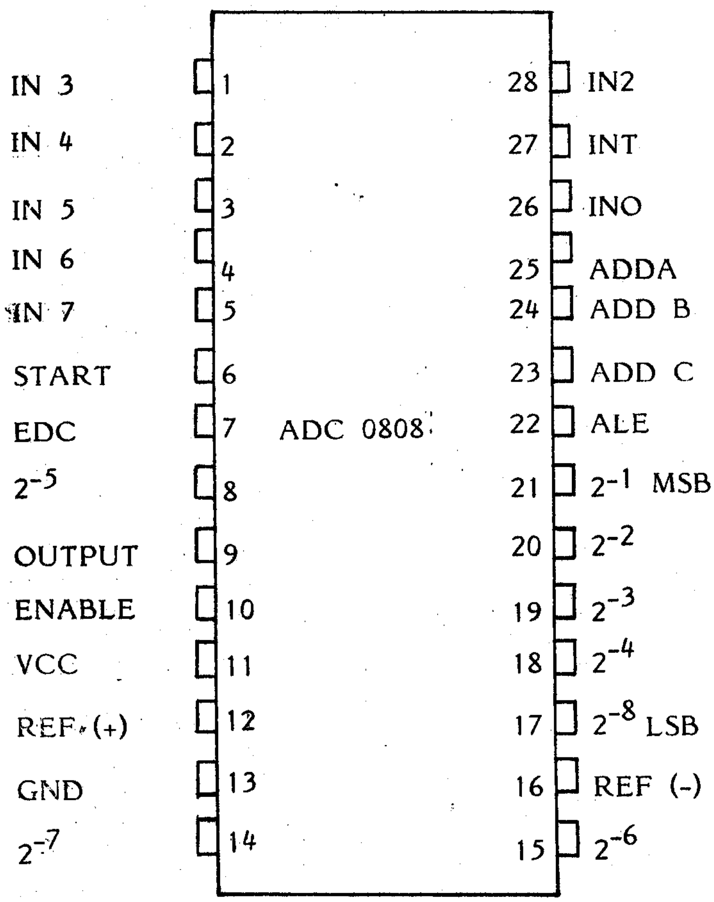



**FIG : 8.3 DUAL - IN - LINE PACKAGE (TOP VIEW)**

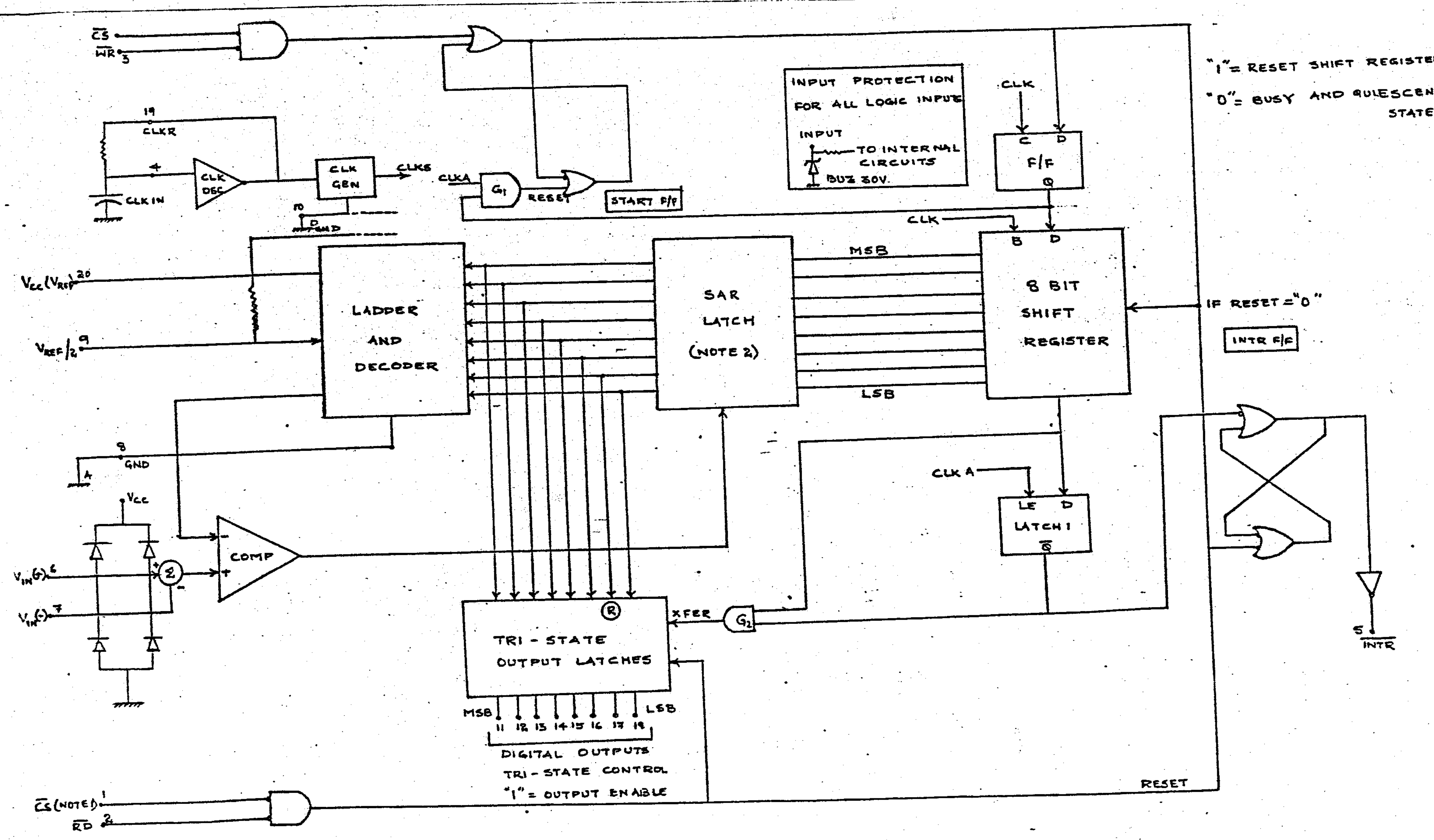



FIG.8.4: ADC 0801

# FEATURES OF PROGRAMMABLE PERIPHERAL INTERFACE(8255)

The 8255 is a general purpose programmable I/O device which interfaces with the microprocessor on one side and with the peripheral devices on the other side.It has 24 I/O pins which may be individually programmed in two groups of 12 and used in three major modes of operation.

For peripheral data transfer,three 8 bit ports are provided.These are termed as A,B and C. For the purpose of programming the 8255,these ports are grouped as

Group A - port A and most significant 4.bits of port C($PC_4$ - $PC_7$)

Group B -port B and least significant 4 bits of port C ($PC_0$ - $PC_3$)

## OPERATING MODES :

The three ports can be programmed to operate in any one of the major three modes viz. MODE 0 ,MODE 1 and MODE 2.

**MODE-0:( BASIC INPUT/OUTPUT):**

The features of this mode includes,

- Outputs are latched
- Inputs are not latched
- Ports do not have handshake or interrupt capability.

**MODE-1: (STROBED INPUT/OUTPUT):**

The features of this mode includes,

-Two ports(A and B) function as 8 bit I/O ports. They can be configured either as input or output ports .

-Each port uses three lines from port C as handshake signals.The remainning two lines of port C can be used for simple I/O functions.

-Input and output data are lactched.

-Interrupt logic is supported.

**MODE-2: (BIDIRECTIONAL DATA BUS):**

The features of this mode includes,

-Port A can be configured as the bidirectional port.

-Port B can be configured either in MODE 0 or MODE 1.

-Port A uses five signals from port C ,as control signals for data transfer.

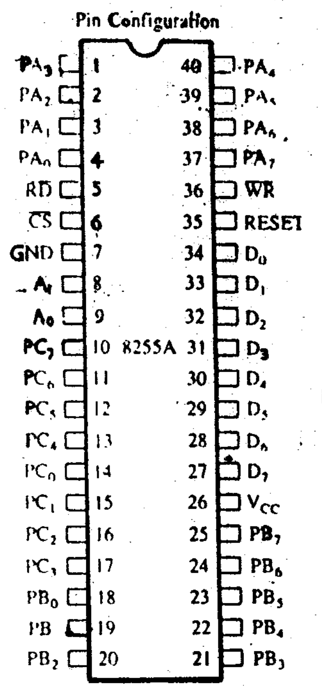
-The three remaining signals from port C can be used either as simple I/O or as handshake for port B.

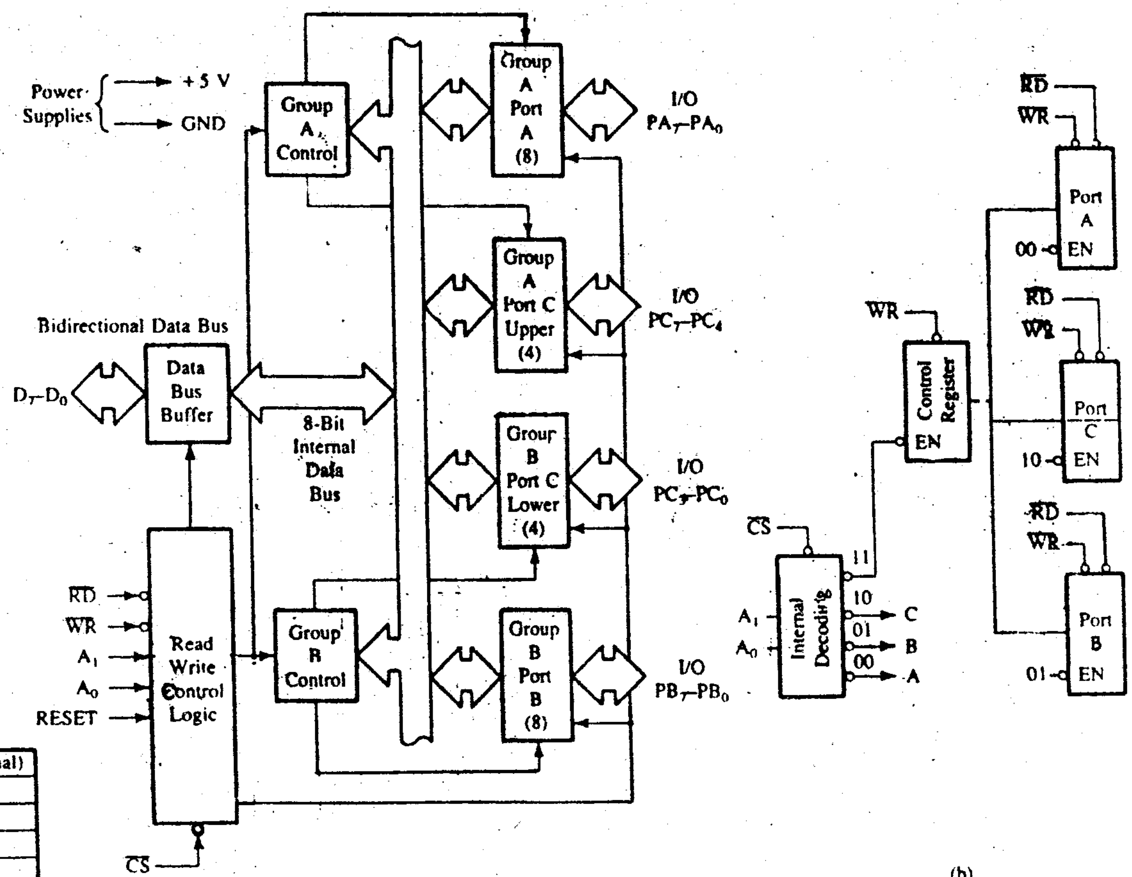
CONTROL WORD :

The Programmable Peripheral Interface 8255 operates in various modes by having a suitable control word. The control word format is as shown in FIG 9.1. Specifying an I/O function for each port.The control register can be accessed to write a control word when $A_o$ and $A_1$ are at logic 1

The register is not accessible for a READ operation.Port A and port C(lower) of 8255 are selected as input ports. Port B is selected as the output port.The device is used in simple input and output mode .

Control word for the selected mode O is 80H.




Pin Names

| | |
|---|---|
| D7–D0 | Data Bus (Bidirectional) |
| RESET | Reset Input |
| $\overline{CS}$ | Chip Select |
| $\overline{RD}$ | Read Input |
| $\overline{WR}$ | Write Input |
| $A_0$, $A_1$ | Port Address |
| $PA_7$–$PA_0$ | Port A (Bit) |
| $PB_7$–$PB_0$ | Port B (Bit) |
| $PC_7$–$PC_0$ | Port C (Bit) |
| $V_{CC}$ | +5 Volts |
| GND | 0 Volts |

(a)

(b)

Fig. 9.1 8255-A B.D (a) and an Expanded Version of the control logic I/O Ports(b)

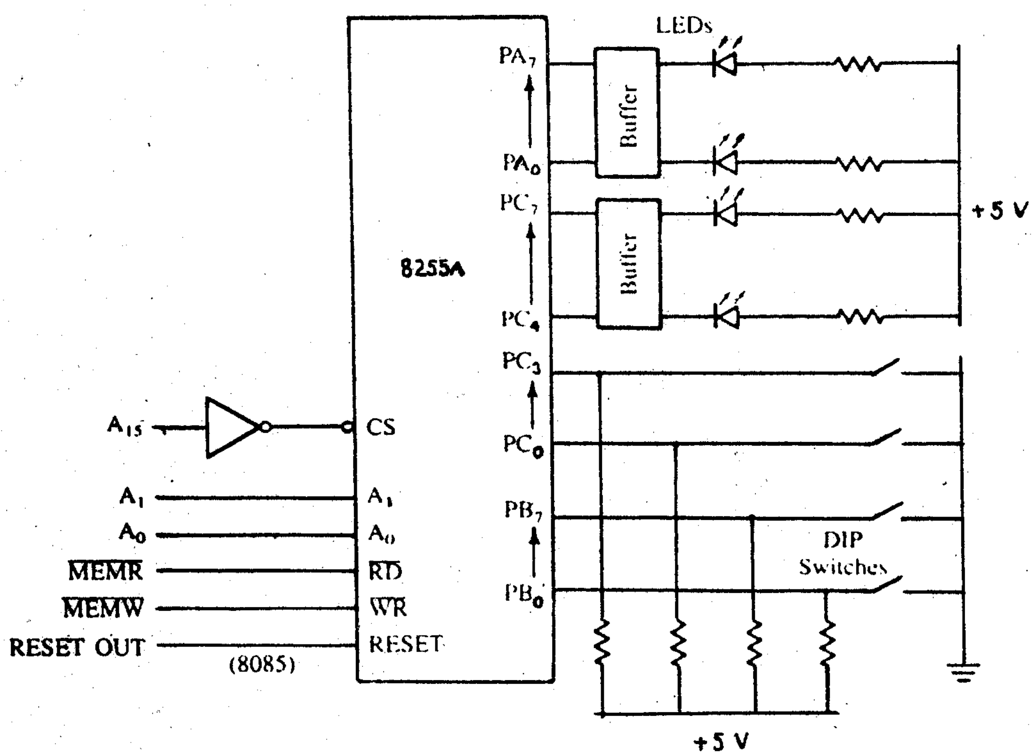



Fig. 9.2 Interfacing 8255-A I/O Ports in Mode 0

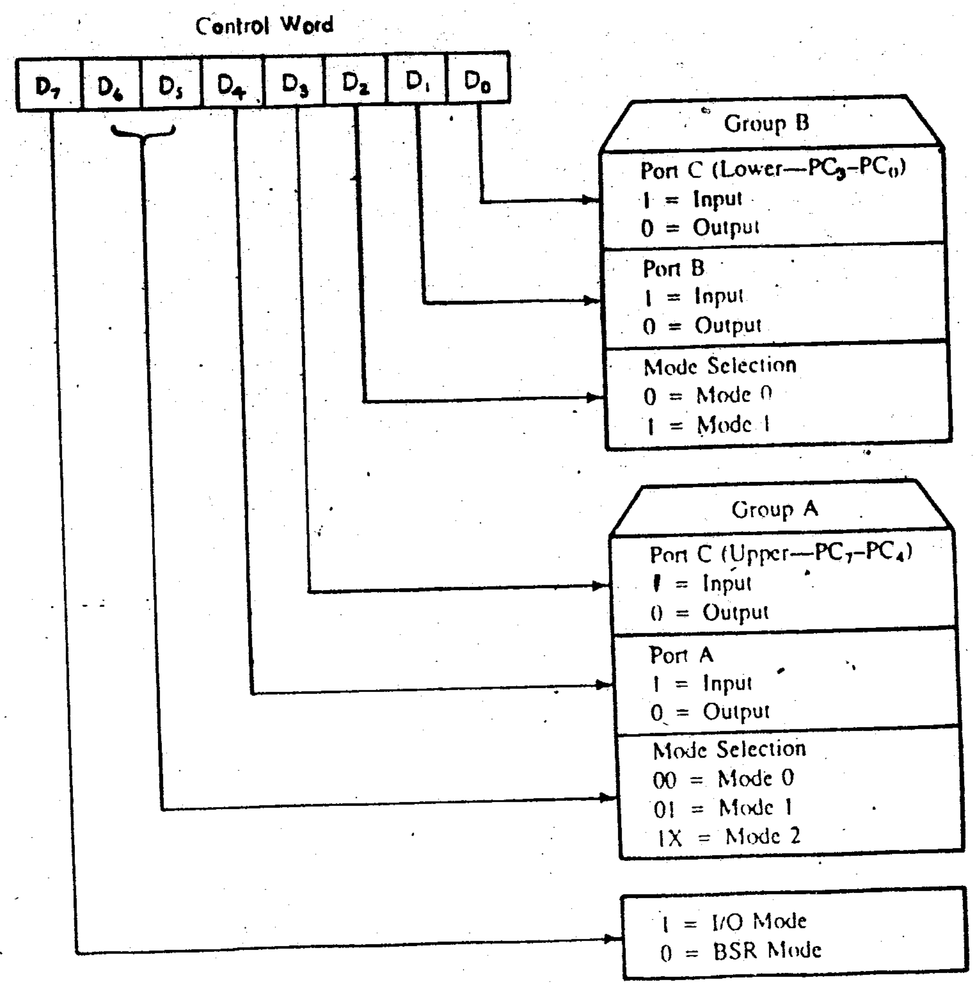



Fig. 9.3 8255-A Control Word Format for I/O Mode.

## FEATURES OF PROGRAMMABLE TIMER (8253)

The 8253 is a programmble intervel timer/counter which can be used with the 8085 microprocessor.It generates accurate time delays and can be used for applications such as a real-time clock,an event counter,a digital one-shot,a square wave generator,and a complex waveform generator.

The 8253 includes three identical 16 bit counters that can operate independently in any one of six modes.The counter can count either in binary or BCD.In addition, a count can be read by the microprocessor while the counter is decrementing.

### OPERATING MODES :

The 8253 can operate in six differnt modes.The gate of a counter is used either to disable or enable counting.

### MODE 0:(INTERRUPT ON TERMINAL COUNT)

The output will be initially low after the mode set operations. The output will remain low after the count is loaded into the selected count register and the counter will count.On reaching the terminal count,the output will go high and remain high until the counter is reloaded.

## MODE 1 (PROGRAMMABLE ONE-SHOT) :

The output will go low on the count following the rising edge of the gate input.The output will go high on the terminal count.



## MODE 2( RATE GENERATOR ; DIVIDE BY N COUNTER) :

The output will be low for one period of the input clock.The period from one output pulse to the next equals the number of input counts in the count register.

## MODE 3 (SQUARE WAVE RATE GENERATOR) :

Similar to mode 2,except that the output will remain high until one half the count has been completed(for even numbers) and go low for the other half of the count.If the count is odd,the output will be high for(N+1)/2 counts and low for(N-1)/2 counts.

## MODE 4 (SOFTWARE TRIGGERED STROBE ):

The output will be high after the strobe is set.When the count is loaded,the counter will begin counting.On terminal count ,the output will go low for one period of input clock,then will go high again.

**MODE 5 ( HARDWARE TRIGGERED STROBE ):**

The counter will start counting after the rising edge of the trigger input and will go low one clock priod when the terminal count is reached.

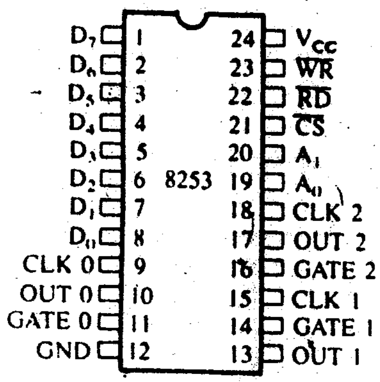
Our system uses MODE 0 of 8253.

**CONTROL WORD:**

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the control word register.

Pin Configuration




Pin Names

| | |
|---|---|
| $D_7$–$D_0$ | Data Bus (8 Bit) |
| CLK N | Counter Clock Inputs |
| GATE N | Counter Gate Inputs |
| OUT N | Counter Outputs |
| $\overline{RD}$ | Read Counter |
| $\overline{WR}$ | Write Command or Data |
| $\overline{CS}$ | Chip Select |
| $A_0$–$A_1$ | Counter Select |
| $V_{CC}$ | +5 Volts |
| GND | Ground |

Block Diagram

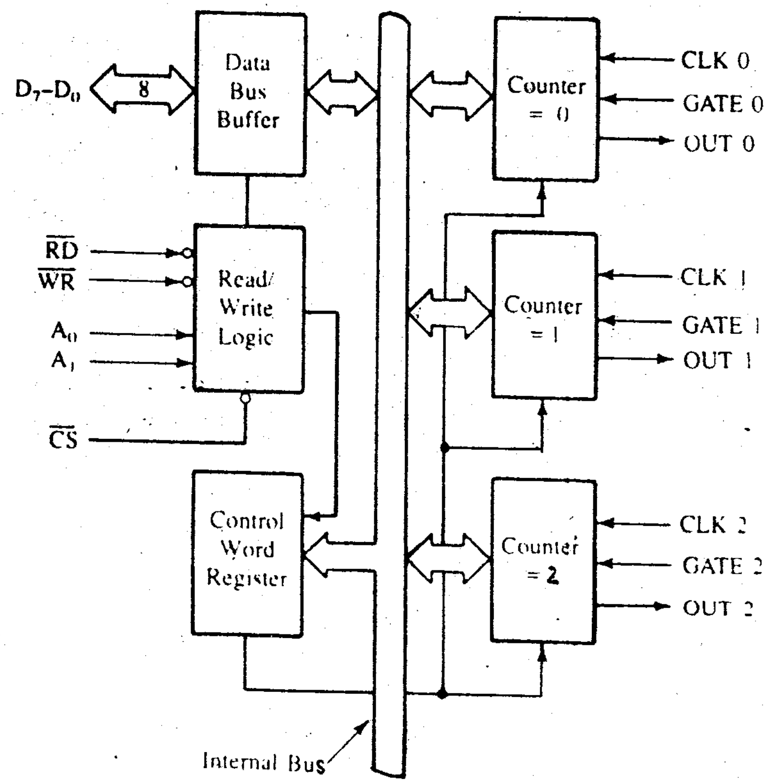


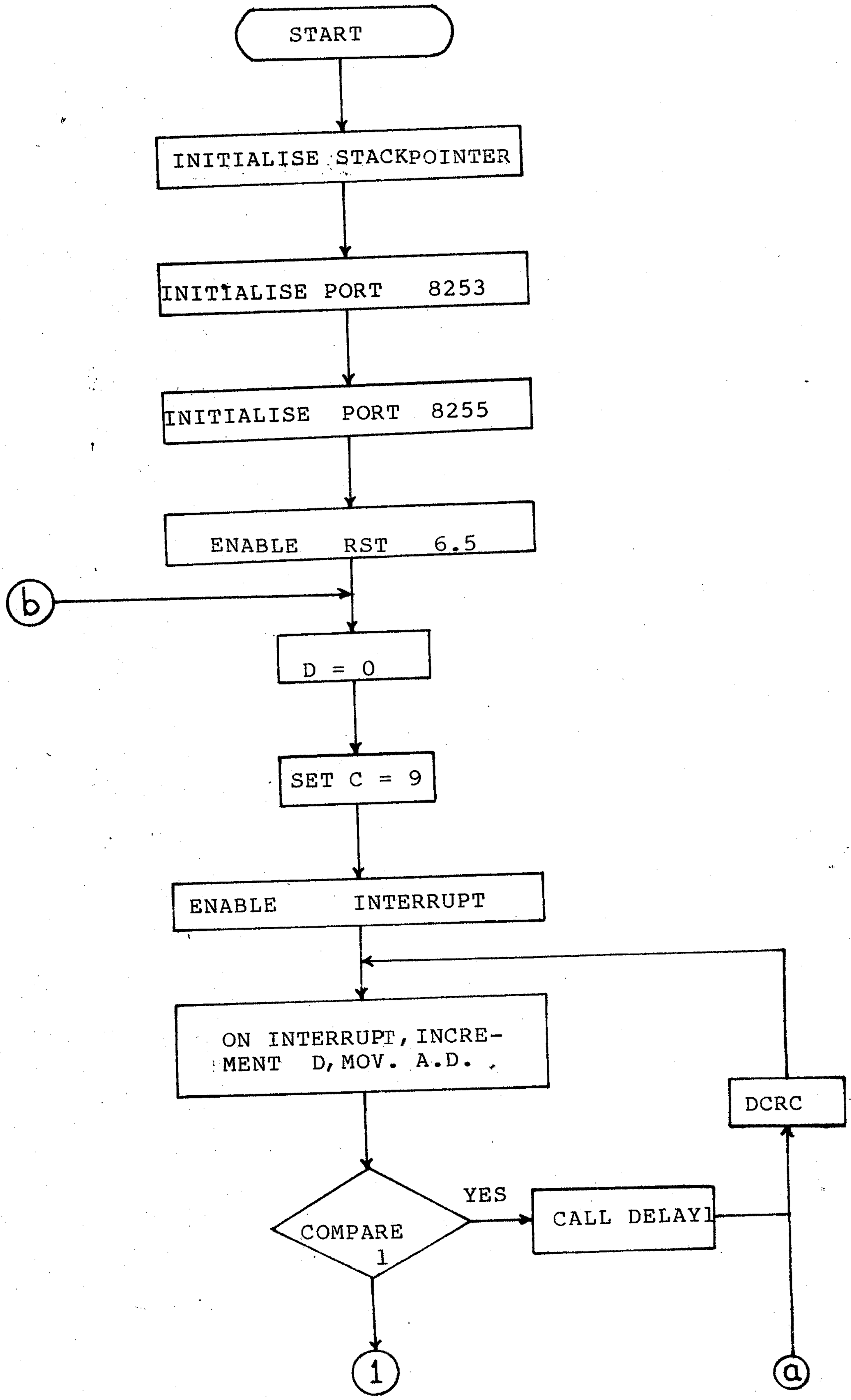

Fig. 10.1 - 8253 Block Diagram

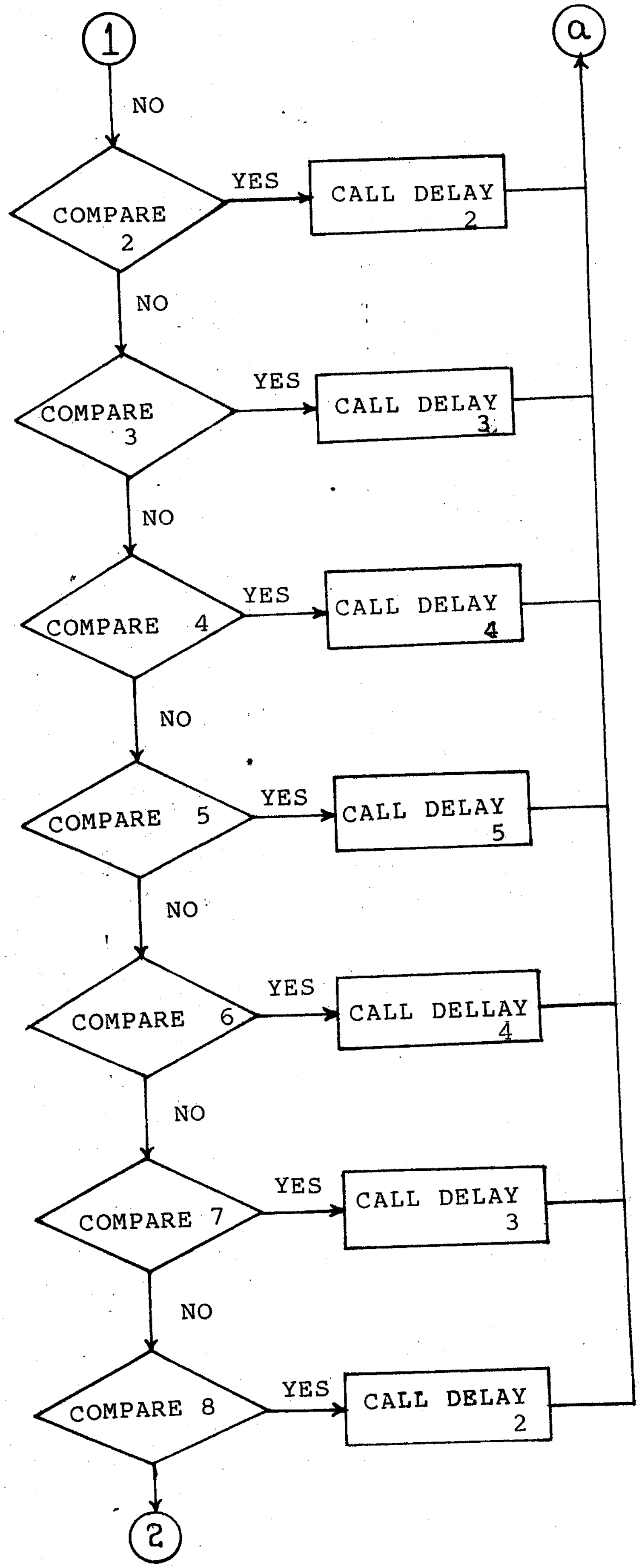
# CONCLUSION

While all the static devices are quite expensive,they are today the only complete solution .In fact if the power supply situation being what it is today in the country its almost mandatory for a computer installation to be equipped with a full fledged UPS.The alternative is to lose several hours of computer time each day while subjecting the hardware to severe abuse which results in component failures .

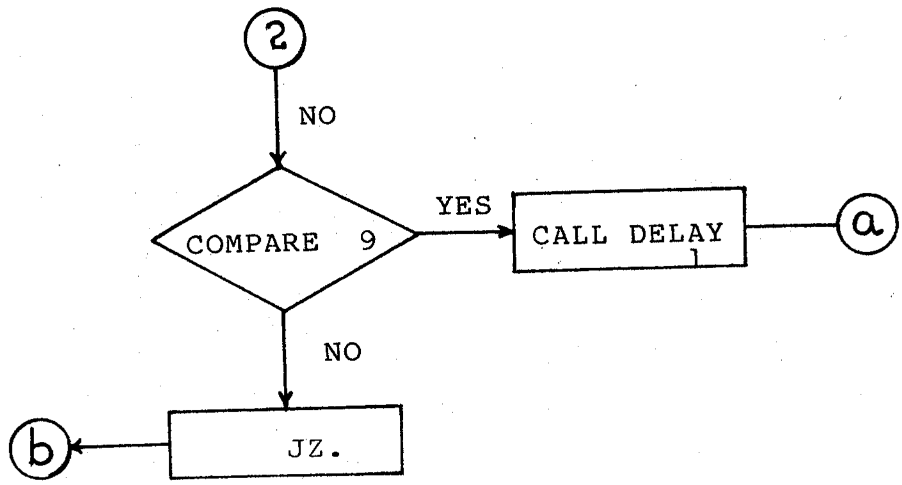
Microprocessor , used to implement the control function in UPS , is most efficient as it allows the change in modulation index, control by time multiplexing and realising the sine weighted pulse width modulation.Additional improvement can be achieved by having an alarm signal just before the shut down of power when there are networks of computers. To achieve increased rating,instead of transistor , Gate Turn Off thyristors (GTO) can be used.

# A P P E N D I C E S


START
INITIALISE STACKPOINTER
INITIALISE PORT 8253
INITIALISE PORT 8255
ENABLE RST 6.5
b
D = 0
SET C = 9
ENABLE INTERRUPT
ON INTERRUPT, INCRE-MENT D, MOV. A.D.
COMPARE 1
YES
CALL DELAY1
DCRC
1
a



1
a
NO
COMPARE 2
YES
CALL DELAY 2
NO
COMPARE 3
YES
CALL DELAY 3
NO
COMPARE 4
YES
CALL DELAY 4
NO
COMPARE 5
YES
CALL DELAY 5
NO
COMPARE 6
YES
CALL DELLAY 4
NO
COMPARE 7
YES
CALL DELAY 3
NO
COMPARE 8
YES
CALL DELAY 2
2




FLOWCHART FOR SINE WEIGHTED PULSE WIDTH MODULATION

SOFTWARE LISTING :

| ADDRESS | LABEL | MNEMONIC | OP-CODE |
|---|---|---|---|
| 1C 00 | | MVI A, 75 | 3E 75 |
| 1C 02 | | OUT 2B | D3 2B |
| 1C 04 | | MVI A, 80 | 3E 80 |
| 1C 06 | | OUT 29 | D3 29 |
| 1C 08 | | MVI A, 07 | 3E 07 |
| 1C 0A | | OUT 29 | D3 29 |
| 1C 0C | | MVI A, 80 | 3E 80 |
| 1C 0E | | OUT 33 | D3 33 |
| 1C 10 | | MVI A, 00 | 3E 00 |
| 1C 12 | | OUT 30 | D3 30 |
| 1C 14 | | MVI A, 1D | 3E 1D |
| 1C 16 | | SIM | 30 |
| 1C 17 | A1 | MVI C, 09 | 0E 09 |
| 1C 19 | | MVI D, 00 | 16 00 |
| 1C 1B | A2 | E1 | FB |
| 1C 1C | BACK | NOP | 00 |
| 1C 1D | | NOP | 00 |
| 1C 1E | | NOP | 00 |
| 1C 1F | | NOP | 00 |
| 1C 20 | | NOP | 00 |

| ADDRESS | LABEL | MNEMONIC | OP-CODE |
|---|---|---|---|
| 1C 21 | | JMP BACK | C3 1C 1C |
| 1F AB | | | C3 30 1C |
| 1C 30 | | LXI SP 1EFFH | 31 FF 1E |
| 1C 33 | | INR D | 14 |
| 1C 34 | | MOV A,D | 7A |
| 1C 35 | | CPI 01 | FE 01 |
| 1C 37 | | JZ DELAY1 | CA BO 1C |
| 1C 3A | | CPI 02 | FE 02 |
| 1C 3C | | JZ DELAY2 | CA DO 1C |
| 1C 3F | | CPI 03 | FE 03 |
| 1C 41 | | JZ DELAY3 | CA FO 1C |
| 1C 44 | | CPI 04 | FE 04 |
| 1C 46 | | JZ DELAY4 | CA 10 1D |
| 1C 49 | | CPI 05 | FE 05 |
| 1C 4B | | JZ DELAY5 | CA 30 1D |
| 1C 4E | | CPI 06 | FE 06 |
| 1C 50 | | JZ DELAY4 | CA 10 1D |
| 1C 53 | | CPI 07 | FE 07 |
| 1C 55 | | JZ DELAY3 | CA FO 1C |
| 1C 58 | | CPI 08 | FE 08 |
| 1C 5A | | JZ DELAY2 | CA DO 1C |
| 1C 5D | | CPI 09 | FE 09 |
| 1C 5F | | JZ DELAY1 | CA BO 1C |
| 1C 62 | | JMP A1 | C3 17 1C |

DELAY 1

| ADDRESS | LABEL | MNEMONICS | GOP CODE |
|---|---|---|---|
| 1C B0 | | LX1 H | 21 E0 1D |
| 1C B3 | | MVI A, 01 | 3E 01 |
| 1C B5 | | OUT 30 | D3 30 |
| 1C B7 | | CALL DELAY | CD A0 1D |
| 1C BA | | MVI A, 02 | 3E 02 |
| 1C BC | | OUT 30 | D3 30 |
| 1C BE | | JMP A3 | C3 C0 1D |

DELAY 2

| | | | |
|---|---|---|---|
| 1C D0 | | LX1 H | 21 E1 1D |
| 1C D3 | | MVI A, 01 | 3E 01 |
| 1C D5 | | OUT 30 | D3 30 |
| 1C D7 | | CALL DELAY | CD A0 1D |
| 1C DA | | MV1 A, 02 | 3E 02 |
| 1C DC | | OUT 30 | D3 30 |
| 1C DE | | JMP A3 | C3 C0 1D |

DELAY 3

| ADDRESS | LABEL | MNEMONIC | OP CODE |
|---|---|---|---|
| 1C F0 | | LX1 H | 21 E2 1D |
| 1C F3 | | MV1 A, 01 | 3E 01 |
| 1C F5 | | OUT 30 | D3 30 |
| 1C F7 | | CALL DELAY | CD A0 1D |
| 1C FA | | MV1 A, 02 | 3E 02 |
| 1C FC | | OUT 30 | D3 30 |
| 1C FE | | JMP A3 | C3 C0 1D |

DELAY 4

| | | | |
|---|---|---|---|
| 1D 10 | | LX1 H | 21 E3 1D |
| 1D 13 | | MV1 A, 01 | 3E 01 |
| 1D 15 | | OUT 30 | D3 30 |
| 1D 17 | | CALL DELAY | CD A0 1D |
| 1D 1A | | MV1 A, 02 | 3E 02 |
| 1D 1C | | OUT 30 | D3 30 |
| 1D 1E | | JMP A3 | C3 C0 1D |

DELAY 5

| ADDRESS | LABEL | MNEMONIC | OP CODE |
|---|---|---|---|
| 1D 30 | | LX1 H IDE4H | 21 E4 1D |
| 1D 33 | | MV1 A, 01 | 3E 01 |
| 1D 35 | | OUT 30 | D3 30 |
| 1D 37 | | CALL DELAY | CD A0 1D |
| 1D 3A | | MV1 A, 02 | 3E 02 |
| 1D 3C | | OUT 30 | D3 30 |
| 1D 3E | | JMP A3 | C3 CO 1D |
| 1D A0 | | PUSH H, L | E5 |
| 1D A1 | | PUSH D, E | D5 |
| 1D A2 | | PUSH B, C | C5 |
| 1D A3 | | PUSH PSW | F5 |
| 1D A4 | | MOV C, M | 4E |
| 1D A5 | LOOP 2 | MV1 B, 01 | 06 01 |
| 1D A7 | LOOP 1 | DCR B | 05 |
| 1D A8 | | JNZ LOOP 1 | C2 A7 1D |
| 1D AB | | DCR C | OD |
| 1D AC | | JNZ LOOP 2 | C2 A5 1D |
| 1D AF | | POP PSW | F1 |
| 1D BO | | POP B, C | C1 |
| 1D B1 | | POP D, E | D1 |

| ADDRESS | LABEL | MNEMONIC | OP CODE |
|---|---|---|---|
| 1D B2 | | POP H, L | E1 |
| 1D B3 | | RET | C9 |
| 1D C0 | | DI | F3 |
| 1D C1 | | DCR C | 0D |
| 1D C2 | | JNZ A2 | C2 1B 1C |
| 1D C5 | | JMP A1 | C3 17 1C |

**LOOK UP TABLE**

| ADDRESS | WIDTH |
|---|---|
| 1D E0 | 3C |
| 1D E1 | 77 |
| 1D E2 | A6 |
| 1D E3 | C4 |
| 1D E4 | CF |

# TECHNICAL SPECIFICATIONS

<u>UPS</u>

| | |
|---|---|
| Capacity | – 300 V A |
| Battery system | – 12 Volts |
| Back up time | – 1 Hour with 80 Ah Battery |

<u>SMPS</u>

| | |
|---|---|
| Input | – 230 V a.c |
| Operating frequency | – 20 KHz |
| Output | – 12 V d.c |
| Efficiency | – More than 70 % |

<u>INVERTERS</u>

| | |
|---|---|
| Input | – 12 V d.c , through battery |
| Operating frequency | – 50 Hz |
| Output | – 230 V a.c , 50 Hz |
| Efficiency | – 70% – 75% according to loading |
| Waveform | – Pure sine wave with 3% THD |

## R E F E R E N C E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Generalised techniques of Harmonic elimination and voltage control in thyristor Inverters : Part II - Voltage control techniques.

v. IEEE Transaction of Industry Applications , Vol 1A-9, No- 3, May / June - 71
Generalised techniques of harmonic elimination and voltage control in thyristor inverters : Part I - Harmonic Elimination

# B I B L I O G R A P H Y


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- Inverters

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