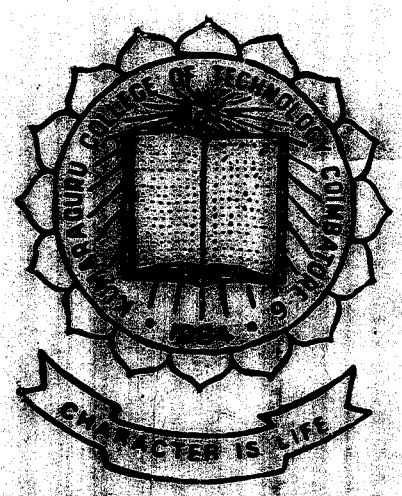
PC BASED DATA ACQUISITION AND ANALYSIS OF ECG

PROJECT WORK



SUBMITTED BY

R. RAVINDRARAJ
E. CHELLIAH SUNDAR
R. RAJARAM

UNDER THE GUIDANCE OF

Mr. S. Mahesh, B.E, M.S.

IN PARTIAL FULFILMENT OF THE REQUIREMENT FOR THE AWARD OF THE DEGREE OF BACHELOR OF ENGINEERING IN ELECTRICAL & ELECTRONICS ENGINEERING OF THE BHARATHIAR UNIVERSITY COIMBATORE

1994 - 1995

Department of Electrical & Electronics Engineering

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COIMBATORE - 641 006.

CERTIFICATE

This is to certify that the Project Report entitled

PC BASED DATA ACQUISITION AND ANALYSIS OF ECG

has been submitted by

Mr.....

in partial fulfilment for the award of the degree of

Bachelor of Engineering in Electrical and Electronics Engineering

Branch of the Bharathiar University, Coimbatore during the academic year 1994-95

Dr. K. A. PALANI

Department of Electrical and Electronics Engineering
Kumaraguru College of Technology
Coimbatore-641 006

.....
Guide

Head of the Department

Certified that the candidate with University Register No. .....

was examined in project work Viva-Voce by us on .....

ACKNOWLEDGEMENT

We are very much indebted to our guide **Mr. S. MAHESH**,B.E, M.S, Lecturer in EEE Department for his able guidance.

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SYNOPSIS

In this project the design and fabrication for the acquisition of ECG signals and software using the language "C++" for the analysis of the ECG signals has been carried out successfully.

The signals received from the ECG machine are analog in nature, it is converted into the Digital form using an A/D converter. This signal is sampled using a sample and hold circuit and amplified for +5V and is given through an interfacing card to a PC. The Analysis of the ECG signals obtained from a patient is done with the help of the software.

The normal linearized ECG waveform is stored in the PC. The signals received from the patient is compared with the normal ECG waveform . The comparison is done for the amplitude as well for the time duration. The diagnosis is made with the help of the software.

The analysis can be carried both for on-line analysis as well as recorded analysis. The main advantage of this type of analysis is that it is very accurate.

CONTENTS

CHAPTER 1

1 ELECTRO CARDIOGRAPHY

1.1 Introduction

The electro cardiogram(ecg) is a graphic recording of the electrical potentials produced in association wiht the heart beat. The heart is unique among the muscles of the body in that it possesses the property of automatic rhythmic contraction. The impulses that precede contracion arise in the conduction system of heart. The impulses result in excitation of the muscle fibres throughout the myocardium. Impulse formation and conduction porduce weak electrical currents that spread through the entire body. By applying electrodes to an electrocardiographic apparatus the ECG is recorded. The connections of the apparatus are such that an upright deflection indicates positive potential and a downward deflection indicates negative potential.

1.2 ELECTRO CARDIOGRAPHIC APPARATUS

In modern electro cardiography, two types of apparatus are used: the string galvanometer and the radio amplifier.

The former records its pattern on photographic paper which must then be developed. It requires more experience to operate, the caution must be taken to prevent damage to the valuable string. The radio amplifier has been combined with a direct writer. It is compact, light and moblie unit which is very simple to operate, and there is much less chance of damaging the machine by technical errors of operation. It has the additional advantage of producing an instantaneous recording, thus making the record immediately available for interpretation. Many modern machines record multiple leads simultaneously.

Oscilloscope viewing of the ECG is commonly used in clinical medicine. This produces a constant electro cardio-

graphic pattern on a fluorescent screen and permanent records can be obtained by connecting the machine to a direct-writing apparatus. Such pieces of equipment are now routine in coronary and intensive care units and in surgery.

Small electro cardiographic tape recorders can be attached to a patient and continous recordings are obtained while the patient is ambulatory (or at rest) for 24-hours periods. The tape is then reviewed by the physician. This is of special value in the study of patients with arrhythmias and myocardial ischemia.

ECG signals can be transmitted via telemetry or telephone lines, thus permitting constant or temporary monitoring and interpretation by a physician many miles from the patient. Memory loops are available to record events prior to the onset of an arrhythmia. Computer facilities are available not only for electrocardiographic interpretation but for the recognition and quantitation of arrhythmias.

1.3 ADVANTAGES OF ELECTRO CARDIOGRAM

1. Atrial and ventricular hpertrophy.

2. Myocardial ischemia and infraction.

Multiple leads, vector cardio grams and modern exercise testing have increased the accuracy of diagnosis and of estimates of extent of disease.

3. Arrhythmias. Not only more exact diagnosis can be made, but unipolar and intracardiac electrocardiography have also contributed substantially to our basic understanding of the origin and conduction of abonormal rhythms.

4. Pericarditis.

5. Systemic diseases that affect the heart.

6. Effect of cardiac (and non cardiac) drugs, especially quinidine.

7. Disturbances in electrolyte metabolism, especially potassium abnormalities.

8. Evaluation of electronic pacemaker function.

1.4 STANDARD LEADS

1.4.1 Bipolar Standard leads:

The bipolar standard lead (I,II, and III) are the original leads selected by einthoven to record the electrical potentials in the frontal plane. Electrodes are applied to the left arm, right arm and left leg. Proper skin contact must be made by rubbing electrode paste on the skin. The LA(left arm), RA(right arm) and LL(left leg) leads are then attached to their respective electrodes. By turning the selector dial to 1,2 and 3 the three standard leads(I,II and III) are taken.

All electro cardiographic machines also have a right leg electrode and lead. This acts as a ground wire and plays no role in the production of the ecg. In areas where there is electrical interface, it may be necessary to run a ground wire from the bed or the machine to an apporpriate ground.

1.4.2 Electrical Potential:

The bipolar leads represent a difference of electrical potential between two selected sites.

Lead I = Difference of potential between the left arm and right arm (LA-RA).

Lead II = Difference of potential between left leg and right arm (LL-RA).

Lead III = Difference of potential between the left leg and left arm (LL-LA).

The relation between the three leads is expressed algebrically by Einthoven's equation.

Lead II = Lead I + Lead III. This is based on Kirchoff's law, which states that the algebric sum of all the potential differences in a closed circuit equals zero. However, since Einthoven did make this alteration in the polarity of the lead II axis, the equation becomes: I - II + III = 0. Hence II = I + III.

The electrical potential as recorded from any one extremity will be the same no matter where the electrode is placed on the extremity. The electrodes are usually applied just above the wrists and ankles. If an extremity has been amputated, the electrode can be applied to the slump. In a patient with an uncontrollable tremor, a more satisfactory record may be obtained by applying the electrodes to the upper portion of the limbs.

1.4.3. Bipolar Chest Leads:

Bipolar chest leads records difference of potential between any given position on the chest(C) and one extremity. Before unipolar electro cardiography was introduced, the left

leg(F) was used as the "indifferent" electrode and the leads were called LF leads. It was assumed that the left leg (or right or left arm) was so remote from the heart that it would act as an "indifferent electrode" and not interfere with the chest potential.

A special bipolar chest lead(lewis lead) is of value in amplifying the waves of artrial activity and thereby clarifying the mechanism of artrial arrhythmia. The right arm electrode is placed in the second intercoastal space to the right of the strenum. The left arm electrode is placed in the fourth intercoastal space right of the strenum. The above two electrodes may be interchanged (RA and LA). This will reverse the polarity of all complices, but it will not alter the interpretation since the basic purpose is to identify artrial activity.

1.4.4 Unipolar Leads (Extremity leads, Precordial leads, Esuphageal leads)

Unipolar leads(VR,VL,VF,multiple chest leads "V" and esuphageal leads "E") were introduced by wilson in 1932. The frontal plane unipolaar lead(VR,VL,VF) bear a definite mathematical relationship to the standard (I,II,III) bipolar leads. The precordial (V) leads record potentials in the horizontal plane wihtout being influenced by actual potentials from an "indifferent" electrode used in recording bipolar chest leads.

All modern electro cardiographic machines are constructed such that augmented extremity leads can be taken with the same lookup as used for standard leads by turning the selector dial to aVR, aVL, and aVF. Unipolar chest leads are taken by applying the chest lead and its electrode to any desired position on the chest and turning the selector dial to the V position. Multiple chest leads are taken by changing the position of the chest electrode. Unipolar esophageal

leads are taken by attaching the esophageal lead to the chest lead and turning the selector dial to the V position.

A universal lead selector is available for a 3-lead electro cardiographic apparatus. With this unit attached, the standard unipolar extremity, and chest leads can be taken by simply rotating the selector dial as is done with all modern electro cardiographic machines.

1.4.5 Unipolar Extremity Leads

Unipolar non augmented extremity leads VR, VL, VF. These have been replaced by the augmented extremity leads aVR, aVL and aVF and are not commonly taken.

Using the indifferent electrode (RA+LA+LL) as one terminal and placing another electrode on the right arm and the zero potential of the central termial (RA-0 = RA). Therefore the "actual" potential of the right arm is recorded. Although it is techincally a bipolar lead, it represents a unipolar lead.

Since one of the potentials is zero. This is designated as VR(vector of right arm). The left arm(VL) and left leg(VF) potentials are obtained in the same way. The selector dial is set on lead I.

1. To take Vr, the LA lead of the machine is attached to an electrode placed on the right arm at a different site from the RA electrode connected to the central terminal.

2. To take VL, the LA lead of the machine is attached to an electrode on the left arm.

3. To take VF, the LA lead of the machine is attached to an electrode on the left leg.

1.4.6 AUGMENTED EXTREMITY

By a slight change in technique from above(this is automatically accomplished by all electrocardiographic machines), the amplitude of the deflections of VR, VL and VF can be increased by about 50%. These leads are called augmented unipolar extremity leads and are designated as aVR,

aVL and aVF. It must be emphasized that the only difference between leads VR, VL and VF and leads aVR, aVL and aVF is this difference in amplitude.

As in the non augmented leads, the 3 wires of the indifferent electrode are connected to the 3 extremities(LA,RA and LL);the central terminal is connected to the RA lead of the machine; the LA leead of the machine becomes the exploring electrode; and the selector dial is set on the lead I.

1. To take aVR, the indifferent lead to the right arm is removed and left unattached and the LA lead of the machine is attached to the RA electrode.

2. To take aVL, the indifferent lead to the left arm is removed and left unattached and the LA lead if the machine is attached to the LA electrode.

3. To take a VF, the indifferent lead to the left leg is removed and left unattached and the LA lead of the machine is attached to the LL electrode.

1.4.7 UNIPOLAR PRECORDIAL(CHEST) LEADS

These are obtained by turning the selector to V on the dial or in the order machine by following directions:

The indifferent electrode leads remain connected to the 3 extremities. The central terminal is attached to the RA lead of the machine. The selector dial is set on lead I. The LA lead of the machine is attached to an electrode that can be applied to the desired chest positions producing multiple unipolar chest leads. This results in a v lead. The common precordial positions used are are as follows

V1: Fourth intercostal space at the right sternal border.

V2: Fourth intercostal space at the left sternal border.

V3: Equidistant between V2 and V4

V4: Fifth intercostal space in the left mid clavicular line. All subsequent leads (V5-V9) are taken in the same horizantal line as V4.

V5: Anterior axillary line

V6: Mid axillary line

V7: Posterior axillary line

V8: Posterior scapular line

V9: Left border of the spine.

V(3R-9R): Taken on the right side of the chest in the same location as the left sided leads V(3-9). V2R is therefor the the same as V1.

3V(1-9): Taken one interspace higher than V(1-9) these are the third interspace leads. The same terminology can be applied to the leads taken in other interspaces, eg:2V(1-9), 6V(1-9) etc.

3V(3R-9R): Right precordial leads taken one interspace higher than V(3R-9R)

VE: Taken over the ensiform cartilage the usual routine ECG consists of 12 leads:I, II, III, aVR, aVL and V(1-6)

The monitor leads, unipola Esophageal leads, Inter cardiac leads are also used.

1.5 TECHNICAL DIFFICULTIES AFFECTING THE ELECTRO CARDIGRAM

1. The examination should be conducted on a suitable bed or table large enough to support the patients entire body and the patient must be completely relaxed in order to ensure a satisfactory tracing. Any muscular motions or twitchings by the patient can alter the record. In new type of ECG machines a muscle filter is used in order to prevent the interuption or disturbance caused due to relaxation or contraction.

2. Be certain that there is a good contact between the skin and the electrode. A poor contact can result in poor record.

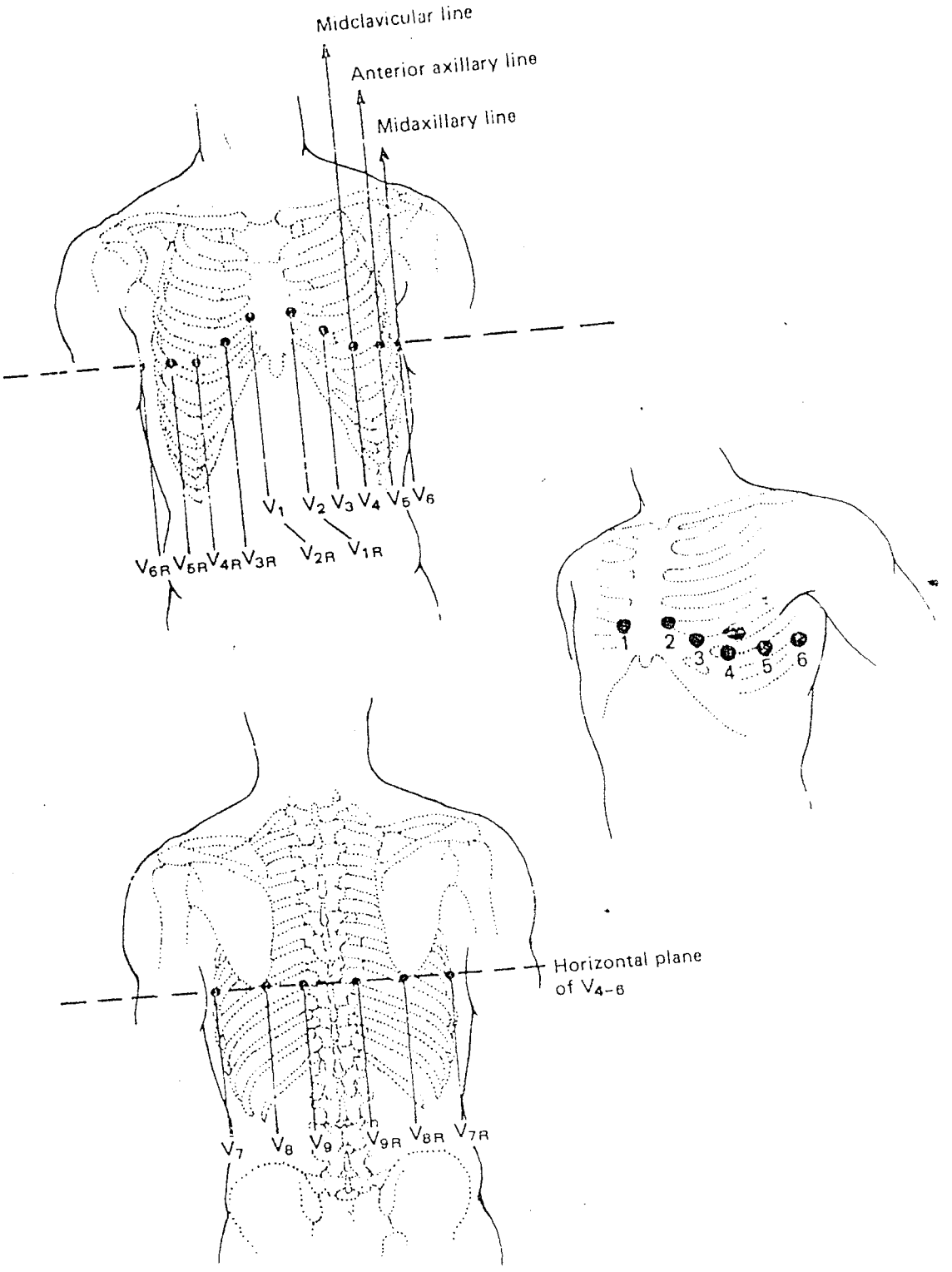
3. The machine must be properly standardized so that 1mV will produce a deflection of 1 cm.

4. The patient and the machine must be properly grounded to prevent alternating current interference.

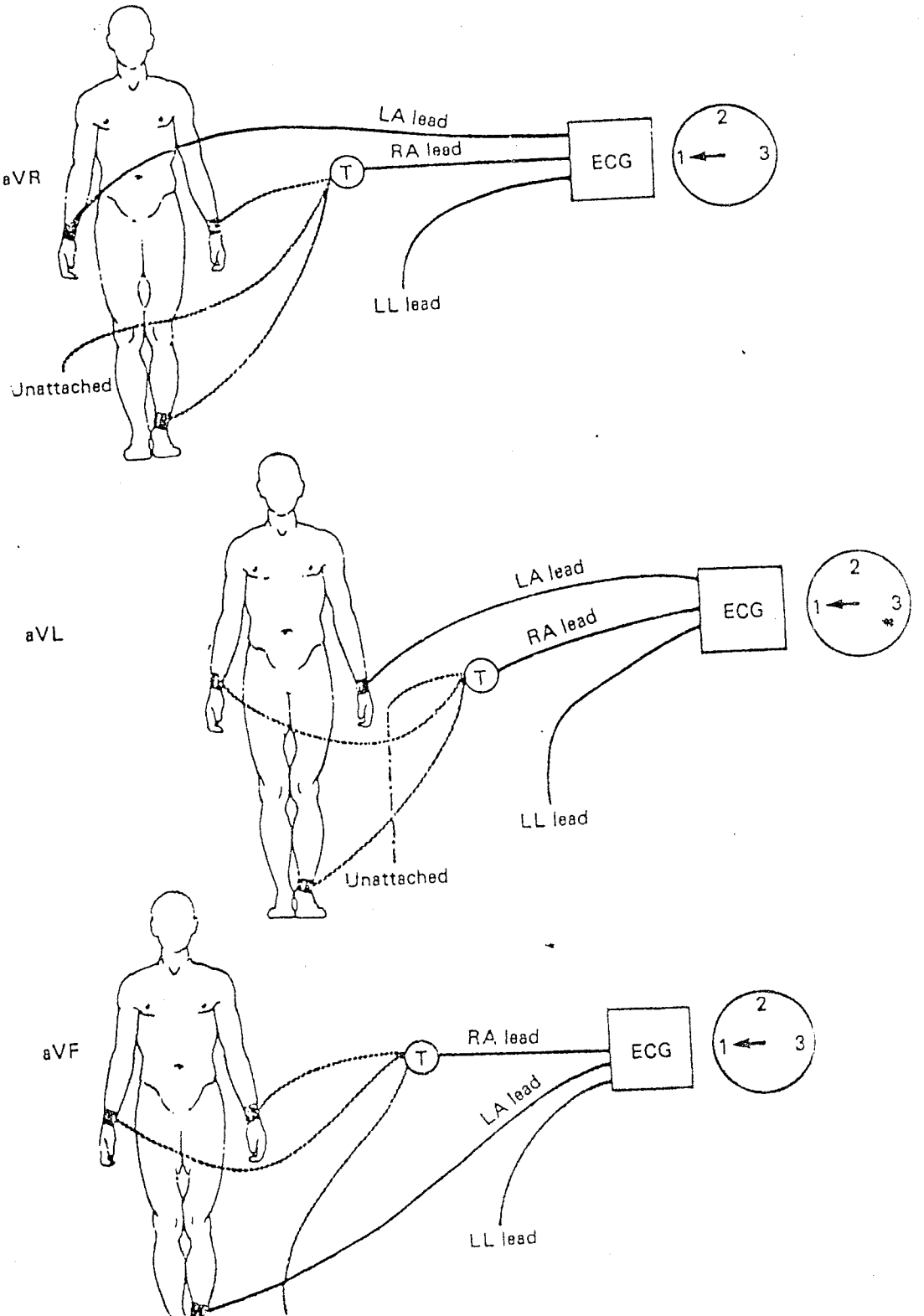
5. Any electonic equipment that comes in contact with the patient can produce artifacts in the ECG.

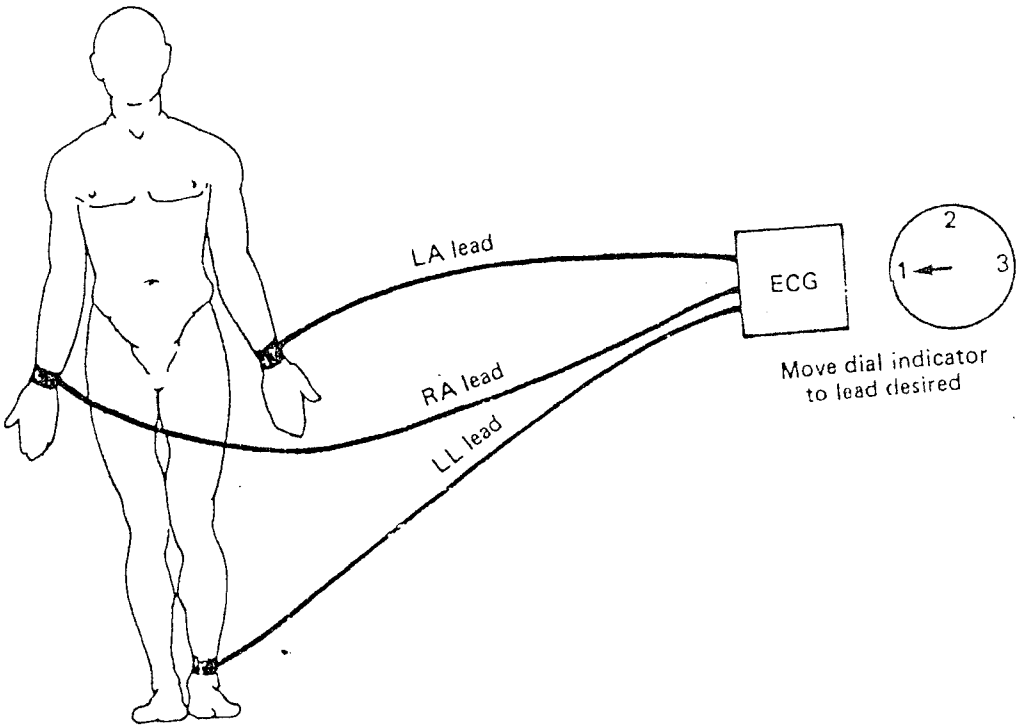
1.6 ELECTRODIOGRAPHIC GRID

Electrocardigraphic paper is a graph in which horizantal and vertical lines are present at 1mm intervals. A heavier line is present every 5mm. Time is measured along the horizantal lines: 1mm=0.045, 5mm=0.25. Voltage is measured along the vertical lines and is expressed as mm(10mm=1mV). The recording speed is 25mm/sec.

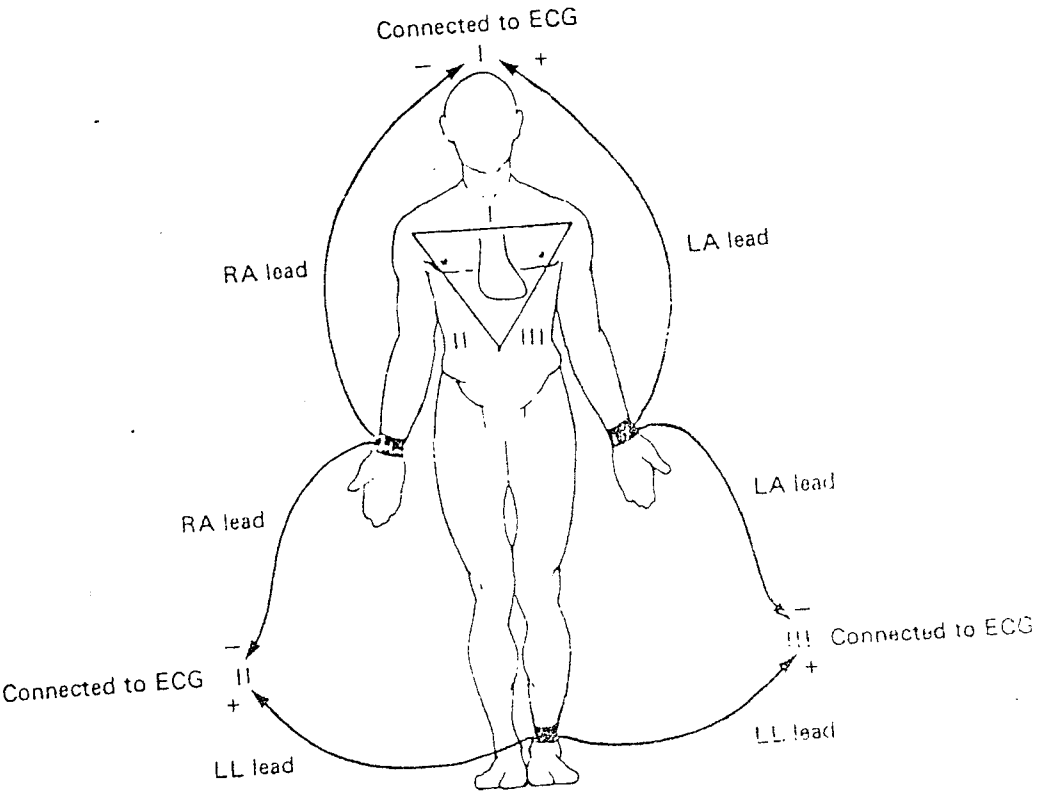


ocations of unipolar precordial leads.

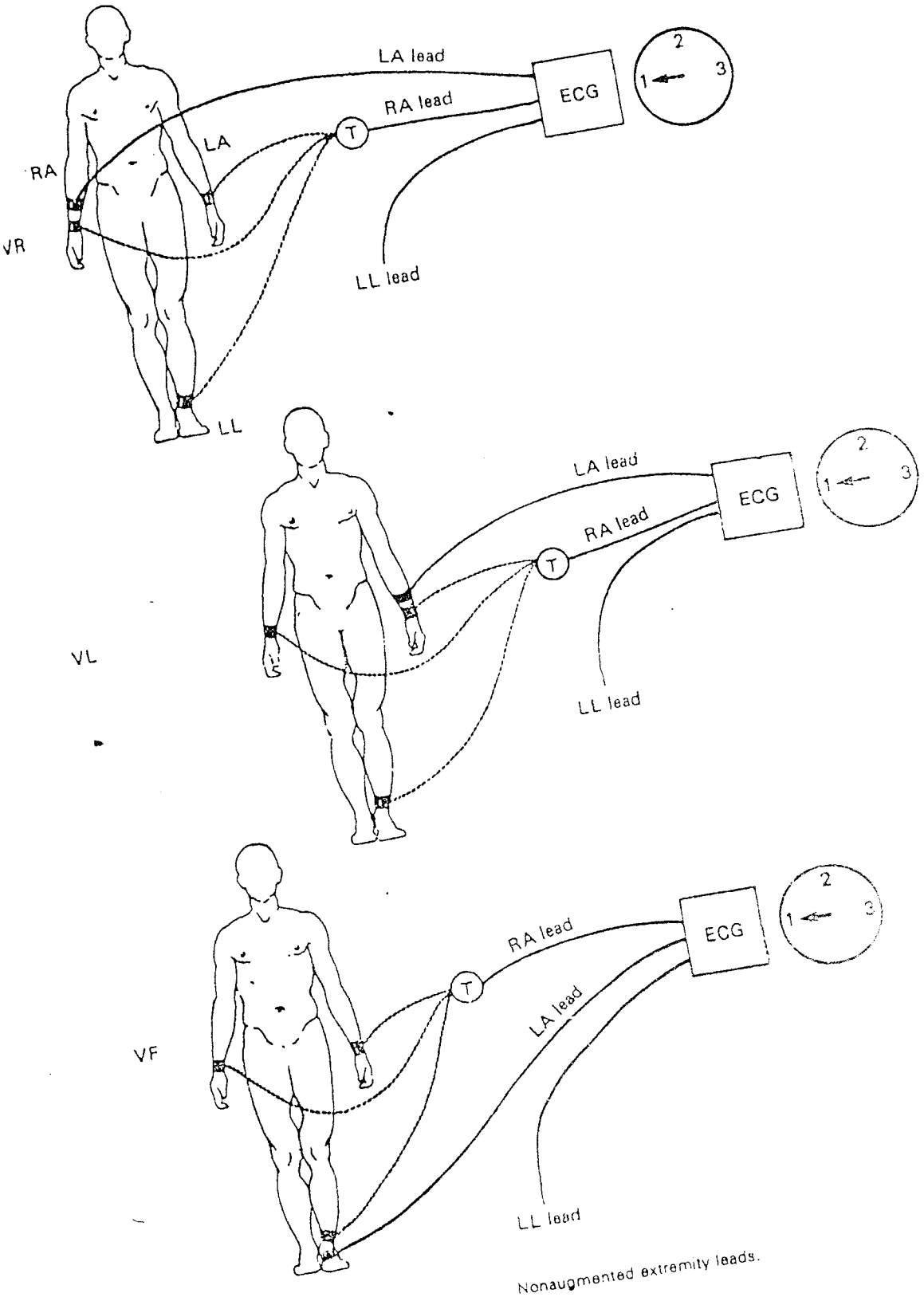

aVR
LA lead
RA lead
ECG
2
1
3
T
LL lead
Unattached
aVL
LA lead
RA lead
ECG
2
1
3
T
LL lead
Unattached
aVF
RA lead
ECG
2
1
3
T
LA lead
LL lead



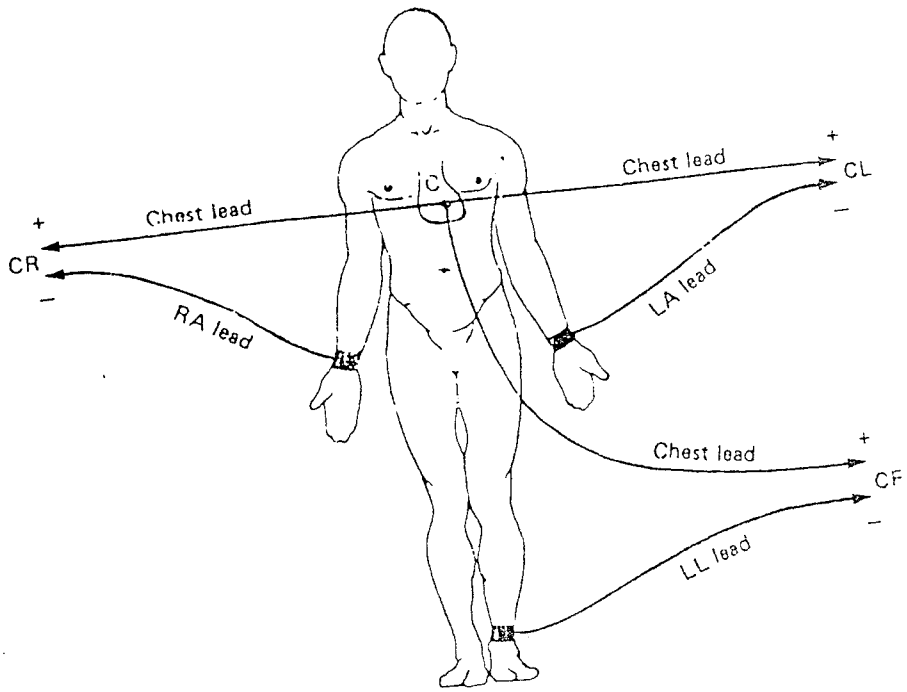
Standard leads.



for bipolar standard leads I, II, and III.



Nonaugmented extremity leads.



Connections for bipolar chest leads CR, CL, and CF

CHAPTER 2

II. ELECTROCARDIOGRAPHIC COMPLEXES

2.1 INTRODUCTION

Q, R, S refer to relatively large waves (over 5mm); q, r, s refer to relatively small wave(under 5mm)

P WAVE:

The deflection is produced by atrial depolarisation Ta(or Pt) wave. The deflection is produced by atrial repolarisation. This deflection produced is usually not seen in the average 12 lead ECG.

Q(q)Wave:

The initial negative deflection results from ventricular depolarisation. It preceded the first positive deflection(R)

R(r) WAVE:

The first positive deflection is during ventricular depolarisation.

S(s) WAVE:

The first negative deflection is of ventricular depolarisation that follows the first positive deflection(R).
R'(r') WAVE: The second positive deflection is during ventricular depolarisation.

S WAVE:

The negative deflection following the r' wave is the S wave.

2.1.1 VENTRICULAR ACTIVATION TIME:

The time taken for an impulse to traverse the myocardium from the endocardial to the epicardial surface is assumed to be reflected in a measurement from the beginning of the Q wave to the peak of the R wave. Such a measurement is accurate only when recorded directly from the surface of the heart(intrinsic deflection) preferably with closely packed bipolar electrodes. The accuracy and significance of this measurement diminishes with the body surface unipolar recordings. The VAT should not exceed .035sec in V(1-2) and 0.05sec in V(5-6)

QT Interval: This is measured from the onset of the wave to the end of the T wave. It measures the duration of the electrical systole. The QT interval varies with the heart rate and must be corrected. This is easily done with the use of monoglan which gives the QTc for a heart rate of 60. The normal QTc should not exceed .42sec in men and 0.43sec in women.

T WAVE:

The deflection produced by ventricular repolarisation.

U WAVE:

U deflection (usually +ve) is seen following the T wave and preceeding the next P wave.

2.2 NORMAL INTERVAL VALUES

RR Interval: The RR interval is the distance between 2 successive R waves. If the ventricular rhythm is regular, the interval in seconds between the peaks of 2 successive R waves divided into 60 will give the heart rate per minute. If the ventricular rhythm is irregular the number of R waves in a given period of time should be counted in a 10 second interval, the ventricular rate is counted as 120 per minute.

PP Interval: In regular sinus rhythm, the PP interval will be same as RR interval. When the ventricular rhythm is irreg-

ular or when atrial and ventricular rates are different but regular, the PP interval should be measured from the same point on 2 successful waves and the atrial rate per minute is computed as the ventricular rate.

PR Interval: This measures the AV conduction time. It includes the time required for

(1) Atrial depolarisation

(2) The normal conduction delay in the AV node and

(3) The passage of the impulse through the bundle of His and bundle branches to the onset of ventricular depolarisation. It is measured from the onset of the P wave to the beginning of the QRS complex.

QRS Interval: This is the measurement of total ventricular depolarisation time. It is measured from the onset of the Q wave(or R if no Q is visible) to the termination of the S wave. The upper limit of the normal is 0.1sec in frontal plane leads. Occasionally in precordial leads or V3 this interval may be 0.11sec.

QU Interval: This measures the interval from the beginning of the Q wave to the end of the U wave. It measures total ventricular repolarisation including the purkinge fibres.

ST Interval: The duration of the RST segment is given by the ST interval.

2.3 NORMAL SEGMENTS AND JUNCTIONS

PR Segment:It is that portion of the electrocardiographic tracing from the end of the P wave to the onset of the QRS complex. It is normally electric.

RST Junction: It is the point at which the QRS complex ends and the RST segment begins.

Rst Segment(called ST Segment): It is that portion of the tracing from the J to the onset of the T wave.

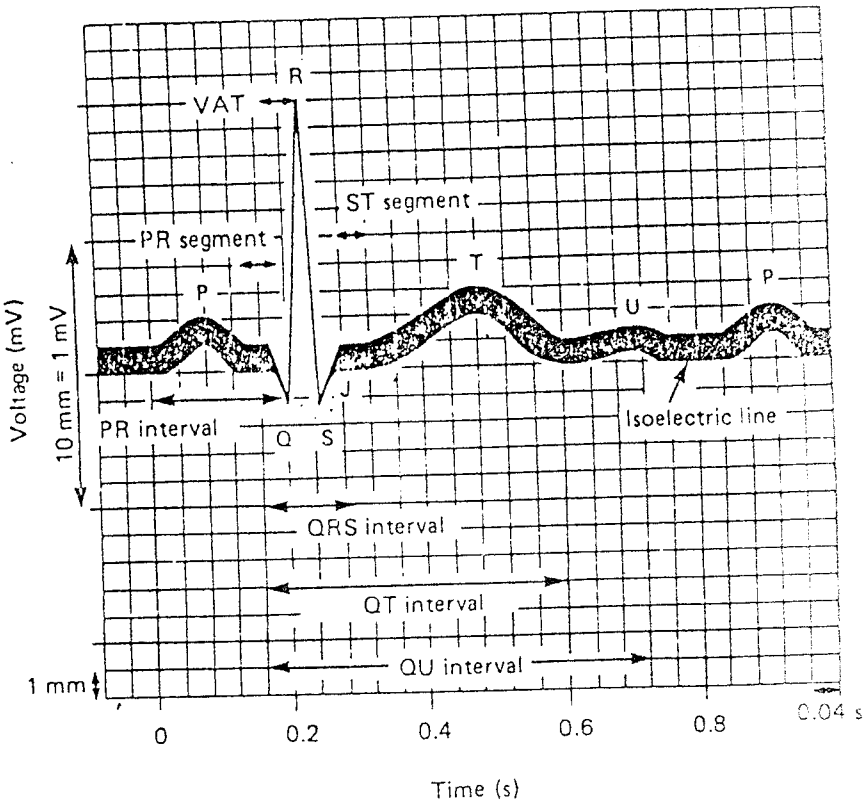


Figure 3–2. Diagram of electrocardiographic complexes, intervals, and segments.

SA node

↓

Atrial myocardium: Depolarization (P); repolarization (T_a)

Internodal pathways

↓

AV node

↓

Bundle of His

↓

Bundle branches

↓

Purkinje system: Late repolarization (U)

↓

Ventricular myocardium: Depolarization (QRS); repolarization (T)

Summary of conduction and excitation

CHAPTER 3

3. POWER SUPPLY DESIGN

3.1 REGULATED POWER SUPPLY

The power supply is a most common IC building block next to the OP-amp. The monolithic form of power supply has replaced discrete assemblies on their portion in conventional supplies because of its small size and low cost. Monolithic power supply is uniquely suited for local regulation. Basically two types of regulation are available, DC or dissipating type and switching type.

3.1.1 Definitions of Terms Related with Power Supply:

The function of the power supply is to maintain a constant output voltage, irrespective of the changes of the input voltage or the output current. It is characterised by several parametes in data sheet. Here we define them to know

the utility while selecting and designing a powersup circuit.

Load Regulation: It is defined as the percentage change regulated output voltage for a change in load from minim load current to the maximum load current.

If V1 is the output voltage with minimum rated lo and V2 is the output voltage with maximum rated load then

$$\text{Load Regulation}(\%) = \frac{V1-V2}{V1} \times 100$$

Line Regulation : It is defined as the percentage change i regulated output voltage for a change in input voltage.

Ripple Rejection: It is the ratio of the peak to peak inpu ripple voltage to the peak to peak output ripple voltage Ripple rejection is known as the live regulation for AC input signals at or above the given frequency with a specifie value of bypass capacitor on the ref. bypass terminals.

STANDBY(QUISCENT) CURRENT DRAIN: It is the supply current drawn by the regulator with no output load and no reference voltage load. More simply it is the current that flows into the power supply through to ground and it does not include any current drawn by the load or by external resistor network.

Reference Voltage: The output of the reference amplifier measures the output shorted to the negative supply.

Short circuited current limit: It is the output current of the regulator with the output shorted to the negative supply.

Sense Voltage: It is the voltage between current sense and current limit terminals necessary to cause current limiting.

Temperatuere Drift: It is the percentage change in output voltage(or ref. voltage) for a temperature variation from the room temperature to either temperature extremes.

Approximately 85 to 90 % of this drift occurs in the power supplies internal circuiting. The remaining 10 to 15% is due to error amplifier or bias current drift. Temperature drift is the major cause of output voltage change in a monolithic power supply.

3.2 DUAL TRACKING POWER SUPPLIES

These are very much suitable as regulated power suppling for Op-amp. There are two ways to provide tracking for dual voltages

1. Dual output power supplies
2. Two single power supplies

Power supply such as LM125,126 and 127 and MC1568 provide +15V or -15V at an output current of 100 mA. These voltages are matched to within 1% with line and voltage regulation of 0.06%. All units provide a terminal for the connection of the current limiting components. The MC1568 has an additional terminal which along wih the external circuit

allows the user to adjust the output voltages from +8V or -8V to +20 or -20V.

Another way of making dual regulated power suply is use of single voltage regulators in pair along with external circuit. The advantage of this method is that it can supply a wide range of voltage at much higher currents.

3.3 General Features of Monolithic Regulated Power Supplies

The monolithic regulated supplies currently available fall under the following catagories.

3.3.1 Adjustable with Positive or Negative Outputs

In such category, regulated output voltage can be chosen and set to a value between two fairly wide limits. For example type 105 regulated supplies fabricated by several manufacturers provide positive regulated output as high as 40V and as low as 4.5V.

3.3.2 FIXED POSITIVE OR NEGATIVE OUTPUTS

It is more common as +5V supply for logic gates such as TTL or +24V for some relay. It does not require external components. Its small size permits it to be located directly on the PCB requiring the regulated voltage.

3.3.3 DUAL TRACKING REGULATED SUPPLIES

These are used to provide a regular voltage for an OP-amp which require both positive and negative voltage. In addition to regulation these voltages must also track. This means that if the positive line decreases the negative line must also decrease such that the magnitude of both the line voltages to the ground is constant.

CHAPTER 4

DIGITAL INPUT /OUTPUT CARD FOR IC

4.1 INTRODUCTION

The digital I/O Card is IBM/XT/AT compatible with two 8255A PPI's which provide 48 programmable I/O lines. The 24 I/O lines of first 8255A are brought out through a 26 pin ribbon cable connector. The next 24 lines of the second 8255A's can be mapped at different addresses, using the 8 way DIP switch provided.

4.2 INSTALLATION

Install the card in any one of the avaible slots in the system. The diagram and pin details are shown in Fig(4.1)

4.3 ADDRESS MAPPING

The ports of the two 8255A's can be mapped addresses. The lower addresses refer to the first 8255A whose output are brought out on 26 pin ribbon cable connector and the higher addresses for the second 8255A whose outputs are brought out on another 26 pin ribbon cable connector. For example if the adress range is specified as 0380H - 0383H refer to the first 8255A and the addresses 0384H - 0387H refer to the second 8255A.

The address 0380H refers to port A of lower 8255A (J1)

0381H to port B

0382H to port C

0383H to control port

similarly the address

0384H refers to port A of upper 8255A (J2)

0385H to port B

0386H to port control port

8 SELECTION DIP SWITCH SETTINGS

SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	ADDRESS
ON	OFF	ON	OFF	ON	OFF	ON	OFF	0380-0387H
ON	OFF	ON	OFF	ON	OFF	ON	OFF	0388-038FH
ON	OFF	ON	OFF	ON	OFF	ON	OFF	0390-0397H
ON	OFF	ON	OFF	OFF	ON	OFF	ON	0398-039FH
ON	OFF	OFF	ON	ON	OFF	ON	OFF	03A0-03A7H
ON	OFF	OFF	ON	ON	OFF	OFF	ON	03A8-03AFH
ON	OFF	OFF	ON	OFF	ON	ON	OFF	03B0-03B7H
ON	OFF	OFF	ON	OFF	ON	OFF	ON	03B8-03BFH
OFF	ON	ON	OFF	ON	OFF	ON	OFF	03C0-03C7H
OFF	ON	ON	OFF	ON	OFF	OFF	ON	03C8-03CFH
OFF	ON	ON	OFF	OFF	ON	ON	OFF	03D0-03D7H
OFF	ON	ON	OFF	OFF	ON	OFF	ON	03D8-03DFH
OFF	ON	OFF	ON	ON	OFF	ON	OFF	03EO-03E7H
OFF	ON	OFF	ON	ON	OFF	OFF	ON	03E8-03EFH
OFF	ON	OFF	ON	OFF	ON	ON	OFF	03F0-03F7H
OFF	ON	OFF	ON	OFF	ON	OFF	ON	03F8-03FFH

The I/O address can be selected by the 8 way DIP switch. All the possible address ranges are given in the table in the previous page.

The following addresses cannot be made use of as they are used by the system for the following

(1) 02D0H - 03DFH : colour graphics adapter

(2) 03F0H - 03F7H : disketter adapter

(3) 03F8H - 03FFH : serial port (COM 1)

4.4 CONNECTOR DETAILS

The 24 programmable I/O lines of the first 8255A are brought out on a 26 pin ribbon cable connector J1. For either case the pin connection are given. Care should be execised to refer to the correct type. The 24 programmable I/O lines of the second 8255A are brought out another 26 pin ribbon cable connector J2, the pin configuration of which is given in the diagram.

CHAPTER – 5

5.1 CIRCUIT COMPONENTS

5.1.1 LM 324

This is a 14 pin dual op-amp I.C. An ideal operational amplifier provides a linear O/P voltage that is proportional to the difference between two input terminals. The output voltage will have same polarity as that of noninverting(+) input with respect to the voltage at the inverting, when it is greater i.e. it has a positive amplitude. Similarly, it will be negative if noninverting input is more negative than the inverting pin.

This I.C. is used here to nullify the D.C. offset in the signal. The D.C. offset is nothing but an increase in voltage level of the signal i.e. even for a zero frequency the signal will have an amplitude.

The E.C.G signal from the machine has the D.C. offset (or) base line shift, which has been briefly explained

in the above paragraph. The input signal is given to the inverting terminal of the op-amp and the positive terminal is connected to wiper arm of the pot whose ends are tied at +5V and GND.

The wiper is adjusted such that voltage at the wiper and the D.C. offset in the signal are same, so the difference between these two inputs is amplified and given out by the operational amplifier. The difference in voltage is nothing but the original input signal so the base line shift is nullified.

5.1.2 LM 725(INSTRUMENTATION AMPLIFIER)

The necessity for an instrumentation amplifier are

1. High gain acuuracy.
2. High common mode rejection ratio (CMRR)
3. High gain stability with low temperature coefficient.

4. Low D.C. offset

5. Low output inpedance.

The instrumentation amplifier is basically made using 3 operational amplifier. In practical aspect no two operational amplifiers of same specification and characteristics behave uniformly so it is difficult to construct with 3 op-amps. In this project the instrumentation amplifier is implemented using LM 725 which is a precision amplifier meeting the above requirements.

5.1.3 LF 398 (Sample and Hold)

A sample and hold circuit samples and input signal and holds on to its last sampled value until the input is sampled again. This type of circuit is very useful in digital interfacing, Analog to Digital conversion and pulse coded modulation.

The LF 398 I.C. is used for analog to digital conversion only. The sampling is controlled by logic pins

7&8, for efficient operation one of the two logic pins should at least be 2V below the supply voltage and the other atleast 3V above the negative supply. The pin no 7 is grounded which is 15V above the negative supply and the time for sampling is determined by control voltage signal frequency. When the signal is high it samples and when it is low it holds. The capacitor connected to the pin no6 is the holding capacitor which holds the sampled input.

5.1.4 ADC 0800

This ADC0800 is a direct type ADC i.e. compares the analog signal with the internally generated equivalent signal. This ADC uses Successive Approximation method.

Successive Approximation technique is a very efficient codesearch statergy to complete n bit conversion in just n clock period. The ADC is run in continous mode i.e. End of Conversion is tied to Start Conversiom. Usually oscillations might occur in this line for 4 clock pulse. So

to avoid this a 4 clock pulse delay is generated using I.C.74175. Another advantage is that manual Starting of conversion is possible.

When Start conversion is given S.A.R.[Succesive Approximation Register] sets D1[MSB] to 1[High] and all other bits to 0[Low]. It compares the output Vd of the ADC with the Analog input Va. If Va>Vd then this code is not correct. So the next MSB is also set to 1[High] and compared. If Va<Vd MSB is set to 0 and the next MSB is set to 1. The comparission is continued until all bit positions have been tested. When ADC output crosses Va the comparator changes state and this can be taken as E.O.C.[End Of Conversion]

5.1.5. 74LS244[Buffer]

It is a 20 pin buffer having 2 sets of 4 bit buffer having active low enable. Buffer is a logic circuit which amplifies the current or power primarily which is used to increase the driving capability of the logic circuit. Each buffer is capable of sinking 24mA and sourcing -15mA.

5.1.6. 74LS04[clock]:

The digital Gate can be used to act as crystal oscillator by first biassing them into linear amplifier mode and connecting the crystal into a positive feedback path between the amplifier's O/P and I/P feedback resistor and then coupled in series via capacitor to give overall phase-shift 0. The circuit oscillates when crystal is connected between the O/P and I/P.

5.1.7. 74LS132[Schmitt Nand Gate]:

A Schmitt trigger can be defined as comparator with positive feedback or hysterisis with an analog I/P signal and the output is square wave or logic output. Hysterises may be made large or small to prevent input noises from appearing at the output. This type of circuit is very useful for pulse shaper. The Nand gate is used as pulse shaper for the High Frequency clock to get a perfect square wave.

5.1.8. 74LS26 [MOS Interface TTL Nand Gate]:

The TTL operates at 5V. When interfacing this logic with other high voltage logics like MOS serious problem arises as it cannot drive them. So a Buffer is needed to interface with other logic. 74LS26 has 2 I/P open collector Nand gates having high voltage rating for interfacing low threshold MOS logic circuits. The output is rated to withstand 15V.

5.1.9. 4020B [Ripple Counter]:

This is a 14 stage ripple counter unit with all O/P's except 2 & 3 being externally accessable giving a maximum division ratio of 16384. It is triggered on the negative transition of each I/P pulse. All counters can be reset by giving an active high pulse to the reset pin.

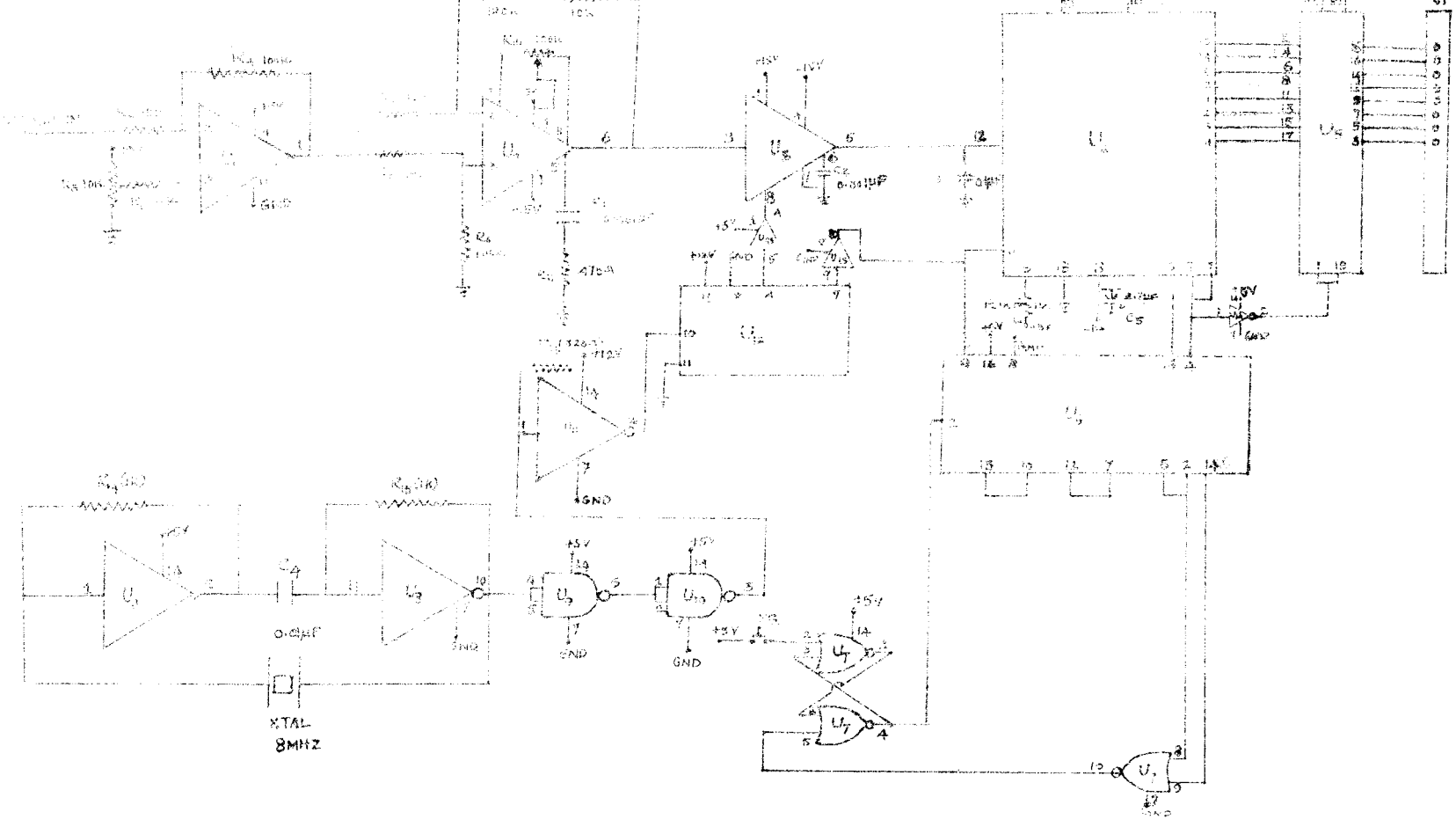
5.1.10. 40106UB[SCHMITT NOT Gate]

This NOT Gate is used as a buffer for interfacing TTL to CMOS through 7426. The pull up resistor connected to input terminal and supply terminal gives the necessary driving current.

5.1.11. 4050B [Hex Non Inverting Buffer]:

This is a Hex non-inverting buffer used for interfacing MOS to low voltage logic circuits like TTL. It sinks the necessary current for driving. The supply is connected to 5V. It is used to interface 4020B[CMOS] to ADC[0800] and 74175.

The output voltage of the buffer is equal to the supply voltage (5V) even though the input voltage level is 12V.



U_1 - LM 324	U_6 - 74LS244	U_9 - 74LS32	
U_2 - LM 725A	U_7 - 74LS174	U_{10} - 74LS20	U_{11} - 40106B
U_3 - LF 398	U_8 - 74LS02	U_{12} - 4020B	
U_4 - ADC0800	U_{9a}, U_{9b} - 74LS04	U_{13} - 4555B	

5.2 INTERFACING HARDWARE

5.2.1 8255A PROGRAMMABLE PERIPHERAL INTERFACE

The 8255A is a widely used, programmable parallel I/O device. It can be programmmed to transfer data under various conditions, from simple I/O to interrupt I/O.

The 8255A has 24 I/O pins that can be grouped primarily in two 8bit parallel ports: A&B, with remaining eight bit as Port C. The eight bits of port C can be used as individual bits of grouped in two 4 bit ports C lower & C upper. The fuctions of 8255A is classified according to two modes. The Bit set/Reset (BSR) mode and the I/O mode. The BSR mode is used to set or reset the bits in port C. The I/O mode is further divided into three modes: mode0, model, &mode2. In mode0, all ports function as simple I/O ports. Model is a handshake mode whereby ports A&/or B uses from port C as handshake signal, either status check or interrupt type of I/O data transfer can be implemented. In mode2 port

A can be setup for bidirection data transfer using handshake signals from port C, and port B can be set up either in mode 0 or 1.

The 8255A has control register, contents of which specify and I/O function for each port. This is called control word.

The control word is 8 bit word. The format of the control word is shown in the figure(5.1). So by writing the required control word in the control register the 8255A, can be used for various operation.

There are six control lines.

$\overline{RD}$(Read). This enables read operation.

$\overline{WR}$(Write). This enables write operation. The data can be written in selected I/O port or control register.

RESET: This active high signal clears the control register and sets all ports in the input mode.

$\overline{CS}$,A0&A1

CS is the master chip select and A0&A1, specify one of the I/O ports or the control register as given below.

$\overline{CS}$	A0	A1	SELECTED
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	x	x	Not selected.

P211

Here the address for 8255A is set as follows.

The address 0380H refers to port A of lower 8255A (J1)

0381H to port B

0382H to port C

0383H to control port

similarly the address

0384H refers to port A of upper 8255A (J2)

0385H to port B

0386H to port control port

By any one of this address to 8255A, the required port can be accessed.

CHAPTER - 6

6.1 PCB DRAWING

The Printed Circuit Board (PCB) making is the arrangement of components in a neat, compact way on a copper clad board with circuit connections.

The various components used in PCB assembly have standard dimensions. Based on this suitable spacing is to be provided while drawing a PCB. First the circuit diagram is thoroughly studied. The size of the different components are noted down. Approximate placing of the different components are taken in preparing a PCB layout. The layout should be a compact, arrange the componenets neatly, spacing is to be provided sufficiently according to the size of the components so that the leads do not break by bending or the components do not get crowded, and all the connecting lines are drawn in the board.

A rough layout for the circuit is prepared on a paper indicating the placing of the components and lines interconnecting them. This diagram is then converted to required PCB layout .

6.2 FABRICATION

The layout of the PCB drawn in graph shhet is transferred to the copper side of the board. This may be done with help of carbon paper. Then the lines and pads on the board are painted with acid resist ink using fine brush. Then the board is put in a solution of ferric chloride in water with little quantity of HCl and the solution is slightly stirred. This process is called etching. After this only copper lines and pads are available for connections. Then the holes are drilled (1mm) for mounting the components.

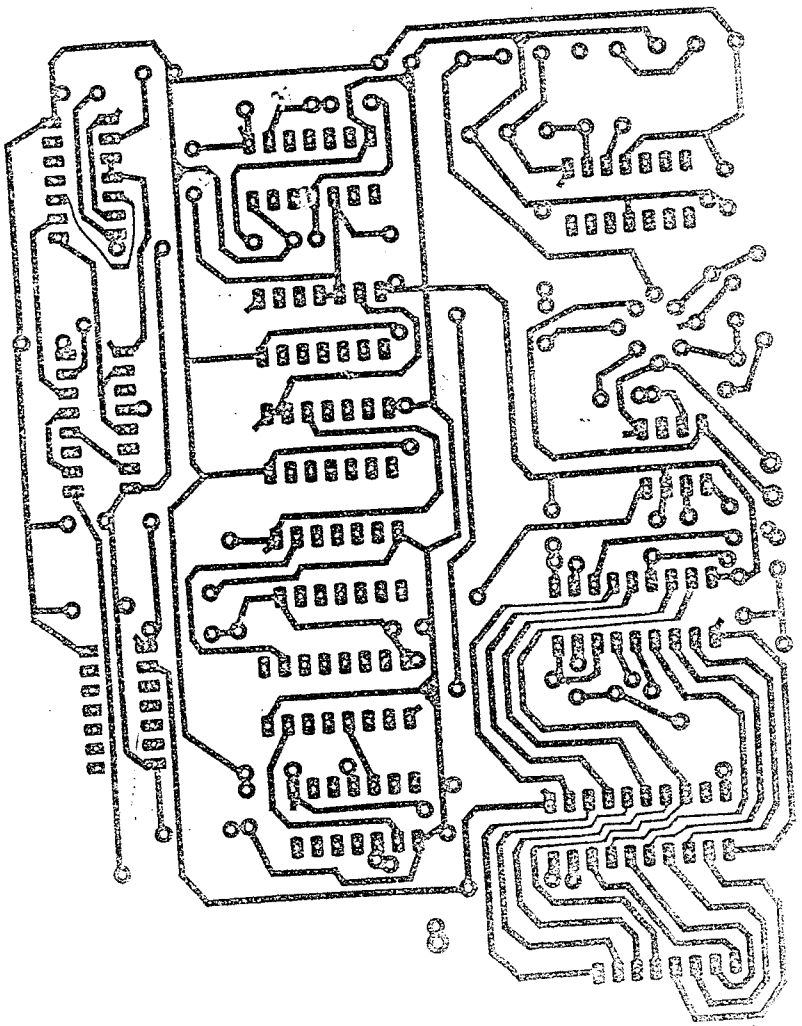
6.3 TESTING

The completed PCB is tested for the continuity wherever required by multimeter. Shorts between lines are

also checked and removed if found. Then assembly of components is done by inserting the leads of the components in to the holes and solder it using lead. Care is to be taken while bending otherwise the leads will break away form the body. Then the assembled PCB is tested and checked whether the required output is obtained.

PCB SOLDER SIDE

Approximate size: 5.50 by 4.4 inches

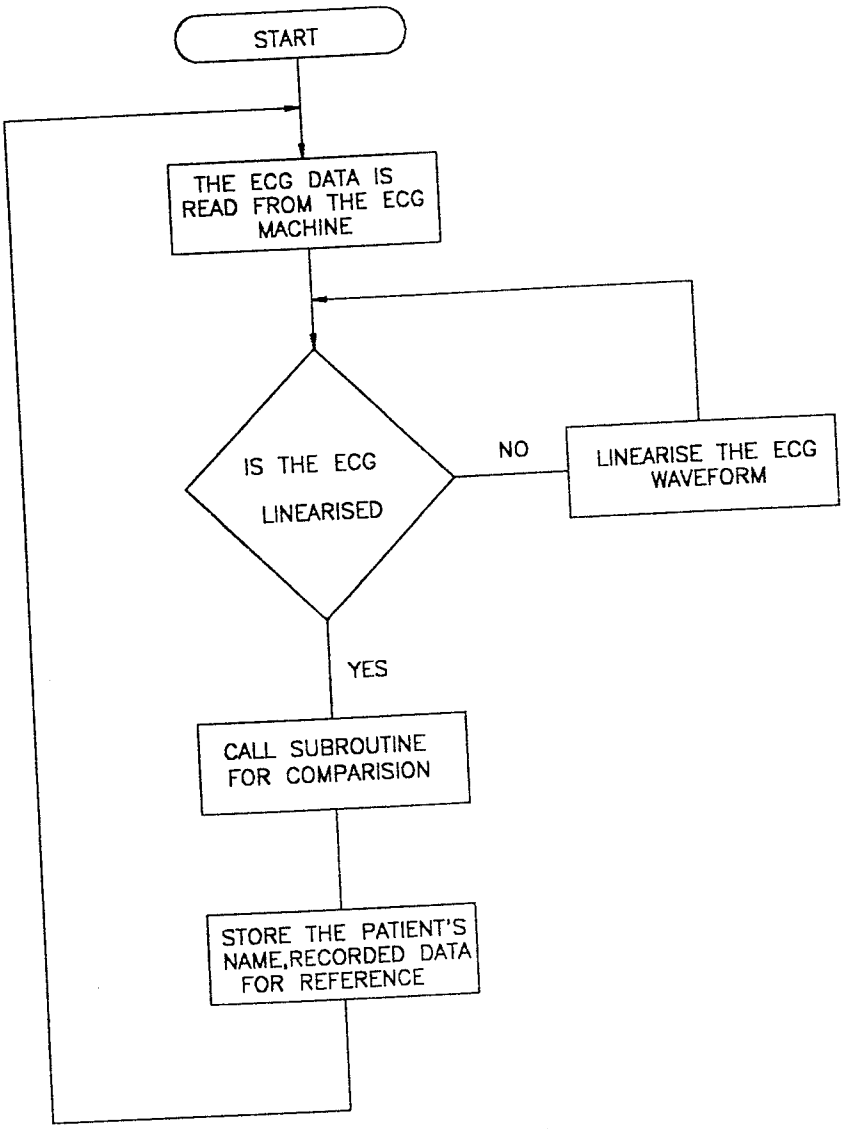


CHAPTER - 7

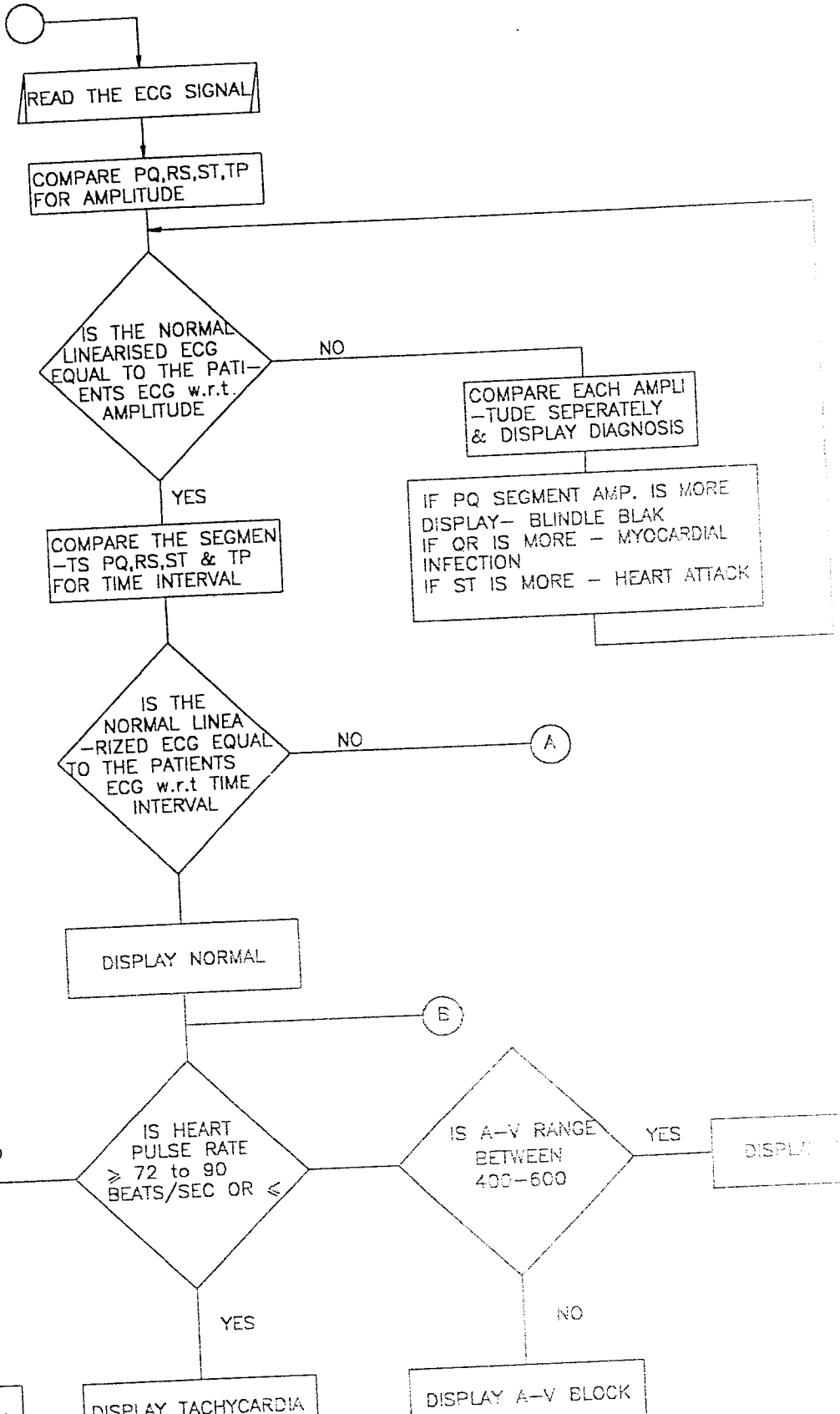
7.1 FLOW CHART

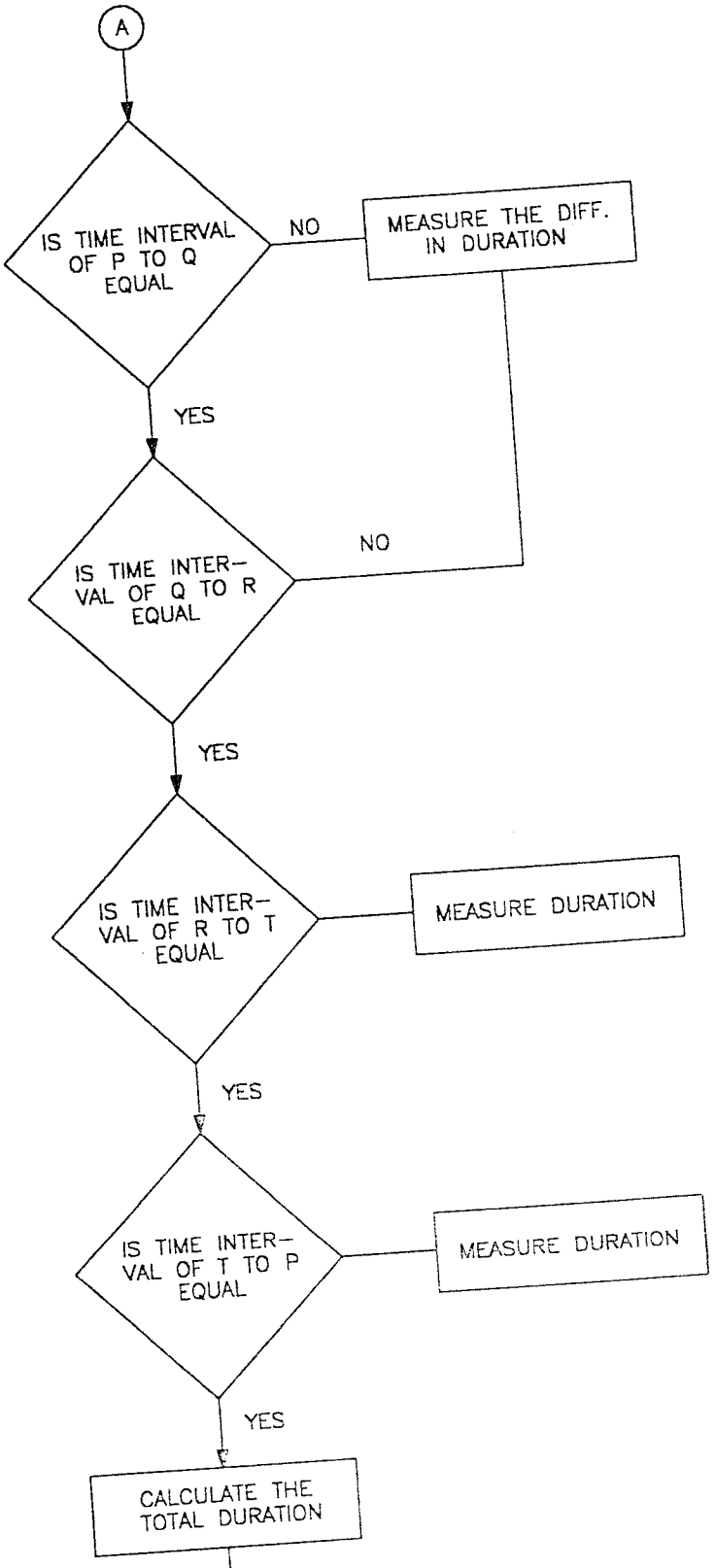
In this chapter, the flow chart and software program are given. The various steps for analysis of ECG Waveform using a Personal Computer are shown in the flow chart Fig(7.1)

FLOWCHART


START
THE ECG DATA IS READ FROM THE ECG MACHINE
IS THE ECG LINEARISED
NO
LINEARISE THE ECG WAVEFORM
YES
CALL SUBROUTINE FOR COMPARISION
STORE THE PATIENT'S NAME,RECORDED DATA FOR REFERENCE

SUBROUTINE


READ THE ECG SIGNAL
COMPARE PQ,RS,ST,TP FOR AMPLITUDE
IS THE NORMAL LINEARISED ECG EQUAL TO THE PATI–ENTS ECG w.r.t. AMPLITUDE
NO
COMPARE EACH AMPLI –TUDE SEPERATELY & DISPLAY DIAGNOSIS
IF PQ SEGMENT AMP. IS MORE DISPLAY– BLINDLE BLAK
IF QR IS MORE – MYOCARDIAL INFECTION
IF ST IS MORE – HEART ATTACK
YES
COMPARE THE SEGMEN –TS PQ,RS,ST & TP FOR TIME INTERVAL
IS THE NORMAL LINEA –RIZED ECG EQUAL TO THE PATIENTS ECG w.r.t TIME INTERVAL
NO
A
DISPLAY NORMAL
B
IS HEART PULSE RATE ⩾ 72 to 90 BEATS/SEC OR ⩽
NO
IS A–V RANGE BETWEEN 400–600
YES
YES
NO
DISPLAY TACHYCARDIA
DISPLAY A–V BLOCK


A
IS TIME INTERVAL OF P TO Q EQUAL
NO
MEASURE THE DIFF. IN DURATION
YES
IS TIME INTER-VAL OF Q TO R EQUAL
NO
YES
IS TIME INTER-VAL OF R TO T EQUAL
MEASURE DURATION
YES
IS TIME INTER-VAL OF T TO P EQUAL
MEASURE DURATION
YES
CALCULATE THE TOTAL DURATION

```
#include "graph.prg"
#include "read.prg"
#define POPUP_BORDER   RED
#define POPUP_COLOR    LIGHTRED
#define TEXT_COLOR     WHITE
#define HIGH_TEXT_COLOR DARKGRAY

#define HIGH   1
#define LOW    0

#define LEFT            0x4b00
#define RIGHT           0x4d00
#define UP              0x4800
#define DOWN            0x5000
#define ENTER           0x000d
#define ESC             0x001b

    char mmenu[4][17]={ "ANALYSIS","REPORT","HELP","QUIT"};
    char popup[4][7][17]=
          { {""},
            {"TO PRINTER","SAVE"},
            {"ABOUT","ECG"},
            {""}};

    int count[4]={0,2,2,0};
    char mess[4][7][50]=
    {
     { "ANALYSING ECG WAVEFORM"
     },
     { "TO PRINT THE REPORT",
       "TO SAVE THE REPORT TO A FILE"
      },
     { "HELP FOR ECG-ANALYSER",
       "HELP FOR ECG"
     },
     {
       "QUIT TO MSDOS"
     }
    };
    int pop_opt[4];
    int main_opt;


union REGS in_reg,out_reg;

int GetKey()
{
 in_reg.h.ah=8;
 int86(0x21,&in_reg,&out_reg);
 out_reg.h.ah=0;
 if(out_reg.h.al!=0) return(out_reg.h.al);
 int86(0x21,&in_reg,&out_reg);
```

```
 out_reg.h.al=0;
 return(out_reg.x.ax);
}

void Block(int left,int top,int len,int ht,int col,int bcol)
 {
   int rec[4][2];
   //To set fill style & color
   if(bcol==17)
   bcol=col;
  setcolor(bcol);
  setfillstyle(SOLID_FILL,col);
  // To set up rectangle coordinates
  rec[0][0]=rec[3][0]=left;
  rec[0][1]=rec[1][1]=top;
  rec[1][0]=rec[2][0]=left+len;
  rec[2][1]=rec[3][1]=top+ht;
  fillpoly(4,&(rec[0][0]));
 }

 void drawbar()
 {
  int i;
  Block(0,0,640,30,WHITE,WHITE);
  settextstyle(TRIPLEX_FONT,HORIZ_DIR,3);
  setcolor(DARKGRAY);
  outtextxy(200,0,"ECG ANALYSER");
  Block(0,456,640,25,LIGHTGRAY,LIGHTGRAY);
  setcolor(TEXT_COLOR);
  outtextxy(120,457,"THILHAN SOFTWARES * SRC ");
  settextstyle(DEFAULT_FONT,HORIZ_DIR,1);
  Block(0,31,640,12,LIGHTGRAY,LIGHTGRAY);
  setcolor(TEXT_COLOR);
  for(i=0;i<4;i++)
    outtextxy(i*120+20,33,mmenu[i]);
 }

 void drawpopup(int pop_num)
 {
  int i,x,y;
  y=44;
  x=pop_num*120+25;
  setcolor(POPUP_BORDER);
  rectangle(x,y,x+110,y+count[pop_num]*12+5);
  setfillstyle(SOLID_FILL,POPUP_COLOR);
  floodfill(x+1,y+1,POPUP_BORDER);
  settextstyle(DEFAULT_FONT,HORIZ_DIR,1);
  setcolor(TEXT_COLOR);
  for(i=0;i<count[pop_num];i++)
   outtextxy(x+4,y+i*11+3,popup[pop_num][i]);
  }


 void highlight(int high)
```

```
{
 int col;
 col=high?HIGH_TEXT_COLOR:TEXT_COLOR;
 setcolor(col);
 if(count[main_opt])
 outtextxy(main_opt*120+29,44+pop_opt[main_opt]*11+3,
           popup[main_opt][pop_opt[main_opt]]);
 outtextxy(main_opt*120+20,33,mmenu[main_opt]);
 Block(0,441,640,15,RED,RED);
 setcolor(WHITE);
 outtextxy(50,443,mess[main_opt][pop_opt[main_opt]]);
}

int trace()
{
 while(1)
 {
  switch(GetKey())
  {
  case RIGHT:
             highlight(LOW);
             main_opt++;
             main_opt%=4;
             Block(0,43,640,120,BLACK,BLACK);
             if(count[main_opt]) drawpopup(main_opt);
             highlight(HIGH);
             break;
   case LEFT:
             highlight(LOW);
             if(!main_opt)
                   main_opt=3;
             else
                main_opt--;
             Block(0,43,640,120,BLACK,BLACK);
             if(count[main_opt]) drawpopup(main_opt);
             highlight(HIGH);
             break;
    case DOWN:
             if(!count[main_opt]) break;
             highlight(LOW);
             pop_opt[main_opt]++;
             pop_opt[main_opt]%=count[main_opt];
             highlight(HIGH);
             break;
     case UP  :
             if(!count[main_opt]) break;
             highlight(LOW);
             if(pop_opt[main_opt])
                 pop_opt[main_opt]--;
             else
                pop_opt[main_opt]=count[main_opt]-1;
             highlight(HIGH);
             break;
     case ENTER:return(main_opt*100+pop_opt[main_opt]+1);
     case ESC : closegraph();exit(0);return(0);
```

```
default: continue;
}


id spopup(int x,int y,int num,char pmenu[7][17])

nt i;
lock(x,y,110,num*11+5,POPUP_COLOR,POPUP_COLOR);
etcolor(TEXT_COLOR);
or(i=0;i<num;i++)
  outtextxy(x+4,y+i*11+3,pmenu[i]);
eturn;


nt tracepopup(int x,int y,int num,char pmenu[7][17],char m[7][50],int opt)

spopup(x,y,num,pmenu);
setcolor(HIGH_TEXT_COLOR);
outtextxy(x+4,y+opt*11+3,pmenu[opt]);
Block(0,441,640,15,RED,RED);
setcolor(WHITE);
outtextxy(50,443,m[opt]);
while(1)
{
 switch(GetKey())
 {
 case DOWN: if(!count[main_opt]) break;
            setcolor(TEXT_COLOR);
            outtextxy(x+4,y+opt*11+3,pmenu[opt]);
            opt++;
            opt%=num;
            setcolor(HIGH_TEXT_COLOR);
            outtextxy(x+4,y+opt*11+3,pmenu[opt]);
            Block(0,441,640,15,RED,RED);
            setcolor(WHITE);
            outtextxy(50,443,m[opt]);
            break;
  case UP  : if(!count[main_opt]) break;
            setcolor(TEXT_COLOR);
            outtextxy(x+4,y+opt*11+3,pmenu[opt]);
            if(opt)
               opt--;
            else
               opt=num-1;
            setcolor(HIGH_TEXT_COLOR);
            outtextxy(x+4,y+opt*11+3,pmenu[opt]);
            Block(0,441,640,15,RED,RED);
            setcolor(WHITE);
            outtextxy(50,443,m[opt]);
            break;
  case ESC  :Block(x,y,110,num*11+8,BLACK,BLACK);
             return(0);
  case ENTER:return(opt+1);
  default  :continue;
```

```
  }
 }
}

void menuscreen()
{
 setbkcolor(LIGHTCYAN);
 drawbar();
 if(count[main_opt])
 drawpopup(main_opt);
 highlight(HIGH);
}

void main()
{
 int i,opt;
 char s[5];
 int  a[400];
 for(i=0;i<4;i++)
          pop_opt[i]=0;
 main_opt=0;
 StartGraph();
 menuscreen();
 while(1)
 {
  opt=trace();
  switch(opt)
  {
   case 1:StdEcgWave();
          clearviewport();
          menuscreen();
          break;
   case 101:
          StoreData(a,100,0x0380);
          EcgWave(a,100);
          clearviewport();
          menuscreen();
          break;
   case 301:
          closegraph();
          exit(0);
          break;
   default: sprintf(s,"%d",opt);
          Block(200,200,40,40,LIGHTGRAY,LIGHTGRA
          setcolor(WHITE);
          outtextxy(200,200,s);

  }
 }
}
```

```
#include<graphics.h>
#include<dos.h>
#include<conio.h>
#include<ctype.h>
#include<iostream.h>

int  FONT=1;
void Block(int left,int top,int len,int ht,int col,int bcol=17)
 {
   int rec[4][2];
   //To set fill style & color
   if(bcol==17)
   bcol=col;
  setcolor(bcol);
  setfillstyle(SOLID_FILL,col);
  // To set up rectangle coordinates
  rec[0][0]=rec[3][0]=left;
  rec[0][1]=rec[1][1]=top;
  rec[1][0]=rec[2][0]=left+len;
  rec[2][1]=rec[3][1]=top+ht;
  fillpoly(4,&(rec[0][0]));
 }

 void RunTitle(char *name,int size,int x,int y,int FG,int BK)
 {
 int i,j,len=0;
 char s[2];
 s[1]='\0';
 i=0;

 settextstyle(FONT,HORIZ_DIR,size);
 while(name[len]!='\0')
        len++;
 Block(x,y,len*size*8,size*8,BK);
  setcolor(FG);
 setwritemode(XOR_PUT);
 for(i=0;i<len;i++)
 {
  setwritemode(XOR_PUT);
  if(isalpha(name[i]))
  for(j='A';j<name[i];j++)
  {
   s[0]=j;
   outtextxy(x+i*size*8,y,s);
   delay(5);
   outtextxy(x+i*size*8,y,s);
  }
   setwritemode(COPY_PUT);
  s[0]=name[i];
  outtextxy(x+i*size*8,y,s);
 }
 setwritemode(COPY_PUT);
 }
```

```
{
 int col[3],col1[3];
 int i=1;
 col[0]=1;
 col[1]=2;
 col[2]=3;
 col1[0]=8;
 col1[1]=9;
 col1[2]=14;
 FONT=7;
 setbkcolor(LIGHTCYAN);
 RunTitle("DATA ACQUISITION & ANALYSIS",3,3,60,col[0],0);
 RunTitle("OF",3,270,110,col[0],0);
 RunTitle("ECG WAVEFORM USING A PC",3,40,150,col[0],0);
 FONT=4;
 RunTitle("BY",4,230,230,col[1],0);
 FONT=6;
 RunTitle("CHELLIAH SUNDAR E",2,260,280,col[2],0);
 RunTitle("RAVINDRA RAJ R",2,260,330,col[2],0);
 RunTitle("RAJARAM R",2,260,380,col[2],0);
  while(!kbhit())
 {
  setpalette(col[i%3],col[i%3]+1);
  i++;
  i%=256;
  delay(100);
 }
 getch();
 /*while(!kbhit())
 {
  col[i]+=col1[i];
  col1[i]=col[i]-col1[i];
  col[i]-=col1[i];
  setpalette(i+1,col1[i]);
  i++;
  i%=3;
  delay(100);
 }
 getch();*/
 setallpalette(getdefaultpalette());
 setbkcolor(LIGHTCYAN);
 Block(200,220,450,260,0,0);
 FONT=8;
 RunTitle("GUIDED BY",3,250,230,col[1],0);
 FONT=6;
 RunTitle("MR.MAHESH S .BE.MS",2,270,280,col[2],0);
  while(!kbhit())
 {
  setpalette(col[i%3],col[i%3]+1);
  i++;
  i%=256;
  delay(100);
 }
```

```
void main()
{
 int gd=DETECT,gm=DETECT;
 initgraph(&gd,&gm,"");
 EcgTitle();
 closegraph();
}
```

```
class Scale
{
 int cx;
 int cy;
 int xsize,ysize;
 int xlow, xhigh, xnum;
 float xincr;
 int ylow, yhigh, ynum;
 float yincr;
 float xratio,yratio;
 char *hmess;
 char *vmess;
 public:
  Scale();
  Scale(int x,int y);
  void HSet(int low,int high,int num,int s,char *m);
  void VSet(int low,int high,int num,int s,char *m);
  void HScale();
  void VScale();
  void Screen();
  void Draw(int n,int *a,int col);
  void Draw(int n,int *a,int col,int m,int dt);
  inline void Plot(int x,int y,int col);
  inline void Plot(int x,int y,int col,int n);
  void RunPort(int port,char *fname,int n);
};
  Scale::Scale()
  {
   cx=100;
   cy=400;
  }
  Scale::Scale(int x,int y)
  {
   cx=x;
   cy=y;
  }
  void Scale::HSet(int low,int high,int num,int s,char *m)
  {
   xlow=low;
   xhigh=high;
   xnum=num;
   hmess=m;
   xsize=s;
   xratio=(float)(xnum*xsize)/(xhigh-xlow);
  }

  void Scale::VSet(int low,int high,int num,int s,char *m)
  {
   ylow=low;
   yhigh=high;
   ynum=num;
   vmess=m;
   ysize=s;
   yratio=(float)(ynum*ysize)/(yhigh-ylow);
```

```
void Scale::HScale()
{
 int i;
 char s[4];
 xincr=(float)(xhigh-xlow)/xnum;
 settextstyle(DEFAULT_FONT,HORIZ_DIR,1);
 line(cx,cy,cx+xnum*xsize,cy);
 for(i=0;i<=xnum;i++)
 {
   sprintf(s,"%d",(int)(xlow+i*xincr));
   outtextxy(cx+xsize*i,cy+5,s);
   line(cx+xsize*i,cy,cx+xsize*i,cy+3);
 }
 outtextxy(cx+xsize*xnum/2,cy+30,hmess);
}


void Scale::VScale()
{
 int i;
 char s[4];
 yincr=(float)(yhigh-ylow)/ynum;
 settextstyle(DEFAULT_FONT,HORIZ_DIR,1);
 line(cx,cy,cx,cy-ynum*ysize);
 for(i=0;i<=ynum;i++)
  {
   sprintf(s,"%d",(int)(ylow+i*yincr));
   outtextxy(cx-30,cy-ysize*i,s);
   line(cx,cy-ysize*i,cx-3,cy-ysize*i);
  }
  settextstyle(DEFAULT_FONT,VERT_DIR,1);
  outtextxy(cx-50,cy-ysize*ynum,vmess);
}

void Scale::Screen()
{
 HScale();
 VScale();
 }

inline void Scale::Plot(int x,int y,int col)
{
 setcolor(col);
 lineto(cx+(int)(x-xlow)*xratio,cy-(int)(y-ylow)*yratio);
}

inline void Scale::Plot(int x,int y,int col,int n)
{
 if(n)
 putpixel(cx+(int)(x-xlow)*xratio,cy-(int)(y-ylow)*yratio,col);
 moveto(cx+(int)(x-xlow)*xratio,cy-(int)(y-ylow)*yratio);
}
```

```
{
 int i;
 setcolor(col);
 moveto(cx+(int)(a[0]-xlow)*xratio,cy-(int)(a[1]-ylow)*yratio);
 for(i=1;i<n;i++)
  lineto(cx+(int)(a[i*2]-xlow)*xratio,cy-(int)(a[i*2+1]-ylow)*yratio
}

void Scale::Draw(int n,int *a,int col,int m,int dt)
{
 int i;
 int *b;
 int start=0;
 b=(int *) malloc(n*2*sizeof(int));
 b[0]=a[0]-xlow;
 b[1]=a[1]-ylow;
 for(i=1;i<n;i++)
 {
  b[i*2]=a[i*2]-a[(i-1)*2];
  b[i*2+1]=a[i*2+1]-a[i*2-1];
 }
 setcolor(col);
 setwritemode(XOR_PUT);
 int s;
 while(!bioskey(1))
 {
 moveto(cx+(int)(b[(start%n)*2])*xratio,
        cy+(int)(a[(start%n)*2+1]-ylow)*yratio);
 for(i=1;i<m;i++)
  linerel(b[((start+i)%n)*2],b[((start+i)%n)*2+1]);
  delay(dt);
 moveto(cx+(int)(b[(start%n)*2])*xratio,
        cy+(int)(a[(start%n)*2+1]-ylow)*yratio);
 for(i=1;i<m;i++)
   linerel(b[((start+i)%n)*2],b[((start+i)%n)*2+1]);
 start++;
 start%=n;
 }
   if(start) start--;
     else start=n-1;
   setwritemode COPY_PUT);
 moveto(cx+(int)(b[(start%n)*2])*xratio,
        cy+(int)(a[(start%n)*2+1]-ylow)*yratio);
 for(i=1;i<m;i++)
   linerel(b[((start+i)%n)*2],b[((start+i)%n)*2+1]);
 getch();
}
```

```
#include<dos.h>
#include<conio.h>
#include<iostream.h>

inline void WriteByte(int port,unsigned char byte)
{
 outportb(port,byte);
}

inline unsigned char ReadByte(int port)
{
 return(inportb(port));
}

inline void WriteWord(int port,int byte)
{
 outport(port,byte);
}

inline int ReadWord(int port)
{
 return(inport(port));
}

void GetData(int port,int n,int *data)
{
 for(int i=0;i<n;i++)
  data[i]=ReadByte(port);
}

void StoreData(int *a,int num,int port)
{
 GetData(0x0380,100,a);
}
```

```
nclude<iostream.h>
nclude<graphics.h>
nclude<alloc.h>
nclude<dos.h>
nclude<bios.h>
nclude<conio.h>
nclude<process.h>
nclude<stdio.h>
nclude<math.h>

oid StartGraph()

int gd=DETECT,gm=DETECT.ecode:
initgraph(&gd,&gm,"");
ecode=graphresult();
if(ecode!=grOk)
{
 cout<<"Graphics Error : %s",grapherrormsg(ecode);
 getch();
 exit(1);
}
}
int GetData(char *fname,int *a)
{
 FILE *in;
 int n,i;
 in=fopen(fname,"r");
 fscanf(in,"%d",&n);
 for(i=0;i<n;i++)
   fscanf(in,"%d",&(a[i]));
 fclose(in);
 return(n);
}

#incluce "graph.h"

 void StoEcgWave()
 {
  int a[800],i,x,y,b[200],n;
  setcolor(GREEN);
  settextstyle(TRIPLEX_FONT,HORIZ_DIR,2);
  outtextxy(100,100,"ECG STANDARED WAVEFORM");
  Scale s(100,290);
  s.HSet(100,400,10,30,"TIME");
  s.VSet(200,400,12,15,"AMPLITUDE");
  setcolor(8);
  rectangle(90,150,520,370);
  setfillstyle(SOLID_FILL,8);
  floodfill(91,151,8);
  n=GetData("ecgstd.dat",b);
  for(i=0;i<300;i+=2)
  {
```

```
 s.Draw(n,a,GREEN,2*n,20);
 getch();
}

void EcgWave(int *a,int n)
{
 int i,x,y,b[200];
 setcolor(GREEN);
 settextstyle(TRIPLEX_FONT,HORIZ_DIR,2);
 outtextxy(100,100,"ANLYSIS ECG WAVEFORM ");
 Scale s(100,290);
 s.HSet(100,400,10,30,"TIME");
 s.VSet(200,400,12,15,"AMPLITUDE");
 setcolor(8);
 rectangle(90,150,520,370);
 setfillstyle(SOLID_FILL,8);
 floodfill(91,151,8);
 s.Draw(n,a,GREEN,2*n,20);
 getch();
 }
```

CHAPTER 8

CONCLUSION

A software has been developed in c++ language for data acquisition and analysis of ECG waveform using a PC. The ECG Waveform is analysed according to the designs in this project using software and hardware.

Since the ECG waveform obtained from each patient differs, the accuracy of the analysis is precise. The A/D converter used in this project samples at the rate of 1000 to 10,000 samples per second. The accuracy can be increased by increasing the sampling rate.

Further Developments in the project can be done using Expert system and Neural Networks. An example for the Expert system in Medical application is mycin. Cable transmission of ECG signals for recording and analysis is possible.

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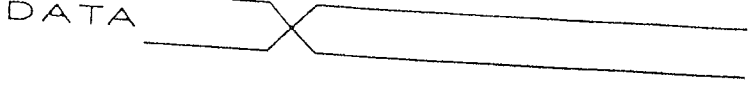
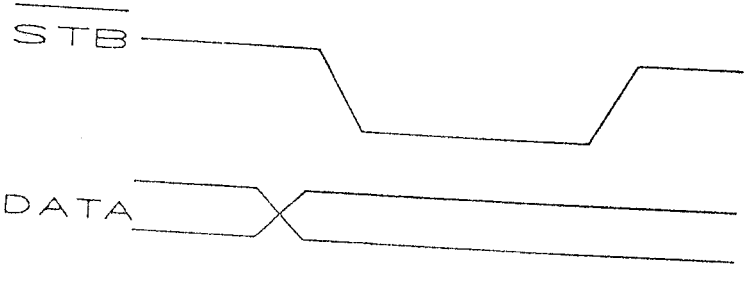
7.TEXAS INSTRUMENTS,LINEAR I.C. APPLICATION DATA MANUAL,1988.

8.TEXAS INSTRUMENT,TTL I.C. DATA MANUAL,1988.



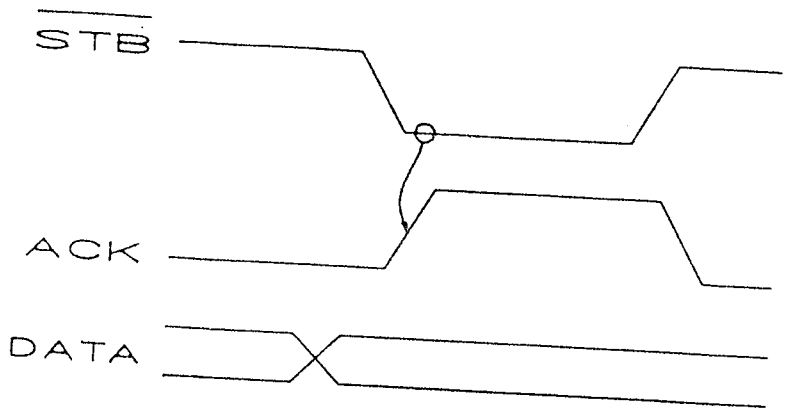
(a) SIMPLE OUTPUT

FIG(2.1.1)



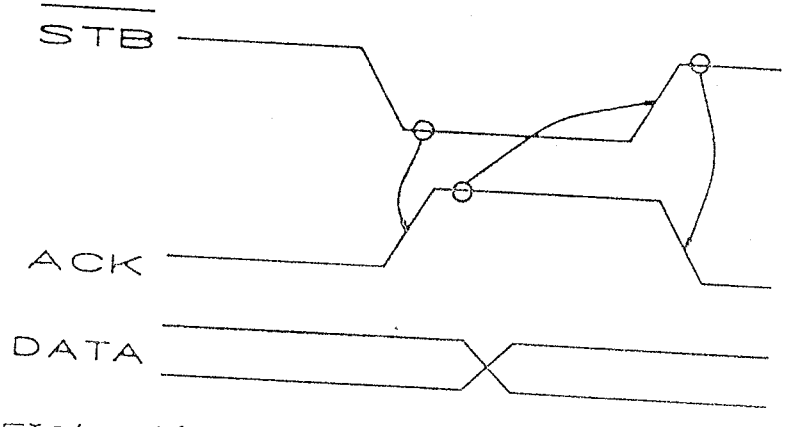
(b) SIMPLE STROBE I/O

FIG(2.1.2)



(c) SINGLE HANDSHAKE I/O

FIG(2.1.3)



FIG( )(d) DOUBLE HANDSHAKE I/O

PARALLEL DATA TRANSFER

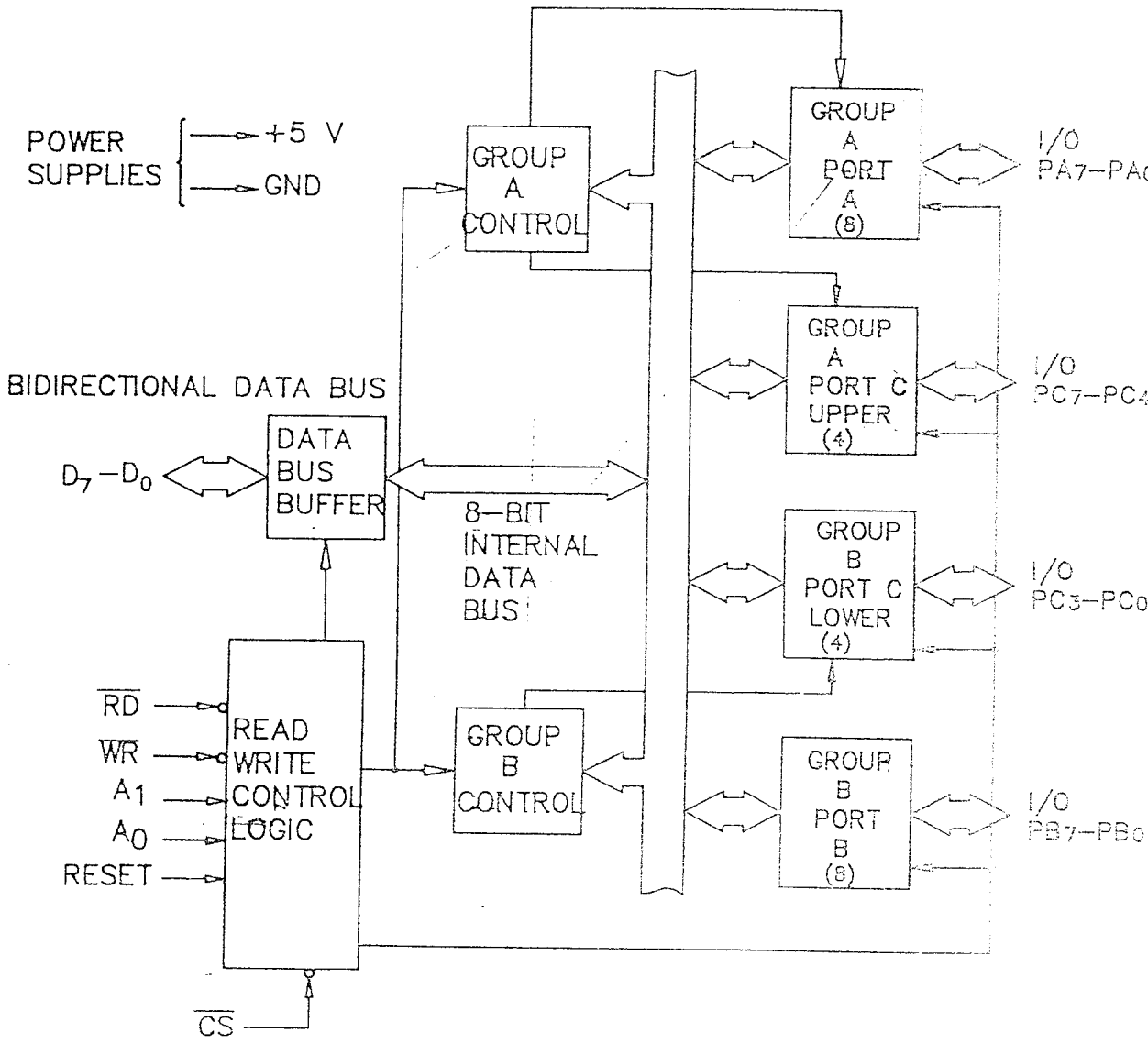
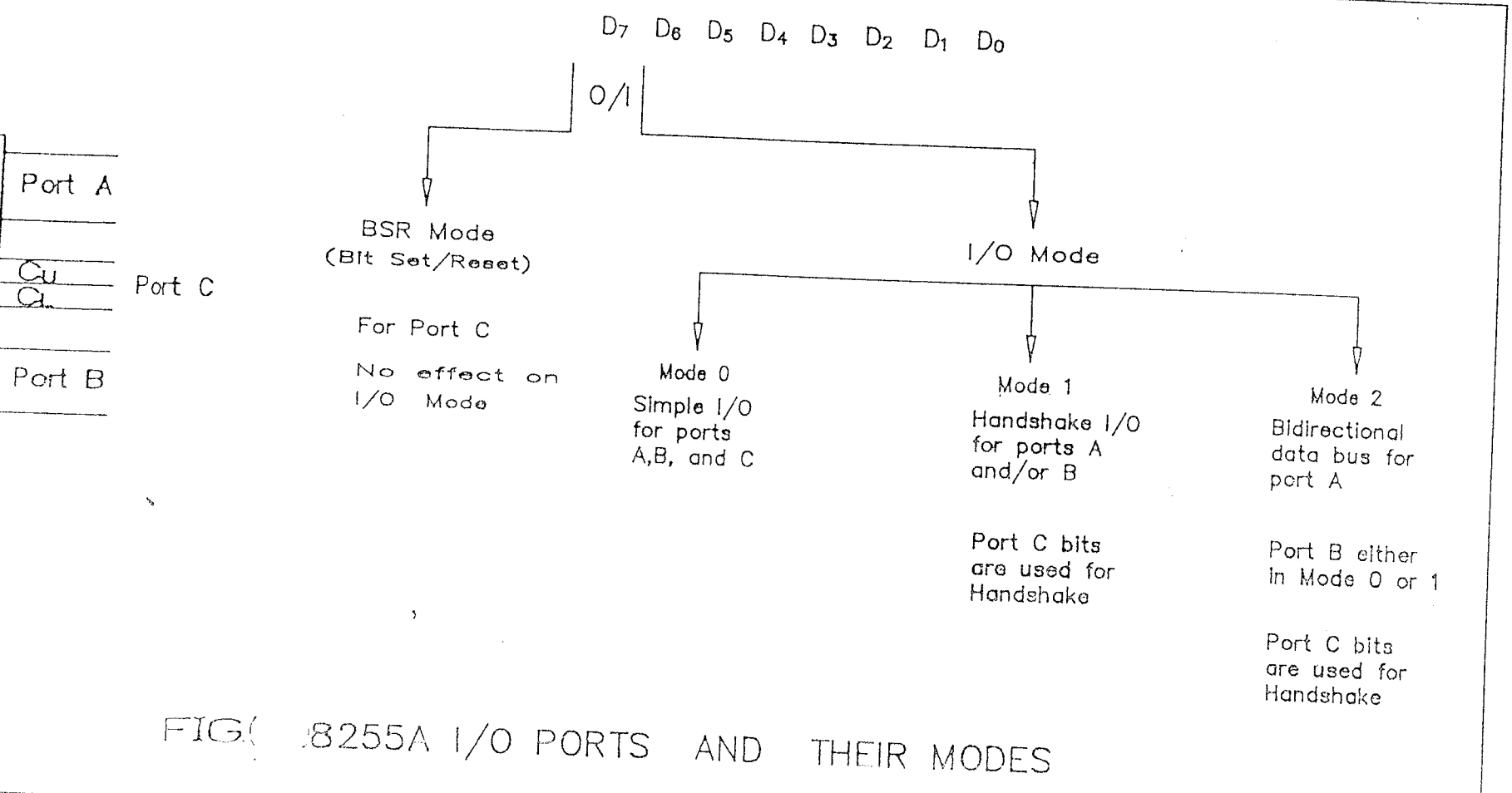


FIG.( ) BLOCK DIAGRAM OF 8255A AND EXPANDED VERSION OF THE CONTROL LOGIC



FIG(8255A I/O PORTS AND THEIR MODES

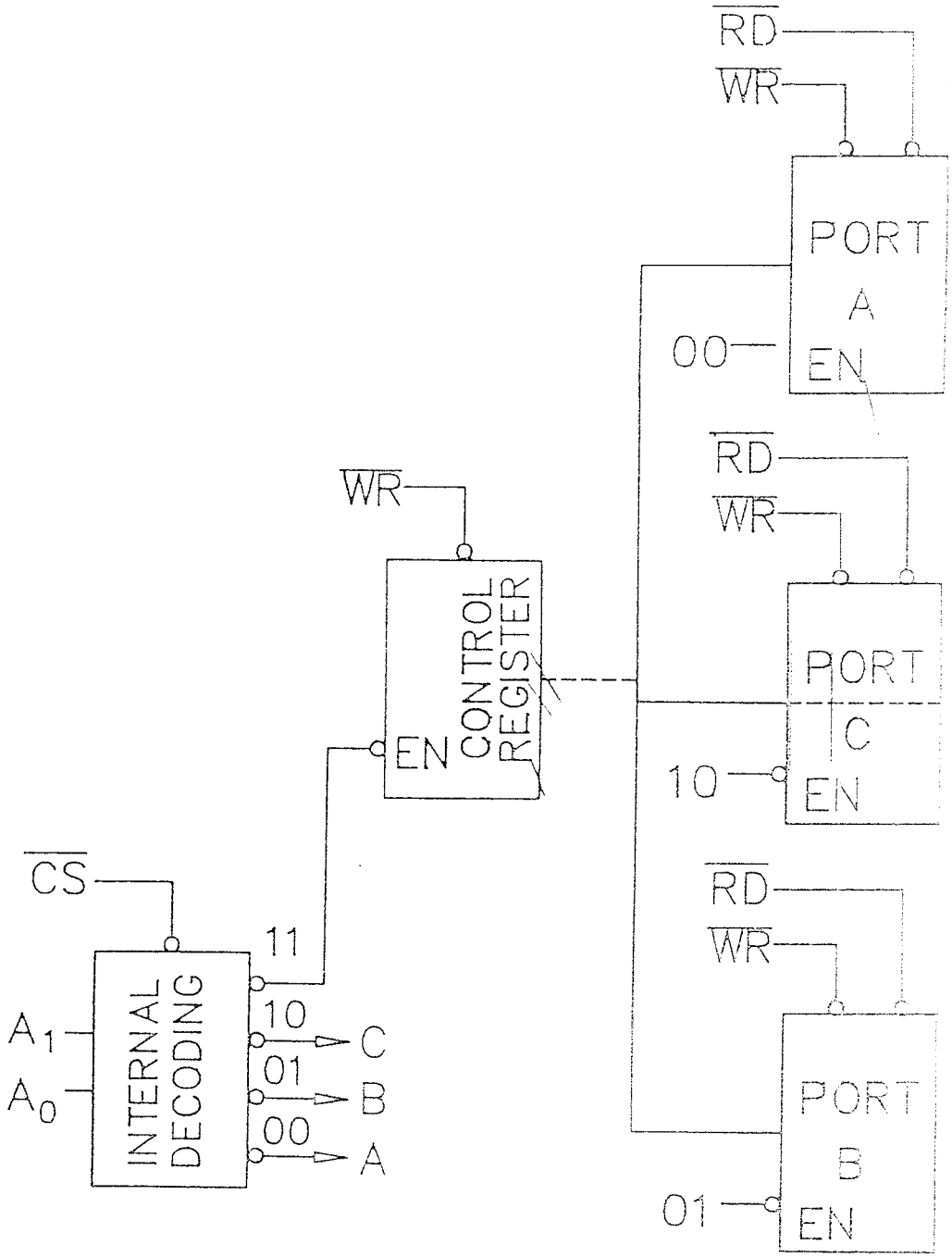


FIG.( ) I/O PORTS OF 8255A

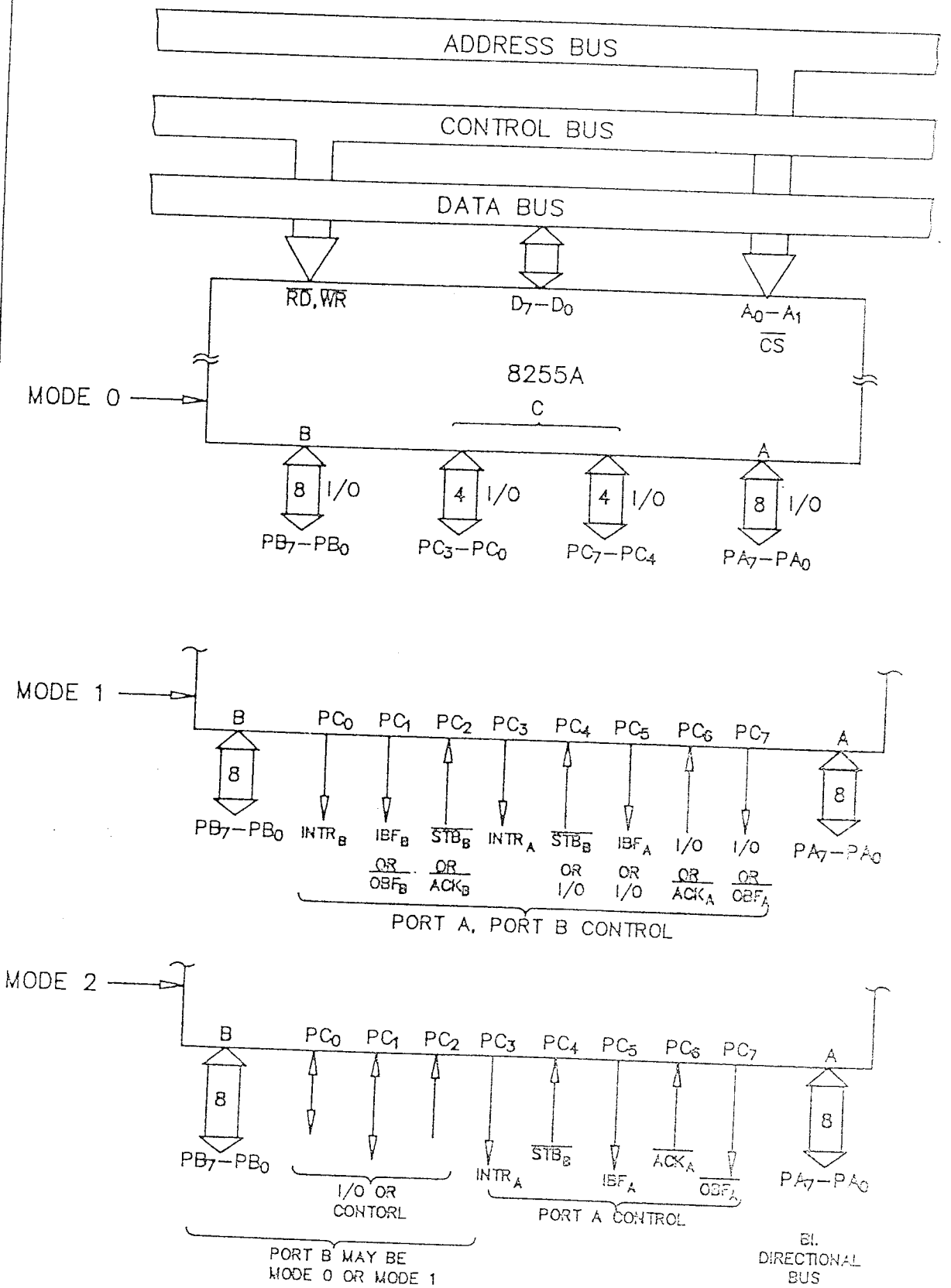
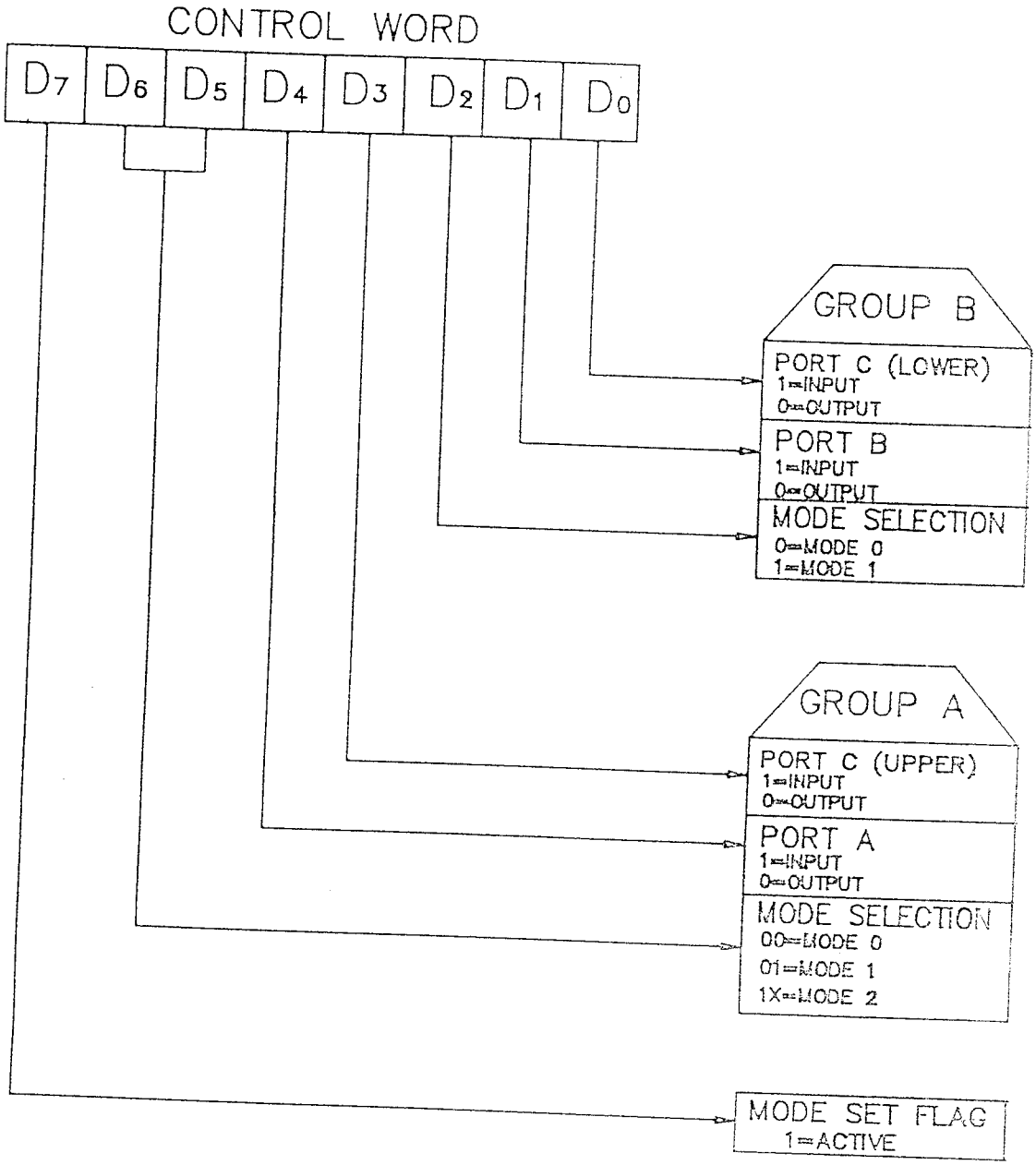


FIG ( ) SUMMARY OF 8255A OP

FIG ( ) 8255A CONTROL WORD FORMATS



(a) MODE SET CONTROL WORD

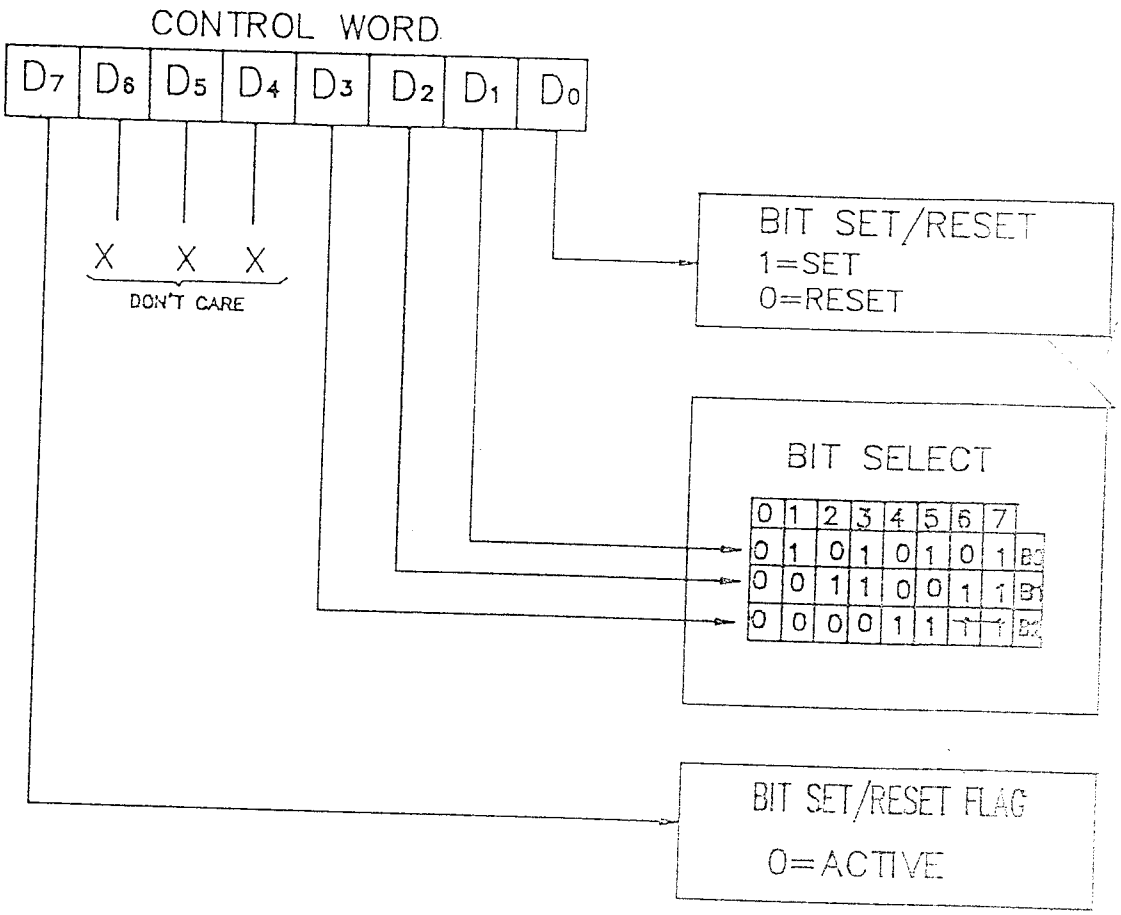
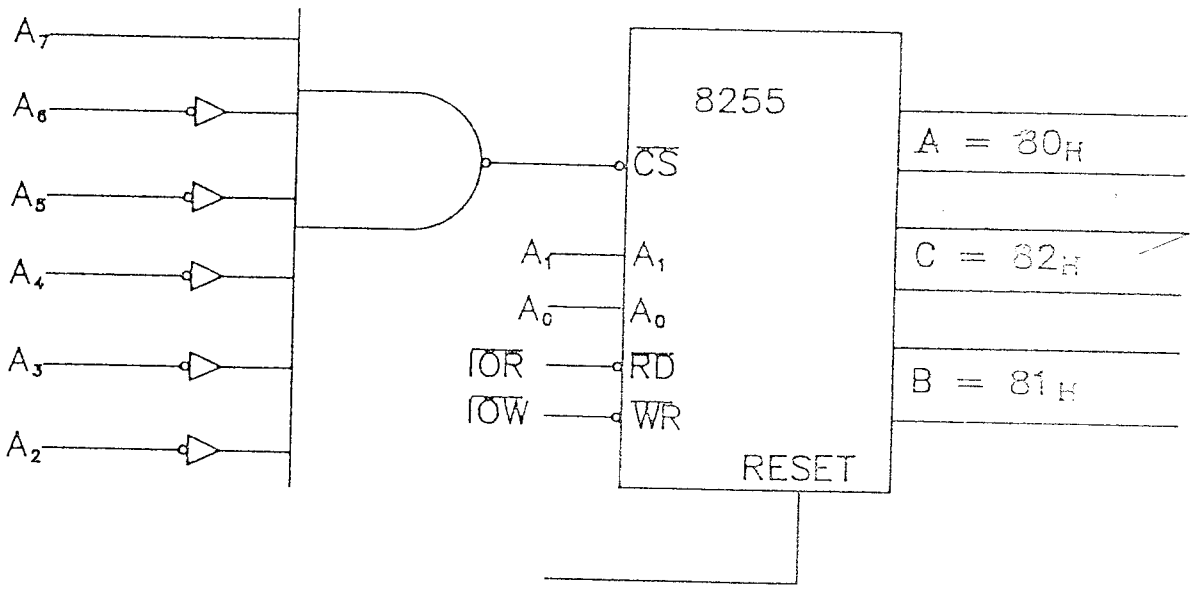


FIG (. .) 8255A CONTROL WORD FORMATS

(b) PORT C BIT SET/RESET CONTROL WORD

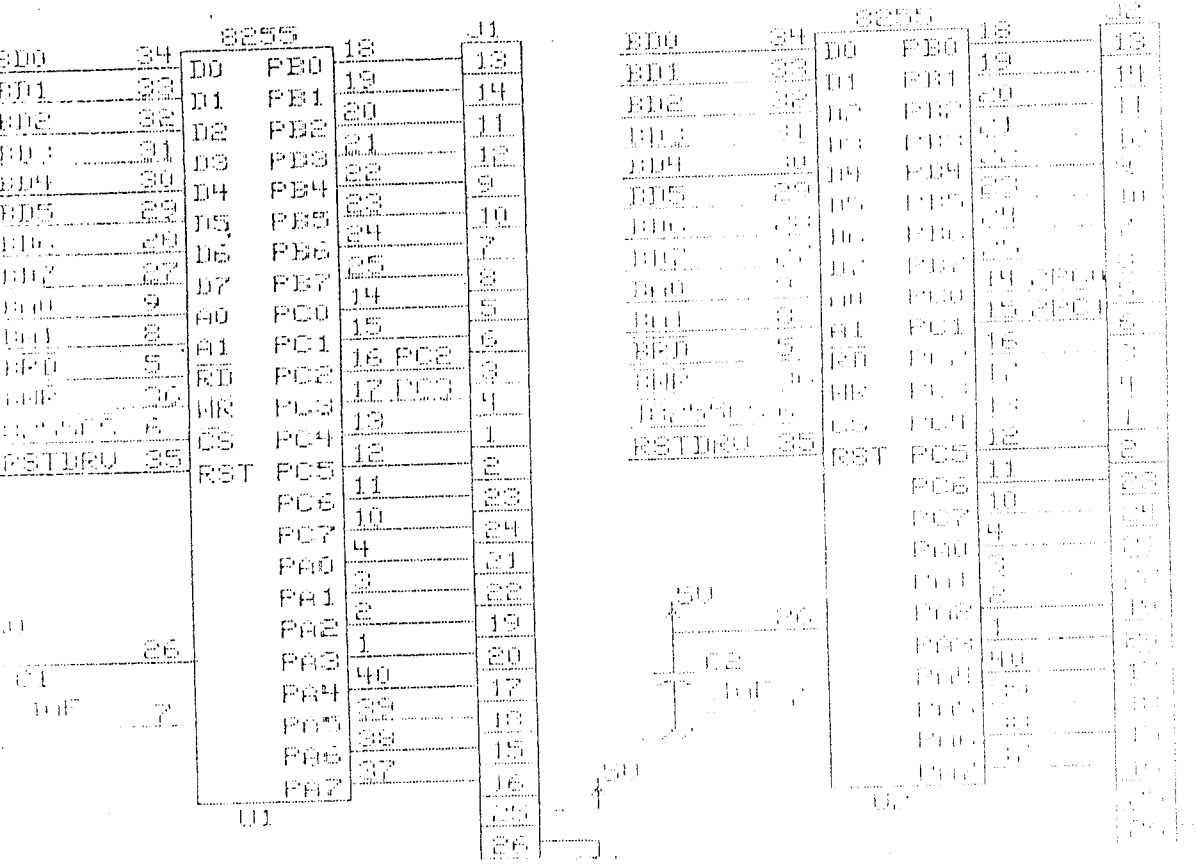


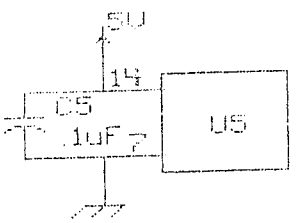
(a)

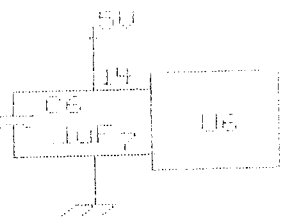
$\overline{CS}$			HEX ADDRESS	PORT
A7 A6 A5 A4 A3 A2	A_1	A_0		
1 0 0 0 0 0	0	0	= 80_H	A
	0	1	= 81_H	B
	1	0	= 82_H	C
	1	1	= 83_H	CONTROL REGISTER

(b)

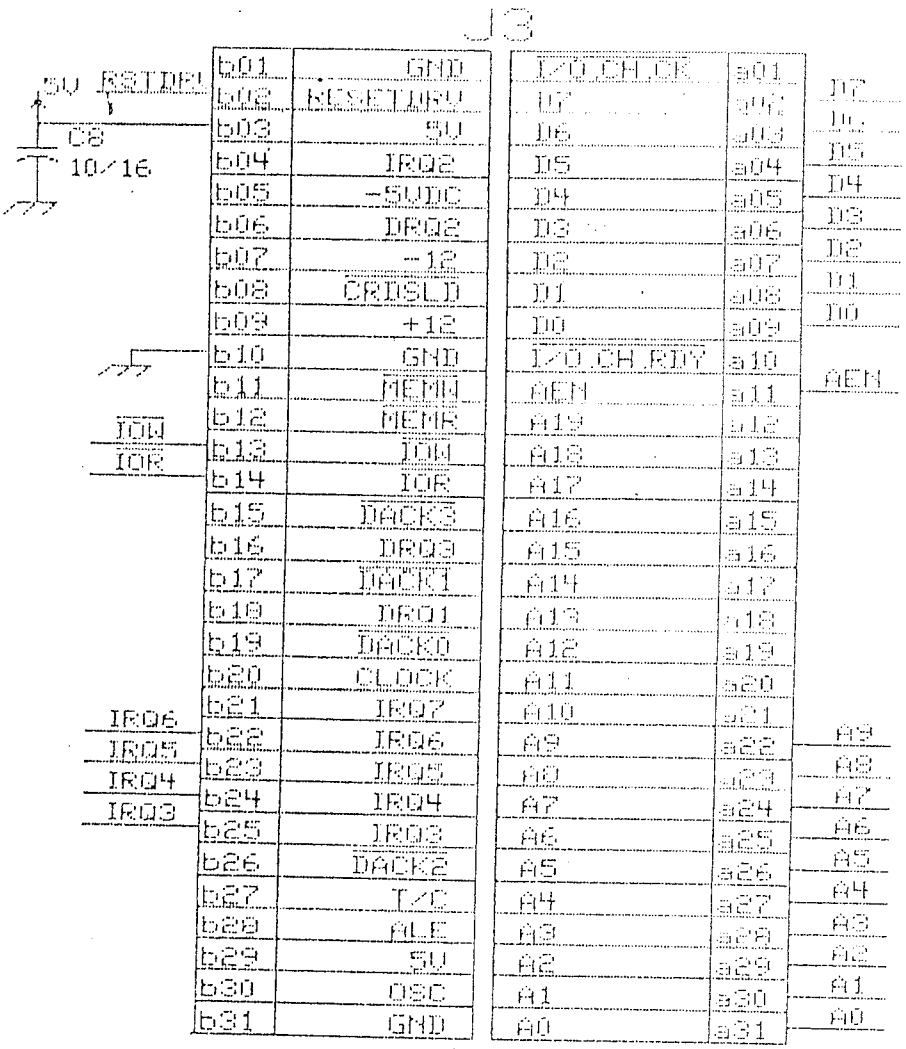
FIG.( ) 8255A CHIP SELECT LOGIC (a) and I/O PORT ADDRESS (b)

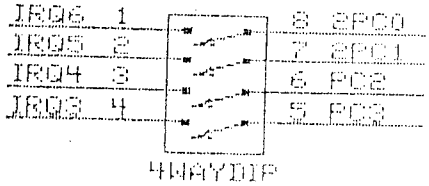




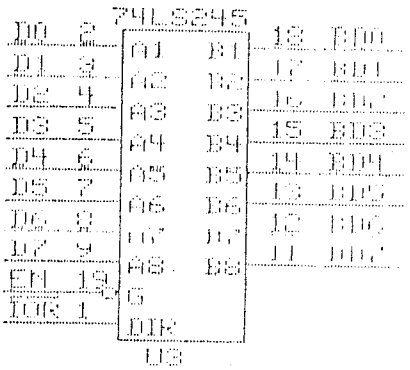


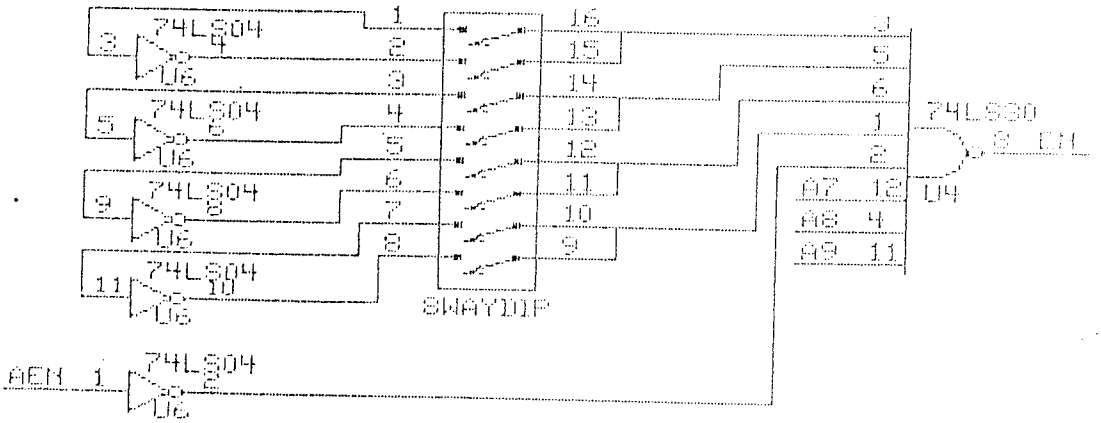
DRAWN:	SMMC	APPVD:
		SHEET: 3 OF 3

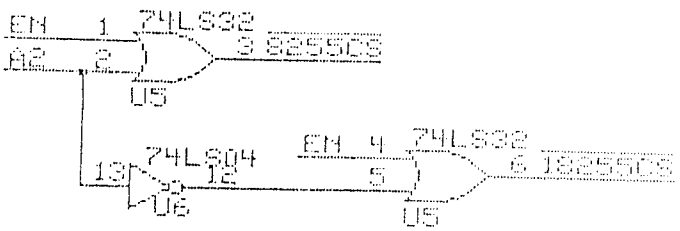


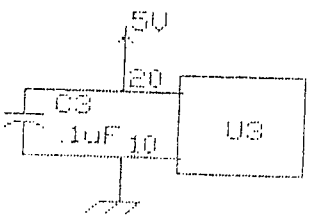


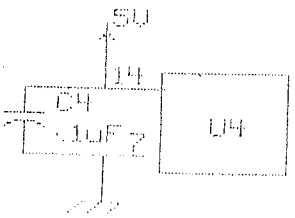
48 BIT CARD FOR IBM PC











48 DIO CHKU FOR IBM PC

DRAWN: SMMK

SN54132, SN54LS132, SN54S132, SN74132, SN74LS132, SN74S132
QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

DECEMBER 1983 · REVISED MARCH 1988

- Operation from Very Slow Edges
- Improved Line-Receiving Characteristics
- High Noise Immunity

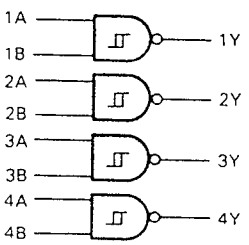
cription

Each circuit functions as a 2-input NAND gate, but because of the Schmitt action, it has different input threshold levels for positive (V_{T+}) and for negative going (V_{T-}) signals.

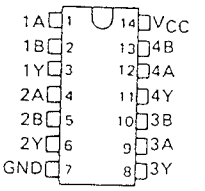
These circuits are temperature-compensated and can be triggered from the slowest of input ramps and still give clear, jitter-free output signals.

The SN54132, SN54LS132, and SN54S132 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74132, SN74LS132, and SN74S132 are characterized for operation from 0°C to 70°C.

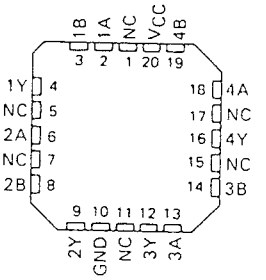
diagram (positive logic)



SN54132, SN54LS132, SN54S132 . . . J OR W PACKAGE
SN74132 . . . N PACKAGE
SN74LS132, SN74S132 . . . D OR N PACKAGE
(TOP VIEW)

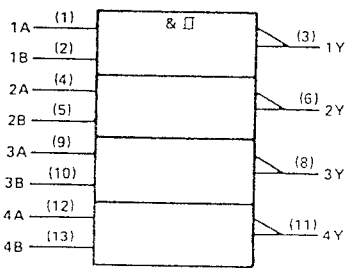


SN54LS132, SN54S132 . . . FK PACKAGE
(TOP VIEW)



NC–No internal connection

logic symbol†



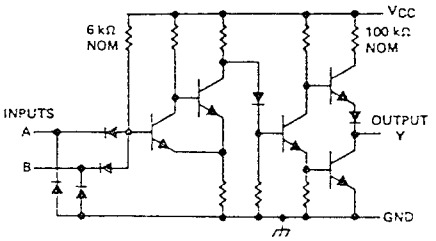
positive logic: $Y = \overline{AB}$ or $Y = \overline{A} + \overline{B}$

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

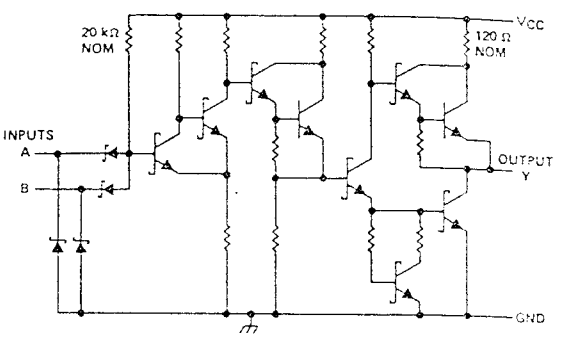
Pin numbers shown are for D, J, N, and W packages.

schematics

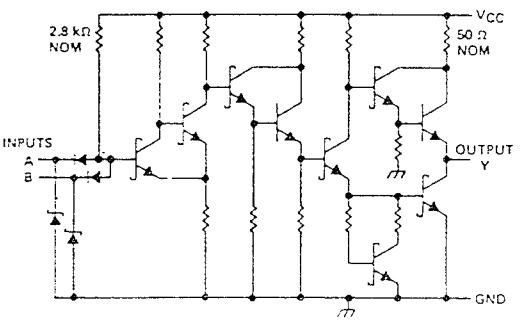
'132 CIRCUITS



'LS132 CIRCUITS



'S132 CIRCUITS



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '132, 'S132 . . . . . 5.5 V
'LS132 . . . . . 7 V
Operating free-air temperature: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltages values are with respect to network ground terminal.

recommended operating conditions

		SN54132			SN74132			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−0.8			−0.8	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{T+}	V_{CC} = 5 V			1.5	1.7	2	V
V_{T-}	V_{CC} = 5 V			0.6	0.9	1.1	V
V_{hys} ($V_{T+} - V_{T-}$)	V_{CC} = 5 V			0.4	0.8		V
V_{IK}	V_{CC} = MIN,	I_I = −12 mA				−1.5	V
V_{OH}	V_{CC} = MIN,	V_I = 0.6 V,	I_{OH} = −0.8 mA	2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_I = 2 V,	I_{OL} = 16 mA		0.2	0.4	V
I_{T+}	V_{CC} = 5 V,	V_I = V_{T+}			−0.43		mA
I_{T-}	V_{CC} = 5 V,	V_I = V_{T-}			−0.56		mA
I_I	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V				40	μA
I_{IL}	V_{CC} = MAX,	V_{IL} = 0.4 V			−0.8	−1.2	mA
I_{OS}§	V_{CC} = MAX			−18		−55	mA
I_{CCH}	V_{CC} = MAX				15	24	mA
I_{CCL}	V_{CC} = MAX				26	40	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	R_L = 400 Ω, C_L = 15 pF		15	22	ns
t_{PHL}					15	22	ns

recommended operating conditions

	SN54LS132			SN74LS132			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS132			SN74LS132			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	V_{CC} = 5 V		1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	V_{CC} = 5 V		0.5	0.8	1	0.5	0.8	1	V
V_{hys} ($V_{T+} - V_{T-}$)	V_{CC} = 5 V		0.4	0.8		0.4	0.8		V
V_{IK}	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_I = 0.5 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_I = 1.9 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_{T+}	V_{CC} = 5 V, V_I = V_{T+}			−0.14			−0.14		mA
I_{T-}	V_{CC} = 5 V, V_I = V_{T-}			−0.18			−0.18		mA
I_I	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX, V_{IL} = 0.4 V				−0.4			−0.4	mA
I_{OS} §	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX			5.9	11		5.9	11	mA
I_{CCL}	V_{CC} = MAX			8.2	14		8.2	14	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	R_L = 2 kΩ, C_L = 15 pF		15	22	ns
t_{PHL}					15	22	ns

recommended operating conditions

		SN54S132			SN74S132			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

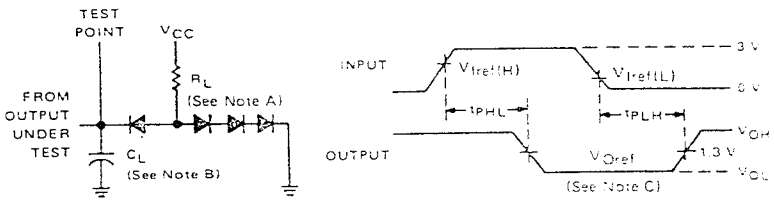
PARAMETER	TEST CONDITIONS†			SN54S132			SN74S132			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	V_{CC} = 5 V			1.6	1.77	1.9	1.6	1.77	1.9	V
V_{T-}	V_{CC} = 5 V			1.1	1.22	1.4	1.1	1.22	1.4	V
V_{hys} ($V_{T+} - V_{T-}$)	V_{CC} = 5 V			0.2	0.55		0.2	0.55		V
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	V_I = 1.1 V,	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_I = 1.9 V,	I_{OL} = 20 mA			0.5			0.5	V
I_{T+}	V_{CC} = 5 V,	$V_I = V_{T+}$			−0.9			−0.9		mA
I_{T-}	V_{CC} = 5 V,	$V_I = V_{T-}$			−1.1			−1.1		mA
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				50			50	μA
I_{IL}	V_{CC} = MAX,	V_{IL} = 0.5 V				−2			−2	mA
I_{OS}§	V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX				28	44		28	44	mA
I_{CCL}	V_{CC} = MAX				44	68		44	68	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 280 Ω,	C_L = 15 pF		7	10.5	ns
t_{PHL}						8.5	13	ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS

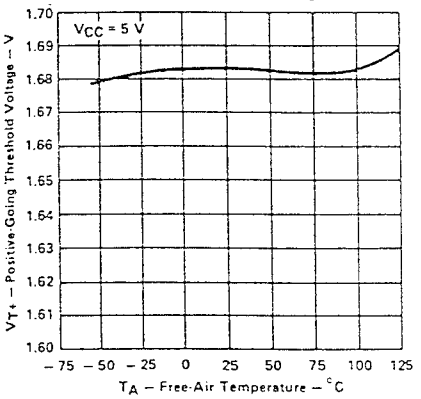
NOTES: A. All diodes are 1N3064 or equivalent.
B. C_L includes probe and jig capacitance.
C. Generator characteristics and reference voltages are:

	Generator Characteristics				Reference Voltages		
	Z_{out}	PRR	t_r	t_f	$V_{I ref(H)}$	$V_{I ref(L)}$	$V_{O ref}$
SN54'/SN74'	50	1 MHz	10 ns	10 ns	1.7 V	0.9 V	1.5 V
SN54LS'/SN74LS'	50	1 MHz	15 ns	6 ns	1.6 V	0.8 V	1.3 V
'S132	50	1 MHz	2.5 ns	2.5 ns	1.6 V	1.2 V	1.5 V

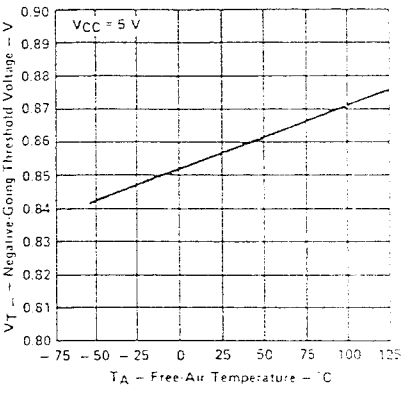
FIGURE 1

TYPICAL CHARACTERISTICS OF '132 CIRCUITS

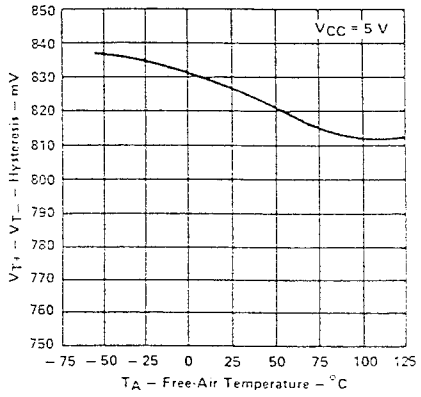
POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



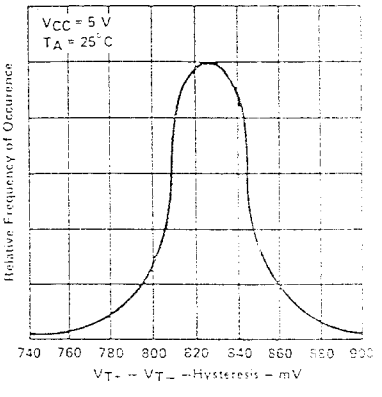
NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



HYSTERESIS
vs
FREE-AIR TEMPERATURE

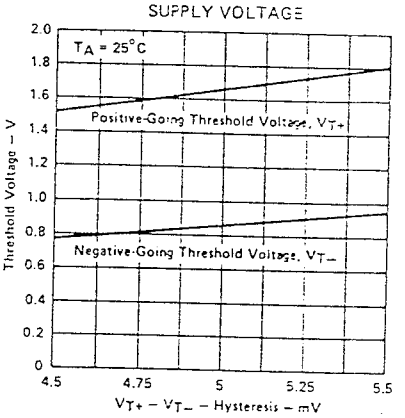


DISTRIBUTION OF UNITS
FOR HYSTERESIS

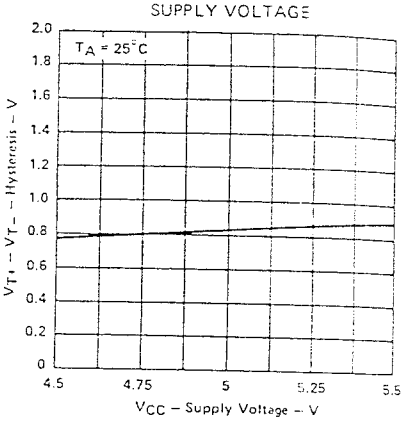


TYPICAL CHARACTERISTICS OF '132 CIRCUITS

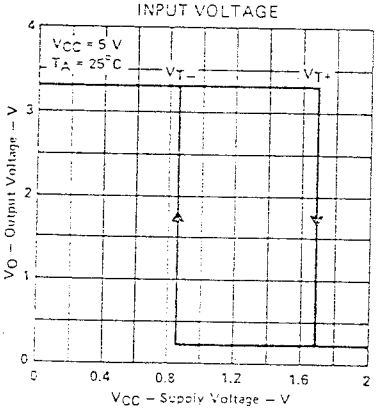
THRESHOLD VOLTAGES
vs
SUPPLY VOLTAGE



HYSTERESIS
vs
SUPPLY VOLTAGE

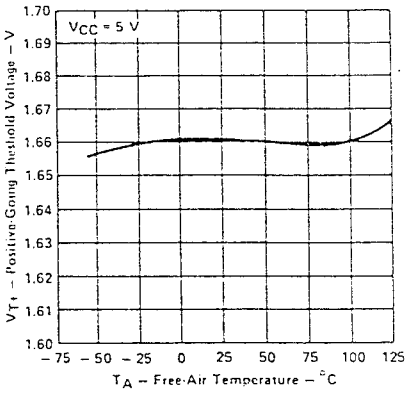


OUTPUT VOLTAGE
vs
INPUT VOLTAGE

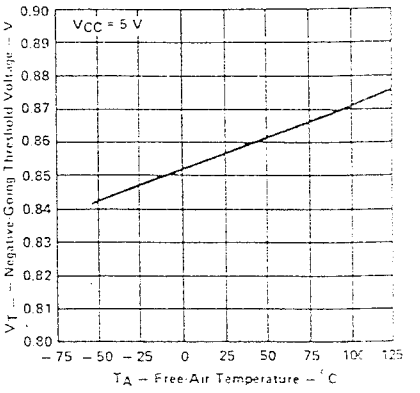


TYPICAL CHARACTERISTICS OF 'LS132 CIRCUITS

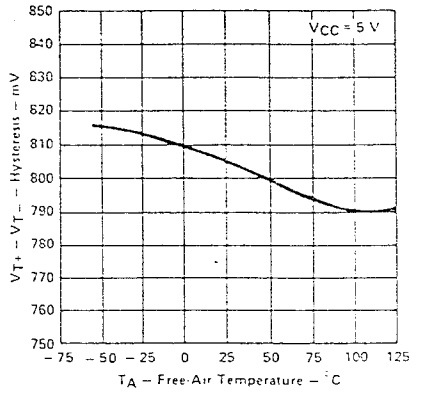
POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



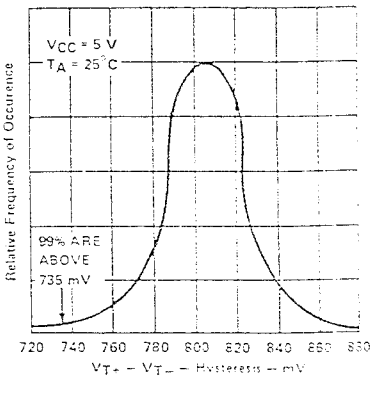
NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



HYSTERESIS
vs
FREE-AIR TEMPERATURE

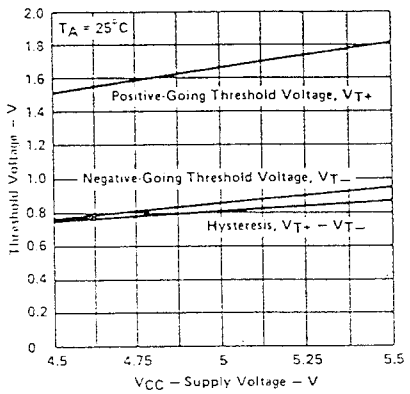


DISTRIBUTION OF UNITS
FOR HYSTERESIS

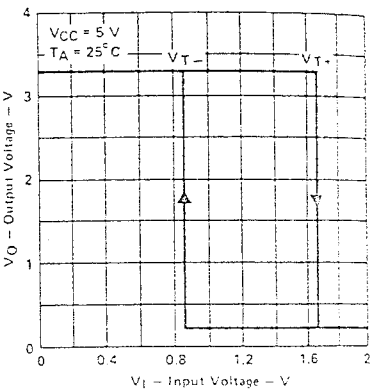


TYPICAL CHARACTERISTICS OF 'LS132 CIRCUITS

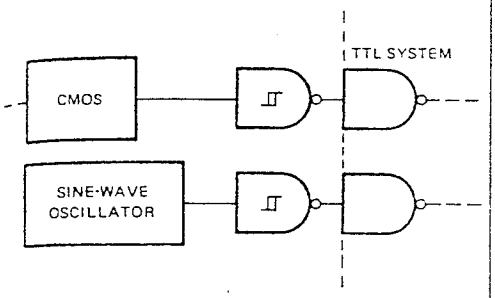
THRESHOLD VOLTAGES AND HYSTERESIS
vs
SUPPLY VOLTAGE



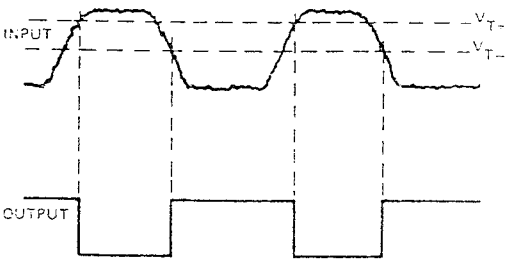
OUTPUT VOLTAGE
vs
INPUT VOLTAGE



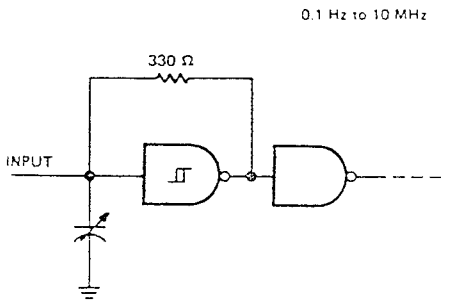
TYPICAL APPLICATION DATA



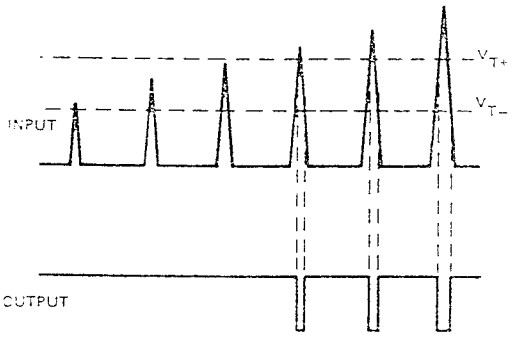
TTL SYSTEM INTERFACE
FOR SLOW INPUT WAVEFORMS



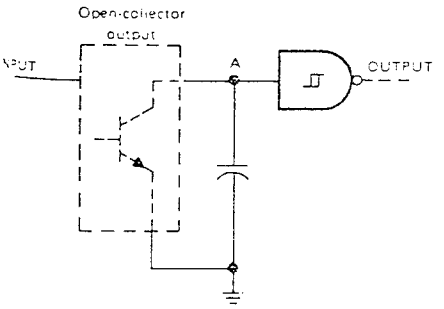
PULSE SHAPER

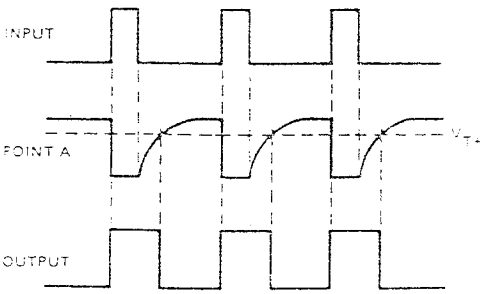


MULTIVIBRATOR



THRESHOLD DETECTOR





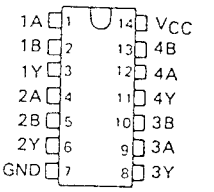
PULSE STRETCHER

SN5426, SN54LS26, SN7426, SN74LS26
QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

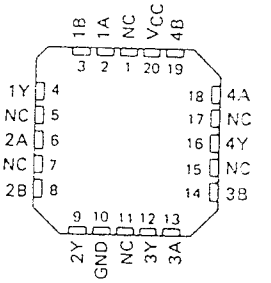
DECEMBER 1983 - REVISED MARCH 1988

- For Driving Low-Threshold-Voltage MOS Inputs

SN5426 . . . J PACKAGE
SN54LS26 . . . J OR W PACKAGE
SN7426 . . . N PACKAGE
SN74LS26 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS26 . . . FK PACKAGE
(TOP VIEW)



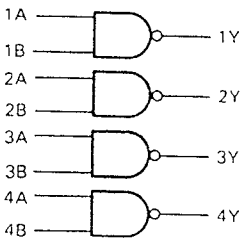
NC - No internal connection

description

These 2-input open-collector NAND gates feature high-output voltage ratings for interfacing with low-threshold-voltage MOS logic circuits or other 12-volt systems. Although the output is rated to withstand 15 volts, the V_{CC} terminal is connected to the standard 5-volt source.

The SN5426 and SN54LS26 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7426 and SN74LS26 are characterized for operation from 0°C to 70°C.

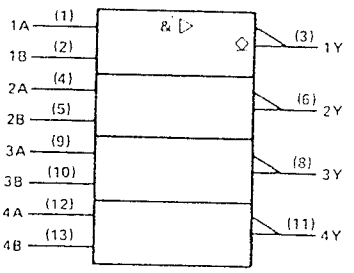
logic diagram



positive logic

$$Y = \overline{AB}$$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

recommended operating conditions

		SN5426			SN7426			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			15			15	V
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5426			SN7426			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 12 V						50	μA
	V_{CC} = MIN, V_{IL} = 0.7 V, V_{OH} = 12 V			50				
	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 15 V						1	mA
	V_{CC} = MIN, V_{IL} = 0.7 V, V_{OH} = 15 V			1				
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA			0.4			0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{CCH}	V_{CC} = MAX, V_I = 0		4	8		4	8	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5 V		12	22		12	22	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 1 kΩ, C_L = 15 pF		16	24	ns
t_{PHL}					11	17	ns

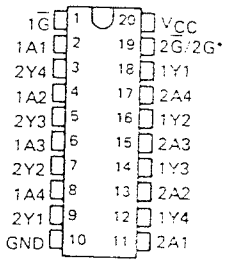
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S
SN74LS240, SN74LS241, SN74LS244, SN74S240; SN74S241, SN74S
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTP

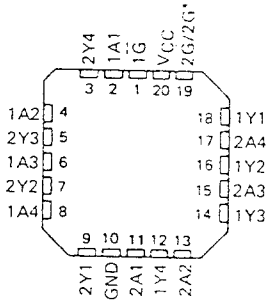
APRIL 1985 – REVISED MARC

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins

SN54LS', SN54S' . . . J OR W PACKAGE
SN74LS', SN74S' . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS', SN54S' . . . FK PACKAGE
(TOP VIEW)



*2G for 'LS241 and 'S241 or 2G̅ for all other drivers.

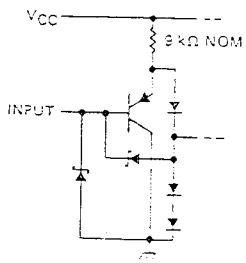
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical G̅ (active-low output control) inputs, and complementary G and G̅ inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise-margin. The SN74LS' and SN74S' can be used to drive terminated lines down to 133 ohms.

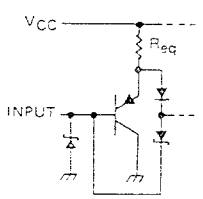
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

'LS240, 'LS241, 'LS244
EQUIVALENT OF EACH INPUT

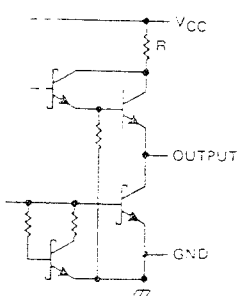


'S240, 'S241, 'S244
EQUIVALENT OF EACH INPUT



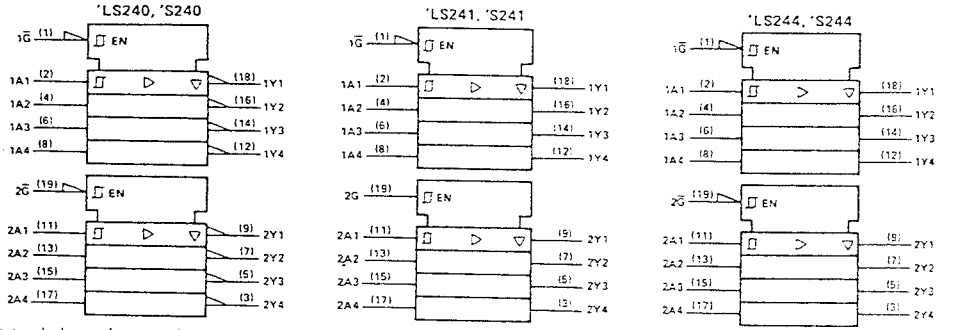
G and G̅ inputs: R_{eq} = 2 kΩ NOM
A inputs: R_{eq} = 2.8 kΩ NOM

TYPICAL OF ALL OUTPUTS



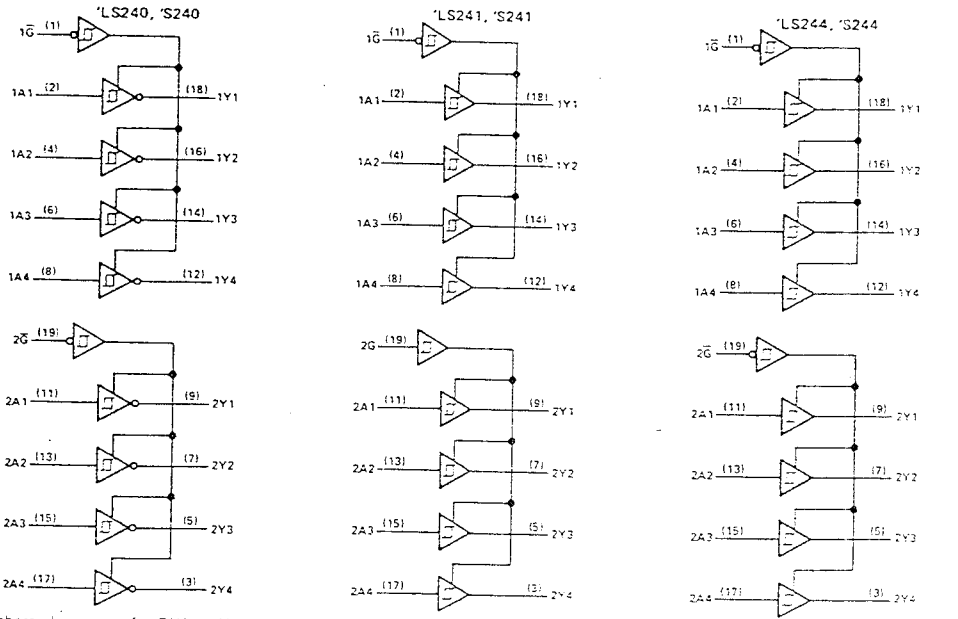
'LS240, 'LS241, 'LS244,
R = 60 Ω NOM
'S240, 'S241, 'S244
R = 25 Ω NOM

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



Pin numbers shown are for DW, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: 'LS Circuits . . . . . 7 V
'S Circuits . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS', SN54S' Circuits . . . . . −55°C to 125°C
SN74LS', SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA					−1.5			−1.5	V
Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN			0.2	0.4		0.2	0.4		V
V_{OH}		V_{CC} = MIN, I_{OH} = −3 mA	V_{IH} = 2 V,	V_{IL} = MAX,	2.4	3.4		2.4	3.4		V
		V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = 0.5 V,	2			2			
V_{OL}		V_{CC} = MIN, V_{IL} = MAX	V_{IH} = 2 V,	I_{OL} = 12 mA			0.4			0.4	V
				I_{OL} = 24 mA						0.5	
I_{OZH}		V_{CC} = MAX, V_{IL} = MAX	V_{IH} = 2 V,	V_O = 2.7 V			20			20	μA
I_{OZL}				V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}		V_{CC} = MAX,	V_{IL} = 0.4 V				−0.2			−0.2	mA
I_{OS}§		V_{CC} = MAX			−40		−225	−40		−225	mA
I_{CC}	Outputs high	V_{CC} = MAX, Output open		All		17	27		17	27	mA
	Outputs low			'LS240		26	44		26	44	
				'LS241, 'LS244		27	46		27	46	
	All outputs disabled			'LS240		29	50		29	50	
				'LS241, 'LS244		32	54		32	54	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		'LS240			'LS241, 'LS244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	R_L = 667 Ω, See Note 2	C_L = 45 pF,		9	14		12	18	ns
t_{PHL}				12	18		12	18	ns
t_{PZL}				20	30		20	30	ns
t_{PZH}				15	23		15	23	ns
t_{PLZ}	R_L = 667 Ω, See Note 2	C_L = 5 pF,		10	20		10	20	ns
t_{PHZ}				15	25		15	25	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

PARAMETER		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage, (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
	External resistance between any input and V_{CC} or ground			40			40	kΩ
T_A	Operating free-air temperature (see Note 3)	−55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
3. An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free-air $R_{\theta CA}$, of not more than 40°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54S'			SN74S'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA					−1.2			−1.2	V
Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN			0.2	0.4		0.2	0.4		V
V_{OH}		V_{CC} = MIN, I_{OH} = −1 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,				2.7			V
		V_{CC} = MIN, I_{OH} = −3 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.4		2.4	3.4		
		V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = 0.5 V,	2			2			
V_{OL}		V_{CC} = MIN, I_{OL} = MAX	V_{IH} = 2 V,	V_{IL} = 0.8 V,			0.55			0.55	V
I_{OZH}		V_{CC} = MAX, V_{IL} = 0.8 V,	V_{IH} = 2 V,	V_O = 2.4 V			50			50	μA
I_{OZL}				V_O = 0.5 V			−50			−50	
I_I		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V				50			50	μA
I_{IL}	Any A	V_{CC} = MAX,	V_I = 0.5 V				−400			−400	μA
	Any G						−2			−2	mA
I_{OS}§		V_{CC} = MAX			−50		−225	−50		−225	mA
I_{CC}	Outputs high	V_{CC} = MAX,	Outputs open	'S240		80	123		80	135	mA
				'S241, 'S244		95	147		95	160	
	Outputs low			'S240		100	145		100	150	
				'S241, 'S244		120	170		120	180	
	Outputs disabled			'S240		100	145		100	150	
				'S241, 'S244		120	170		120	180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175, SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

DECEMBER 1972—REVISED MARCH 1988

'174, 'LS174, 'S174 . . . HEX D-TYPE FLIP-FLOPS
'175, 'LS175, 'S175 . . . QUADRUPLE D-TYPE FLIP-FLOPS

- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- '175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

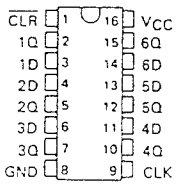
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

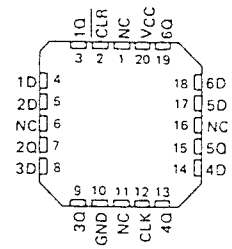
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
† = '175, 'LS175, and 'S175 only

TYPES	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'174, '175	35 MHz	38 mW
'LS174, 'LS175	40 MHz	14 mW
'S174, 'S175	110 MHz	75 mW

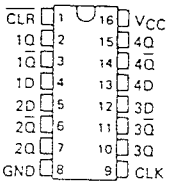
SN54174, SN54LS174, SN54S174 . . . J OR W PACKAGE
SN74174 . . . N PACKAGE
SN74LS174, SN74S174 . . . D OR N PACKAGE
(TOP VIEW)



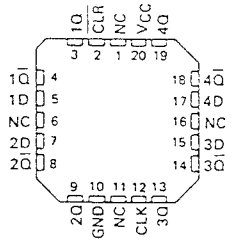
SN54LS174, SN54S174 . . . FK PACKAGE
(TOP VIEW)



SN54175, SN54LS175, SN54S175 . . . J OR W PACKAGE
SN74175 . . . N PACKAGE
SN74LS175, SN74S175 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS175, SN54S175 . . . FK PACKAGE
(TOP VIEW)

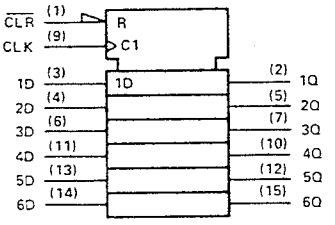


NC – No internal connection

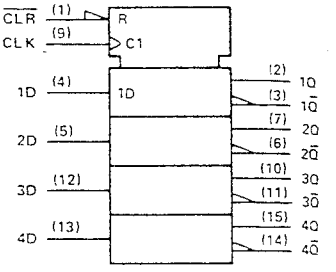
SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175, SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

logic symbols†

'174



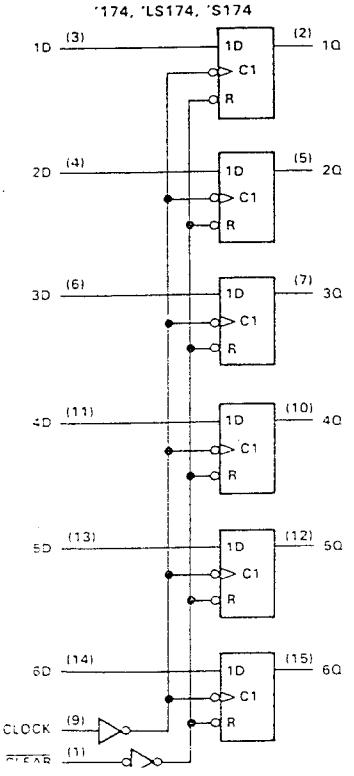
'175



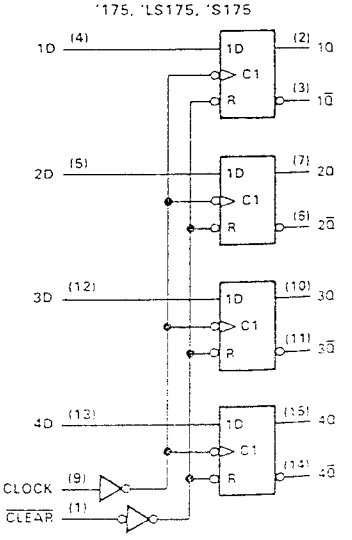
†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagrams (positive logic)

'174, 'LS174, 'S174



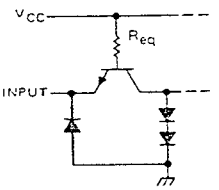
'175, 'LS175, 'S175



schematics of inputs and outputs

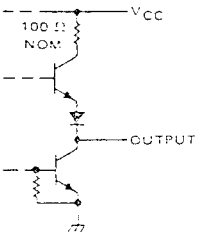
SN54174, SN54175, SN74174, SN74175

EQUIVALENT OF ALL INPUTS



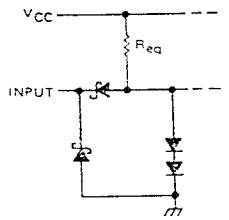
Clock, D: R_{eq} = 8 kΩ NOM
$\overline{\text{Clear}}$: R_{eq} = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS



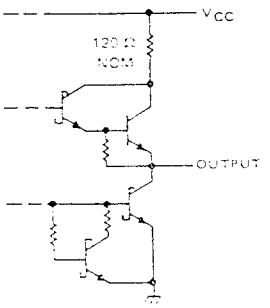
SN54LS174, SN54LS175, SN74LS174, SN74LS175

EQUIVALENT OF ALL INPUTS



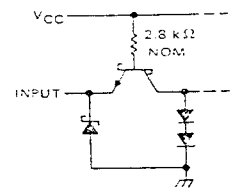
Clock: R_{eq} = 23 kΩ NOM
$\overline{\text{Clear}}$, D: R_{eq} = 28 kΩ NOM

TYPICAL OF ALL OUTPUTS

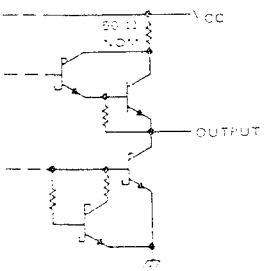


SN54S174, SN54S175, SN74S174, SN74S175

EQUIVALENT OF ALL INPUTS



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS174, SN54LS175 Circuits . . . . . −55°C to 125°C
SN74LS174, SN74LS175 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS174 SN54LS175			SN74LS174 SN74LS175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{su}	Data input	20			20			ns
	Clear inactive-state	25			25			ns
Data hold time, t_h		5			5			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS174 SN54LS175			SN74LS174 SN74LS175			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	'LS174		16	26		16	26	mA
			'LS175		11	18		11	18	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	'LS174			'LS175			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Note 3	30	40		30	40		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear						20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35		20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			20	30		13	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	30		15	25	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN5402, SN54LS02, SN54S02, SN7402, SN74LS02, SN74S02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

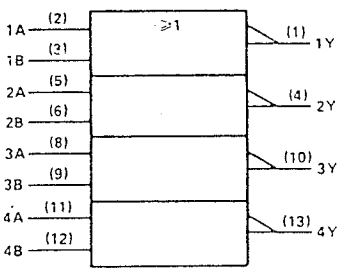
These devices contain four independent 2-input NOR gates.

The SN5402, SN54LS02, and SN54S02 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7402, SN74LS02, and SN74S02 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

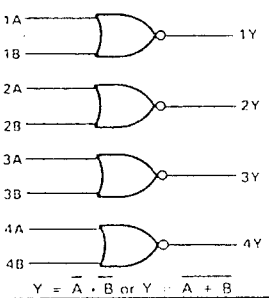
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



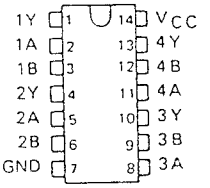
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)

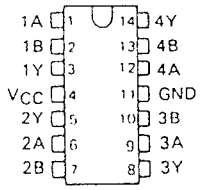


$Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$

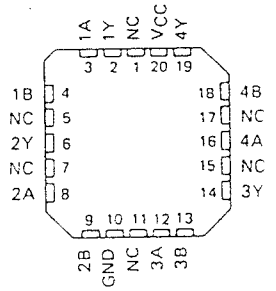
SN5402 . . . J PACKAGE
SN54LS02, SN54S02 . . . J OR W PACKAGE
SN7402 . . . N PACKAGE
SN74LS02, SN74S02 . . . D OR N PACKAGE
(TOP VIEW)



SN5402 . . . W PACKAGE
(TOP VIEW)



SN54LS02, SN54S02 . . . FK PACKAGE
(TOP VIEW)

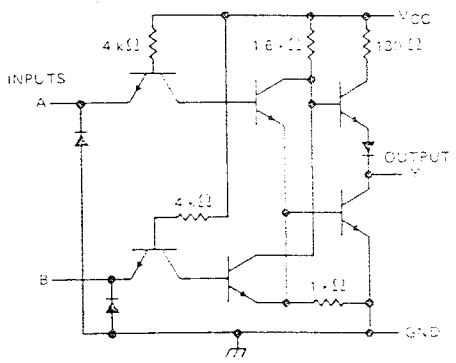


NC – No internal connection

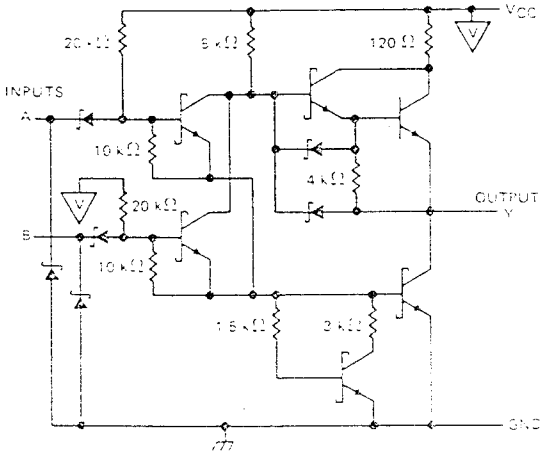
SN5402, SN54LS02, SN54S02,
SN7402, SN74LS02, SN74S02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

schematics (each gate)

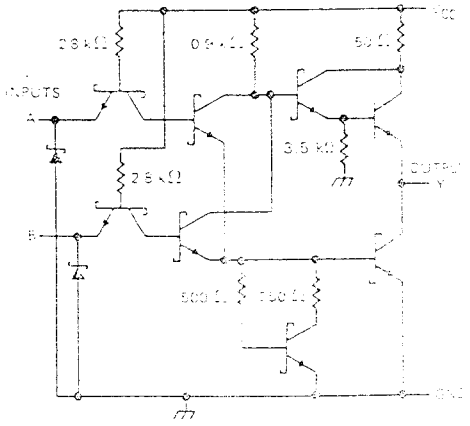
'02



'LS02



'S02



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '02, 'S02	5.5 V
'LS02	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: S'54'	−55°C to 125°C
S'74'	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5402			SN7402			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5402			SN7402			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		8	16		8	16	mA
I_{CCL}	V_{CC} = MAX, See Note 2		14	27		14	27	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		12	22	ns
t_{PHL}					8	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

	SN54LS02			SN74LS02			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS02			SN74LS02			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX	−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		1.6	3.2		1.6	3.2	mA
I_{CCL}	V_{CC} = MAX, See Note 2		2.8	5.4		2.8	5.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 2 kΩ, C_L = 15 pF		10	15	ns
t_{PHL}					10	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54S02			SN74S02			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S02			SN74S02			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V			50			50	μA
I_{IL}	V_{CC} = MAX, V_I = 0.5 V			−2			−2	mA
I_{OS}§	V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		17	29		17	29	mA
I_{CCL}	V_{CC} = MAX, See Note 2		26	45		26	45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 280 Ω, C_L = 15 pF		3.5	5.5	ns
t_{PHL}					3.5	5.5	ns
t_{PLH}			R_L = 280 Ω, C_L = 50 pF		5		ns
t_{PHL}					5		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.