AUTOMATION OF DM WATER STORAGE TANK

A PROJECT REPORT

Submitted by

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BONAFIDE CERTIFICATE

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This is to certify that **K. LOGANATHAN, T. MOHANRAJ, J. PHILIPS SANDEEP** and **K.S.P. PRADEEP CHANDRAN** of **KUMARAGURU COLLEGE OF TECHNOLOGY, COIMBATORE** have successfully completed their Project on **"AUTOMATION OF DM WATER STORAGE TANK"** in the Utilities & Services Department, Hyundai Motor India Limited during the period 04.02.2008 ~ 08.03.2008. The Trainees have submitted their **Project Report** and a **Prototype Working Model** of the proposed plan. The proposed plan can be implemented in HMI.

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ABSTRACT

Industrial automation is an art of optimizing the man power and reducing the fatigue which occurs due to repetition of the same work at regular intervals. The primary step in the process of industrial automation is to interface the physical quantities to PC. This is because once these quantities are fed to the PC a wide of manipulations may be done on the parameters that are interfaced. It is also possible to monitor the variation of a particular parameter continuously and represent in the form as per the requirement.

In this project we have made an attempt of automating the functioning of DM water plant with the use of water level in the DM water storage tank. The pressure induced by water in the storage tank is used as the parameter to identify the water level. This water level is then used for the optimized functioning of the DM plant and the boiler feed pump. The water level indication is also interfaced to a PC which functions as a real time water level monitoring system. The entire operation is controlled using a microcontroller which can be re-programmed according to future requirements.This project is mainly aimed at reducing the human fatigue and optimized use of energy.

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LIST OF ABREVATIONS

DM Water	-Demineralised Water
EEPROM	-Electrically Erasable Programmable Read Only Memory
LCD	-Liquid Crystal Display
LED	-Light Emitting Diode
RAM	-Random Access Memory
TTL	-Transistor Transistor Logic
TXD	-Transmit Data
RXD	-Receive Data

1. INTRODUCTION

1.1 STUDY OF THE EXISTING SYSTEM

The water from various sources are demineralised at the DM plant to avoid the rusting of boilers at Hyundai Motors India Limited. This demineralised water is stored in a tank of 30Kl capacity. This water is fed to the boiler supply tank through a feed pump. From the boiler supply tank water is supplied to al the boilers used at the production shops. The water level in the DM water storage tank decides the operation of the entire DM plant.

The current system existing at the company is that an employee checks the pressure level of the DM tank using the analog pressure gauge fixed in the storage tank. This process is carried out regularly at the intervals of half an hour. Based on the pressure level the DM plant is turned on or off. The DM plant control room is about 30 metres from the DM water storage tank. The boiler feed pump is always kept on, even if the boiler supply tank is full the DM water flow is stopped by the control valve and the feed pump is kept on continuously.

Disadvantages of the existing system

- The repetition of same work at regular intervals cause human fatigue.
- There occurs wastage of energy as the boiler supply tank feed pump is always kept on.

1.2 FEATURES OF THE PROPOSED SYSTEM

The entire operation the DM plant is automated by taking the level of water in DM water storage tank as the reference. A pressure sensor is used here to detect the level of water in the tank. The use of mechanical float to detect the water was not possible because of the high temperature prevailing within the DM water storage tank.

The following are the features of the proposed system :

- The level of the water in the DM tank is continuously monitored and displayed using a LCD at the tank.
- The level is also displayed in a PC placed at the control room.
- The DM plant gets automatically switched on as the water level reaches the low set point. The boiler feed pump is also switched off automatically.
- The DM plant gets automatically switched off as the water level reaches the high set point. The boiler feed pump is also switched on automatically.
- When there occurs any problem in DM plant and if the water level goes to very low set point an alarm is raised.

Advantages of the proposed system

- The fatigue of the employee gets reduced as the entire process is automated and the level can be monitored in the PC at the control room.
- The energy wastage caused due to continuous functioning of the Boiler feed pump is saved.

- As the water level is interfaced to the PC a number of manipulation may be carried out and pictorial representation is made possible

1.3 SPECIFICATIONS FOR DESIGN

- Maximum pressure = 0.45 kg/cm2
- Tank capacity = 30kl
- Low set point = 15kl
- Very low set point = 10kl
- High set point = 25kl
- Temperature = 45deg – 80deg Celcius

2. ANALYSIS OF LEVEL SENSORS

Level sensors are used to detect liquid level. The liquid to be measured can be inside a container or can be in its natural form (e.g. a river or a lake). The level measurement can be either continuous or point values. Continuous level sensors measure level within a specified range and are used to know the exact amount of liquid in a certain place and Point level sensors only measures a specific level, generally this is used to detect high level alarms or low level alarms.

There are many physical and application variables that affect the selection of the optimal level monitoring solution for industrial and / or commercial processes. The selection criteria include the physical: state (liquid, solid or slurry), temperature, pressure or vacuum, chemistry, dielectric constant of medium, density or specific gravity of medium, agitation, acoustical or electrical noise, vibration, mechanical shock, tank or bin size and shape; and the application constraints: price, accuracy, appearance, response rate, ease of calibration or programming, physical size and mounting of the instrument, monitoring or control of continuous or discrete (point) levels.

2.1 MAGNETIC AND MECHANICAL FLOAT LEVEL SENSOR

The principle behind magnetic, mechanical, cable, and other float level sensors involves the opening or closing of a mechanical switch, either through direct contact with the switch, or magnetic operation of a reed. With magnetically actuated float sensors, switching occurs when a permanent magnet sealed inside a float rises or falls to the actuation level. With a mechanically actuated float, switching occurs as a result of the movement of a float against a miniature (micro) switch. For both magnetic and mechanical float level sensors, chemical compatibility, temperature, specific gravity (density), buoyancy, and viscosity affect the selection of the stem and the float. For example, larger floats may be used with liquids with specific gravities as low as 0.5 while still maintaining buoyancy. The choice of float material is also influenced by temperature-induced changes in specific gravity and viscosity - changes that directly affect buoyancy.

Float-type sensors can be designed so that a shield protects the float itself from turbulence and wave motion. Float sensors operate well in a wide variety of liquids, including corrosives. When used for organic solvents, however, one will need to verify that these liquids are chemically compatible with the materials used to construct the sensor. Float-style sensors should not be used with high viscosity (thick) liquids, sludge or liquids that adhere to the stem or floats, or materials that contain contaminants such as metal chips; other sensing technologies are better suited for these applications.

2.2 PNEUMATIC LEVEL SENSOR

Pneumatic level sensors are indicated where hazardous conditions exist, where there is no electric power or its use is restricted, and in applications involving heavy sludge or slurry. As the compression of a column of air against a diaphragm is used to actuate a switch, no process liquid contacts the sensor's moving parts. These sensors are suitable for use with highly viscous liquids such as grease, as well as water-based and corrosive liquids. It has the additional benefit of being a relatively low cost technique for point level monitoring.

2.3 CONDUCTIVE (ELECTRODE-BASED) LEVEL SENSORS

Conductive level sensors are ideal for the point level detection of a wide range of conductive liquids such as water, and is especially well suited for highly corrosive liquids such as caustic soda, hydrochloric acid, nitric acid, ferric chloride, and similar liquids. For those conductive liquids that are corrosive, the sensor's electrodes need to be constructed from titanium, Hastelloy B or C, or 316 stainless steel and insulated with spacers, separators or holders of ceramic, polyethylene and Teflon-based materials. Depending on their design, multiple electrodes of differing lengths can be used with one holder. Since corrosive liquids become more aggressive as temperature and pressure increase, these extreme conditions need to be considered when specifying these sensors.

The technology behind conductive level sensing involves a low-voltage, current-limited power source applied across separate electrodes. The power supply is matched to the conductivity of the liquid, with higher voltage versions designed to operate in less conductive (higher resistance) mediums. The power source frequently incorporates some aspect of control, such as high-low or alternating pump control. A conductive liquid contacting both the longest probe (common) and a shorter probe (return) completes a conductive circuit. Conductive sensors are extremely safe because they use low voltages and currents. Since the current and voltage used is inherently small, for personal safety reasons, the technique is also capable of being made "Intrinsically Safe" to meet international standards for hazardous locations. Conductive probes have the additional benefit of being solid-state devices and are very simple to install and use. In some liquids and applications, maintenance can be an issue. The probe must continue to be conductive. If buildup insulates the probe from the medium, it will stop working properly. A simple inspection of the probe will require an ohmmeter connected across the suspect probe and the ground reference.

2.4 CAPACITANCE LEVEL SENSORS (ALSO CALLED RF)

Capacitance level sensors excel in sensing the presence of a wide variety of solids, aqueous and organic liquids, and slurries. The technique is frequently referred to as RF for the radio frequency signals applied to the capacitance circuit. The sensors can be designed to sense material with dielectric constants as low as 1.1 (coke and fly ash) and as high as 88 (water) or more. Sludges and 50)»»slurries such as dehydrated cake and sewage slurry (dielectric constant 90) can also be»and liquid chemicals such as quicklime (dielectric constant sensed. Dual-probe capacitance level sensors can also be used to sense the interface between two immiscible liquids with substantially different dielectric constants, providing a solid state alternative to the aforementioned magnetic float switch for the "oil-water interface" application. Since capacitance level sensors are electronic devices, phase modulation and the use of higher frequencies makes the sensor suitable for applications in which dielectric constants are similar. The sensor contains no moving parts, is rugged, simple to use, easy to clean, and can be designed for high temperature and pressure applications. A danger exists from build up and discharge of a high-voltage static charge that results from the rubbing and movement of low dielectric materials, but this danger can be eliminated with proper design and grounding.

Appropriate choice of probe materials reduces or eliminates problems caused by abrasion and corrosion. Point level sensing of adhesives and high-viscosity materials such as oil and grease can result in the build up of material on the probe; however, this can be minimized by using a self-tuning sensor. For liquids prone to foaming and applications prone to splashing or turbulence, capacitance level sensors can be designed with splashguards or stilling wells, among other devices.

A significant limitation for capacitance probes is in tall bins used for storing bulk solids. The requirement for a conductive probe that extends to the bottom of the measured range is problematic. Long conductive cable probes (20 to 50 meters long) suspended into the bin or silo, are subject to tremendous mechanical tension due to the weight of the bulk powder in the silo and the friction applied to the cable. Such installations will frequently result in a cable breakage.

2.5 ULTRASONIC LEVEL SENSORS

Ultrasonic level sensors (sometimes called sonic) are ideal for non-contact level sensing of highly viscous liquids such as heavy oil, grease, latex, and slurries as well as bulk solids like cement, sand, grain, rice, and plastic pellets. The sensors emit high frequency, “ultra” sonic (20 kHz to 200 kHz) acoustic waves that are reflected back to and detected by the emitting transducer.

Since the speed of sound in air fluctuates with moisture level and temperature, ultrasonic level sensors are also affected by changing moisture levels and varying temperatures and pressures inside the hopper or container. But when ultrasonic sensors are used in conjunction with humidity and temperature sensors, or a distance reference, correction factors can be applied to the level measurement making the technology very accurate.

Proper mounting is important to ensure that sound waves are reflected perpendicularly back to the sensor. Otherwise, even slight misalignment of the sensor in relation to the process material reduces the amount of sound wave detected by the transducer. Since the ultrasonic transducer is used both for transmitting and receiving the acoustic energy, it is subject to a period of mechanical vibration known as "ringing". This vibration must attenuate (stop) before the echoed signal can be processed. The net result is a distance from the face of the transducer that is blind and cannot detect an object.

2.6 PRESSURE SENSOR

A pressure sensor measures the pressure, typically of gases or liquids. Pressure is an expression of the force required to stop a gas or fluid from expanding, and is usually stated in terms of force per unit area. A pressure sensor generates a signal related to the pressure imposed. Typically, such a signal is electrical, but it might also include additional means, such as optic signals, visual signals and/or auditory signals.

Pressure sensors are used in numerous ways for control and monitoring in thousands of everyday applications. Pressure sensors can be used in systems to measure other variables such as fluid/gas flow, speed, water level, and altitude. Pressure sensors can alternatively be called pressure transducers, pressure transmitters, pressure senders, pressure indicators among other names.

Pressure sensors can vary drastically in technology, design, performance, application suitability and cost. A conservative estimate would be that there may be over 50 technologies and at least 300 companies making pressure sensors worldwide.

There are also a category of pressure sensors that are designed to measure in a dynamic mode for capturing very high speed changes in pressure. Example applications for this type of sensor would be in the measuring of combustion pressure in an engine cylinder or in a gas turbine. These sensors are commonly manufactured out of piezoelectric materials like quartz.

Some pressure sensors function in a binary manner, i.e., when pressure is applied to a pressure sensor, the sensor acts to complete or break an electrical circuit. Some speed cameras use them. These types of sensors are also known as a pressure switches.

2.7 TYPES OF FLUID PRESSURE MEASUREMENTS

2.7.1 Silicon piezoresistive pressure sensors

Pressure sensors can be classified in term of pressure ranges they measure, temperature ranges of operation, and most importantly the type of pressure they measure. In term of pressure type, we can categorize them in five categories.

2.7.2 Absolute pressure sensor

This sensor measures the pressure relative to perfect Vacuum pressure (0 PSI or no pressure). Atmospheric pressure, is about 100kPa (14.7 ? PSI) at sea level. Atmospheric pressure is an absolute pressure.

2.7.3 Gauge pressure sensor

This sensor is used in different applications because it can be calibrated to measure the pressure relative to a given atmospheric pressure at a given location. An example of gauge pressure would be a tire pressure gauge. When the tire pressure gauge reads 0 PSI, there is really 14.7 PSI (atmospheric pressure) in the tire.

2.7.4 Vacuum pressure sensor

This sensor is used to measure pressure less than the atmospheric pressure at a given location.

2.7.5 Differential pressure sensor

This sensor measures the difference between two or more pressures introduced as inputs to the sensing unit, for example, measuring the pressure drop across an oil filter. Differential pressure is also used to measure flow or level in pressurized vessels.

2.7.6 Sealed pressure sensor

This sensor is the same as the Gauge pressure sensor except that it is previously calibrated by manufacturers to measure pressure relative to sea level pressure (14.6 PSI).

3. SIMPLIFIED BLOCK DIAGRAM

This part of chapter gives a brief explanation about the various basic blocks of the project

3.1 PRESSURE SENSOR

Pressure sensor block consists of a pressure sensor and an instrumentation amplifier. The output of the pressure sensor is converted as a voltage value with respect to ground with the help of an instrumentation amplifier.

3.2 ANALOG TO DIGITAL CONVERTER

The microcontroller can accept only digital signals. The ADC plays the role of converting the analog voltage from the pressure senor circuitry to digital form.

3.3 MICROCONTROLLER

The microcontroller plays the role of decision making. It is programmed to take the input from the ADC as reference and takes the appropriate calculations to carry out the necessary functions. It is interfaced to a series of modules such as LCD, relay driver and RF transmitter.

3.4 RECEIVER PART

The receiver part consists of three blocks namely RF receiver, optocoupler and relay circuitry.

The RF receiver receives the pulse transmitted and this is used as the control pulse for the relay cicutry. The optcoupler is used isolate the power circuit from the low power DC circuit.

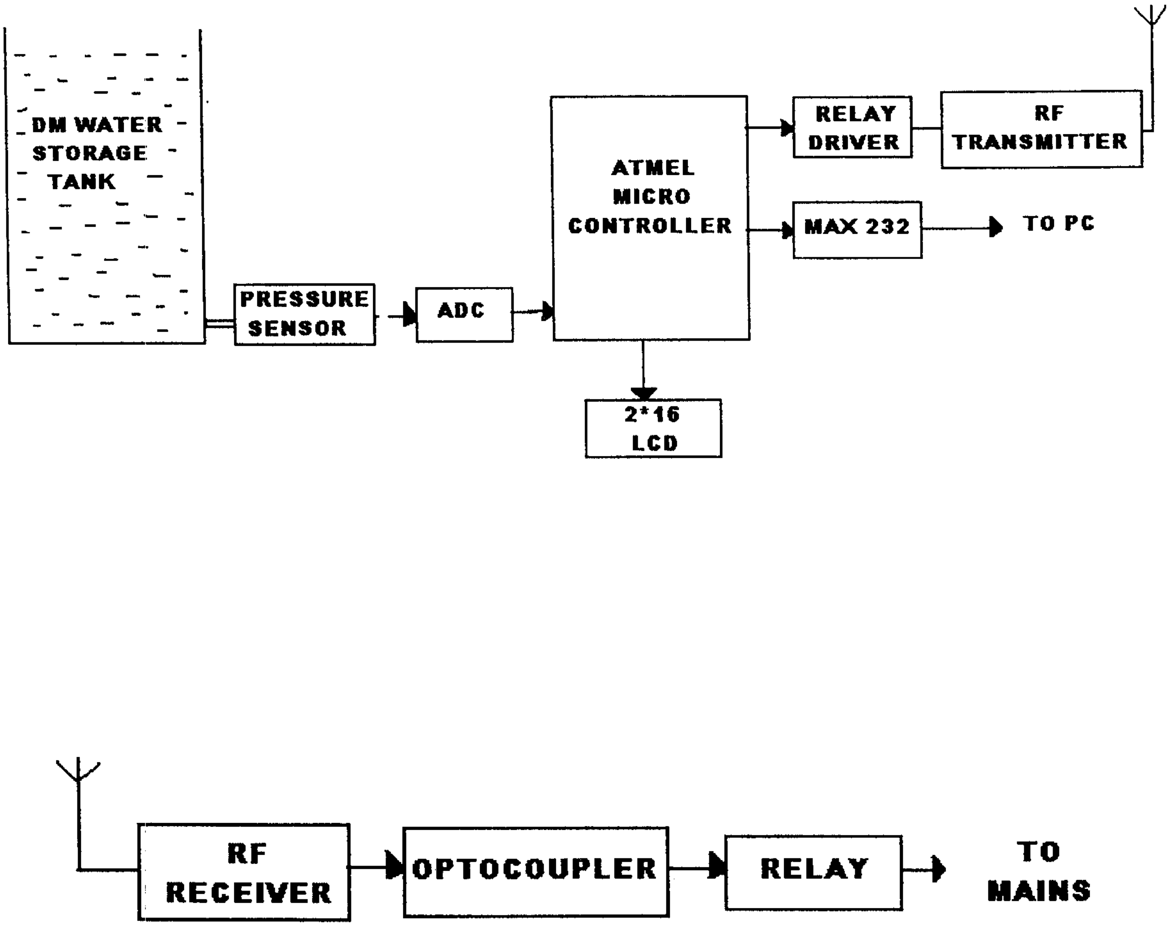


Figure 3.1 Simplified Block diagram

4. MICROCONTROLLER

A MICRO CONTROLLER ATMEL 89C51 being backed up by suitable interface and relay driver boards controls the entire operation.

4.1 INTRODUCTION

Industrial automatic controllers have been available for years but have a price tag in the thousands of dollars. In addition, they are not very adaptable to aqua cultural operations due to the severe environment in which they operate and the changing requirements of agricultural control systems. On the other hand, Micro controller chips are very inexpensive, usually costing much less than $100. They are very small, can operate under very severe environmental conditions, and lend them to new, simplified programming procedures. These features make the Micro controller the preferred choice for embedded control, such as that used in appliances, automotive engine control, camera exposure control and industrial automation.

A Microcontroller is an enhanced microprocessor. In addition to the microprocessor, a Microcontroller typically contains several parallel and serial ports, system clock generators, data and program memory, timers, counters, interrupt logic, analog-to-digital converters, digital-to-analog converters, and even digital signal processing subsystems on the same chip. Thus, a single-chip Microcontroller may be placed in an application to perform as an embedded controller with no other support chips. Only within the last few years have Microcontrollers advanced to the point that they can handle a large number of inputs and outputs and accommodate enough memory and processing power to control a complex system such as those used in aqua cultural production. The Microcontroller used in this robot is ATMEL 89C51. The ATMEL 89C51 Micro controller belonging to the ATMEL family. This Microcontroller has features that seem to make it more accessible than any other does single chip Microcontroller with a reasonable price tag.

4.2 COMPARISON OF MICROPROCESSOR AND MICRO CONTROLLER

The difference between Microprocessor and Microcontroller is Microprocessor can only process with the data, Microcontroller can control external device. That is if you want switch "ON" or "OFF" a device, you need peripheral ICs to do this work with Microcontroller you can directly control the device.

4.3 ADVANTAGES OF MICROCONTROLLERS

1. If a system is developed with a Microprocessor, the designer has to go for external memory such as RAM, ROM *or* EPROM and peripherals and hence the size of the PCB will be large enough to hold all the required peripherals. But the Microcontroller has got all these peripheral facilities on a single chip so development of a similar system with a Microcontroller reduces PCB size and cost of the design.

2.One of the major difference between a Microcontroller and a Microprocessor is that a controller often deals with bits, not bytes as in the real world application, for example switch contacts can only be open or close, indicators should be lit or dark and motors can be either turned on or off and so forth.

3.The Microcontroller has two 16 bit timers / counters built within it, which makes it more suitable to this application since we need to produce some accurate timer delays. It is even more advantageous that the timers also act as interrupt.

4.4 ATMEL 89C51

The 89C5l, an 8 bit single chip Microcontroller has got a powerful CPU optimized for control applications, 64K program memory address space, 64K data memory address space, 128 bytes of on chip RAM(raed/write memory), for 8 bit bi- directional parallel ports one full duplex serial ports two 16 bit timers/counters and an extensive interrupt structure.

The 89C51 are a second-generation 8-bit single chip Microcontroller. The 89C51 provides a significantly more powerful architecture, a more powerful instruction set and a full serial port.

The 89C51 are a complete Microcontroller. We will start our discussion on the programming model by looking at the architectural block diagram. As we can see the external connections very simple.

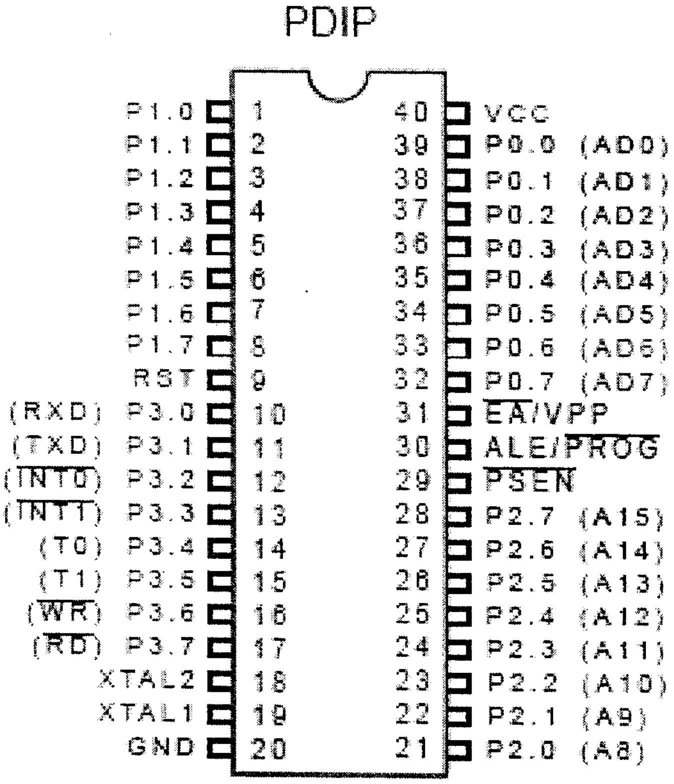


Figure 4.1 Pin details of ATMEL 89C5

There are 32 pins needed by the four 8 bit bi-directional ports. Eight additional pins are providing power, allow you to connect a crystal clock and provide a few timing and control signals.

The architecture includes the ALU, the accumulator, the stack pointer, a block of registers and a general purpose register-the B register. All these devices are connected to the 89C51 internal 8-bit data bus.

Each I/O port is also connected to the 8-bit internal data bus through a series of registers. These registers hold data during I/O transfers and control the I/O ports. The architectural block diagram also shows the 89C51 ROM and RAM.

Block Diagram

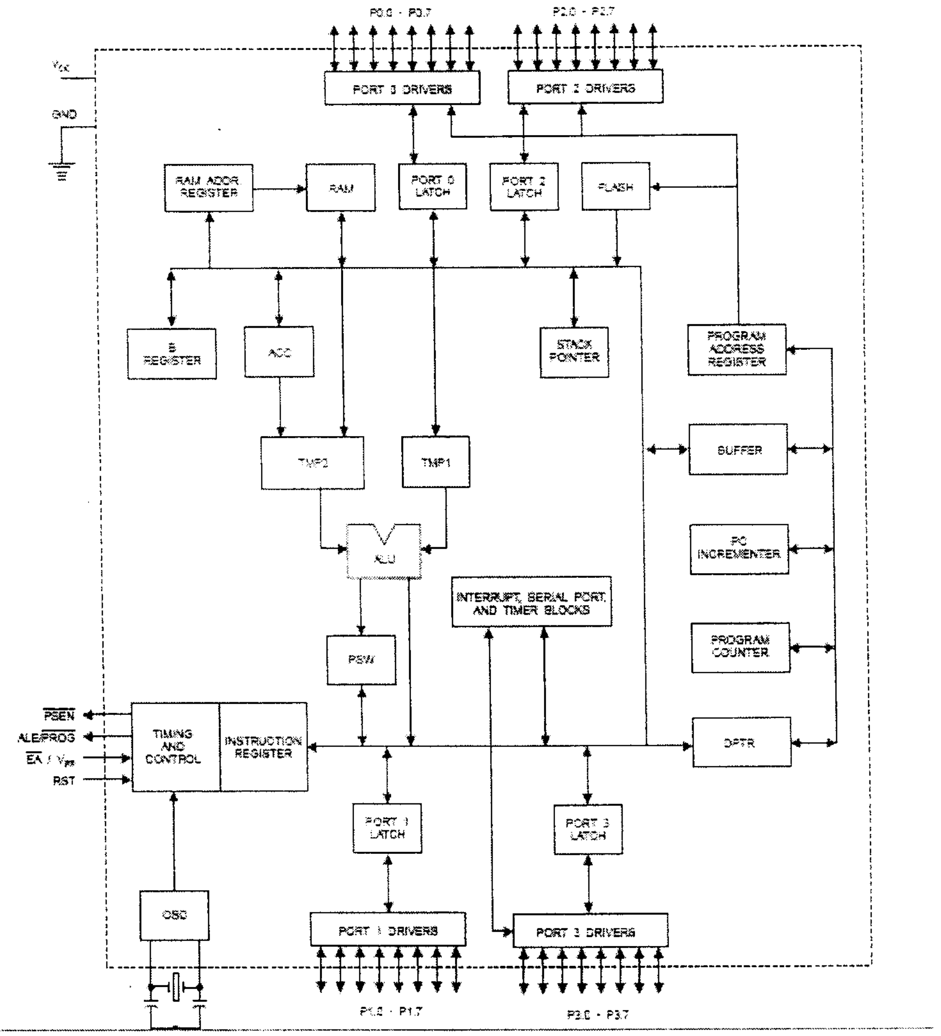


Figure 4.2 Block diagram of Atmel 89C51

4.4.1 SPECIAL FEATURES OF ATMEL 89C51

- 8 Bit CPD optimized for control applications.
- Extensive Boolean processing (Single - Bit Logic) Capabilities.
- On - Chip Flash Program Memory. On - Chip Data RAM.
- Bi - directional and Individually Addressable *VO* Lines. . Multiple 16 - Bit Timer *I* Counters.
- Full Duplex DART.
- Multiple Source *I* Vector *I* Priority Interrupt Structure.
- On - Chip Oscillator and Clock circuitry. On - Chip EEPROM..
- SPI Serial Bus Interface. Watch Dog Timer.

FLASH ROM

Flash ROM can be well explained with a block diagram as shown in the following figure. 4-ki10 byte ROM is available in the Microcontroller. It can be erased and reprogrammed. If the available memory is not enough for your program, you can interface the external ROM with this IC, it has 16 address lines, so maximum of (216) i.e. 64 bytes of ROM can be interfaced with this Microcontroller. Both internal and external ROM cannot be used simultaneously.

RAM

Internal 256 bytes of RAM are available for user. These 256 bytes of RAM can be used along with the external RAM. Externally you can connect 64-kilo bytes of RAM with Microcontroller. In internal RAM first 128 bytes of RAM is available for user and the remaining 128 bytes are used as Special Function Registers (SFR). These SFR's are used as Control Registers for Timer, Serial Port etc.

INPUT / OUTPUT PORTS

There are four I/O ports available in A T89C51. They are Port 0, Port 1, Port 2, Port 3. All these ports are eight bit ports. All these ports can be controlled as eight-bit port or it can be controlled individually. One of the main feature of this Microcontroller is it can control the port pins individually. For example to control a LED we need to use one I/O line in Microprocessor with 8255 we have to use an eight bit port. In 89C51 Port 1 is available for users Port 3 is combined with interrupts. This can be used as interrupts (or) I/O Ports, Port 2 & Port 0 is combined with address bus and data bus. All these port lines are available with internal pull-ups except Port O. If we want to use Port 0 as I/O Port we have to use pull-up resistors.This Microcontroller is working in a speed of maximum of 24 MHz. This Microcontroller is available with Inbuilt Oscillator; just we have to connect the crystal to its terminal.

POWER MODES

To exploit the power savings available in CMOS circuitry, ATMEL's Flash Microcontroller have two software - Invited & Reduced Power Modes.

IDLE MODE

The CPU is turned off while the Ram and other on - chip peripherals continue operating. In this mode current draw is reduced to about 15 percent of the current drawn when the device is fully active.

POWER DOWN MODE

All on - chip activities are suspended while the on - chip RAM continues to hold its data. In this mode, the device typically draws Jess than 15 _A and can be as low as 0.6 _A.

POWER ON RESET

When power is turned on, the circuit holds the RST pin high for an amount of time that depends on the capacitor value and the rate at which it charges. To ensure a valid reset, the RST pin must be held high long enough to allow the oscillator to start up plus two machine cycles.

PROGRAM MEMORY

As shown the map of the lower part of the program memory, after reset, the CPU begins execution from location OOOOh. As shown each interrupt is assigned a fixed location in program memory. The interrupt causes the CPU to jump to that location, where it executes the service routine. External Interrupt 0 for examples assigned to location 0003h. If the Interrupt is not used, its service location is available as general purpose program memory.

The interrupt service locations are spaced at 8 byte intervals 0003h for external interrupt 0, OOOBh for Timer 0, 0013h for External interrupt 1, 001Bh for Timer 1 and so on. If an Interrupt service routine is short enough (as is often the case in control . applications) it can reside entirely within that 8-byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations. If other interrupts are ill use.

For example, in the AT89C51 with 4K bytes of on - chip Flash, if the EA pin is strapped to YCC, program fetches to addresses OOOOh through OFFFh _are directed to internal Flash. Program fetches to addresses 1000h through FFFFh are directed to external memory.

DATA MEMORY:

The Internal Data memory is divided into three blocks namely,

- The Lower 128 Bytes of Internal RAM.
- The upper 128 Bytes of Internal RAM.
- Special Function Registers.

Internal Data memory Addresses are always 1 byte wide, which implies an address space of only 256 bytes. However, the Addressing Modes for internal RAM can in fact accommodate 384 bytes. Direct addresses higher than 7Fh access one memory space and indirect addresses higher than 7Fh access a different memory space.

The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as RO through R7. Two bits in the Program Status Word (PSW) Select, which register bank, is in use. This architecture allows more efficient use of code space, since register instructions are shorter than instructions are shorter than instructions that use direct addressing.

The next 16 - bytes above the register banks form a block of bit 'addressable memory space. The Microcontroller instruction set includes a wide selection of single bit instructions and this instruction can directly address the 128 bytes in this area. These bit addresses are OOh through 7Fh.

PROGRAM STATUS WORD

Program Status Word Register in ATMEL Flash Microcontroller is

CY	AC	F0	RS	RS0	0V	-	P
PSW7	PSW6	PSW5	PSW4	PSW3	PSW2	PSW1	PSW0

Table 4.1 Program status word of Atmel89C51

PSWO: Parity of Accumulator Set By Hardware to 1 ifit contains an Odd number of 1s Otherwise it
is reset O.

PSW1: User Definable Flag.

PSW2: Overflow Flag Set By Arithmetic Operations.

PSW3: Register Bank Select.

PSW 4: Register Bank Select.

PSW5: General Purpose Flag.

PSW6: Auxiliary Carry Flag Receives Carry Out from Bit of Addition Operands .

PSW7: Carry Flag Receives Carry Out From Bit 1 of ALU Operands.

INTERRUPTS

The AT89C51 Provides 5 interrupts sources: Two External interrupts, Two-Timer Interrupts and a Serial Port Interrupt.

The External Interrupts INTO and INTI can each either level activated or transition - activated, depending on bits ITO and ITI in register TCON. The Flags that actually generate these interrupts are the IEO and IEI bits in TCON. When the service routine-is vectored to hardware clears the flag that generated an external interrupt. If the interrupt was transition - activated. If the interrupt was level - activated, then the external requesting source (rather than the on - chip hardware) controls the requested flag.

The Timer 0 and Timer 1 interrupts are generated by TFI and TFO which are set by a roll over in their respective Timer / counter Register (except for Timer 0 in Mode 3). When a timer interrupt is generated it when the service routine is vectored to.

The logical OR and TI generate the serial port interrupt. Neither of these flag is cleared by hardware when the service routine is vectored to. In fact, the service routine normally must determine whether RI and TI generated the interrupt and the must be cleared in software.

INTERRUPT ENABLE REGISTER

EA	**-**	**ET2**	**ES**	**ET1**	**EX1**	**ET0**	**EX0**
IE7	**IE6**	**IE5**	**IE4**	**IE3**	**IE2**	**IE1**	**IE0**

Table 4.2 Iterrupt enable register

Enable bit=1 enabled the interrupt.
Enable bit=0 disables it.

EA Global enable / disable all interrupts.
If EA = 0, no interrupt will be acknowledged.
If EA = I, each interrupt source is individually enabled or disabled by setting or clearing its enabled bit

IE.6 Undefined / reserved.ET2

IE.5 Timer 2 Interrupt enables bit.ES

IE.4 Serial Port Interrupt enabled bit.ET1

IE.3 Timer 1 Interrupt enables bit.EX1

IE.2 External Interrupt 1 enables bit.ET0

IE.1 Timer 0 Interrupt enables bit.EX0
IE.0 External Interrupt 0 enables bit

INTERRUPT PRIORITY REGISTER

-	-	PT2	PS	PT1	PX1	PT0	PX0
IP7	**IP6**	**IP5**	**IP4**	**IP3**	**IP2**	**IP1**	**IP0**

Table 4.3 Interrupt priority register

Enable bit=1 enabled the interrupt
Enable bit=0 disables it

IP.7 Reserved.
IP.6 Reserved.
IP.5 Timer 2 Interrupt priority bit.
IP.4 Serial Port Interrupt priority bit
IP.3 Timer I Interrupt priority bit.
IP.2 External Interrupt I priority bit
IP.I . Timer 0 Interrupt priority bit.
IP.O External Interrupt 0 priority bit.

PRIORITY LEVEL STRUCTURE

Each interrupt source can also be individually programmed to one of two priority levels by setting or clearing a bit in special function register IP (interrupt priority) at address OB811. IP is cleared after a system reset to place all interrupts at the lower priority levelly default. A low - priority interrupt can be interrupted by a high - priority interrupt but not by another low - priority interrupt. A high - priority interrupt can be interrupted by any other interrupt sources.

If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If request of the same priority level is received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is second priority structure determined by the polling sequence as follows.

PRIORITY LEVEL STRUCTURE:

Priority level Structure of the same Microcontroller is as follows

1. IEO(Highest) 0003h
2. TFO OOOBh
3. IEI 0O13h
4. TFI OOIBh
5. RT + TIOO23h

OSCILLATOR AND CLOCK CIRCUIT:

To drive the chip with an internal oscillator, one would ground XTALI and XTAL2. Since the input to the clock generator is a divide – by two Flip – Flops, there is no requirement on the duty cycle of the external oscillator signal. However, minimum high and low times must be observed.

The clock generator divides the oscillator frequency by 2 and provides a twophase clock signal to the chip. The Phase 1 signal is active during the first half of each clock period and the Phase 2 signal is active during the second half of each clock period.

CPU TIMING

All A TMs Flash Microcontroller have an on – Chip Oscillator, which can be used, as the clock source for the Cpu. To use the on – chip oscillator, connect a crystal or ceramic resonator between the

XTAL1 and XTAL2 pins of the Microcontroller and connect the capacitors to ground as shown.

The internal clock generator defines the sequence of states that make up the Microcontroller machine cycles.

TIMER CONTROL AND STATUS REGISTER:

Two Special Function Registers, TMOD and TCON, are used to define operating modes and control the functions of the timer / counters. When an instruction changes the content of TMOD or TCON, the change is latched into the special function register and takes effect at SIPI of the nest instruction's first cycle.

5. CIRCUIT DESCRIPTION

5.1 TRANSDUCER BOARD

The function of the transducer board is to convert a physical quantity into appropriate analog voltage. Here the pressure exerted by the water in the tank is converted into appropriate voltage by the pressure sensor. The pressure sensor used here is SPDG150.

This is a six pin IC with pins 1 & 5 connected to supply and ground respectively. The output voltage due to the pressure exerted at the pressure port is obtained at pins 2&4 as +ve and –ve voltages.

This voltage cannot be directly given as input to the ADC. The output voltage is in the range of millivolts.

An instrumentation amplifier is used with a variable resistance to adjust the gain value. We have set the value of the variable resistance in order to obtain a gain value of 10.

The instrumentation amplifer is constructed using IC LM324N which consists of three op amps in a single IC.

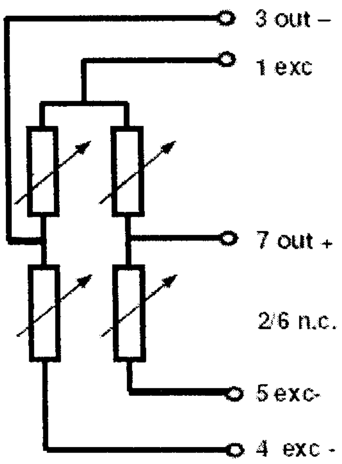


Figure 5.1 Block diagram of pressure sensor

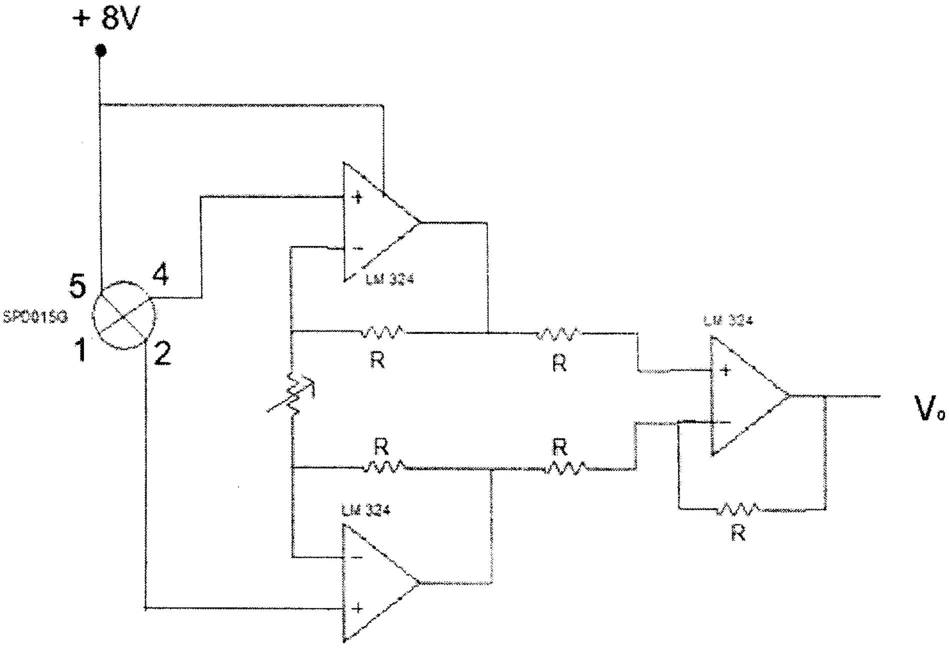


Figure 5.2 Pressure sensor with instrumentation amplifier

5.2 MAIN BOARD

The Main board consists of Microcontroller ATMEL 89C51 along with its Crystal Oscillator to supply required clock pulses for its operation and a RC Circuit for the total system reset.

The 2 bits of Port 0, Pins 38 and 39 are connected to IC ULN2003 which acts as the relay and buzzer driver.

All the 8 bits of Port 1,Pins 1-8 are connected to the analog to digital converter, ADC 0804.The input from the pressure sensor is fed through this port.

The first 4 pins of Port 2, Pins 21-24 are connected to the data bits of the 16*2 LCD display.

The first 2 bits of Port 3, Pins 10 and 11 are connected to the TTL IN and TTL OUT pins of MAX 232.

The Pins 18 and 19 are connected to a Crystal with a parallel combination of two capacitors of 33 pF, which delivers the necessary clock pulses of 11.0592 MHz to the controller.

The Pins 9 and 31 are connected with a parallel combination of 10K resistor and a 10MFD capacitor for total system reset.

The Pin 40 is connected to +5V and Pin 20 is connected to ground.

5.3 RELAY & BUZZER DRIVER :

The current strength of data signals that is sent from the Microcontroller is not sufficient to drive the stepper motors. An average of 0.4 mA is available on the port pins of the Microcontroller. But the relay an buzzer needs a higher current rating to operate. The driver produce the necessary current to drive the relay. This project consists of two relays to control the DM plant main switch and the boiler tank feed pump. It also consists of a buzzer to indicate the emergency situation.

The output from the port pins is connected to the Buffer IC ULN2003. The ULN2003 is a high voltage, high current Darlington arrays each containing seven open collector Darlington pairs with common emitters. Each channel rated 500mA and can withstand peak currents of 600mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The output pins of the buffer , ULN2003, 15 and 16 are connected to relay and buzzer. The relay in turn is connected to a RF transmitter which transmits the signal.

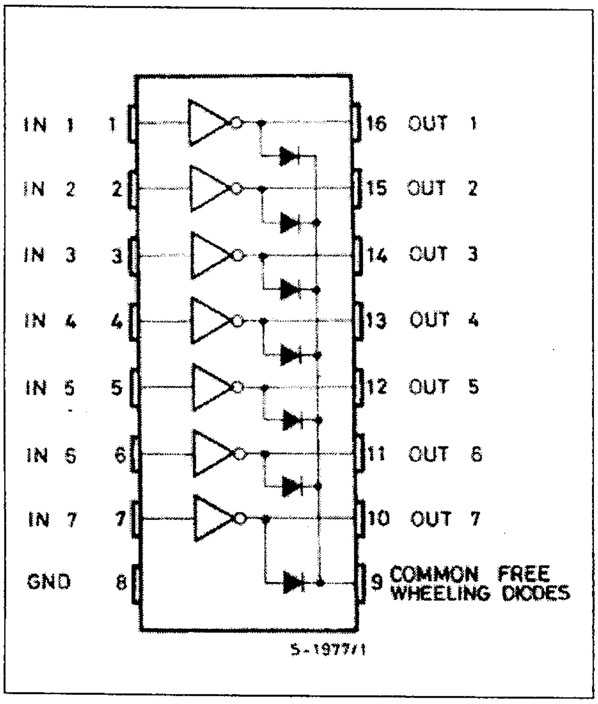


Figure 5.3 Pin details of ULN2003

5.4 ANALOG TO DIGITAL CONVERTER

The ADC080X family are CMOS 8-Bit, successive approximation A/D converters which use a modified potentiometric ladder and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, and hence no interfacing logic is required. The differential analog voltage input has good common mode- rejection and permits offsetting the analog zero-input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

- 80C48 and 80C80/85 Bus Compatible - No Interfacing Logic Required
- Conversion Time <100μs
- Easy Interface to Most Microprocessors
- Differential Analog Voltage Inputs
- TTL Compatible Inputs and Outputs
- On-Chip Clock Generator
- Analog Voltage Input Range 0V to 5V
- No Zero-Adjust Required
- 80C48 and 80C80/85 Bus Compatible - No Interfacing Logic Required

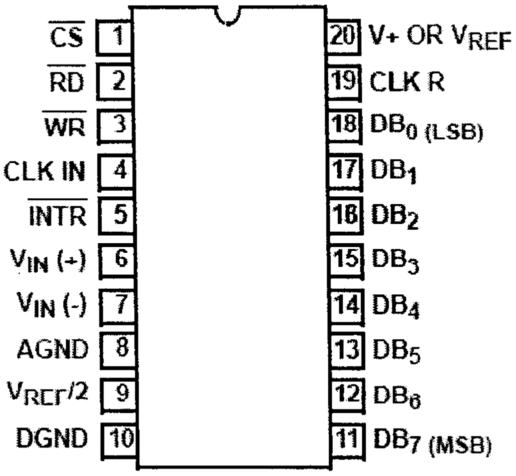


Figure 5.4 Pin details of ADC 0804

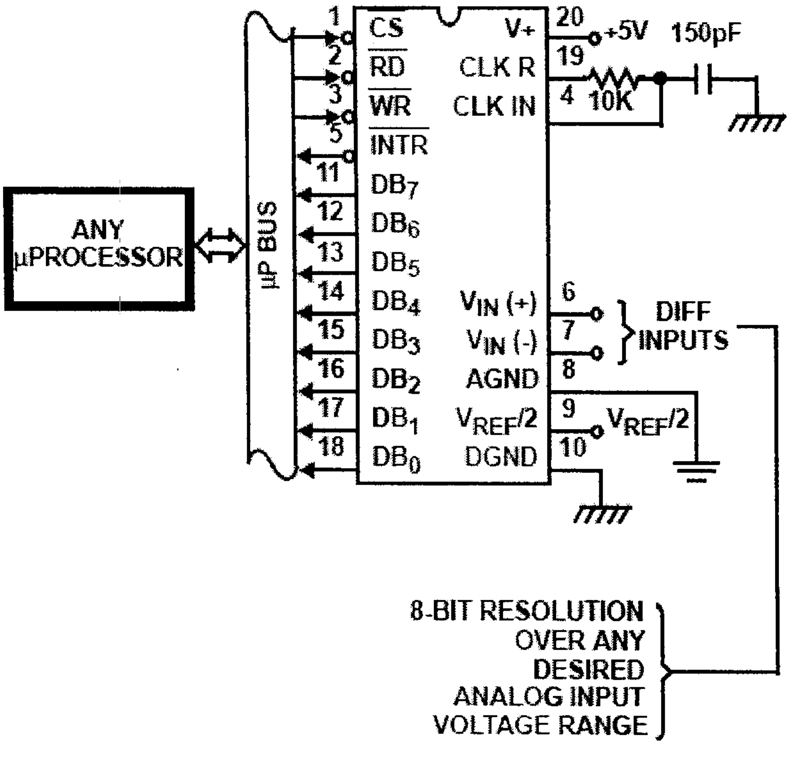


Figure 5.5 Typical application circuit

5.5 RS 232 STANDARDS

To allow compatibility among data communication equipment made by various manufactures, an interfacing standards called RS 232 are said byelectronics industries association (EIA) in 1960. However, since the standards were set longed before the advent of the TTL logic family, its input and output voltages levels are not TTL compatible. In RS232, 1 bit is represented by -3 to -25 volt while a 0 bit is +3 to + 25 Volt, making -3 to +3 undefined. For this reason to connect any RS 232 to a micro controller system we must use voltage converters such as MAX 232 to convert the TTL level to the RS232 voltage level and Vice versa. MAX 232 Ie chip are commonly referred to as line drivers

5.5.1 RS 232 PINS

The table provides the pins and the labels for the RS 232 cable, commonly referred to as the DB-25 connector.

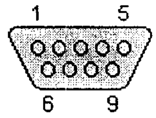


Fig 5.6 RS232 Pin Details

DB-9 Pin	IDC internal pin name*	Name	Dir	Description
1	1	CD	←	Carrier Detect
2	3	RXD	←	Receive Data
3	5	TXD	→	Transmit Data
4	7	DTR	→	Data Terminal Ready
5	9	GND	—	System Ground
6	2	DSR	←	Data Set Ready
7	4	RTS	→	Request to Send
8	6	CTS	←	Clear to Send
9	8	RI	←	Ring Indicator

The standards for RS 232 and similar interfaces usually restrict RS232 to 20 Kbps or less and line length of l5m or less. RS232 is fair more robust than the traditional limits of 20Kbps over a 15m line would imply RS232 is perfectly adequate at speed up to 200 Kbps most RS232 ports on main frame and midrange computers are capable of far higher speeds than their rated 19.2kbps. Usually these 1000 speed parts will run error free at 56kbps and above the 15m limitation for enable length can be stretched to about 30 ill for ordinary cable if well screened and grounded, and about 100m if the cable is 10m capacity.

5.5.2 FEATURES OF RS 232

The essential feature of RS 232 is the signals are carried as signal voltages referred to a common earth and print data to a common earth pin data is transmitted and received on pins 2 and 3 respectively. Data set ready (DSR) is an indication from the data set i.e., the modem DSU/CSU that's it is on. Similarly, DTR indicates to the data set that the DTE is on. Data carrier (DCD) indicates that carrier for transmit data is on. Pins 4 and 5 carry the R TS and CTS signals. In most situations R TS and CTS are constantly go throughout the communication session. However when the DTE is connected to a turn carrier on the modem on and off. On a multipoint linear, it is imperative that only one station is transmitting at a line when a station wants to transmit, it raises RTS, the modem turns on carrier.

The truth table for RS 232

Signal> +3V=0

Signal < - 3V=1

The output signal level usually swings between +12V and -12V. The "dead area" between +3V and -3V is designed to absorb line noise.

5.6 MAX 232

MAX 232 chips are commonly referred to as line drivers. Since the RS232 is not compatible with today's micro processors and micro controllers, we need a line driver (voltage converter) to convert the RS232's signals to TTL voltage levels that will be acceptable to the 8051's TxD and RxD pins. The MAX 232 converts from RS232 voltage levels to TTL voltage levels and viz. one advantage of the MAX 232 chip is that it uses a +5 volt power source, which is the same as the source voltage for the 8051. In other words with a signal +5 V power supply we can power both the 8051 and MAX 232, with no need for the dual power supplies that is common in many holder systems.

The MAX 232 has two sets of line drivers for transferring and receiving data. The line drivers used for TxD are called Tl and T2, while the line drivers for RxD designated as Rl and R2 In many applications only one of each is used. For example Tl and R1 are used together for TxD and RxD of the 8051 and the second set is left unused. Notice in MAX 232 that the T1line driver has a designation of Tl in and T1 out on pin numbers 11 and 14 respectively.

The T1 in pin is the TTL side and is connected to TxD of the microcontroller, while T1 out is the RS 232 side that is connected to the RxD pin of the RS 232 DB connector. The Rl line driver has a designation of Rl in :md Rl out on pin numbers 13 and 12 respectively.

The R1 in (pin 13) is the RS232 side that is connected to the TxD pin of the RS 232 DB connector and R1 out (pin 12) is the TTL side that is connected to the RXD pin of the micro controller.

MAX 232 requires four capacitors ranging from 1 to 22 μF. the most widely used value for this capacitor is 22μF.

5.7 SERIAL COMMUNICATION

To transfer to a device located many meters away, the serial data transfer is used. In serial communication, the data is sent one bit at a time. Atmel89C51 has serial communication capability built into it, thereby making possible the data transfer using only a few wire.

For serial data communication to work, the byte of data must be converted to serial bits using a parallel-in-serial-out shift register, because the micro controller is sending parallel data. Then it can be transmitted over a single data line. This also means at the receiving end there must be a serial in-parallel-out shift register.

5.7.1 SERIAL DATA TRANSFER

Serial data transfer uses two methods, Asynchronous and Synchronous. The synchronous method transfers a block of data (character) at a time while the asynchronous transfer a single byte at a time. It is possible to write software to use either of these methods, but the programs can be tedious and long. For this reason, there are special IC chips made by many manufactures for serial data communication.

These chips are to as UART (Universal Asynchronous Receiver Transmitter) and USART (Universal Synchronous-Asynchronous Receiver Transmitter).

5.7.2 ASYNCHRONOUS SERIAL COMMUNICATION

Asynchronous serial data communication is widely used for character oriented transmissions, while block -oriented data transfers use the synchronous method. In the asynchronous method, each character is placed in between a start bit and a stop bit. The start bit is always one bit but the stop bit can be one or two bits. The start bit is always a 0 (low) and the stop bit can be one (or) two bits. The start bit is always a 0 (low) and the stop bit is 1 (High).

5.7.3 DATA TRANSFER RATE

The rate of data transfer in serial data communication is stated in bps (bits per second). Another widely used technology for bps is baud rate. However, the baud rate and bps rates are not necessarily equal. This is due to the fact that baud rate is the modem terminology and is defined as the number of signal changes per second.

The data transfer rate of a given computer system depends on communication ports incorporated into that system. For e.g. the early IBM PC could transfer data at the rate of 100 to 9600 bps. Now the recent computers can transfer data at rate as high as 512 kbps. In asynchronous serial communication the baud rate is generally limited to 100,000 bps.

5.8 LCD OPERATION

The LCD's are widely used in all applications instead of LEDs or other multi segment LEDs. This is due to

- The decline prices of LCDs
- The ability to display numbers, chracters and graphics. This in contrast to LEDs, which are limited to numbers and a few chracters.
- Incorporation of a refreshing controller into LCD, thereby relieving the CPU from the task of refreshing the LCD. In contrast, the LED must be refreshed by the CPU to keep displaying the data.
- Ease of programming for chracters and graphics.

5.8.1 INITIALIZATION OF LCD

Clear display

Clears the display and returns the cursor to home position. The busy flag is kept in the Busy state (BF=1) unit initialization ends.

Function set

Sets the interface data length (DL), number of display lones (N) and

character font (F).

Entry mode set

Set the cursor move direction and specifies or not shift the display. These operation are performed during data write and read of RAM.

5.8.2 ADVANTAGES

1. Consumes much lesser energy (i.e., low power) when compared to LEDs.
2. Utilizes the light available outside an no generation of light.
3. Since very thin layer of liquid crystal is used, more suitable to act as display elements (in digital watches, pocket calculators, etc..)
4. Since reflectivity is highly sensitive to temperature, used as temperature measuring sensor.
5. Low cost.

5.8.3DISADVANTAGES

1. Angle of viewing is and external light is a must for display.
2. Since it do not generate its own light, its contrast is poor.
3. cannot be used under wide range of temperature.

5.9 POWER SUPPLY

5.9.1 Block diagram

The ac voltage, typically 220V rms, is connected to a transformer, which steps that ac voltage down to the level of the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation.

A regulator circuit removes the ripples and also remains the same dc value even if the input dc voltage varies, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of the popular voltage regulator IC units.

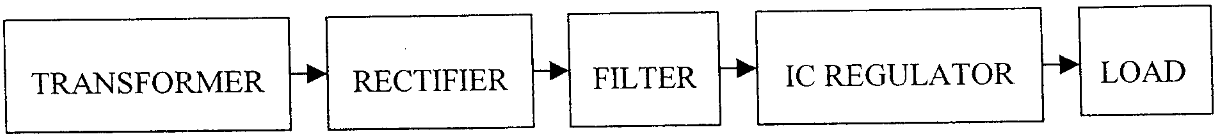


Figure 5.7 Block diagram (Power supply)

5.9.2 Working principle

Transformer

The potential transformer will step down the power supply voltage (0-230V) to (0-6V) level. Then the secondary of the potential transformer will be connected to the precision rectifier, which is constructed with the help of op–amp. The advantages of using precision rectifier are it will give peak voltage output as DC, rest of the circuits will give only RMS output.

Bridge rectifier

When four diodes are connected as shown in figure, the circuit is called as bridge rectifier. The input to the circuit is applied to the diagonally opposite corners of the network, and the output is taken from the remaining two corners.

One advantage of a bridge rectifier over a conventional full-wave rectifier is that with a given transformer the bridge rectifier produces a voltage output that is nearly twice that of the conventional full-wave circuit.

IC voltage regulators

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustably set voltage. The regulators can be selected for operation with load currents from hundreds of milli amperes to tens of amperes, corresponding to power ratings from milli watts to tens of watts.

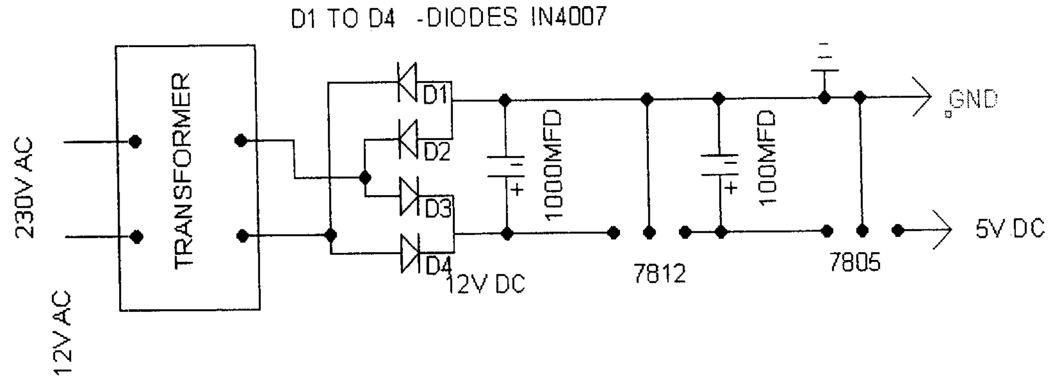


Figure 5.8 Circuit diagram (Power supply)

A fixed three-terminal voltage regulator has an unregulated dc input voltage, Vi, applied to one input terminal, a regulated dc output voltage, Vo, from a second terminal, with the third terminal connected to ground.

The series 78 regulators provide fixed positive regulated voltages from 5 to 24 volts. Similarly, the series 79 regulators provide fixed negative regulated voltages from 5 to 24 volts.

- For ICs, microcontroller, LCD --------- 5 volts
- For alarm circuit, op-amp, relay circuits ---------- 12 volts

5.10 RELAY CONTROL

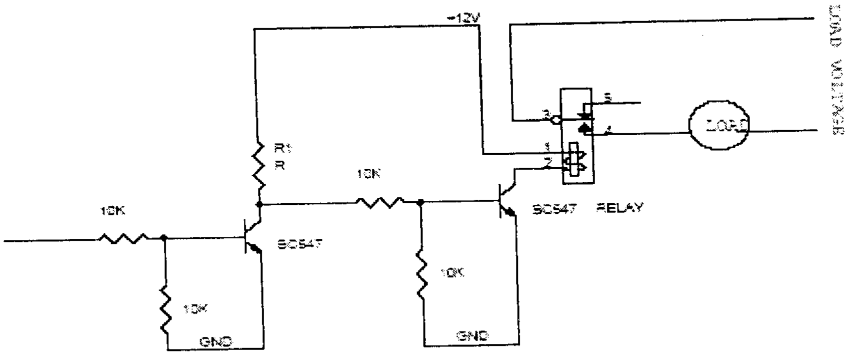


Figure 5.9 Circuit diagram (Relay control)

This circuit is designed to control the load. The load may be motor or any other load. The load is turned ON and OFF through relay. The relay ON and OFF is controlled by the pair of switching transistors (BC 547). The relay is connected in the T2 transistor collector terminal. A Relay is nothing but electromagnetic switching device which consists of three pins. They are Common, Normally close (NC) and Normally open (NO).

The relay common pin is connected to supply voltage. The normally open (NO) pin connected to load. When high pulse signal is given to base of the T1 transistors, the transistor is conducting and shorts the collector and emitter terminal and zero signals is given to base of the T2 transistor. So the relay is turned OFF state.

When low pulse is given to base of transistorT1transistor, the transistor is turned OFF. Now 12v is given to base of T2transistor so the transistor is conducting and relay is turned ON. Hencethe common terminal and NO terminal of relay are shorted. Now load gets the supply voltage through relay

5.11 RF TRANSMITTER/RECEIVER

5.11.1 RF TRANSMITTER

TWS-434:

The transmitter output is up to 8mW at 433.92MHz with a range of approximately 400 foot (open area) outdoors. Indoors, the range is approximately 200 foot, and will go through most walls.The TWS-434 transmitter accepts both linear and digital inputs, can operate from 1.5 to 12 Volts-DC.

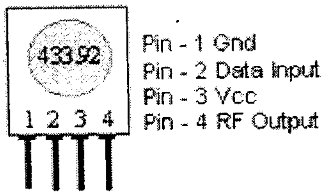
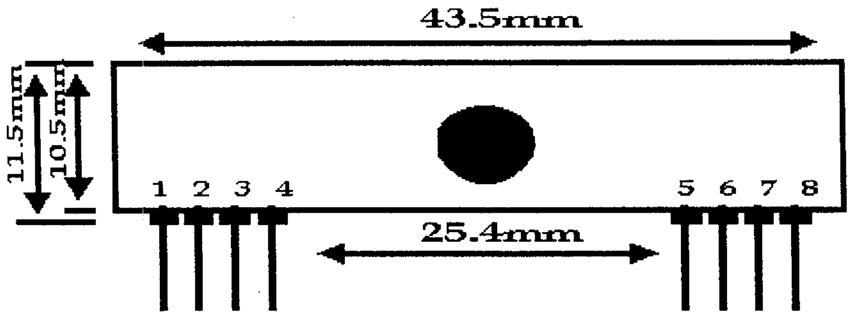


Figure 5.10 Pin details of TWS-434

The input is given at the pin 2.When a high volt is given a RF wave of 433MHz is generated. This RF wave can be transmitted by connecting antenna at pin4.

5.11.2 RF RECEIVER

The RWS-434 receiver also operates at 433.92MHz, and has a sensitivity of 3uV. The RWS-434 receiver operates from 4.5 to 5.5 volts-DC, and has both linear and digital outputs.



pin 1 : Gnd
pin 2 : DigitaL Output
pin 3 : Linear Output
pin 4 : Vcc
pin 5 : Vcc
pin 6 : Gnd
pin 7 : Gnd
pin 8 :Ant (About 30 - 35 cm)

Figure 5.11 Pin details of RWS-434

The antenna is connected to pin8. The receiver is adjusted to lock the transmitter. The digital output is taken from the pin 2. The output from pin2 is given to CIP-8D IC for decoding.

5.11.3 ENCODER AND DECODER

The CIP-8 series 8-bit encoder/decoder IC's offer an easy to use, low-cost solution for simple remote control applications in a convenient industry standard 20-pin PDIP package.

5.11.3.1 ENCODER OPERATION

On power-up the encoder enters low power sleep mode. When the transmit enable pin is pulled to ground, the encoder will wake up and begin the transmit process. First, the encoder will record the state of the 8-bit address/data lines, encode for error correction and assemble the packet. It will then sample the A0/BAUD pin to fix the data rate, and then output the address and encoded data packet on DOUT. The encode/transmit process will continue for as long as the /TE pin is low, and return to low power sleep mode when /TE returns high. It will update the state of the address and data lines with each packet and finish the current transmission even after the /TE pin is released from ground.

Encoded Data Packet

Each data packet consists of seven bytes of information to be transmitted.

- The preamble
- The synchronization byte
- The 1st address byte
- The 1st data byte
- The 2nd address byte
- The 2nd data byte
- The address/data checksum

A 10mS guard time is inserted between each encoded packet transmission to allow the decoder time to receive, decode, verify, and process each packet. The encoder returns to low power sleep mode for power conservation immediately once /TE returns to logic 1, and the packet transmission is complete.

Features

- Latched or momentary outputs
- No programming necessary
- Very easy to use
- Very low component count

- Low current consumption
- Up to 25mA per decoder output
- Eight bit data (D0 to D7)
- Eight bit binary address (0 to 255)
- Selectable baud rates (2400/4800)
- High noise immunity
- Standard 20-pin PDIP package

5.11.3.2 DECODER OPERATION

The decoder enters a timed loop waiting for the synchronization byte. An internal 16-bit timer is used to force an exit from the receive loop, and reset the output pins (in momentary mode) every 65.5mS if no valid synch byte is received during this time period. Once a valid synch byte is received, the timer is disabled, and the remainder of the data packet is received and stored for the verification process. Immediately after receiving a valid data packet it begins the process of verifying the data, and checking it for errors. Once data has been verified, the decoded data will be placed on the output pins, and the decoder re-enters the timed loop waiting for the next valid packet. If the decoder is operating in latch mode, the last valid 8-bit binary data value received will remain on the decoder outputs until a different valid binary data packet is received.

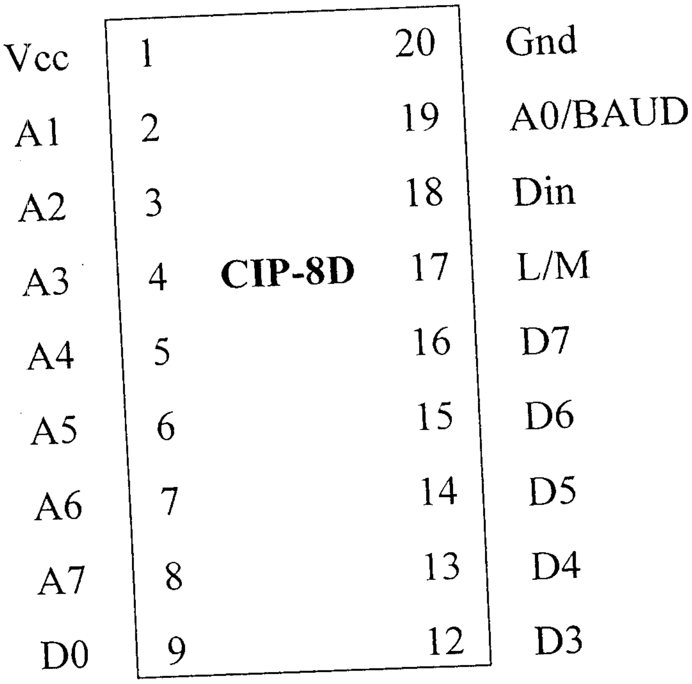


Figure 5.12 Pin details of CIP-8D

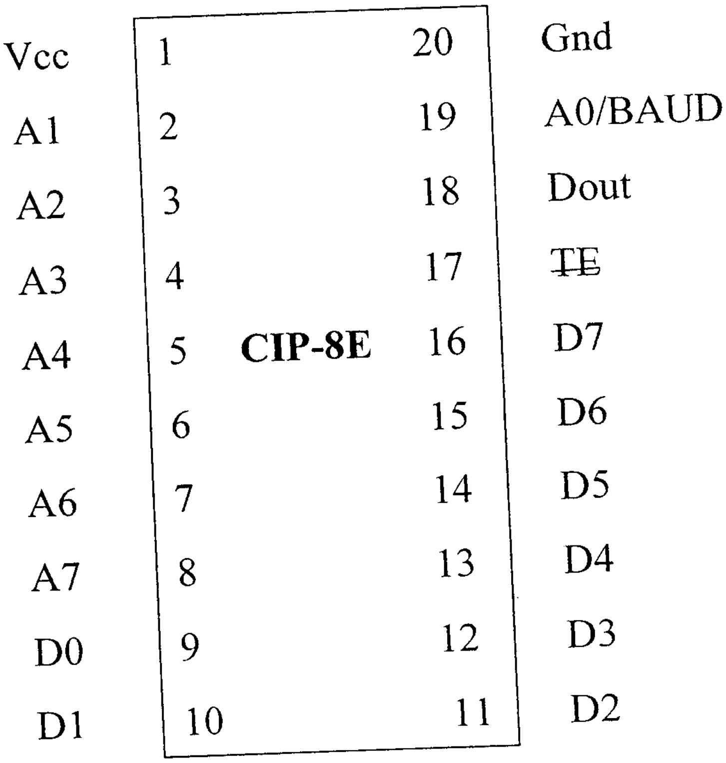


Figure 5.13 Pin details of decoder

Pin Descriptions

Pins A0 to A7 on the CIP-8 encoder and decoder IC's are used to set a unique address relationship between the encoder and decoder. This helps prevent accidental activation of decoder outputs, and allows a single encoder the ability to control multiple decoders by simply changing the encoder address to match the decoder to control. Ensure the address set on the encoder matches the decoder you wish to control. A single bit difference, and the decoder will not respond.

A0/BAUD Pin

The A0/BAUD input serves two functions. One is being the least significant bit of the 8- bit encoder/decoder address. Two is being the data rate selection pin. With A0/BAUD connected to ground, the least significant bit of the 8 bit binary address is 0, and the serial data rate is 2400bps. With this pin at Vcc, the least significant address bit is 1, and the serial data rate is 4800bps. This option allows support for lowend RF modules that require the lower data rates, while providing the faster data rate option for higher end RF modules such as the excellent Linx Technologies® LR series, and others.

Encoder & Decoder Data Pins D0-D7

On the encoder, pins D0-D7 are the data nput pins. The logic value present n these inputs will be transferred to the corresponding D0-D7 data output pins on the decoder when /TE (transmit enable) pin on the encoder is pulled to ground.

Encoder /TE Pin

TE is the transmit enable pin. This pin will cause the encoder to sample the address and data pins, and transmit continuously while held at ground. Returning /TE to Vcc through the pull-up resistor as shown in the CIP-8 example schematics will end the transmission, and place the encoder in low power sleep mode.

Decoder Latch/Momentary Modes

The decoder L/M pin provides a mode select to switch between momentary or latched decoder operating modes.

Logic 1 = Latch Mode
Logic 0 = Momentary Mode

In momentary mode, the decoder outputs that will maintain the 8-bit data value being received for the duration of valid address and data reception. If any part of the verification process fails, or reception is interrupted for longer than 65.5mS, decoder will timeout, immediately discard the packet, reset the timer, force all decoder data outputs back to ground, and re-enter the timed loop waiting for the next packet. When receiving a continuous stream of valid data, the timer is disabled, and the decoder will respond rapidly to changing data values, and hold the received binary pattern on the outputs.

All address, data, and function select pins such as TE, and L/M pins must be connected to either Vcc or ground as required. Leaving any pins floating (not connected) will cause erratic operation of the encoder, decoder, or both. Ensure that encoder data inputs D0-D7 are at the required logic levels before the /TE pin is pulled to ground. When prototyping circuits on a breadboard, it may be desirable to test logic levels on all encoder/decoder pins with a logic probe or meter before operation.

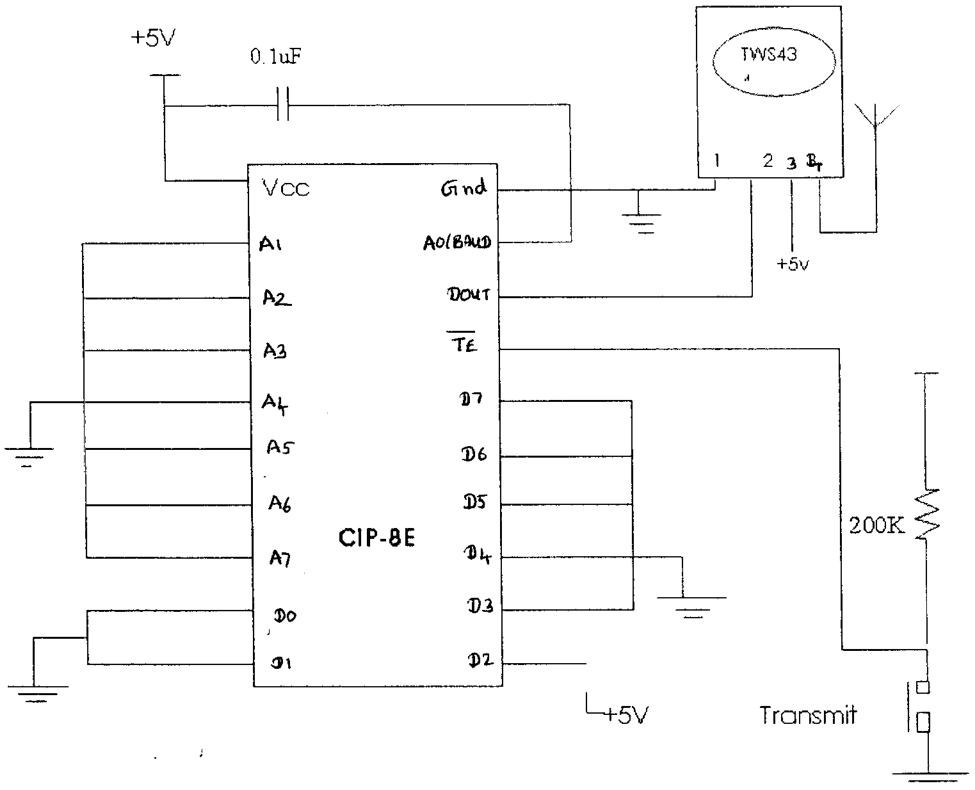


Figure 5.14 RF Transmitter circuit

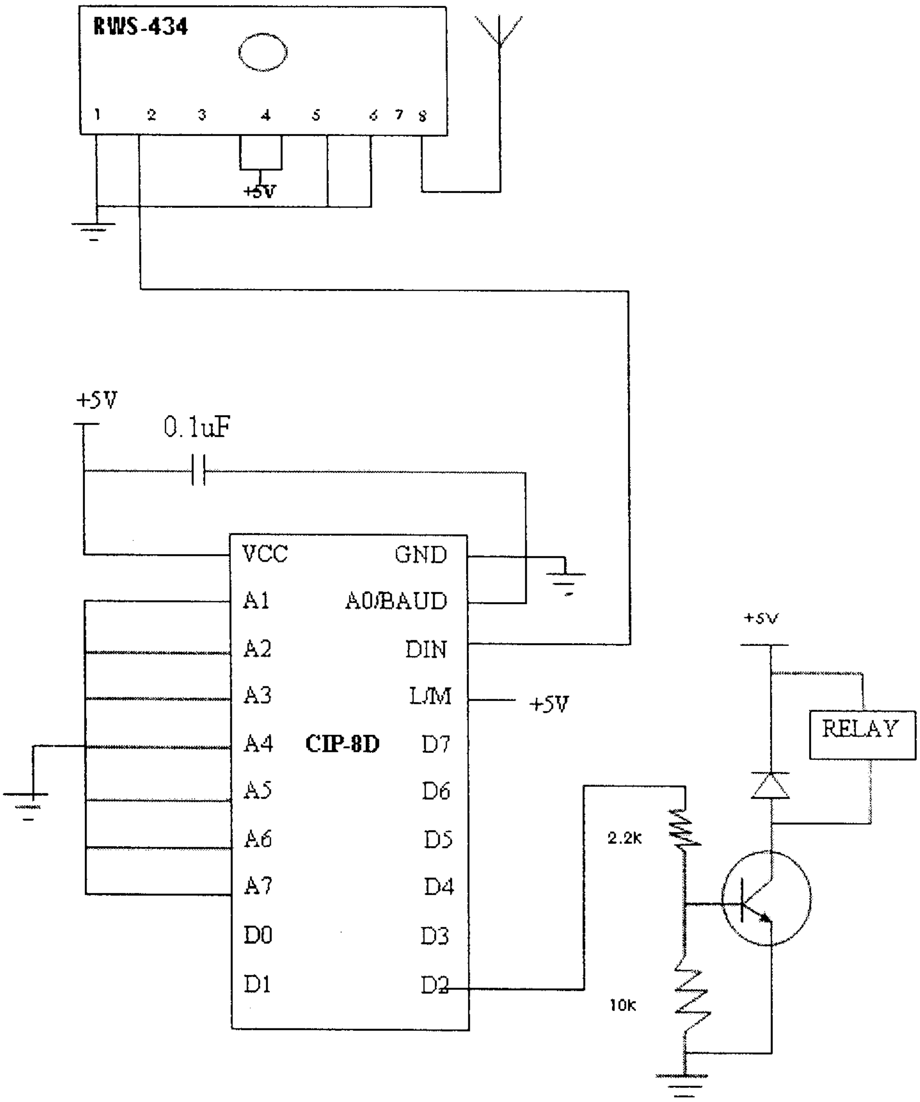


Figure 5.15 RF Receiver circuit

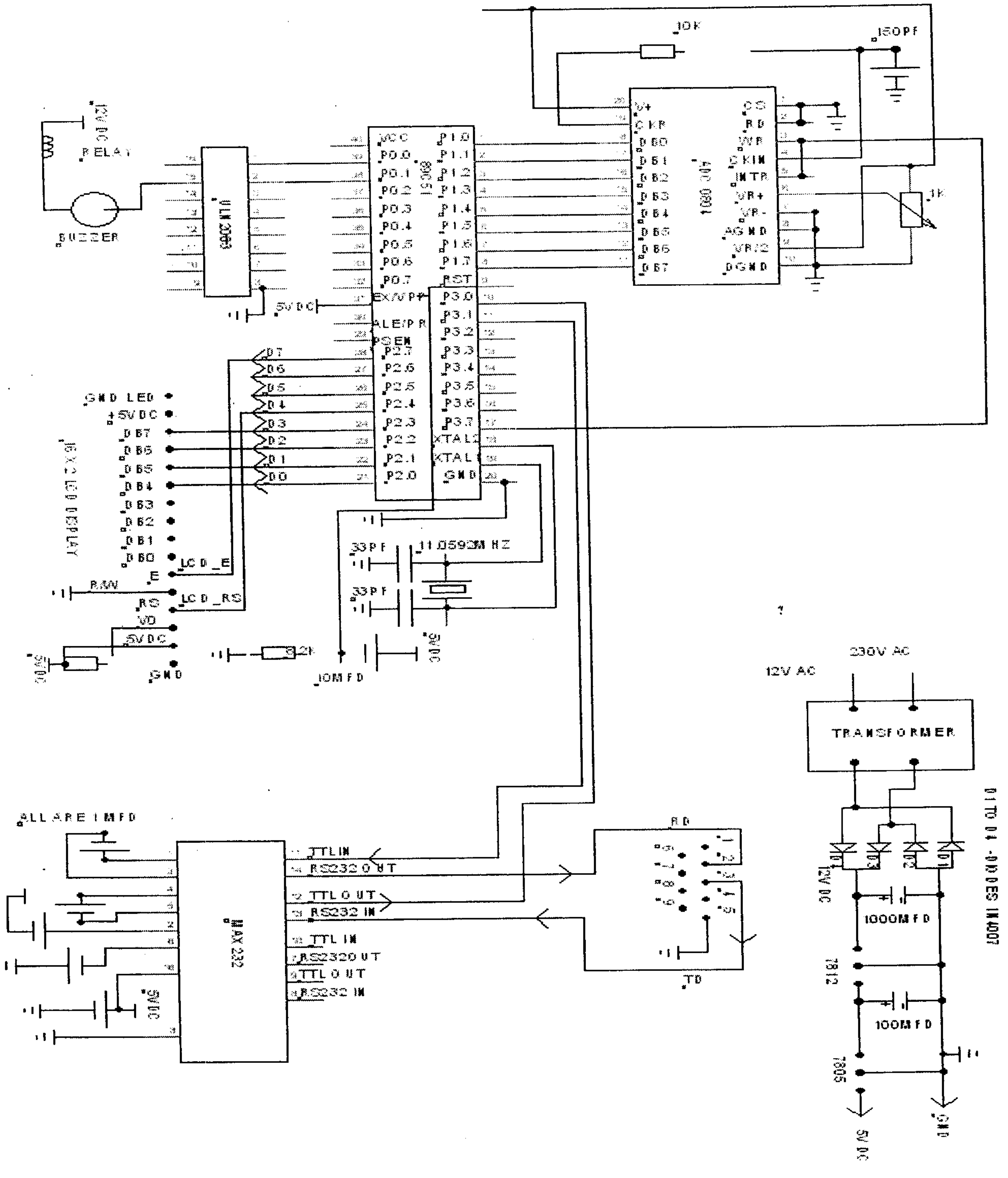


Fig 5.16 Main Board Circuit Diagram

6. PROGRAM

6.1 ALGORITHM

Starting point of program when microcontroller is reset

1. Configuring microcontroller for transmission
    1. enable timer1
    2. enter 50H to SCON for setting model transmission and enabling receive
    3. enter 40H to TMOD for setting 8bit auto reload mode and setting gate
    4. load FDH(253d) to TH1
    5. enter 80H to PCON for doubling the baud rate
2. Reset the LCD by calling Reset function
3. Initially write "LEVEL INDICATOR" to LCD by calling the appropriate function.
4. Give negative pulse to WR of ADC to get converted output through P3.7.
5. Jump to Main cycle.

Main Cycle:

1. Wait for previous serial transmission to end and deal TI flag.
2. Store the ADC data from port0 to tempADC.
3. Convert the ADC output to BCD form by calling Binary to BCD function.

4. The BCD output is stored in address stored in RO.

5. The BCD data is displayed in LCD by calling outdata function.

6. Check if ADC value is less than 50%.

    a) YES: switch ON the motor by following procedure

        i. move 000Hto Motor80

        ii. move FFH to Motordata

        iii. clear PO.0

        iv. Then test for below 40%

            YES:On the buzzer by clearing PO.1

            NO: OFF the buzzer by setting PO.1

    b) NO: check if level is greater than 80%

        YES: OFF motor by following procedure:

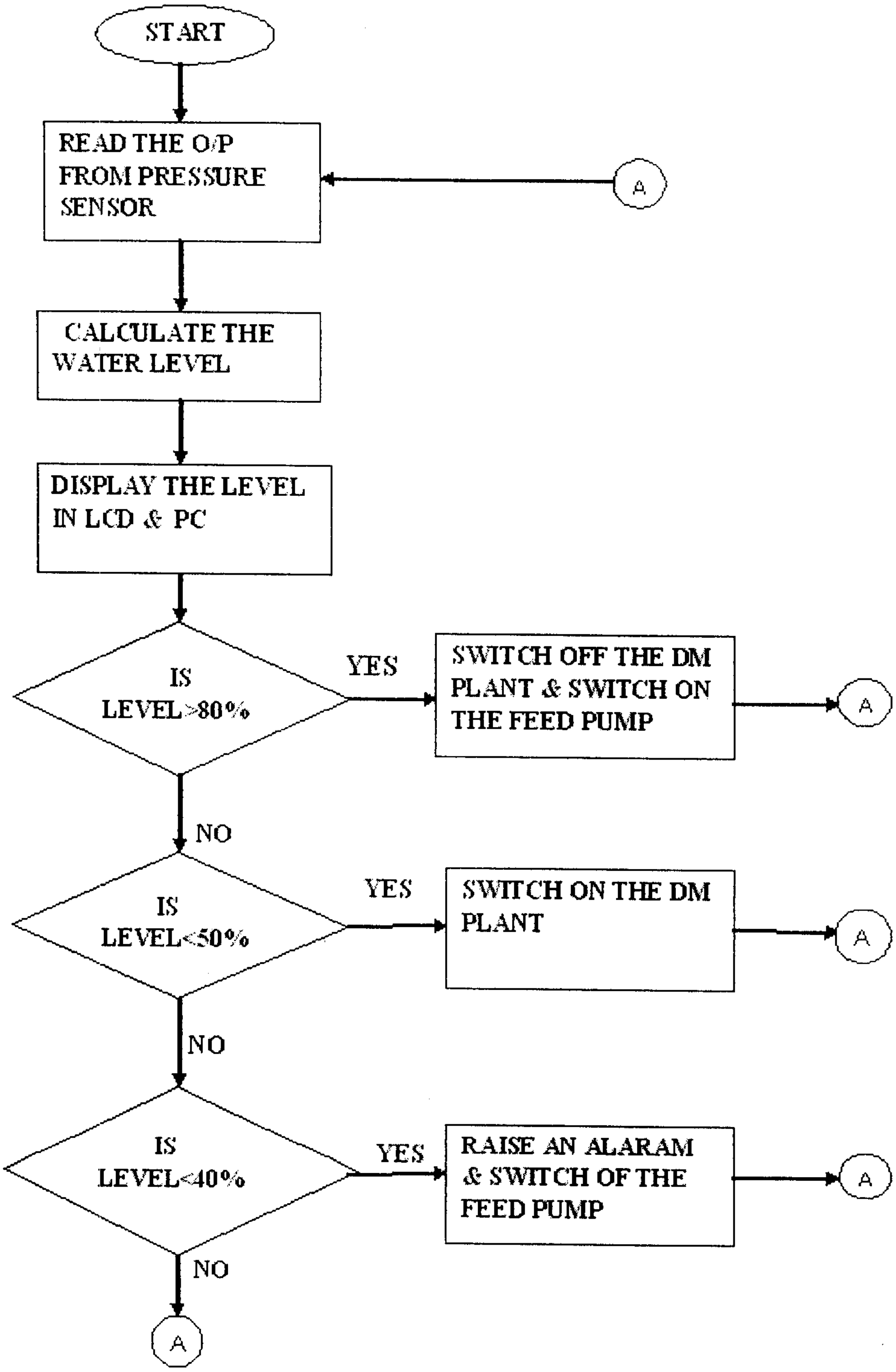
        i. move OOH to Motordata.

        ii. set PO.0

7. Send the ADC value to SBUF for serial transmission

8. Jump to maincycle

6.2 FLOWCHART



7. VISUAL BASIC

The output of the micro controller is displayed through PC an LCD. For viewing the results through PC, VISUAL BASIC program is used. The level of the water is continuously displayed in the PC.

The COM port is used connected to the reader through MAX 232. The data communication is checked through Hyper terminal.

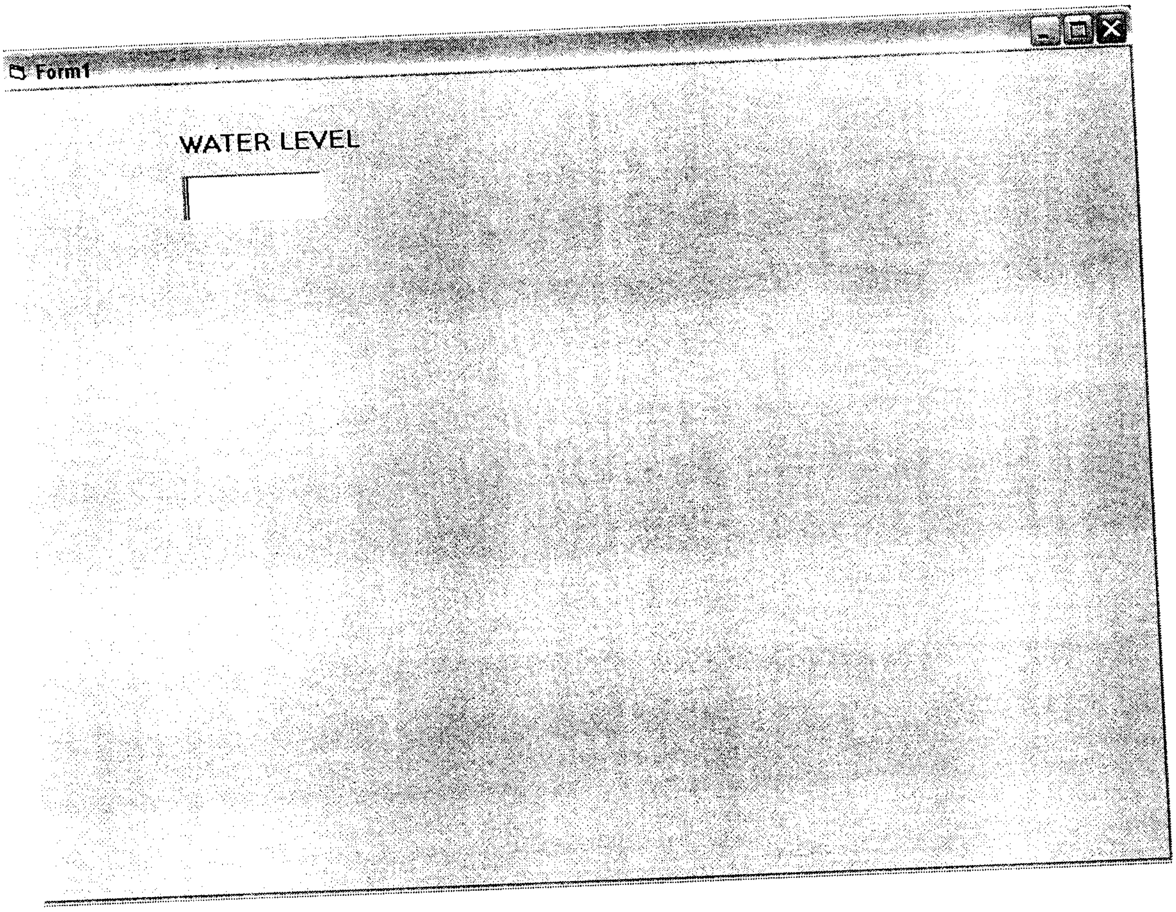
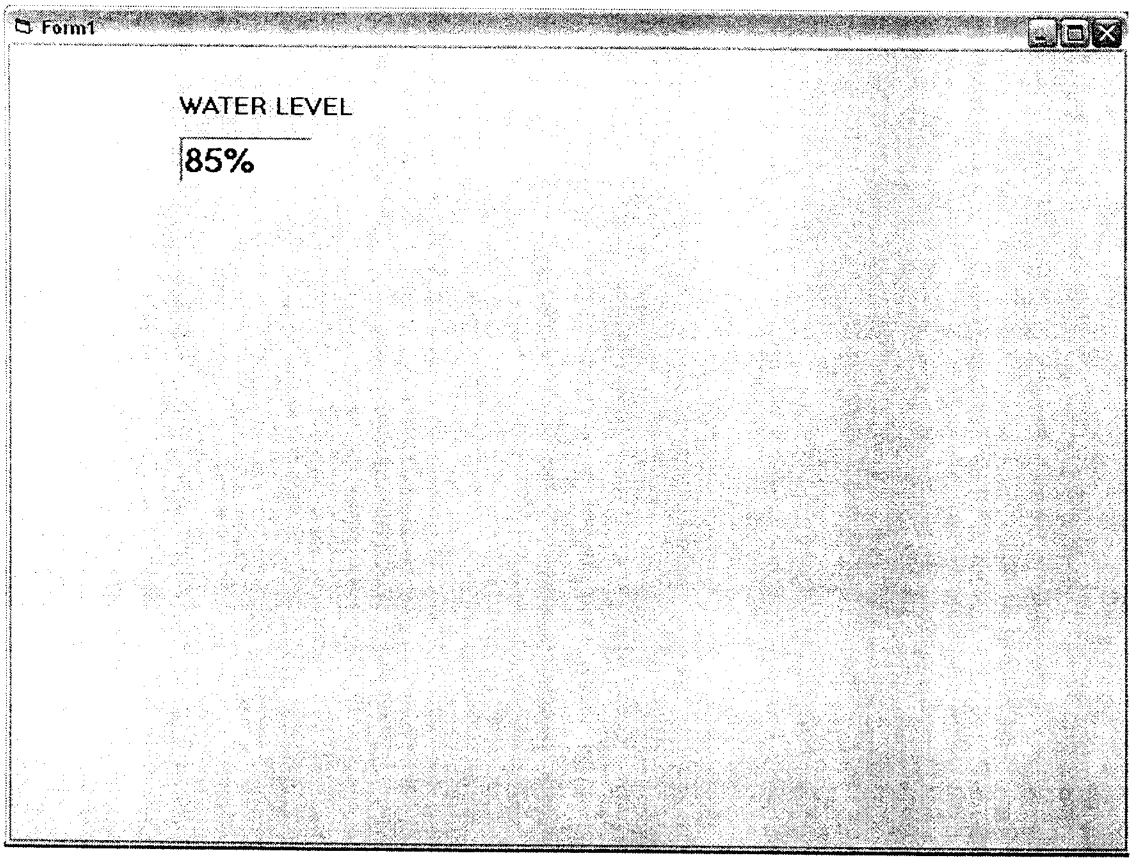


Figure7.1 Initial stage



WATER LEVEL

85%

Figure7.2 Water level displayed in PC

8. FUTURE ENHANCEMENTS

The future enhancements of this project are as follows

- Additional sensors like temperature sensor can be interfaced to process more physical quantities.
- Wireless interface to the PC may be done with the help another RF module with a microcontroller at the receiving end.
- The parameters interfaced to the PC may be represented in graphical representations for official records.

9. CONCLUSION

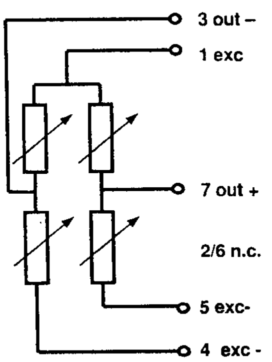
Our project reduces the human fatigue caused due the repetition of same work at regular intervals by automating the entire operation of the DM plant and the boiler feed pump. The wastage of energy caused due to unwanted functioning of feed pump and DM plant has been reduced by making them function only when necessary. Errors caused due to the analog meters have been overcome by the use of Liquid Crystal display which displays the reading in digital form. The interfacing of the parameter to the PC allows to perform manipulations and provide graphical representation which may be used for official purpose. An additional temperature sensor may also be interfaced to monitor the temperature of the DM water storage tank.

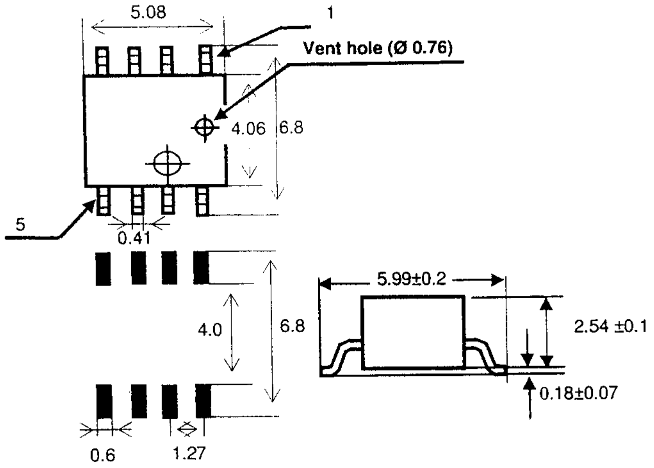
APPENDIX – DATA SHEETS

SPD015A/100A SO8

Solid State pressure sensor for Absolute pressure in SO8.

The SO8 series SPD Absolute Pressure sensors are designed for space sensitive applications and are encapsulated in a standard SO-8 package. The sensors are for use with non-corrosive and non-ionic media. Two ranges are standard available and other ranges can be made on request.





Wetted materials: PPA, silicon, glass, RTV and gold

All sizes in mm.

Parameter	Min	Typ	Max	Unit
Span				
SPD015	85	125	165	mV
SPD100	65	100	135	mV
Offset	-50	0	50	mV
TC span				
SPD 015	-10	-15	-20	%FS/100° C
SPD 100	-15	-20	-25	%FS/100 ℃
TC Offset		8		%FS/100° C (estimation)
Linearity		0.2		%FS (estimation)
Impedance	4	5	6	KΩ
Overload		x3		Rated pressure
Operating/	-40		125	℃
Storage temp				

Description

The CIP-8 series 8-bit encoder/decoder IC's offer an easy to use, low-cost solution for simple remote control applications in a convenient industry standard 20-pin PDIP package.

Encoder Operation

On power-up the encoder enters low power sleep mode. When the transmit enable pin is pulled to ground, the encoder will wake up and begin the transmit process.

First, the encoder will record the state of the 8-bit address/data lines, encode for error correction and assemble the packet.

It will then sample the A0/BAUD pin to fix the data rate, and then output the address and encoded data packet on DOUT.

The encode/transmit process will continue for as long as the /TE pin is low, and return to low power sleep mode when /TE returns high.

It will update the state of the address and data lines with each packet and finish the current transmission even after the /TE pin is released from ground.

Encoded Data Packet

Each data packet consists of seven bytes of information to be transmitted.

- The preamble
- The synchronization byte
- The 1st address byte
- The 1st data byte
- The 2nd address byte
- The 2nd data byte
- The address/data checksum

A 10mS guard time is inserted between each encoded packet transmission to allow the decoder time to receive, decode, verify, and process each packet. The encoder returns to low power sleep mode for power conservation immediately once /TE returns to logic 1, and the packet transmission is complete.

Features

- Latched or momentary outputs
- No programming necessary
- Very easy to use
- Very low component count
- Low current consumption
- Up to 25mA per decoder output
- Eight bit data (D0 to D7)
- Eight bit binary address (0 to 255)
- Selectable baud rates (2400/4800)
- High noise immunity
- Standard 20-pin PDIP package

Applications

- Simple remote control
- Wire elimination
- Remote status monitoring
- Remote lighting control

Decoder Operation

The decoder enters a timed loop waiting for the synchronization byte. An internal 16-bit timer is used to force an exit from the receive loop, and reset the output pins (in momentary mode) every 65.5mS if no valid synch byte is received during this time period.

Once a valid synch byte is received, the timer is disabled, and the remainder of the data packet is received and stored for the verification process.

Immediately after receiving a valid data packet it begins the process of verifying the data, and checking it for errors.

Once data has been verified, the decoded data will be placed on the output pins, and the decoder re-enters the timed loop waiting for the next valid packet.

If the decoder is operating in latch mode, the last valid 8-bit binary data value received will remain on the decoder outputs until a different valid binary data packet is received.

Pin Descriptions

Pins A0 to A7 on the CIP-8 encoder and decoder IC's are used to set a unique address relationship between the encoder and decoder.

This helps prevent accidental activation of decoder outputs, and allows a single encoder the ability to control multiple decoders by simply changing the encoder address to match the decoder to control.

Ensure the address set on the encoder matches the decoder you wish to control. A single bit difference, and the decoder will not respond.

A0/BAUD Pin

The A0/BAUD input serves two functions. One is being the least significant bit of the 8-bit encoder/decoder address. Two is being the data rate selection pin. With A0/BAUD connected to ground, the least significant bit of the 8-bit binary address is 0, and the serial data rate is 2400bps.

With this pin at Vcc, the least significant address bit is 1, and the serial data rate is 4800bps. This option allows support for low-end RF modules that require the lower data rates, while providing the faster data rate option for higher end RF modules such as the excellent Linx Technologies® LR series, and others.

Encoder & Decoder Data Pins D0-D7

On the encoder, pins D0-D7 are the data input pins. The logic value present on these inputs will be transferred to the corresponding D0-D7 data output pins on the decoder when /TE (transmit enable) pin on the encoder is pulled to ground.

Encoder /TE Pin

/TE is the transmit enable pin. This pin will cause the encoder to sample the address and data pins, and transmit continuously while held at ground. Returning /TE to Vcc through the pull-up resistor as shown in the CIP-8 example schematics will end the transmission, and place the encoder in low power sleep mode.

Decoder Latch/Momentary Modes

The decoder L/M pin provides a mode select to switch between momentary or latched decoder operating modes.

Logic 1 = Latch Mode
Logic 0 = Momentary Mode

In momentary mode, the decoder outputs that will maintain the 8-bit data value being received for the duration of valid address and data reception.

If any part of the verification process fails, or reception is interrupted for longer than 65.5mS, decoder will timeout, immediately discard the packet, reset the timer, force all decoder data outputs back to ground, and re-enter the timed loop waiting for the next packet.

When receiving a continuous stream of valid data, the timer is disabled, and the decoder will respond rapidly to changing data values, and hold the received binary pattern on the outputs.

Connect All Pins

All address, data, and function select pins such as /TE, and L/M pins must be connected to either Vcc or ground as required. Leaving any pins floating (not connected) will cause erratic operation of the encoder, decoder, or both.

Ensure that encoder data inputs D0-D7 are at the required logic levels before the /TE pin is pulled to ground.

When prototyping circuits on a breadboard, it may be desirable to test logic levels on all encoder/decoder pins with a logic probe or meter before operation.

VCC And Ground

VCC is the positive power supply. GND is ground.

Ordering Information	
Part #	Description
CIP-8D	8-Bit Decoder IC
CIP-8E	8-Bit Encoder IC

□

Electrical Characteristics

□

Parameter	Designation	Min.	Typ.	Max.	Units	Notes
Supply Voltage	Vcc	3.0	--	5.5	VDC	
Supply Current	IDD					
@ 3.0V VCC		---	500	TBD	µA	1
@ 5.0V VCC		---	800	TBD	µA	1
Sleep Current						
@ 3.0V VCC		---	0.1	0.85	µA	
@ 5.0V VCC		---	0.2	0.95	µA	
Input Low Voltage	VIL	GND	---	0.2 VCC	V	2
Input High Voltage	VIH	0.8 VCC	---	VCC	V	3
Output Low Voltage	VOL	---	---	0.6	V	
Output High Voltage	VOH	VCC – 0.7	---	---	V	

□

Notes

1. Current consumption with no active loads
2. For 3V supply, (0.2 x 3.0) = 0.6V max.
3. For 3V supply, (0.8 x 3.0) = 2.4V min.

Absolute Maximum Ratings

Ambient temperature under bias .... -40° to +125°C
Storage temperature .... -65°C to +150°C
Voltage on V_{DD} with respect to Vss .... -0.3V to +6.5V
Voltage on MCLR with respect to Vss .... -0.3V to +13.5V
Voltage on all other pins with respect to Vss .... -0.3V to (V_{DD} + 0.3V)
Total power dissipation .... 800 mW
Maximum current out of Vss pin .... 300 mA
Maximum current into V_{DD} pin .... 250 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > $_{DD}$) .... ± 20 mA
Output clamp current, I_{OK} (Vo < 0 or Vo V_{DD}) .... ± 20 mA
Maximum output current sunk by any I/O pin .... 25 mA
Maximum output current sourced by any I/O pin .... 25 mA
Maximum current sunk or sourced by all pins combined .... 200 mA

Disclaimer

□

These devices are not intended for use in applications of a critical nature where safety, life, or property is at risk. The user of this product assumes full liability for the use of this product in all applications. Under no conditions will Reynolds Electronics be responsible for losses arising from the use or failure of the device in any application, other than the repair, replacement, or refund limited to the original product purchase price.

□

7□F□□FD□□□SSRUW□(P DL□□WF□□ □□□WR□□FRP □
6D□□□□□D□□□□ □□□WR□□FRP □
□□WE□WR□□□T□□□□□□D□□□□ □□□WR□□FRP □
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□RS□□□□W□□ □□□□□5 □□□R□□□(□□FWR□□F□□
12300 Highway A1A
Vero Beach, Fl. 32963□
3□R□□□□□72□□89□8510□
)D□□□□72□□89□8620□
: □E□6LW□□□WS□□□□□□□□□□WR□□FRP □
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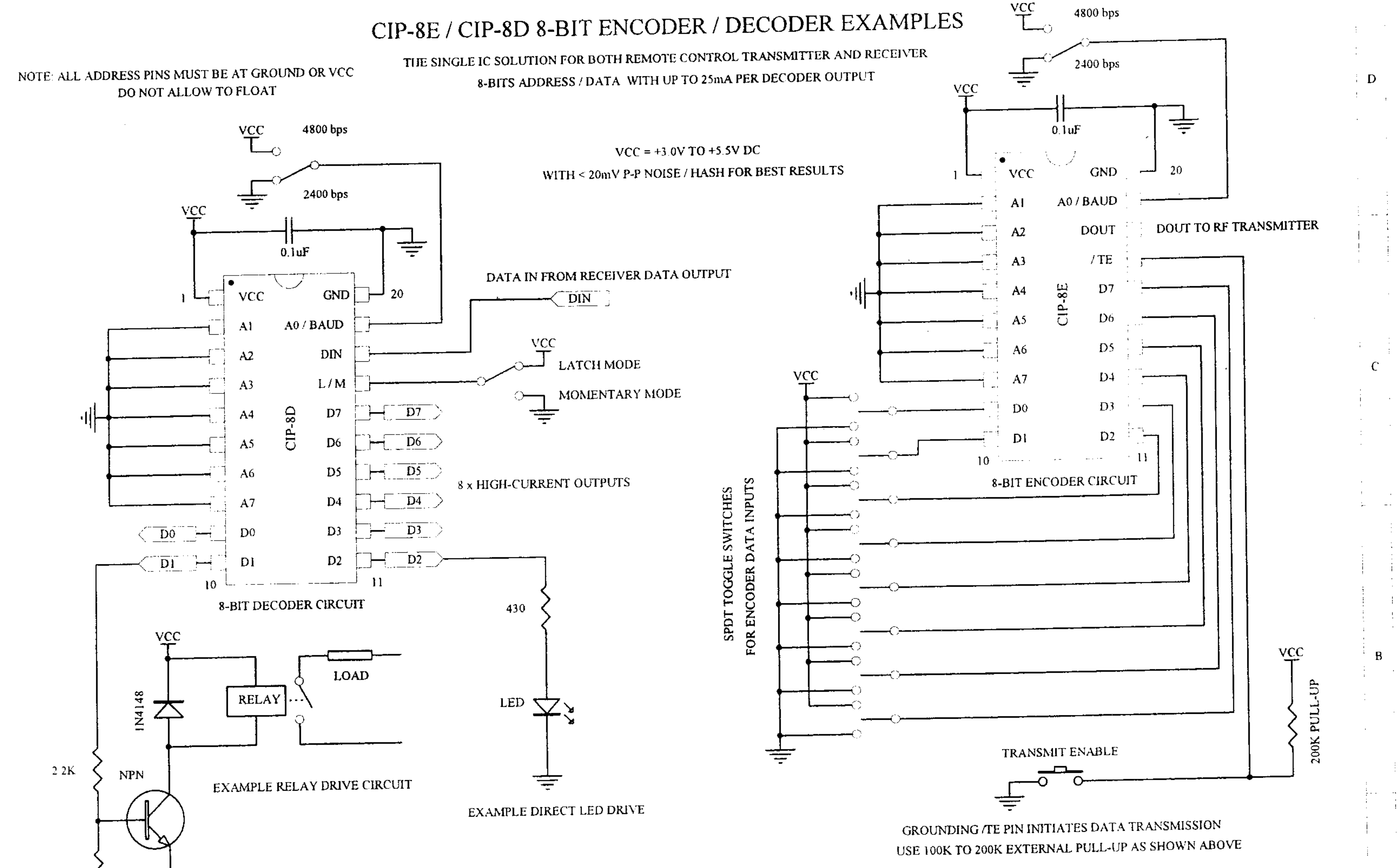
CIP-8E / CIP-8D 8-BIT ENCODER / DECODER EXAMPLES

THE SINGLE IC SOLUTION FOR BOTH REMOTE CONTROL TRANSMITTER AND RECEIVER
8-BITS ADDRESS / DATA WITH UP TO 25mA PER DECODER OUTPUT

NOTE: ALL ADDRESS PINS MUST BE AT GROUND OR VCC
DO NOT ALLOW TO FLOAT

VCC = +3.0V TO +5.5V DC
WITH < 20mV P-P NOISE / HASH FOR BEST RESULTS



GROUNDING /TE PIN INITIATES DATA TRANSMISSION
USE 100K TO 200K EXTERNAL PULL-UP AS SHOWN ABOVE

DECODER ABSOLUTE MAX DRIVE CURRENT
25 mA MAX PER OUTPUT PIN | SINK OR SOURCE | 200 mA MAX (ALL COMBINED)

ADDRESS PINS MAY BE CONNECTED TO GROUND, VCC, OR ANY COMBINATION
OF GROUND & VCC, AND SHOULD NOT BE ALLOWED TO FLOAT

12300 Highway A1A
Vero Beach, Fl 32963
Ph 772-589-8510 Fax 772-589-8620
Website http://www.rentron.com

Title: SAMPLE ENCODER / DECODER CIRCUIT SCHEMATICS
FOR 8-BIT "CIP-8E" ENCODER & "CIP-8D" DECODER IC's
Size: Orcad A
Number: CIP-8E / CIP-8D
Revision: A.1
Date: 7-Nov-2006
Sheet 1 of 1
File: C:\CAD\SCHEMATICS.Ddb
Drawn By: B. REYNOLDS

Features

- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - – Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

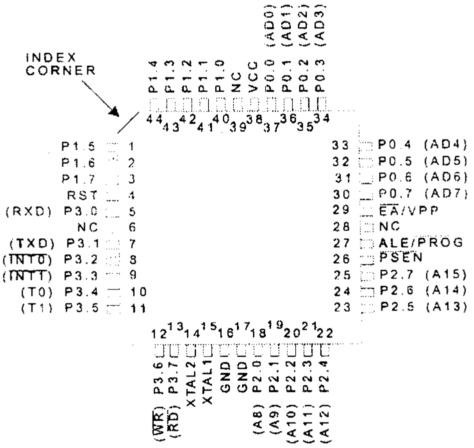
Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

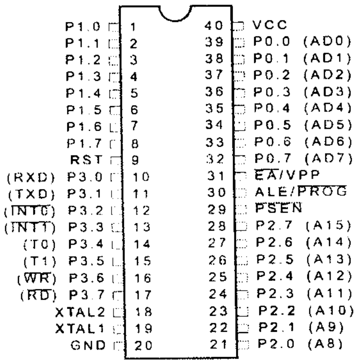
(continued)

Pin Configurations

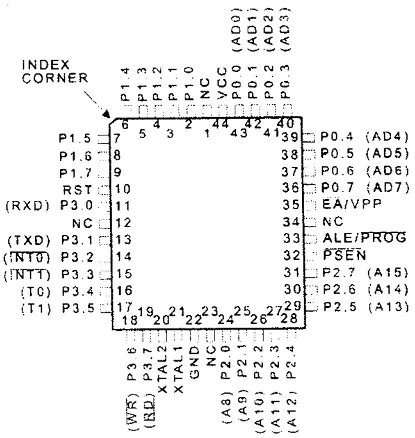
PQFP/TQFP



PDIP



PLCC

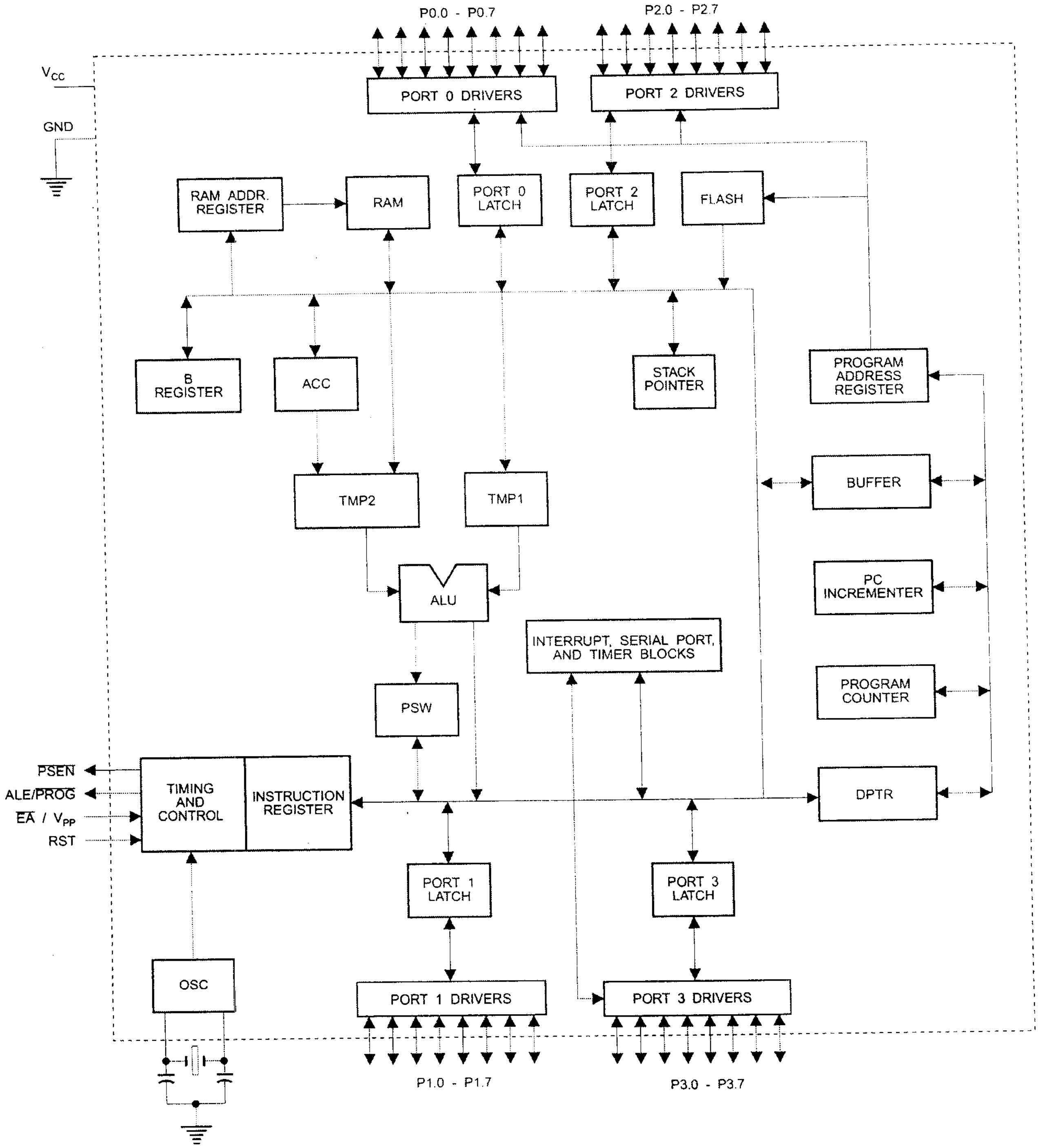


8-Bit Microcontroller with 4K Bytes Flash

AT89C51

0265F-A-12/97

ock Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
PSEN
ALE/PROG
EA / VPP
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR
PORT 1 LATCH
PORT 3 LATCH
OSC
PORT 1 DRIVERS
PORT 3 DRIVERS
P1.0 - P1.7
P3.0 - P3.7

The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

V_{CC}
Supply voltage.

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2
Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3
Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{\text{PROG}}$
Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{\text{PSEN}}$
Program Store Enable is the read strobe to external program memory.

When the AT89C51 is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

$\overline{\text{EA}}$/V$_{PP}$
External Access Enable. $\overline{\text{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be nternally latched on reset.

$\overline{\text{EA}}$ should be strapped to V$_{CC}$ for internal program executions.

This pin also receives the 12-volt programming enable voltage (V$_{PP}$) during Flash programming, for parts that require 12-volt V$_{PP}$.

XTAL1
nput to the inverting oscillator amplifier and input to the nternal clock operating circuit.

XTAL2
Output from the inverting oscillator amplifier.

Oscillator Characteristics

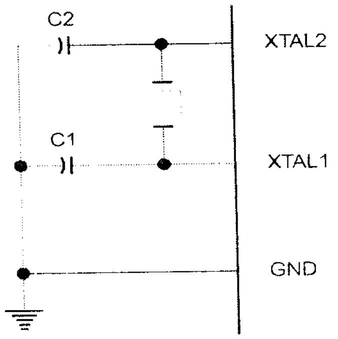
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

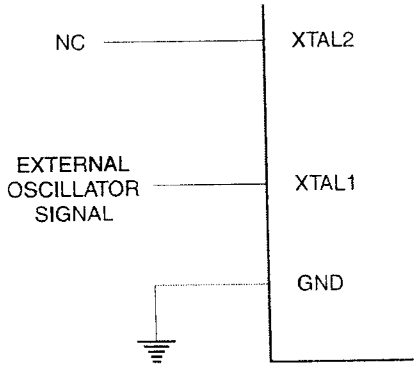
It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



Status of External Pins During Idle and Power Down Modes

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the $\overline{\text{EA}}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{\text{EA}}$ be in agreement with the current logic level at that pin in order for the device to function properly.

Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{\text{EA}}$ is sampled and latched on reset, and further programming of the Flash is disabled.
3	P	P	U	Same as mode 2, also verify is disabled.
4	P	P	P	Same as mode 3, also external execution is disabled.

Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (V_{CC}) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

	V_{PP} = 12V	V_{PP} = 5V
Top-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
Signature	(030H)=1EH (031H)=51H (032H)=FFH	(030H)=1EH (031H)=51H (032H)=05H

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{\text{EA}}$/V_{PP} to 12V for the high-voltage programming mode.
5. Pulse ALE/$\overline{\text{PROG}}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{\text{Data}}$ Polling: The AT89C51 features $\overline{\text{Data}}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{\text{Data}}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{\text{PROG}}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

Mode		RST	$\overline{\text{PSEN}}$	ALE/$\overline{\text{PROG}}$	$\overline{\text{EA}}$/V_{PP}	P2.6	P2.7	P3.6	P3.7
Write Code Data		H	L	⎺\⎽/⎺	H/12V	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit - 1	H	L	⎺\⎽/⎺	H/12V	H	H	H	H
	Bit - 2	H	L	⎺\⎽/⎺	H/12V	H	H	L	L
	Bit - 3	H	L	⎺\⎽/⎺	H/12V	H	L	H	L
Chip Erase		H	L	⎺\⎽/⎺ (1)	H/12V	H	L	L	L
Read Signature Byte		H	L	H	H	L	L	L	L

Note: 1. Chip Erase requires a 10-ms PROG pulse.

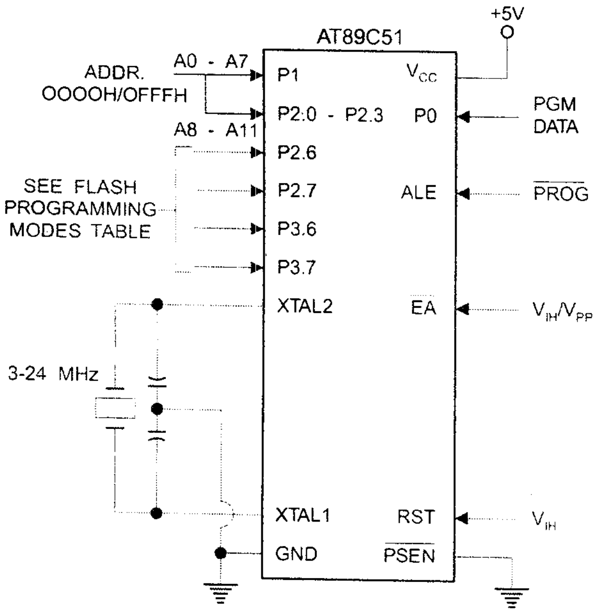


Figure 3. Programming the Flash

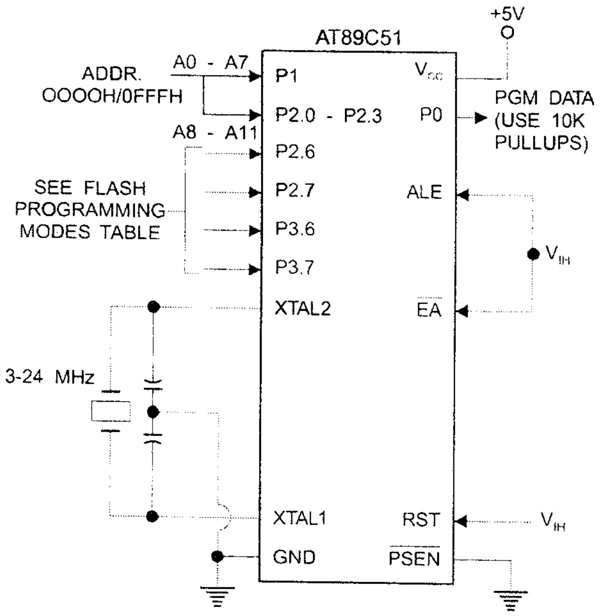


Figure 4. Verifying the Flash

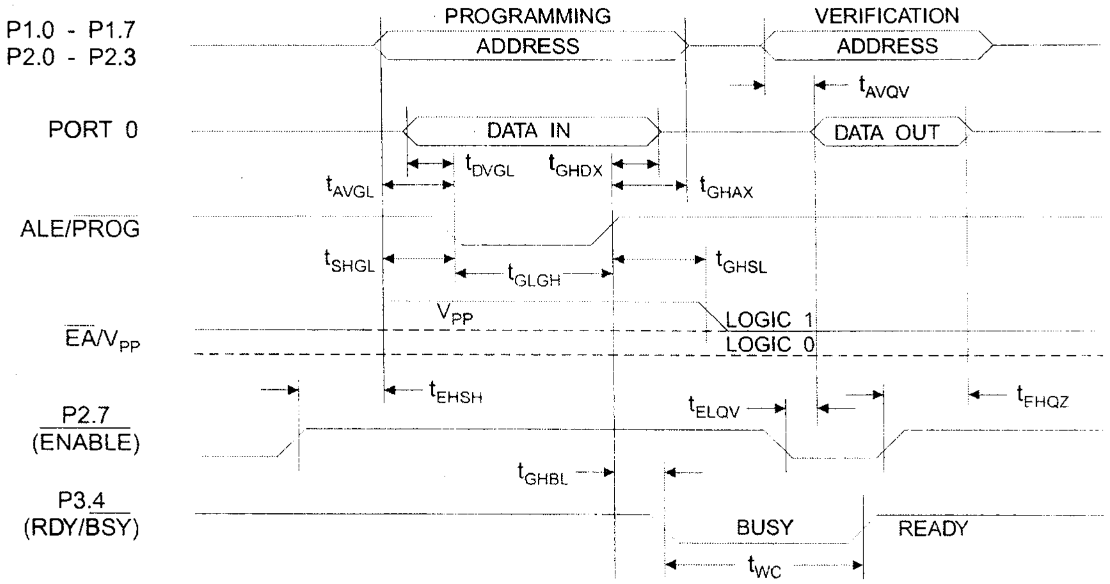
Flash Programming and Verification Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 ± 10%

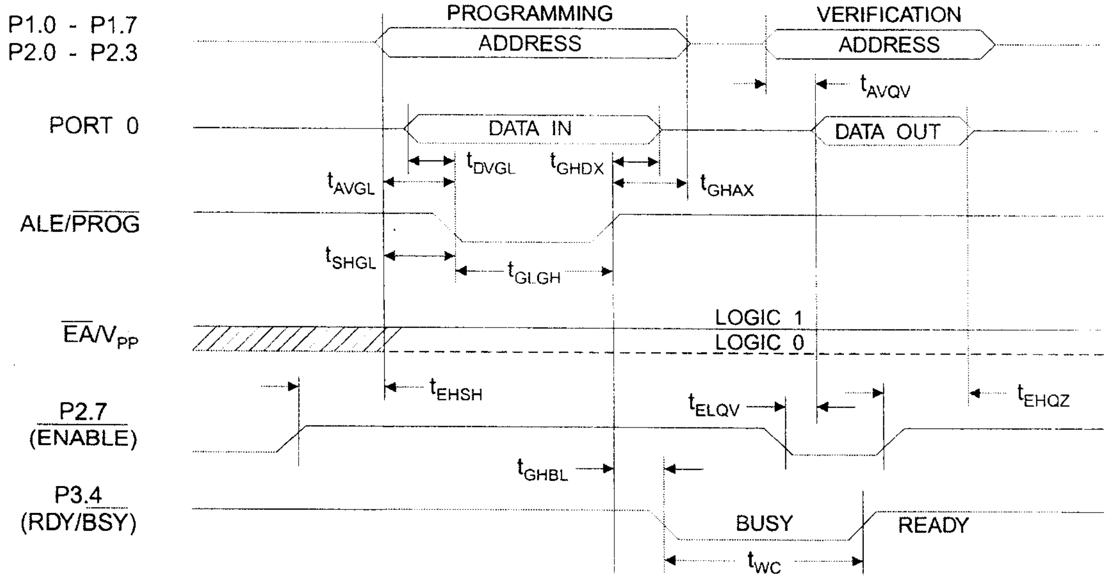
Symbol	Parameter	Min	Max	Units
V_{PP}(1)	Programming Enable Voltage	11.5	12.5	V
I_{PP}(1)	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}(1)	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Note: 1. Only used in 12-volt programming mode.

Flash Programming and Verification Waveforms - High Voltage Mode (V_{PP} = 12V)



Flash Programming and Verification Waveforms - Low Voltage Mode (V_{PP} = 5V)



Absolute Maximum Ratings*

Operating Temperature .... -55°C to +125°C

Storage Temperature .... -65°C to +150°C

Voltage on Any Pin
with Respect to Ground ....-1.0V to +7.0V

Maximum Operating Voltage.. 6.6V

DC Output Current.. 15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage(1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage(1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power Down Mode(2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power Down is 2V.

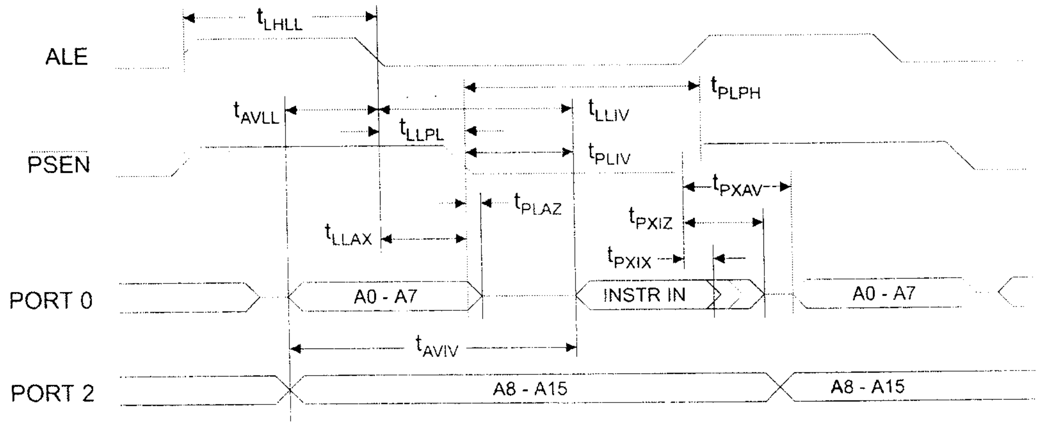
AC Characteristics

(Under Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$, and $\overline{\text{PSEN}}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

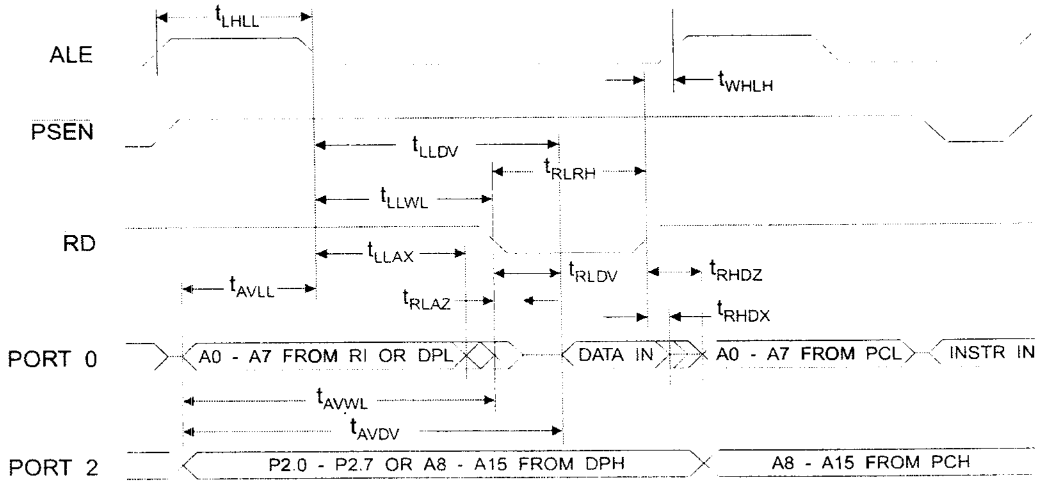
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-13		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-20		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{\text{PSEN}}$ Low	43		t_{CLCL}-13		ns
t_{PLPH}	$\overline{\text{PSEN}}$ Pulse Width	205		$3t_{CLCL}$-20		ns
t_{PLIV}	$\overline{\text{PSEN}}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
t_{PXIX}	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{\text{PSEN}}$		59		t_{CLCL}-10	ns
t_{PXAV}	$\overline{\text{PSEN}}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
t_{PLAZ}	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{\text{RD}}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{\text{WR}}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{\text{RD}}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{\text{RD}}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{\text{RD}}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{\text{WR}}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to $\overline{\text{WR}}$ High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold After $\overline{\text{WR}}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{\text{RD}}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

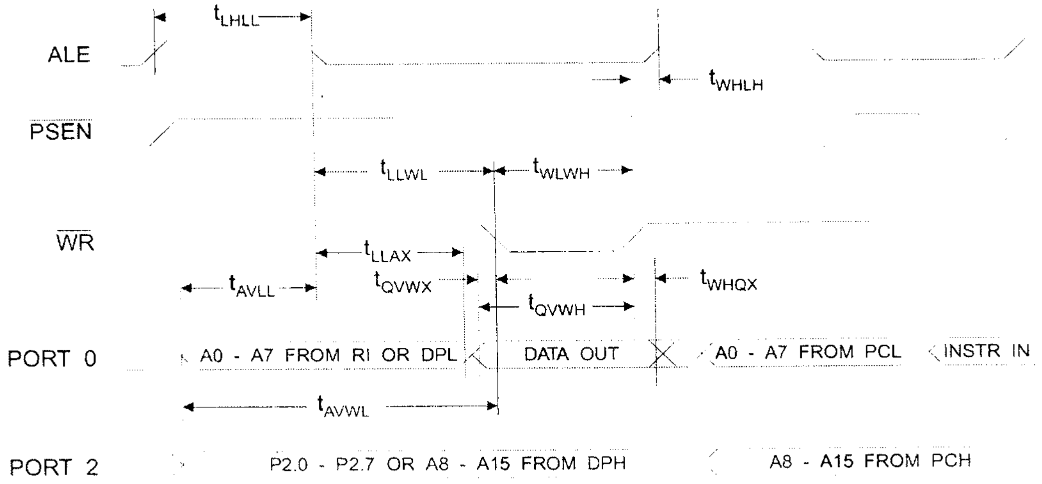
External Program Memory Read Cycle



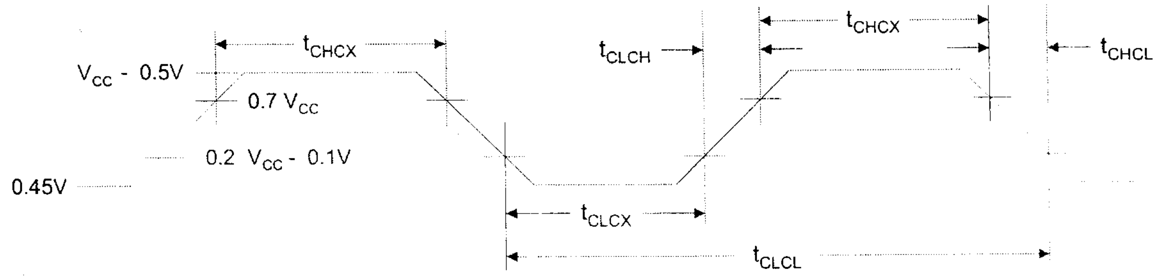
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

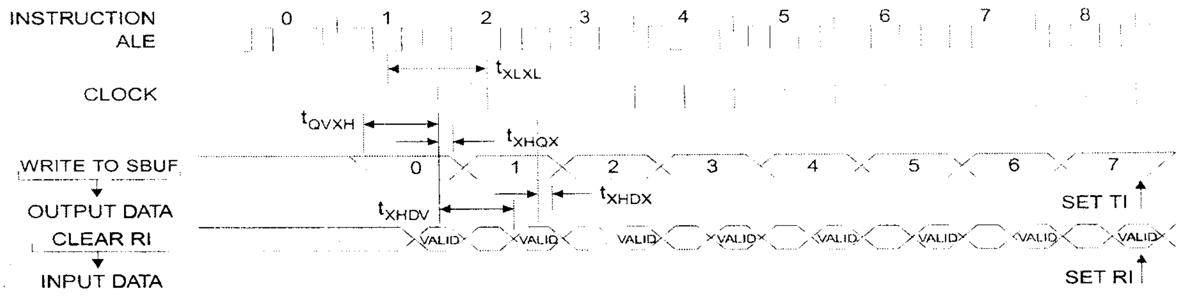
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

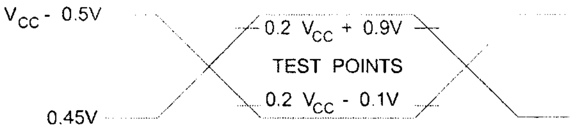
(V_{CC} = 5.0 V ± 20%; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		μs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}-133$		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}-117$		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}-133$	ns

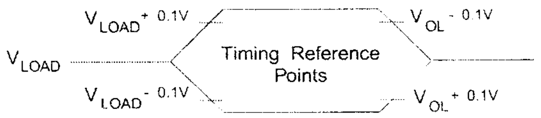
Shift Register Mode Timing Waveforms



AC Testing Input/Output Waveforms[1]



Float Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ± 20%	AT89C51-12AC	44A	Commercial
		AT89C51-12JC	44J	(0°C to 70°C)
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial
		AT89C51-12JI	44J	(-40°C to 85°C)
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
		AT89C51-12AA	44A	Automotive
		AT89C51-12JA	44J	(-40°C to 105°C)
		AT89C51-12PA	40P6	
		AT89C51-12QA	44Q	
16	5V ± 20%	AT89C51-16AC	44A	Commercial
		AT89C51-16JC	44J	(0°C to 70°C)
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial
		AT89C51-16JI	44J	(-40°C to 85°C)
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
		AT89C51-16AA	44A	Automotive
		AT89C51-16JA	44J	(-40°C to 105°C)
		AT89C51-16PA	40P6	
		AT89C51-16QA	44Q	
20	5V ± 20%	AT89C51-20AC	44A	Commercial
		AT89C51-20JC	44J	(0°C to 70°C)
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial
		AT89C51-20JI	44J	(-40°C to 85°C)
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	5V ± 20%	AT89C51-24AC	44A	Commercial
		AT89C51-24JC	44J	(0°C to 70°C)
		AT89C51-24PC	44P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial
		AT89C51-24JI	44J	(-40°C to 85°C)
		AT89C51-24PI	44P6	
		AT89C51-24QI	44Q	

Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)

REFERENCES

1. Kenneth.J. Ayala., '8051 Microcontroller – Architecture, Programming and Applications', Second Edition.

2. D.Roy Choudhury and Shail.B.Jain, "Linear Integrated Circuits", 3rd Edition, New Age International International, New Delhi.