SLIDING MODE CONTROL STRATEGY OF DYNAMIC VOLTAGE RESTORER

A Project Report

Submitted by

G.ASHA SEKAR	-	**71204105010**
V.SURIYA	-	**71204105055**
K.SWATHI	-	**71204105057**

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COIMBATORE – 641 006

ANNA UNIVERSITY: CHENNAI 600 025

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ANNA UNIVERSITY: CHENNAI 600 025

BONAFIDE CERTIFICATE

Certified that this project report entitled **" SLIDING MODE CONTROL STRATEGY OF DYNAMIC VOLTAGE RESTORER"** is the bonafide work of

MS. G.ASHA SEKAR	-	REGISTER NO. **71204105010**
MS. V.SURIYA	-	REGISTER NO. **71204105055**
MS. K.SWATHI	-	REGISTER NO. **71204105057**

who carried out the project work under my supervision.

Signature of the Head of the Department
Prof .K. Regupathy Subramanian

Signature of the Guide
Prof .K.T. Varadarajan

Certified that the candidate with university Register No. 71204105057 (71204105010, 71204105055) was examined in project viva voce Examination held on 19-4-2008

Internal Examiner

External Examiner

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING
KUMARAGURU COLLEGE OF TECHNOLOGY, COIMBATORE- 641006

ABSTRACT

Our project, "SLIDING MODE CONTROL STRATEGY OF DYNAMIC VOLTAGE RESTORER" is based on the ***IEEE*** paper (Pei Ruilin and Zhao Yuegen , 2005).

Significant deviation from the normal voltage is a problem for sensitive consumers in the grid system. Voltage sags are characterized by a reduction in voltage when the load is still connected to the supply. Voltage sags have been reported as a threat to sensitive equipments and have resulted in shut downs, loss of production and hence a major cost burden. Dynamic Voltage Restorer is an effective device to mitigate voltage sags.

The Objective of the project is to compensate voltage sag using Dynamic Voltage Restorer.

Dynamic Voltage Restorer (DVR) is one of the devices which prevents the voltage sags and improves effectively the application quality of electrical energy. It realizes that during the time electrical equipment is running, DVR compensates the difference between general voltage and fault voltage, to make them run normally.

This project implements Sliding Mode Control (SMC) method for DVR including feedback control. DVR system mainly includes energy storage device, Rectifier-inverter unit, filter, controller and series transformer. The essence of DVR is that a voltage is injected via a series connected boost transformer to achieve the load voltage previous to the voltage dip.

The summary of this project is that, the sag in the input voltage is detected, voltage difference between the normal voltage and fault voltage is calculated and fed into rectifier-inverter unit and stored. This additional voltage is fed to the line through series transformer and the voltage dip is compensated.

ACKNOWLEDGEMENT

The completion of our project can be attributed to the combined efforts made by us and the contribution made in one form or the other by the individuals we hereby acknowledge.

We are greatly indebted to our beloved Principal **Dr. JOSEPH V. THANIKAL, B.E., M.E., Ph.D., PDF., CEPIT.,** who has been the backbone of all our deeds.

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We would like to express our deep sense of gratitude and profound thanks to our guide **Prof .K.T.VARADARAJAN, M.E.**, Electrical and Electronics Engineering Department, for his valuable guidance, support, constant encouragement and co-operation rendered throughout the project.

We are also grateful to all our faculty members and the non-teaching staffs of the Department of Electrical and Electronics Engineering for their kind help and encouragement.

We extend our sincere thanks to all our parents and friends who have contributed their ideas and encouraged us for completing the project.

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CHAPTER-1

INTRODUCTION

1. INTRODUCTION

1.1 OBJECTIVE:

This project aims at improving power quality as a cost effective solution for the protection of sensitive loads from voltage sags.

1.2 NEED OF THE PROJECT:

Among all categories of electrical disturbances, the voltage dip (sag) and momentary interruption are the nemesis of the automated processes. In comparison with interruptions, voltage dips affect a larger number of customers. Modern electrical drives require high stationary precision. Power quality is obtaining increasing attention by the utilities, both the industrial and commercial electrical consumers. For higher power sensitive loads where the energy storage capabilities of Uninterruptible Power Supplies(UPS) become very costly, the Dynamic Voltage Restorer(DVR) shows promise in providing a more cost-effective solution. The DVR can be implemented at both a low voltage level as well as a medium voltage level and gives an opportunity to protect high power applications from voltage sags. The DVR uses a series connected topology to add voltage to the supply in the case when a sag is detected. This aims to protect critical loads against voltage sags. It is expected to have a better performance in compensating a broader range of voltage sags.

1.3 STATEMENT OF THE PROBLEM:

A voltage dip is commonly defined as any low voltage drop event between 10% and 90% of the nominal RMS voltage, lasting between 0.5 cycles and 1 min. The DVR is a Static Series Compensator (SSC) suitable for protecting industrial plant against voltage dip. Voltage dips are mainly caused by Single line to ground faults, symmetrical fault occurrences are relatively infrequent. Asymmetrical faults will cause unbalance and phase shift from the nominal values. Voltage dips at the customer bus are different depending upon the location in the electrical network. Large or medium power motors starting can also generate voltage dips. Hence, DVR is installed on a critical load feeder and the line voltage is restored to its nominal value within the time of a few milliseconds thus avoiding any power disruption to the load.

1.4 ORGANISATION OF THE REPORT:

CHAPTER 1:
Introduction to the project stating the problem, need for the project and objective of the work.

CHAPTER 2:
Dynamic Voltage restorer system-An overview.

CHAPTER 3:
Sliding mode control

CHAPTER 4:
Hardware implementation

CHAPTER 5:
Features of PIC microcontroller.

CHAPTER 6:
An introduction to PSIM

CHAPTER 7:
Simulation of DVR in PSIM

CHAPTER 8:
Conclusion and Recommendations.

CHAPTER-2

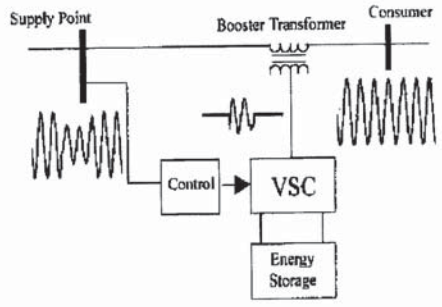
DYNAMIC VOLTAGE RESTORER SYSTEM

2.1 INTRODUCTION:

Dynamic Voltage Restorer (DVR) have been recently used as active solution for voltage sag mitigation. It is a device that injects a Dynamic controlled voltage in series to the bus voltage by means of a booster transformer. DVR installed in front of a critical load will appropriately provide correction to the load only.

The Dynamic Voltage Restorer (DVR), is designed to mitigate voltage sags on lines feeding sensitive equipment. A viable alternative to uninterruptible power systems (UPS's) and other utilization voltage solutions to the voltage sag problem, the DVR is specifically designed for large loads (2 MVA and up) served at distribution voltage. A DVR is expected to be a lower cost alternative to UPS for applications at distribution voltage. A DVR typically requires less than one-third the nominal power rating of the UPS. Also, the DVR can be used to mitigate troublesome harmonic voltages on the distribution system. The DVR is available in 2 MVA increment sizes up to 10 MVA.

The majority of voltage sags are within 40% of the nominal voltage. Therefore, by designing drives and other critical loads, capable of riding through sags, with magnitude of up to 40%, interruption of processes can be reduced significantly. The DVR can correct sags resulting from faults in either the transmission or the distribution system.



2.1 SCHEMATIC DIAGRAM OF DVR SYSTEM

2.2 VOLTAGE SAGS:

Power quality has a significant influence on high-technology equipments related to communication, advanced control, automation, precise manufacturing technique and on-line service. For example, voltage sag can have a bad influence on the products of semiconductor fabrication with considerable financial losses. Power quality problems include transients, sags, interruptions and other distortions to the sinusoidal waveform. One of the most important power quality issues is voltage sag that is a sudden short duration reduction in voltage magnitude between 10 and 90% compared to nominal voltage. Voltage sag is deemed as a momentary decrease in the rms voltage, with duration ranging from half a cycle up to one minute. Deep voltage sags, even of relatively short duration, can have significant costs because of the proliferation of voltage-sensitive computer-based and variable speed drive loads.

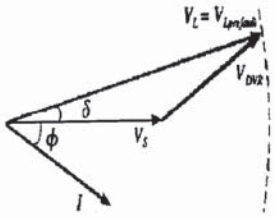
The fraction of load that is sensitive to low voltage is expected to grow rapidly in the coming decades. Studies have shown that transmission faults, while relatively rare, can cause widespread sags that may constitute a major source of process interruptions for very long distances from the faulted point. Distribution faults are considerably more common but the resulting sags are more limited in geographic extent. The majority of voltage sags are within 40%of the nominal voltage. Therefore, by designing drives and other critical loads capable of riding through sags with magnitude of up to 40%, interruption of processes can be reduced significantly. The DVR can correct sags resulting from faults in either the transmission or the distribution system.

2.3 CONVENTIONAL DVR VOLTAGE INJECTION METHODS:

The possibility of compensating voltage sag can be limited by a number of factors including finite DVR power rating, different load conditions, and different types of voltage sag. Some loads are very sensitive to phase angle jump and others are tolerant to phase angle jump. Therefore, the control strategy depends on the type of load characteristics. There are three distinguishing methods to inject DVR compensating voltage, that is, pre-sag

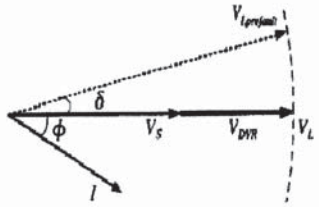
compensation method, in-phase compensation method, and phase advance method.

Pre-sag compensation methods are to track supply voltage continuously and compensate load voltage during fault to pre-fault condition. Fig. 2.2 shows the single-phase vector diagram of the pre-sag compensation. In this method, the load voltage can be restored ideally, but injected active power cannot be controlled and is determined by external conditions such as the type of faults and load condition.



2.2 VECTOR DIAGRAM OF PRE-SAG COMPENSATION

In in-phase compensation shown in Fig. 2.3 the injected DVR voltage is in phase with measured supply voltage regardless of the load current and the pre-fault voltage. The advantage of this method is that magnitude of injected DVR voltage is minimized for constant load voltage magnitude.

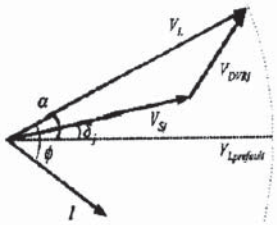


2.3VECTOR DIAGRAM OF IN-PHASE COMPENSATION

Pre-sag compensation and in-phase compensation must inject active power to loads almost all the time. However, the amount of possible injection active power is confined to the stored energy in DC link, which is one of the most expensive components in DVR. Due to the limit of energy storage capacity of DC link, the DVR restoration time and performance are confined in these methods.

For the sake of controlling injection energy, phase advance method was proposed (Fig. 2.4).The injection active power is made zero by means of having the injection voltage phasor perpendicular to the load current phasor. This method can reduce the consumption of energy stored in DC link by injecting reactive power instead of active power. Reducing energy consumption means that ride-through ability is increased when the energy storage capacity is fixed. On the other hand, the injection voltage magnitude of phase advance method is larger than those of pre-sag or in-phase method and the voltage phase shift can cause voltage waveform discontinuity, inaccurate zero crossing, and load power swing. Therefore, phase

advance method should be adjusted to the load that is tolerant to phase angle jump, or transition period should be taken while phase angle is moved from pre-fault angle to advance angle.



2.4VECTOR DIAGRAM OF PHASE ADVANCE COMPENSATION

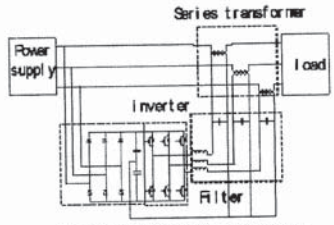
CHAPTER-3

SLIDING MODE CONTROL

3. SLIDING MODE CONTROL

3.1 INTRODUCTION:

The main circuit of DVR is shown below.



3.1 MAIN CIRCUIT OF DVR SYSTEM

This circuit is implemented in POWER SIMULATOR using the necessary components in it. The overall circuit is split into various blocks. Each block is simulated separately and the results are verified.

Until now, DVR control strategy consists of two kinds: Forward-feed control and feedback control. The feedback control methods mainly use PI control which include output voltage feedback for single loop control, and voltage and current feedback for double loop control.

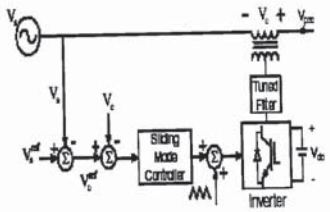
3.2 FORWARD-FEED CONTROL:

Forward feed control is defined as the difference between reference voltage and measuring voltage for system. According to the calculation of inverter to obtain the benchmark signal of voltage compensation, drive inverter injects the voltage compensation to system by the drive pulse with PWM. The above method have some advantages, such as swiftness speed response for dynamics quality and easy control.

3.3 FEED BACK CONTROL:

Feedback control comprises two spices: voltage feedback control and current feedback control. Single loop voltage control and double loop current control is widely used. In this case single loop voltage feedback control is used.

The feedback control methods mainly use PI control which include output voltage feedback for single loop control, and voltage and current feedback for double loop control.



3.2 CONTROL CIRCUIT OF DVR

CHAPTER-4

HARDWARE IMPLEMENTATION

4. HARDWARE IMPLEMENTATION

4.1 INTRODUCTION:

A voltage dip is commonly defined as any low voltage drop event between 10% and 90% of the nominal RMS voltage, lasting between 0.5 cycles and 1 min. The voltage sags exist for very short duration of time and hence they cannot be practically implemented. Due to this difficulty, the hardware is implemented for compensating voltage drop. The components and the operation of the hardware is explained below.

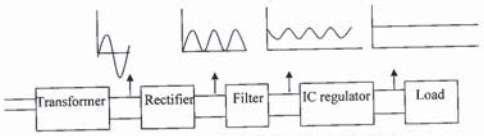
4.2 POWER SUPPLIES:

4.2.1 BLOCK DIAGRAM:

The present chapter introduces the operation of power supply circuits built using filters, rectifiers, and then voltage regulators. Starting with an ac voltage, a steady dc voltage is obtained by rectifying the ac voltage, then filtering to a dc level, and finally, regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies, or the output load connected to the dc voltage changes.

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in fig 19.1. The ac voltage, typically 120 V rms, is connected to a transformer, which steps that ac voltage down to the level for the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has

some ripple or ac voltage variation. A regulator circuit can use this dc input to provide a dc voltage that not only has much less ripple voltage but also remains the same dc value even if the input dc voltage varies somewhat, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units.



4.1 BLOCK DIAGRAM OF POWER SUPPLY

4.2.2 WORKING PRINCIPLE:

TRANSFORMER:

The potential transformer will step down the power supply voltage (0-230V) to (0-6V) level. Then the secondary of the potential transformer will be connected to the precision rectifier, which is constructed with the help of op-amp. The advantages of using precision rectifier are it will give peak voltage output as DC, rest of the circuits will give only RMS output.

BRIDGE RECTIFIER:

When four diodes are connected as shown in figure, the circuit is called as bridge rectifier. The input to the circuit is applied to the diagonally opposite corners of the network, and the output is taken from the remaining two corners.

Let us assume that the transformer is working properly and there is a positive potential, at point A and a negative potential at point B. the positive potential at point A will forward bias D3 and reverse bias D4.

The negative potential at point B will forward bias D1 and reverse D2. At this time D3 and D1 are forward biased and will allow current flow to pass through them; D4 and D2 are reverse biased and will block current flow.

The path for current flow is from point B through D1, up through RL, through D3, through the secondary of the transformer back to point B. this path is indicated by the solid arrows. Waveforms (1) and (2) can be observed across D1 and D3.

One-half cycle later the polarity across the secondary of the transformer reverse, forward biasing D2 and D4 and reverse biasing D1 and D3. Current flow will now be from point A through D4, up through RL, through D2, through the secondary of T1, and back to point A. This path is indicated by the broken arrows. Waveforms (3) and (4) can be observed across D2 and D4. The current flow through RL is always in the same direction. In flowing through RL this current develops a voltage corresponding to that shown waveform (5). Since current flows through the load (RL) during both half cycles of the applied voltage, this bridge rectifier is a full-wave rectifier.

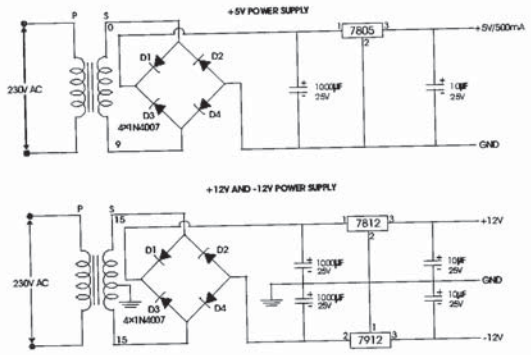
One advantage of a bridge rectifier over a conventional full-wave rectifier is that with a given transformer the bridge rectifier produces a voltage output that is nearly twice that of the conventional full-wave circuit.

This may be shown by assigning values to some of the components shown in views A and B. assume that the same transformer is used in both circuits. The peak voltage developed between points X and y is 1000 volts in both circuits. In the conventional full-wave circuit shown—in view A, the peak voltage from the center tap to either X or Y is 500 volts. Since only one diode can conduct at any instant, the maximum voltage that can be rectified at any instant is 500 volts.

The maximum voltage that appears across the load resistor is nearly-but never exceeds-500 v0lts, as result of the small voltage drop across the diode. In the bridge rectifier shown in view B, the maximum voltage that can be rectified is the full secondary voltage, which is 1000 volts. Therefore, the peak output voltage across the load resistor is nearly 1000 volts. With both circuits using the same transformer, the bridge rectifier circuit produces a higher output voltage than the conventional full-wave rectifier circuit.

IC VOLTAGE REGULATORS:

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustably set voltage. The regulators can be selected for operation with load currents from hundreds of milli-amperes to tens of amperes, corresponding to power ratings from milli-watts to tens of watts.



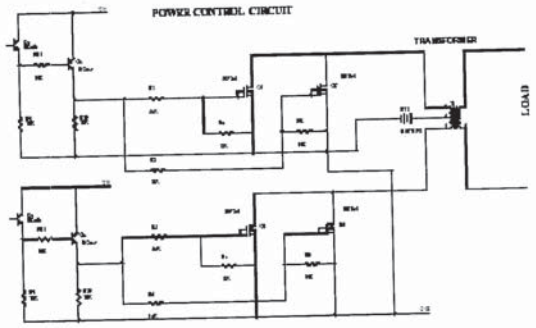
4.2 CIRCUIT DIAGRAM (POWER SUPPLY)

A fixed three-terminal voltage regulator has an unregulated dc input voltage, Vi, applied to one input terminal, a regulated dc output voltage, Vo, from a second terminal, with the third terminal connected to ground.

The series 78 regulators provide fixed positive regulated voltages from 5 to 24 volts. Similarly, the series 79 regulators provide fixed negative regulated voltages from 5 to 24 volts.

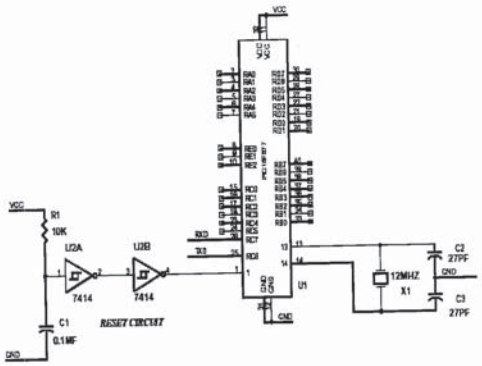
- For ICs, microcontroller, LCD --------- 5 volts
- For alarm circuit, op-amp, relay circuits ---------- 12 volts

4.3 PWM SINE WAVE INVERTER MODULE:



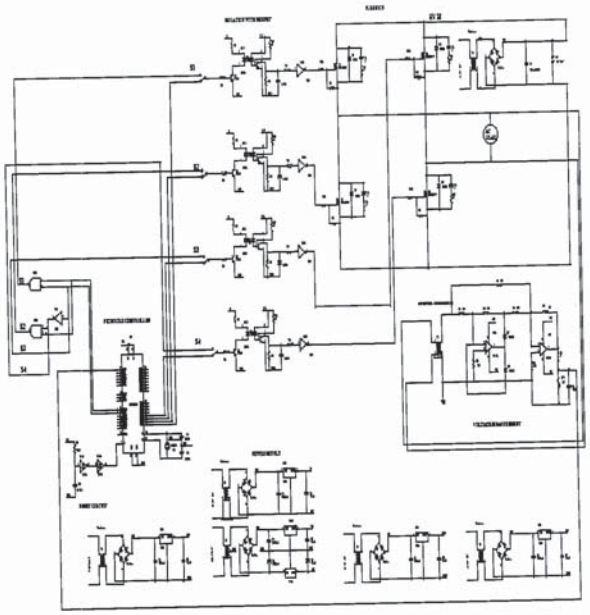
4.3 SINE WAVE INVERTER MODULE

4.4 PIC MICROCONTROLLER MODULE:



4.4 PIC MICROCONTROLLER MODULE

4.5 OVERALL CIRCUIT:



4.5 OVERALL CIRCUIT

4.5.1 OPERATION:

When there is a voltage drop in the transmission line, it is measured and fed back to PIC microcontroller. In PIC, the difference between the drop voltage and required voltage is found and corresponding firing pulses are generated. These pulses are fed to inverter which produces desired output voltage. Hence, the voltage drop is compensated.

In PIC microcontroller pulses are generated in 15 and 16th pin. These pulses are logically connected to rectifier-inverter circuit through opto-coupler. The opto-coupler isolates the MOSFET from power supply distortions. The pulse is rectified and then inverted to remove ripples. From inverter it is fed to load.

The firing pulses are fed to MOSFET inverter through switches. These pulses are generated in PIC microcontroller using C program. The voltage from load is measured using potential transformer and fed back to PIC microcontroller.

Hence, when a drop occurs it is detected from measurements of potential transformer and in PIC microcontroller the corresponding firing pulses are generated to modify MOSFET output and hence to compensate the drop.

CHAPTER-5

FEATURES OF PIC MICROCONTROLLER

5. PIC MICROCONTROLLER

5.1 CONCEPTS OF MICROCONTROLLER:

Microcontroller is a general purpose device, which integrates a number of the components of a microprocessor system on to single chip. It has inbuilt CPU, memory and peripherals to make it as a mini computer. A microcontroller combines on to the same microchip:

- The CPU core
- Memory(both ROM and RAM)
- Some parallel digital i/o

5.2 INTRODUCTION TO PIC:

The microcontroller that has been used for this project is from PIC series. PIC microcontroller is the first RISC based microcontroller fabricated in CMOS (complimentary metal oxide semiconductor) that uses separate bus for instruction and data allowing simultaneous access of program and data memory.

The main advantage of CMOS and RISC combination is low power consumption resulting in a very small chip size with a small pin count. The main advantage of CMOS is that it has immunity to noise than other fabrication techniques.

5.2.1 PIC (16F877):

Various microcontrollers offer different kinds of memories. EEPROM, EPROM, FLASH etc. are some of the memories of which FLASH is the most recently developed. Technology that is used in pic16F877 is flash technology, so that data is retained even when the power is switched off. Easy Programming and Erasing are other features of PIC 16F877.

5.3 CORE FEATURES:

- High-performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory,
  Up to 368 x 8 bytes of Data Memory (RAM)
  Up to 256 x 8 bytes of EEPROM data memory
- Pin out compatible to the PIC16C73/74/76/77
- Interrupt capability (up to 14 internal/external
- Eight level deep hardware stack
- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC Oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS EPROM/EEPROM technology
- Fully static design
- In-Circuit Serial Programming (ICSP) via two pins
- Only single 5V source needed for programming capability
- In-Circuit Debugging via two pins
- Processor read/write access to program memory
- Wide operating voltage range: 2.5V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial and Industrial temperature ranges

- Low-power consumption:
  < 2mA typical @ 5V, 4 MHz
  20mA typical @ 3V, 32 kHz
  < 1mA typical standby current

5.4 PERIPHERAL FEATURES:

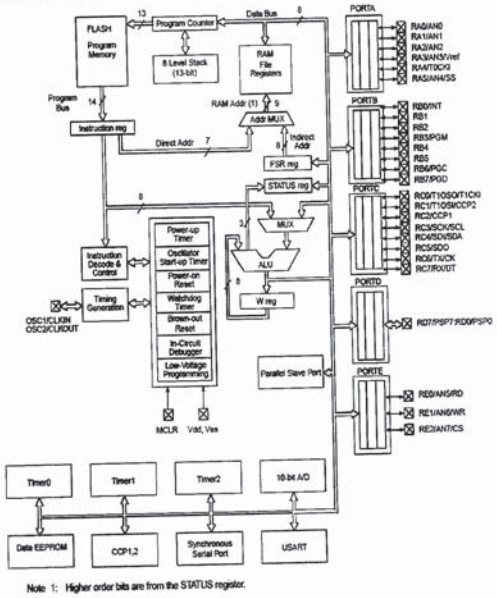
- Timer0: 8-bit timer/counter with 8-bit pre-scaler
- Timer1: 16-bit timer/counter with pre-scaler, can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, pre-scaler and post- scaler.
- Two Capture, Compare, PWM modules
  Capture is 16-bit, max resolution is 12.5 ns,
  Compare is 16-bit, max resolution is 200 ns,
  PWM max. resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI. (Master Mode) and I2C. (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9- bit address detection.
- Brown-out detection circuitry **for Brown-out Reset (BOR)**

5.5 SPECIFICATIONS:

DEVICE	PROGRAM FLASH	DATA MEMORY	DATA EEPROM
PIC 16F877	8K	368 Bytes	256 Bytes

5.6 ARCHITECTURE OF PIC 16F877 :

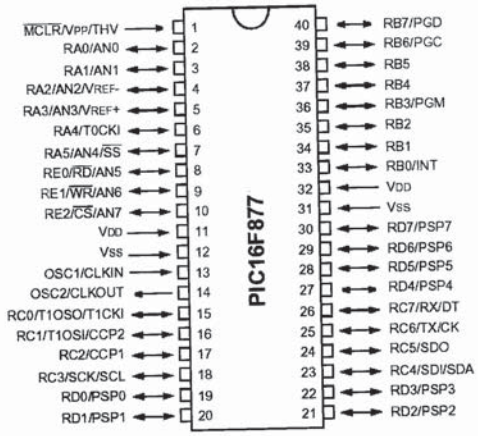
The complete architecture of PIC 16F877 is shown in the fig 2.1. Table 2.1 gives details about the specifications of PIC 16F877. Fig 2.2 shows the complete pin diagram of the IC PIC 16F877.



Note 1: Higher order bits are from the STATUS register.

5.1 ARCHITECTURE OF PIC 16F877

5.7 PIN DIAGRAM:



5.2 PIN DIAGRAM OF PIC 16F877

CHAPTER-6

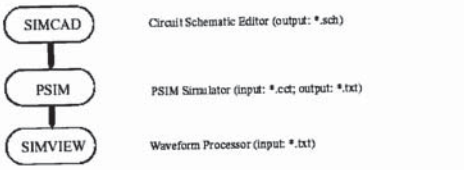
AN INTRODUCTION TO PSIM

6. PSIM INTRODUCTION

6.1 POWER SIMULATOR:

PSIM is a simulation package specifically designed for power electronics and motor control. With fast simulation, friendly user interface and waveform processing, PSIM provides a powerful simulation environment for power converter analysis, control loop design, and motor drive system studies.

The PSIM simulation package consists of three programs: circuit schematic editor SIMCAD*, PSIM simulator, and waveform processing program SIMVIEW*. The simulation environment is illustrated as follows.

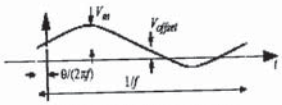


6.2 SOFTWARE/HARDWARE REQUIREMENT:

PSIM runs in Microsoft Windows 95 or NT on PC computers. The RAM memory requirements 16 MB.

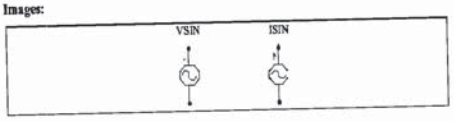
6.3 ELEMENTS USED IN THE PROJECT:

6.3.1 SINUSOIDAL SOURCES:



6.1 SINUSOIDAL WAVEFORM

Images:



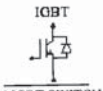
6.2 SINGLE PHASE SOURCES

Vm - peak voltage.
Voffset- DC offset voltage.

6.3 THREE PHASE SOURCE

6.3.2SWITCHES:

An IGBT or MOSFET switch consist of an active switch with an anti-parallel diode. A bi-directional switch (SSWI) conducts currents in both directions. It is on when the gating is high and is off when the gating is low, regardless of the voltage bias conditions of the switch.



6.4 IGBT SWITCH

6.3.3 TRANSFORMER:

6.5 SINGLE PHASE TRANSFORMER

6.3.4 DLL BLOCK:

Unlike the simple DLL blocks with fixed number of inputs and outputs (such as the DLL Block with 3 inputs and 3 outputs), the general DLL block provides more flexibility and capability in interfacing PSIM with custom DLL files. This file describes the convention and basis of the general DLL block.

The general DLL block allows users to write code in C or C++, compile it as a Windows DLL, and link to PSIM. There are four exported functions. PSIM simulation engine uses three of them, and one is used by the user interface.

The three simulation functions are: **RUNSIMUSER**, **OPENSIMUSER** and **CLOSESIMUSER**. The user interface function is: **REQUESTUSERDATA**.

RUNSIMUSER:

```
void RUNSIMUSER(
        double t,
        double delt,
        double *in,
        double *out,
        void ** ptrUserData,
        int *pnError,
        char * szErrorMsg)
```

This function is the only function in the DLL routine that is mandatory. All other functions are optional. This function is called by PSIM at each time step.

OPENSIMUSER:

```
void OPENSIMUSER(
        const char *szId,
        const char * szNetlist,
        void ** ptrUserData,
```



```
        LPSTR szErrorMsg,
        void * pPsimParams)
```

This function is optional. It is called only once at the beginning of the simulation. It receives information from the DLL routine, and allows the DLL routine to allocate memory for its own use.

CLOSESIMUSER:

```
void CLOSESIMUSER(
        const char *szId,
        void ** ptrUserData)
```

This function is optional. It is called only once at the end of the simulation. Its main purpose is to allow DLL to free any memory or resources that it has allocated.

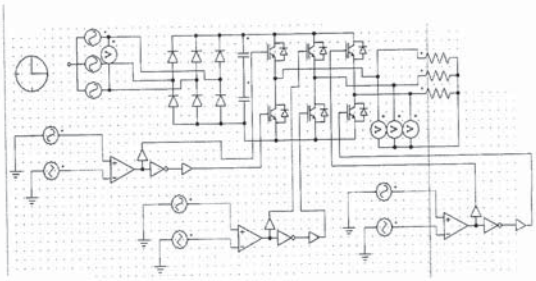
CHAPTER-7

SIMULATION OF DVR IN PSIM

7. SIMULATION OF DVR IN PSIM

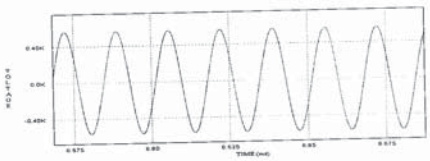
7.1 RECTIFIER-INVERTER BLOCK:

This is the rectifier-inverter block of the entire DVR system.

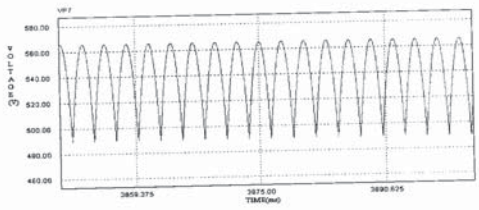


7.1 RECTIFIER-INVERTER BLOCK

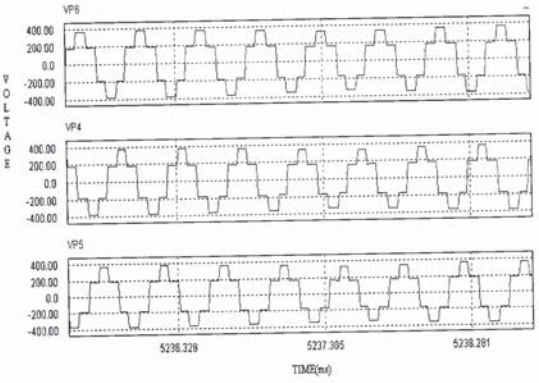
7.1.1 SIMULATION RESULT:



7.2 INPUT WAVEFORM



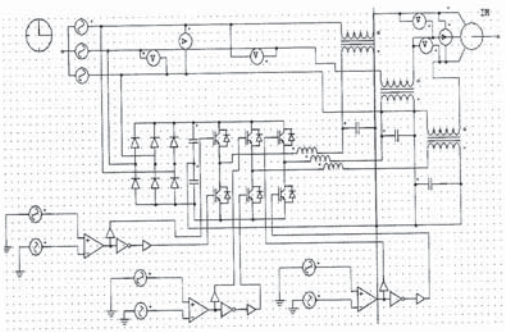
7.3 RECTIFIER OUTPUT WAVEFORM



7.4 RECTIFIER-INVERTER OUTPUT WAVEFORM

7.2 OVERALL CIRCUIT:

The project is simulated using PSIM software. The overall circuit of DVR is constructed using the components and blocks available in PSIM.

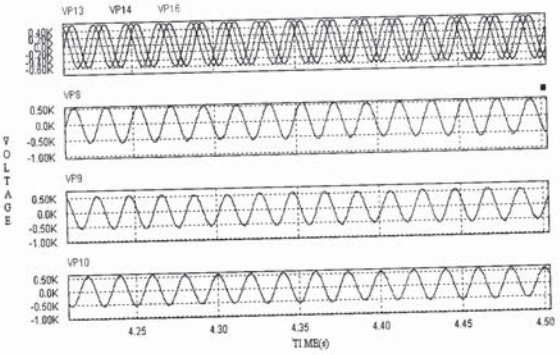


7.5 OVERALL CIRCUIT

CHAPTER-8

CONCLUSION AND RECOMMENDATION

7.2.1 SIMULATION RESULT:



7.6 OVERALL OUTPUT WAVEFORMS

There were some difficulties in creating the voltage sag directly in the line. So, we tried to create the sag by linking the DLL block using codes in VC++ platform. But, we were not completely successful in linking the block with the overall circuit.

8. CONCLUSION AND RECOMMENDATIONS

8.1 CONCLUSION:

This project is focused on the design and operation of sliding mode control of dynamic voltage restorer. The hardware for the compensation of voltage drop is implemented using the feedback control. The simulation is carried out in PSIM software. From the results, it is observed that the voltage sags can be effectively compensated using the Dynamic Voltage Restorer(DVR).

8.2 RECOMMENDATIONS:

The control of a DVR is not straight-forward because of the requirements of fast response, large variation in the type of sags to be compensated and variation in the type of connected load. The DVR must also be able to distinguish between background power quality problems and the voltage sags to be compensated. Hence, the type of sag must be detected using suitable control circuit, which can be added to DVR under proper conditions.

We have chosen a challenging project, there are many difficulties in creating the voltage sag both in simulation and real time (hardware). We have succeeded in completing the rectifier inverter module in simulation. There is more scope for enhancing this project in future for better results.

APPENDIX-A

CODING:

```
#include<pic.h>
#include<lcd.h>
void adc_init();
void adc0();
void set_mode();
static bit p1 @((unsigned) &PORTB*8+2);
static bit p2 @((unsigned) &PORTB*8+3);
static bit p3 @((unsigned) &PORTB*8+0);
static bit p4 @((unsigned) &PORTB*8+1);
static bit k1 @((unsigned) &PORTB*8+4);
static bit k2 @((unsigned) &PORTB*8+5);
static bit k3 @((unsigned) &PORTB*8+6);
static bit k4 @((unsigned) &PORTB*8+7);
static bit  sign  @((unsigned) &PORTC*8+2);// this pin outs the square wave forms
static bit ky @((unsigned) &PORTC*8+0);
static const unsigned int data1[12]={31,63,94,125,156,188}; // the array contains the on time
period of the pwm wave form
unsigned int on,count,off,temp0,temp1;
unsigned char j,pr2_val,volt,sv,prev,difr;
bank1 unsigned char lsb[12],i;     // these variables are stored in bank1 instead of bank0
bank2 unsigned int temp[12];              // this array is stored on bank2
unsigned char msb[12];
void main()
{
TRISC=0x01;                                                    // PortC as o/p port
```



```
TRISB=0xf0;
p1=p2=p3=p4=0;
lcd_init();                                                    // LCD Initialization
adc_init();                                                    // ADC Initialization

if(ky)
{
command(0x80);
lcd_condis("Square wave ctrl",16);
command(0xc0);
lcd_condis("Vol:000  SV:000 ",16);
set_mode();
on=count=0;
GIE=1;                  // enable global interrupt
PEIE=1;                 // enable peripheral interrupt
T0IE=1;                 // enable timer0 interrupt
OPTION = 0x02;      // set prescale (00)
TMR0 = 0xfc; // timer reg set value for ten micro sec  F7
 TMR2IE=0;        // timer2 interrupt enable
 TMR2ON=0;        // timer 2 enable
while(1)
{
adc0();
command(0xc4);
hex_dec(volt);

if(volt<sv)
{
difr=sv-volt;
if(difr>20 && on<148) on+=10;
```



```
else if(difr>10 && on<153) on+=5;

else if(difr>5 && on<155) on+=3;
else if(difr>1 && on<158) on++;

off=on+160;
}
else if(volt>sv)
{
difr=volt-sv;
if(difr>20 && on>10) on-=10;
else if(difr>10 && on>5) on-=5;
else if(difr>5 && on>3) on-=3;
else if(difr>1 && on>0) on--;

off=on+160;
}

if(k4==0) set_mode();
//command(0x80);
//hex_dec(on);
//command(0x8c);
//hex_dec(off);
}
}
else if(!ky)
{
command(0x80);
lcd_condis(" Sine wave ctrl ",16);
command(0xc0);
```



```
lcd_condis("             ",16);
TMR2=0;
// TRISC=0x00;
T2CON=0x03;
difr=50;
pr2_val=48;
for(i=0;i<6;i++)                  // selecting the switching frequency as 6 times
 {
  temp[i]=data1[i];
  lsb[i]=temp[i]&0x03;
  if(lsb[i]==0x00) lsb[i]=0x0c;
  else if(lsb[i]==0x01) lsb[i]=0x1c;  // converting the 2 lsbs to suitable position on ccpr1l
  else if(lsb[i]==0x02) lsb[i]=0x2c;
  else if(lsb[i]==0x03) lsb[i]=0x3c;
  msb[i]=temp[i]>>2;
 }
for(i=5,j=6;j<12;i--,j++)          // assigning the reverse swithcing frequency as same as forward
{
 lsb[j]=lsb[i];
 msb[j]=msb[i];
}
 GIE=1;          // global interrupt enable
 PEIE=1;         // peripheral interrupt enable
 TMR2IE=1;       // timer2 interrupt enable
 TMR2ON=1;       // timer 2 enable

 while(1);
 }
 else
 {
```

```
command(0x80);
lcd_condis("Key Not selected",16);
command(0xc0);
lcd_condis("              ",16);
}
}
void adc_init()
{
 ADCON1=0x09;              // 8-channel,ADC control
 TRISA=0xff;          // to select the port A as input port
}
void adc0()
{
unsigned char j;

temp0=temp1=0;
for(j=0; j<=29; j++)
{
   ADCON0=0x00;                    // Channel select (Cha: 0)
   ADON=1;                              // ADC module ON
        delay(50);
   ADCON0 =0x05;          // selecting a particular channel and making the go/done bit high
   while(ADCON0!=0X01);  // Chk whether conversion finished or not
        temp0 = ADRESH;                 // 8 bit value taken into one variable
//      temp0 /=6;
        temp1 = temp1 + temp0;
 }
 volt = temp1/30;
 }
 void interrupt timer(void)
```



```
{
 if(T0IF==1)
 {
 T0IF=0;
 count++;
        if(count>320){count=0;}
        if(count<158) p3=1;
        else p3=0;
        if(count>162) p4=1;
        else p4=0;

        if(count<on) p1=1;
        else p1=0;
        if(count>160&&count<=off) p2=1;
        else p2=0;
 TMR0 = 0Xfc;
 }
 if(TMR2IF==1)                  // checking whether timer2 interrupt has occured or not
 {
 TMR2ON=0;                      // disable the timer
 PR2 = pr2_val;                 // transfer the pwm period to period register of timer 2
 CCPR2L=msb[i];                   // transfer the msb 2 bits
 T2CON=0x07;                    // timer 2 control register settings
 TMR2IF=0;                      // clearing the flag
 CCP2CON=lsb[i];                  // transfer the lsb 8 bits

 if(i==0)                       // this loop is to generate the corresponding square waveform with
 pwm wave
  {
   while(!TMR2IF)
```



```
  {
   if(TMR2>=PR2-10)
   {
    sign=!sign;
    break;
   }
  }
 }
 i++;
 TMR2IF=0;
 if(i>11) i=0;
 }
}
void set_mode()
{
GIE=T0IE=0;
p1=p2=p3=p4=0;
command(0x01);
command(0x80);
lcd_condis("  Set Mode...  ",16);
while(k4==0);
delay(60000);
command(0x01);
command(0x80);
lcd_condis("Set the Voltage ",16);
command(0xc0);
lcd_condis("Voltage:000 V  ",16);
prev=sv;
while(1)
{
```



```
if(k1==0)
{
if(sv<250) sv+=10;
command(0xc8);
hex_dec(sv);
delay(15000);
}
if(k2==0)
{
if(sv>10) sv-=10;
command(0xc8);
hex_dec(sv);
delay(15000);
}
if(k3==0) goto end;
}
end:
command(0x01);command(0x80);
lcd_condis("Square wave ctrl",16);
command(0xc0);
lcd_condis("Vol:000  SV:000 ",16);
command(0xcc);
hex_dec(sv);
p1=p2=p3=p4=0;
on=off=count=0;
GIE=T0IE=1;
}
```

APPENDIX-B

DATA SHEETS:

PIC16F87X

Key Features PICmicro™ Mid-Range Reference Manual (DS33023)	PIC16F873	PIC16F874	PIC16F876	PIC16F877
Operating Frequency	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz
Resets (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
FLASH Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
EEPROM Data Memory	128	128	256	256
Interrupts	13	14	13	14
I/O Ports	Ports A,B,C	Ports A,B,C,D,E	Ports A,B,C	Ports A,B,C,D,E
Timers	3	3	3	3
Capture/Compare/PWM modules	2	2	2	2
Serial Communications	MSSP, USART	MSSP, USART	MSSP, USART	MSSP, USART
Parallel Communications	—	PSP	—	PSP
10-bit Analog-to-Digital Module	5 Input channels	8 Input channels	5 Input channels	8 Input channels
Instruction Set	35 Instructions	35 Instructions	35 Instructions	35 Instructions

54LS14/DM74LS14 Hex Inverters with Schmitt Trigger Inputs

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 7V
Input Voltage 7V
Operating Free Air Temperature Range
54LS −55°C to +125°C
DM74LS 0°C to +70°C
Storage Temperature Range −65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	54LS14 Min	54LS14 Nom	54LS14 Max	DM74LS14 Min	DM74LS14 Nom	DM74LS14 Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.5	1.6	2.0	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.6	0.6	1.1	0.5	0.8	1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS		0.25	0.4	V
			DM74		0.35	0.5	
		V_{CC} = Min, I_{OL} = 4 mA	DM74		0.25	0.4	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}	DM74		−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}	DM74		−0.18		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_{CC} = Max, V_I = 10.0V	54LS				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current (Note 3)	V_{CC} = Max	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			6.8	16	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			12	21	mA

Note 1: V_{CC} = 5V.
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

2

BC546; BC547
NPN general purpose transistors

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\,j-a}$	thermal resistance from junction to ambient	note 1	0.25	K/mW

Note
1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	I_E = 0; V_{CB} = 30 V	–	–	15	nA
		I_E = 0; V_{CB} = 30 V; T_j = 150 °C	–	–	5	µA
I_{EBO}	emitter cut-off current	I_C = 0; V_{EB} = 5 V	–	–	100	nA
h_{FE}	DC current gain BC546A	I_C = 10 µA; V_{CE} = 5 V; see Figs 2, 3 and 4	–	90	–	
	BC546B; BC547B		–	150	–	
	BC547C		–	270	–	
	DC current gain BC546A	I_C = 2 mA; V_{CE} = 5 V; see Figs 2, 3 and 4	110	180	220	
	BC546B; BC547B		200	290	450	
	BC547C		420	520	800	
	BC547		110	–	800	
	BC546		110	–	450	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA	–	90	250	mV
		I_C = 100 mA; I_B = 5 mA	–	200	600	mV
V_{BEsat}	base-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA; note 1	–	700	–	mV
		I_C = 100 mA; I_B = 5 mA; note 1	–	900	–	mV
V_{BE}	base-emitter voltage	I_C = 2 mA; V_{CE} = 5 V; note 2	580	660	700	mV
		I_C = 10 mA; V_{CE} = 5 V	–	–	770	mV
C_c	collector capacitance	I_E = I_e = 0; V_{CB} = 10 V; f = 1 MHz	–	1.5	–	pF
C_e	emitter capacitance	I_C = I_c = 0; V_{EB} = 0.5 V; f = 1 MHz	–	11	–	pF
f_T	transition frequency	I_C = 10mA; V_{CE} = 5 V; f = 100 MHz	100	–	–	MHz
F	noise figure	I_C = 200 µA; V_{CE} = 5 V; R_S = 2 kΩ; f = 1 kHz; B = 200 Hz	–	2	10	dB

Notes
1. V_{BEsat} decreases by about 1.7 mV/K with increasing temperature.
2. V_{BE} decreases by about 2 mV/K with increasing temperature.

N–CHANNEL POWER MOSFET

V_{DSS}	200V
$I_{D(cont)}$	30A
$R_{DS(on)}$	0.085Ω

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

V_{GS}	Gate – Source Voltage		±20V
I_D	Continuous Drain Current	(V_{GS} = 0 , T_{case} = 25°C)	30A
I_D	Continuous Drain Current	(V_{GS} = 0 , T_{case} = 100°C)	19A
I_{DM}	Pulsed Drain Current [1]		120A
P_D	Power Dissipation @ T_{case} = 25°C		150W
	Linear Derating Factor		1.2W/°C
E_{AS}	Single Pulse Avalanche Energy [2]		200mJ
I_{AR}	Avalanche Current [2]		30A
E_{AR}	Repetitive Avalanche Energy [2]		15mJ
dv/dt	Peak Diode Recovery [3]		5V/ns
T_j , T_{stg}	Operating and Storage Temperature Range		-55 to +150°C
T_L	Lead Temperature 1.6mm (0.63") from case for 10 sec.		300°C

APPENDIX-C
PHOTOGRAPHIC IMAGES

REFERENCES:

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