P-2657

Single-Phase Uninterruptible Power Supply Based on Z-Source Inverter

A Project Report

Submitted by

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in partial fulfillment for the award of the degree
of

Bachelor of Engineering
in
Electrical & Electronics Engineering

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

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APRIL– 2009

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BONAFIDE CERTIFICATE

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ABSTRACT

This project introduces a design of an Impedance Source and control of the single phase inverter of uninterrupted power supply which has become an indispensable element of many data processing installations, from desktop PCs to mainframe computer systems.

This new design replaces the existing voltage source and current source inverters which are having the following disadvantages. Since the Voltage source inverter is a buck converter, the obtainable output voltage is limited below the input line voltage. Voltage sags can interrupt the system and shut down critical loads and processes. Inrush and harmonic current from diode rectifier can pollute the line. Low power factor is another issue of the traditional system. Also performance and reliability are compromised by the V-source inverter structure.

Even current source inverters cannot be a better option because it's a boost converter. Both traditional inverters are disadvantageous in terms of reliability, cost, power factor etc.

This Impedance source employs a unique LC-Network in the DC link and an input capacitor on the ac side of the diode rectifier. By controlling the shoot through duty cycle, it can produce any desired output ac voltage even greater than the line voltage. It provides ride-through capability during voltage sags, reduces line harmonics, improves power factor, reliability and extends output voltage range.

ACKNOWLEDGEMENT

The completion of this project can be attributed to the combined efforts made by us and the contribution made in one form or the other by the individuals we hereby acknowledge.

We express my indebtedness to our guides *Prof* **K.T.Varadharajan, Mrs.R.Mahalakshmi,** *Assistant Professor* in Electrical and Electronics Engineering department for their valuable guidance, which helped us in the completion of this project.

Last but not the least we thank one and all of my friends and other staff of Electrical and Electronics Engineering department for their whole hearted support.

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LIST OF SYMBOLS AND ABBREVIATIONS

S.No	SYMBOL/ABBREVIATION	DESCRIPTION
1.	V_{c1}	Voltage in capacitor C1
2.	V_{c2}	Voltage in capacitor C2
3.	Vl_1	Voltage induced in inductor L1
4.	Vl_2	Voltage induced in inductor L2
5.	Vd	DC voltage from rectifier
6.	Vi	Voltage to inverter
7.	Vo	Output Voltage
8.	M, m	Modulation index
9.	B	Boost factor
10.	Bb	Buck boost factor
11.	Vs	Supply Voltage
12.	fc	Carrier frequency
13.	f_0	Output frequency
14.	Ac	Amplitude of carrier wave
15.	Ar	Amplitude of reference wave
16.	mf	Frequency modulation ratio
17.	μH	Micro Henry (Unit of inductance)
18.	μF	Micro Farad (unit of capacitance)
19.	$V_{o(t)}$	Instantaneous output voltage
20.	δ	Pulse width
21.	P	Number of Pulses
22.	ZSI	Impedance Source Inverter
23.	CSI	Current Source Inverter
24.	VSI	Voltage Source Inverter
25.	DC	Direct Current
26.	AC	Alternating Current
27.	UPS	Uninterruptible Power Supply

CHAPTER 1

INTRODUCTION

1.1 GENERAL

An Inverter is a circuit which converts a DC input into an AC output. Traditionally there are two inverters available. They are voltage source inverter and current source inverter. Each inverter has four switches in the main circuit. These switches are power switches with anti–parallel diodes. These diodes are to provide bidirectional current flow and reverse voltage blocking capability.

Traditional inverters have following limitations

- They can be operated either as a Buck or a Boost inverter and cannot be operated as a buck-boost inverter.
- Their output voltage range is limited to either greater or smaller than the input voltage.
- Their main circuit is not interchangeable. In other words the voltage source inverter cannot be used as the current source inverter and vice versa.
- They are vulnerable to EMI noise which affects their reliability.

The above limitations can be rectified by an impedance source inverter to provide higher efficiency. This concept can be applied for all AC to DC, AC to AC, DC to DC, DC to AC power conversions.

1.2 OBJECTIVE

The Primary Objective of this project is to implement an impedance source to the single phase inverter for UPS applications. This inverter can buck as well as boost the input voltage, minimize the component count, increase the efficiency and reduce the cost.

This project focuses on the development of an impedance source inverter system and control for uninterruptible power supply applications (UPS) which have become an indispensable element of many data processing installations, from desktop PCs to mainframe computer systems.

1.3 ORGANISATION OF THE REPORT

This report has been organized into seven chapters.

Chapter 1: Gives introduction to Inverters and the objective of this project and the way the various chapters are organized

Chapter 2: Focuses on the traditional inverters and their disadvantages.

Chapter 3: Explains the impedance source inverter, its advantages and how this can be implemented in UPS

Chapter 4: Provides the analysis and design of this impedance network.

Chapter 5: Shows the Matlab simulation circuit of the Impedance source inverter and the output waveforms.

Chapter 6: Describes the hardware implementation of the impedance source inverter

Chapter 7: Concludes the project with scope for future work

CHAPTER 2

INVERTER

2.1 TRADITIONAL INVERTERS

Traditional inverters are voltage source inverter and current source inverter. Voltage source inverter is the one which the dc source has small or negligible impedance. In other words a voltage source inverter has stiff dc source voltage at its input terminals. The switching device can be a conventional MOSFET, thyristor or a power transistor.

A current source inverter is fed with adjustable dc current source. In current source inverter output current waves are not affected by the load.

2.2 VOLTAGE SOURCE INVERTER [VSI]

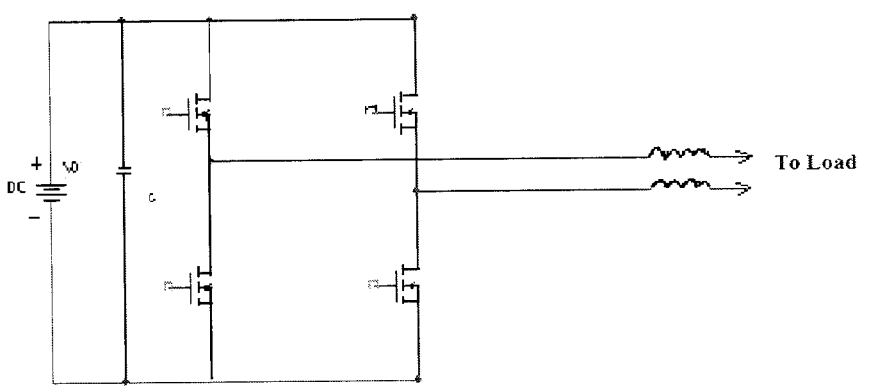


Figure 2.1 Voltage Source Inverter

Figure 2.1 shows the traditional single-phase voltage-source inverter structure .A dc voltage source supported by a relatively large capacitor feeds the main inverter circuit, a single-phase bridge. The dc voltage source can be a battery, fuel-cell stack or a diode rectifier.

Four switches are used in the main circuit; each is traditionally composed of a power transistor and an anti parallel diode to provide bidirectional current flow and unidirectional voltage blocking capability.

The V-source inverter is widely used however; it has the following conceptual limitations.

2.2.1 Limitations of Voltage Source Inverter

The V-source inverter is a buck (step down) inverter for dc-to-ac power conversion. For applications where over drive is desirable and the available dc voltage is limited, an additional dc-dc boost (step up) stage is needed to obtain a desired ac output. The additional power converter stage increases system cost and lowers efficiency.

The upper and lower devices of each phase leg cannot be gated on simultaneously either by purpose or by EMI noise. Otherwise, a shoot-through would occur and destroy the devices [2]. The shoot-through problem by electromagnetic interference (EMI) noise's mis gating-on is a major killer to the inverter's reliability. Dead time to block both upper and lower devices has to be provided in the V-source inverter, which causes waveform distortion, etc. An output *LC* filter is needed for providing a sinusoidal voltage compared with the current-source inverter, which causes additional power loss and control complexity.

Voltage sags can interrupt and the system and shutdown critical loads and processes. Over 90% of power quality related problems are from momentary voltage sags of 10–50% below nominal Voltage [3]. The dc capacitor in VSI is a relatively small energy storage element, which cannot hold dc voltage above the operable level under such voltage sags. Lack of ride-through capacity is a serious problem for sensitive loads.

The ASD(Adjustable speed drives) industry provides options using fly back converter or boost converter with energy storage or diode rectifier to achieve ride-through; however, these options come with penalties of cost, size/weight, and complexity.

Inrush and harmonic current from the diode rectifier can pollute the line. Low power factor is another issue of the traditional inverters.

2.3 CURRENT SOURCE INVERTER [CSI]

Figure 2.2 shows the traditional single-phase current-source inverter structure. A dc current source feeds the main converter circuit, a single-phase Bridge. The dc current source can be a relatively large dc inductor fed by a voltage source such as a battery, fuel-cell stack, diode rectifier, or thyristor converter.

Four switches are used in the main circuit; each is traditionally composed of a semiconductor switching device with reverse block capability such as a gate-turn-off thyristor (GTO) and SCR or a power transistor with a series diode to provide unidirectional current flow and bidirectional voltage blocking.

However, the I-source inverter has the following conceptual and theoretical barriers and limitations.

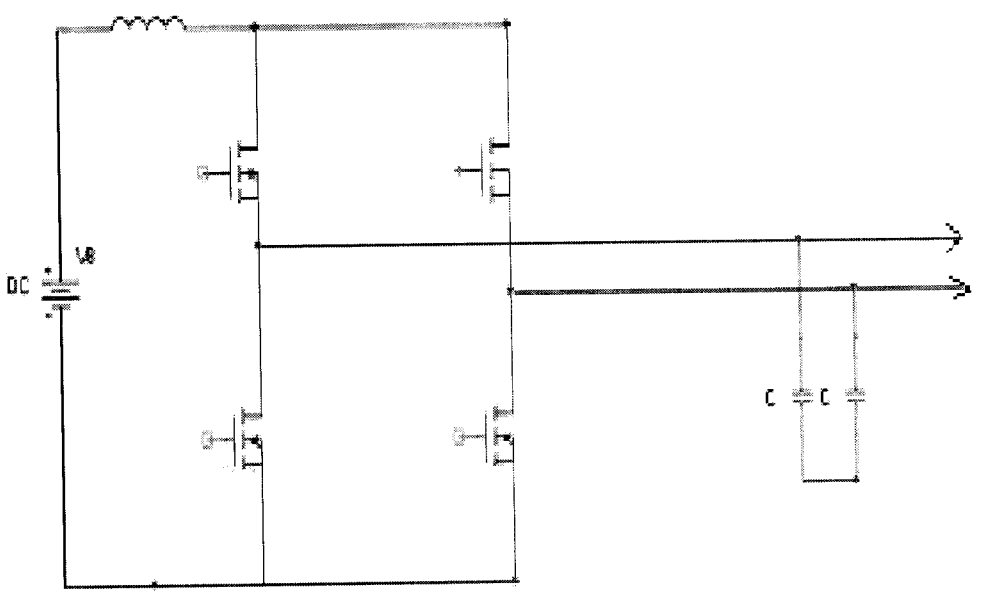


Figure 2.2 Current Source Inverter

2.3.1 Limitations of Current Source Inverter

The ac output voltage has to be greater than the original dc voltage that feeds the dc inductor or the dc voltage produced is always smaller than the ac input voltage.

For applications where a wide voltage range is desirable, an additional dc–dc boost stage is needed. The additional power conversion stage increases system cost and lowers efficiency.

At least one of the upper devices and one of the lower devices have to be gated on and maintained on at any time. Otherwise, an open circuit of the dc inductor would occur and destroy the devices. The open-circuit problem by EMI noise's mis gating-off is a major concern of the converter's reliability. Overlap time for safe current commutation is needed in the I-source converter, which also causes waveform distortion, etc.

The main switches of the I-source inverter have to block reverse voltage that requires a series diode to be used in combination with high-speed and high-performance transistors such as insulated gate bipolar transistors (IGBTs). This prevents the direct use of low-cost and high-performance IGBT modules .In addition, both the V-source inverter and the I-source inverter have the following common limitations.

2.4 COMPARISON OF VSI AND CSI

TABLE 2.1

COMPARISON OF VOLTAGE & CURRENT SOURCE INVERTERS

S.NO	CURRENT SOURCE INVERTER	VOITAGE SOURCE INVERTER
1	An inductor is used in the dc link the source impedance is high. It provides constant current	A capacitor is used in the dc link, it provides constant voltage source
2	A current source inverter is capable of withstanding short circuit across any two of its output terminals. Hence momentary short circuit on load and short circuit of switches are acceptable	A VSI is more dangerous situation as the parallel capacitor feeds more powering to the fault.
3	It can be used for only Buck or Boost operation	It can be used for only Buck or Boost operation
4	The main circuit cannot be interchanged.	The main circuit cannot be interchanged
5	It is affected by the EMI	It is affected by the EMI

CHAPTER 3

IMPEDANCE SOURCE INVERTER

3.1 IMPEDANCE SOURCE INVERTER

This is an inverter which is supplied by an Impedance source. In voltage source inverter the stiff dc supply is provided by a battery in parallel with a capacitor. In current source inverter the constant direct current is provided by a battery in series with an inductor. But in Impedance Source Inverter the DC source is provided by the cross combination of both Capacitors and Inductors

3.2 ADVANTAGES OF THE IMPEDANCE SOURCE NETWORK

- The impedance source inverter concept can be applied in all ac-ac, dc-dc, ac-dc, dc-ac power conversion.
- The output voltage range not limited.
- The impedance source inverter is used as a buck- boost inverter.
- The impedance source inverter does not affect the electromagnetic interference noise.
- The impedance source inverter cost is low.
- The impedance source inverter provides the buck- boost function by two stage power conversion

3.3 UNINTERRUPTIBLE POWER SUPPLY

The AC power supplies are commonly used as standby sources for critical loads and in applications where normal AC supplies are not available. The standby power supplies are also known as uninterruptible power supply (UPS) system

The block diagram of UPS is shown in figure 3.1. The load is normally supplied from the ac main supply and the rectifier maintains the full charge of the battery. If the supply fails

the load is switched to the output of the inverter, which then takes over the main supply. Here the inverter is either voltage source inverter or current source inverter.

This inverter part can be replaced with this new Impedance Source Inverter which is more advantageous than the other two traditional inverters.

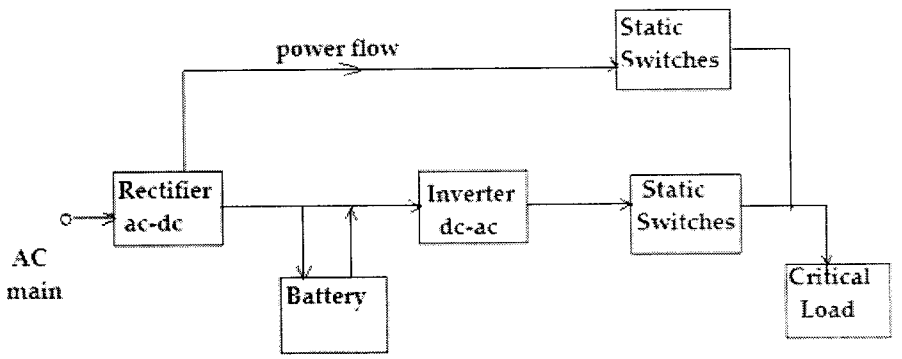


Figure 3.1 UPS Block diagram

The two configurations commonly used in UPS are given below.

1) Load normally connected to ac main supply.
2) Load normally connected to inverter

In the first case the inverter runs only during the time when the supply failure occurs. Where as in the second case inverter operates continuously and its output is connected to the load. There is no need for breaking the supply in the event of supply failure.

In either case this new type of inverter can perform well without shutting down the critical loads during voltage sags.

3.4. BLOCK DIAGRAM OF IMPEDENCE SOURCE INVERTER

To overcome the limitations of the traditional V-source and I-source inverter, this thesis deals an impedance-source inverter and its control method for implementing dc-to-ac power conversion. This thesis also deals with how to overcome the limitations of voltage source inverter and current source inverter.

UPS MODULE

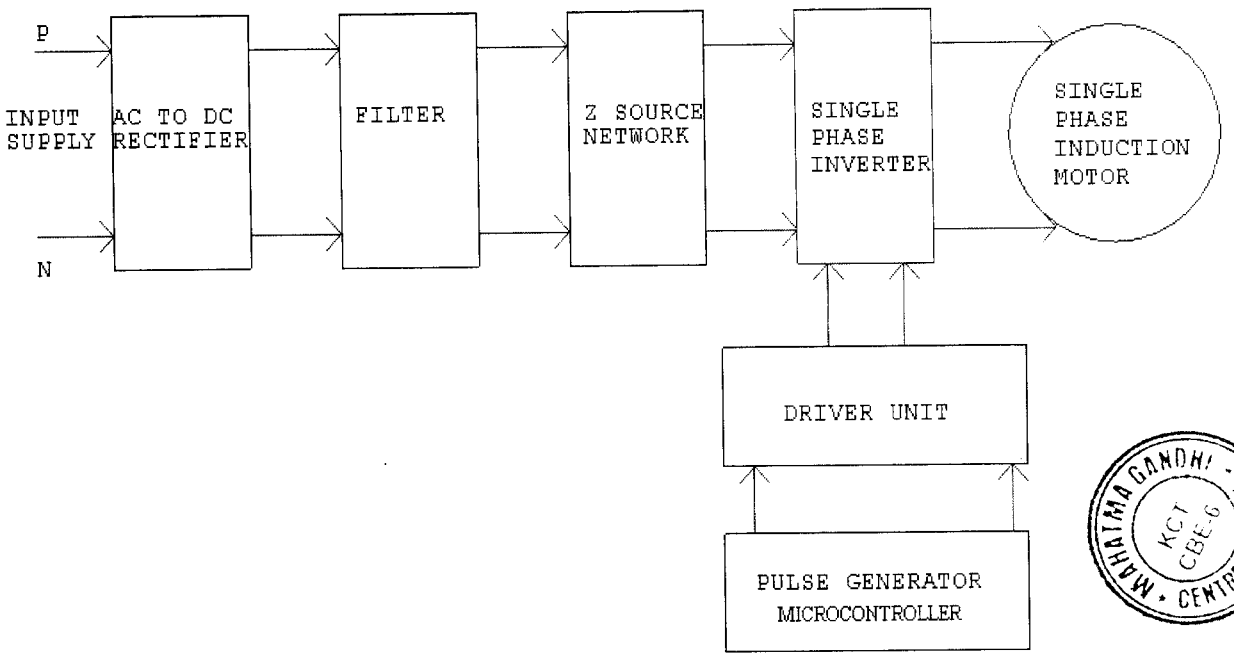


Figure 3.2 Block diagram of Impedance Source Inverter

The proposed impedance source inverter block diagram is shown in figure 3.2. It consists of voltage source from the rectifier supply, Impedance network, single phase inverter and AC load. AC voltage is rectified to DC voltage by the rectifier. In the rectified output Dc voltage fed to the impedance network.

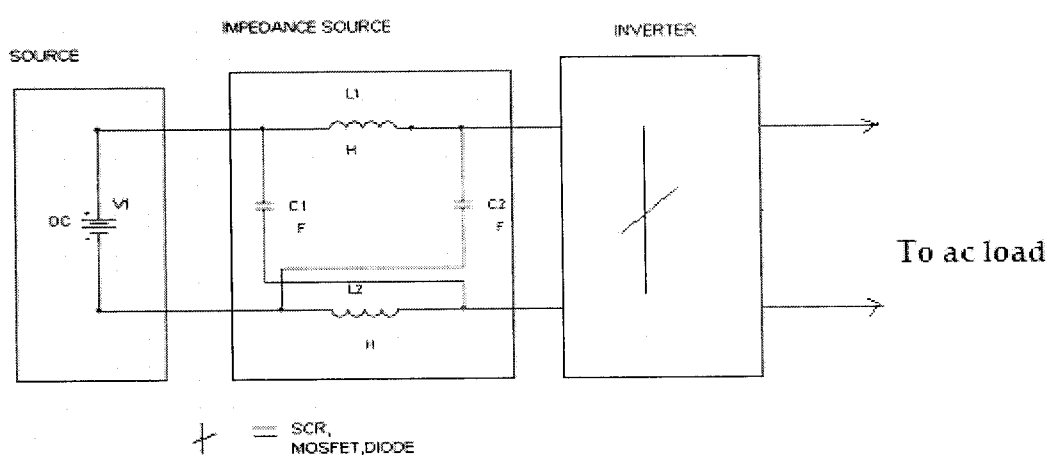


Figure 3.3 Impedance Source Inverter

Figure 3.3 show the proposed impedance source inverter diagram. It employs a unique impedance network to couple the inverter main circuit to the power source and load for providing unique features that cannot be observed in the traditional Voltage and current source inverter where a capacitor and inductor are used respectively. The impedance source inverter overcomes the above-mentioned conceptual and theoretical barriers.

In Figure.3.3, a two-port network that consists of a split-inductor and capacitors are connected in X shape is employed to provide an impedance source coupling the inverter to the dc source .The dc source can be either a voltage or a current source. Therefore, the dc source can be a battery, diode rectifier, thyristor converter, fuel cell. Switches used in the inverter can be a combination of switching devices and diodes.

3.5. SINGLE PHASE IMPEDENCE SOURCE INVERTER FOR UPS

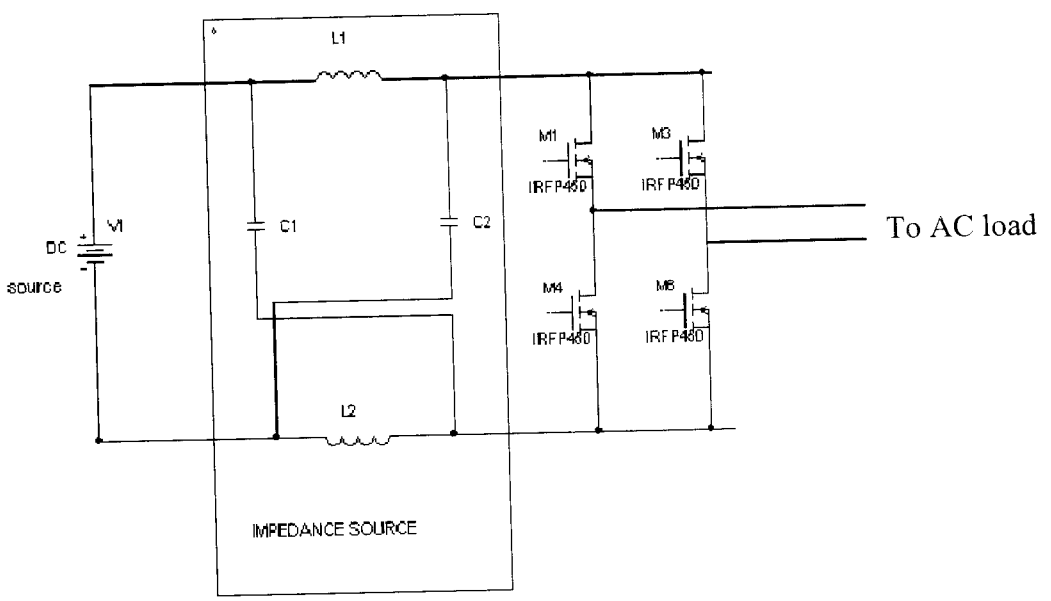


Figure 3.4 Single-Phase Impedance Source Inverter

The impedance concept can be applied to all dc-to-ac power conversion. To describe the operating principle and control, this thesis focuses on an application example of the impedance-source inverter. The proposed impedance source inverter for UPS is shown in Figure.3.4 which can directly produce an AC voltage greater and less than the DC input voltage.

CHAPTER 4

ANALYSIS AND DESIGN OF THE IMPEDANCE NETWORK

4.1 EQUIVALENT CIRCUIT, OPERATING PRINCIPLE, AND CONTROL

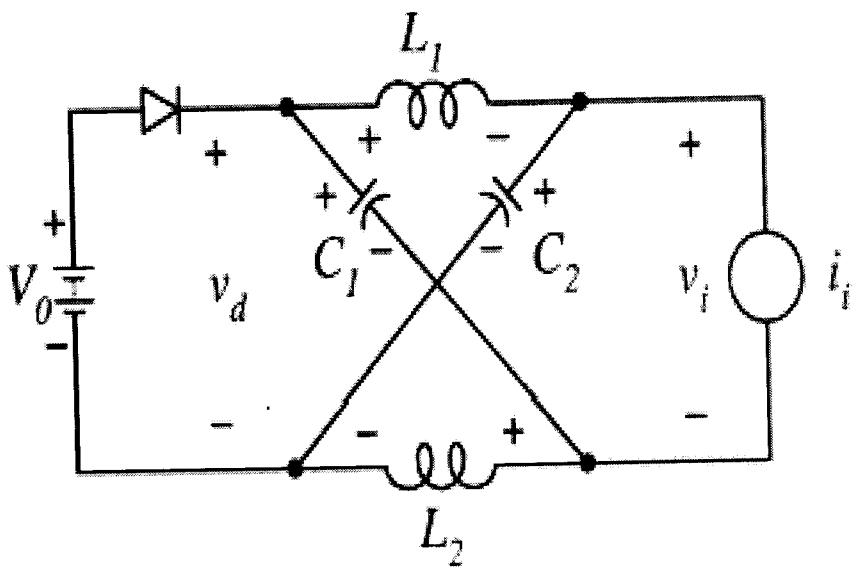


Figure 4.1 Equivalent Circuit of Impedance Source Inverter

The unique feature of the impedance-source inverter is that the output ac voltage can be any value between zero to infinity regardless of the DC voltage. That is, the Impedance-source inverter is a buck–boost inverter that has a wide range of obtainable voltage. The traditional Voltage and current source inverters cannot provide such feature. To describe the operating principle and control of the impedance-source inverter in Figure 4.1 let us briefly examine the impedance-source inverter structure.

The single-phase impedance-source inverter bridge has nine permissible switching states unlike the traditional singe-phase Voltage source inverter that has eight. The traditional single-phase Voltage source inverter has four active vectors when the dc voltage is impressed

across the load and two zero vectors when the load terminals are shorted through either the lower or upper single devices, respectively. However, the single-phase impedance-source inverter bridge has one extra zero state.

When the load terminals are shorted through both the upper and lower devices of any one phase leg, or both two phase legs a shoot through state occurs .This shoot-through zero state is forbidden in the traditional Voltage source inverter, because it would cause a shoot-through.

We call this third zero state the shoot-through zero state, which can be generated by seven different ways: shoot-through via any one phase leg, combinations of two phase legs. The impedance-source network makes the shoot-through zero state possible.

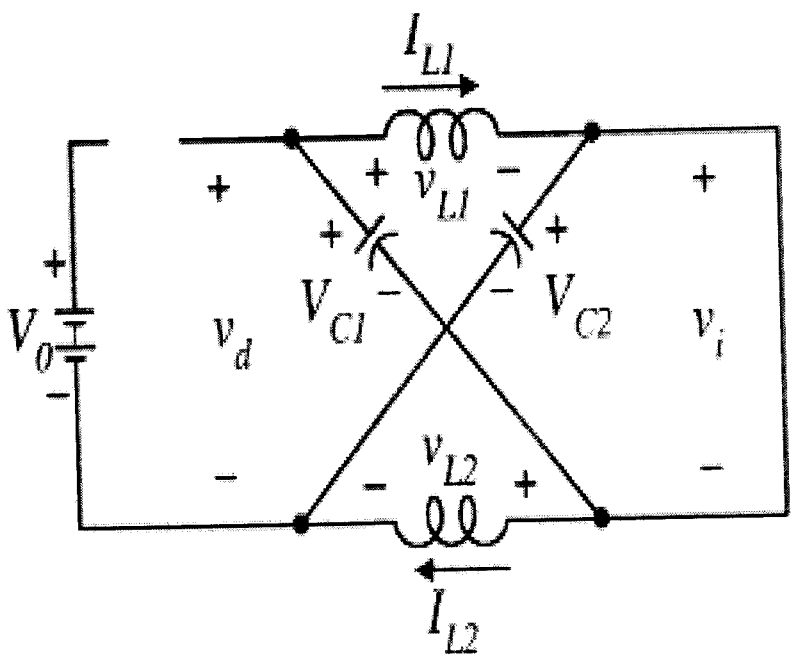


Figure 4.2 Equivalent circuit of the impedance-source inverter for shoot through state

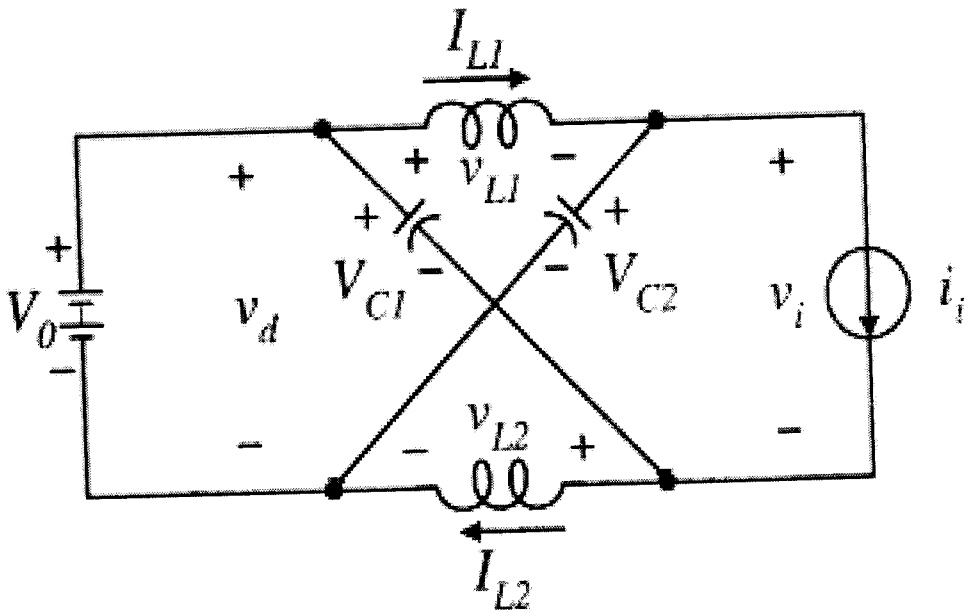


Figure 4.3 Equivalent circuit of the impedance-source inverter for active state

The inverter bridge is equivalent to a short circuit when the inverter bridge is in the shoot-through zero state, as shown in Figure 4.1, whereas the inverter bridge becomes an equivalent current source as shown in Figure 4.2.

When in one of two active states, Note that the inverter bridge can be also represented by a current source with zero value (i.e., an open circuit) when it is in one of the two traditional zero states. Therefore, Figure 4.2 shows the equivalent circuit of the impedance-source inverter viewed from the dc link when the Inverter Bridge is in one of the eight non shoot-through switching states. All the traditional pulse width-modulation (PWM) schemes can be used to control the impedance-source inverter and their theoretical input–output relationships still hold.

4.2 CIRCUIT ANALYSIS AND OBTAINABLE OUTPUT VOLTAGE

From the impedance–source equivalent circuits we have

$$Vc1=Vc2=Vc;\ Vl1=Vl2=Vl \quad (1)$$

Given the inverter bridge is in the shoot through zero state for an interval of To, during a switch cycle, T and from the equivalent circuit, fig 4.2 one has

$$Vl=Vc;\ Vd=2Vc;\ Vi=0; \quad (2)$$

Now consider that the inverter bridge is in one of the eight Non-shoot through states for an interval of $T1$, during the Switching cycle T. From the equivalent circuit

$$Vl=Vo-Vc;\ Vd=Vo;\ Vi=Vc-Vl=2Vc-Vo \quad (3)$$

Where Vo is the dc source voltage and $T=To-T1$

The average voltage of the inductors over one switching Period (T) should be zero in steady state, from (2) and (3). We have

$$Vl(av)=[To.Vc+T1(Vo-Vc)]/T=0 \quad (4)$$

$$Vc/Vo = T1/(T1-To) \quad (5)$$

Similarly, the average dc-link voltage across the inverter bridge can be found as follows:

$$Vi=Vi(av)=[To.0+T1(2Vc-Vo)]/T=[T1/(T1-To)]\ Vo=Vc \quad (6)$$

The peak dc link voltage across the inverter bridge is expressed in equation 3 and it can be rewritten as

$$Vi=Vc-Vl=2Vc-Vo=[T/(T1-To)]\ Vo=B.Vo \quad (7)$$

Where

$$B=T/(T1-To)=1/[1-2(To/T)] \geq 1 \quad (8)$$

B =Boost factor resulting from the shoot through zero state.

The peak dc link voltage Vi is the equivalent dc link voltage of the inverter.

The output peak phase voltage from the inverter can be expressed as

$$Vac=m.(Vi/2) \quad (9)$$

where m is the modulation index.

Substituting equation (7) in equation (9) gives

$$Vac=m.B.(Vo/2) \quad (10)$$

In traditional voltage source pwm inverter, we have the well known relationship $Vac=m.(Vo/2)$.

Equation (10) can be modified into

$$Vac=Bb(V0/2)$$

Where Bb= Buck boost factor

$$Bb=m.B$$

From the above equation the output voltage can be stepped up and stepped down by choosing an appropriate buck- boost factor Bb .

$Bb=m.B$ (B ranges from 0 to infinity)

The buck–boost factor is determined by the modulation index and boost factor. The boost factor as expressed it can be controlled by duty cycle (i.e., interval ratio) of the shoot-through zero state over the no shoot-through states of the inverter PWM Note that the shoot-through zero state does not affect the PWM control of the inverter, because it equivalently produce the same zero voltage to the load terminal.

The available shoot through period is limited by the zero-state period that is determined by the modulation index. The impedance source network should require less capacitance and smaller size compared with the traditional Voltage source inverter. Similarly, when the two capacitors are small and approach zero, the impedance source network reduces to two inductors in series and becomes a traditional current source . Therefore, a traditional current source inverter's inductor requirements and physical size is the worst case requirement for the inverter source network.

Considering additional filtering and energy storage by the capacitors, the impedance-source network should require less inductance and smaller size compared with the traditional I-source inverter.

CHAPTER 5

SIMULATION CIRCUIT AND RESULTS OF THE IMPEDANCE SOURCE INVERTER

5.1 MATLAB SIMULINK MODEL FOR IMPEDANCE SOURCE INVERTER:

Simulations have been performed to confirm the above analysis. Figure.5.1 shows the network parameters are $L1 = L2 = L = 160mH$ and $C1 = C2 = C = 1000\mu F$.

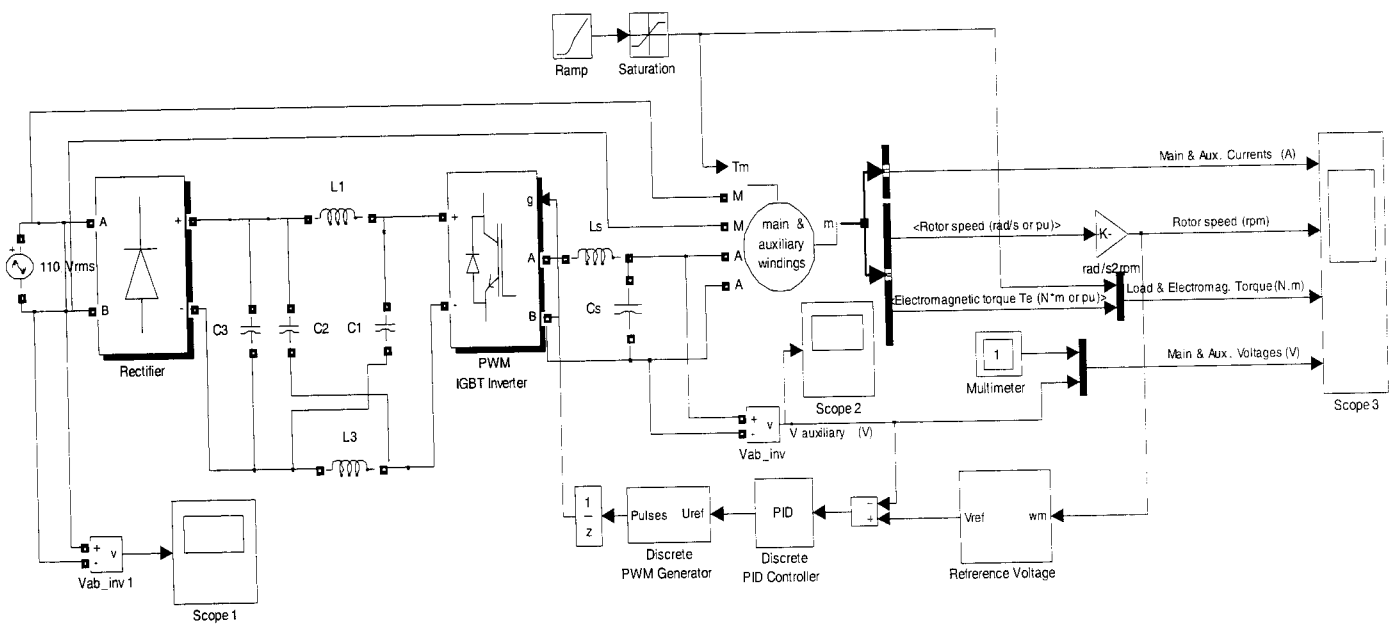


Fig 5.1 Matlab Simulink Model for Impedance Source Inverter

Before fabricating the hardware, the Z-Source Inverter Circuit is simulated using Matlab Software.

5.2 SIMULATION RESULTS

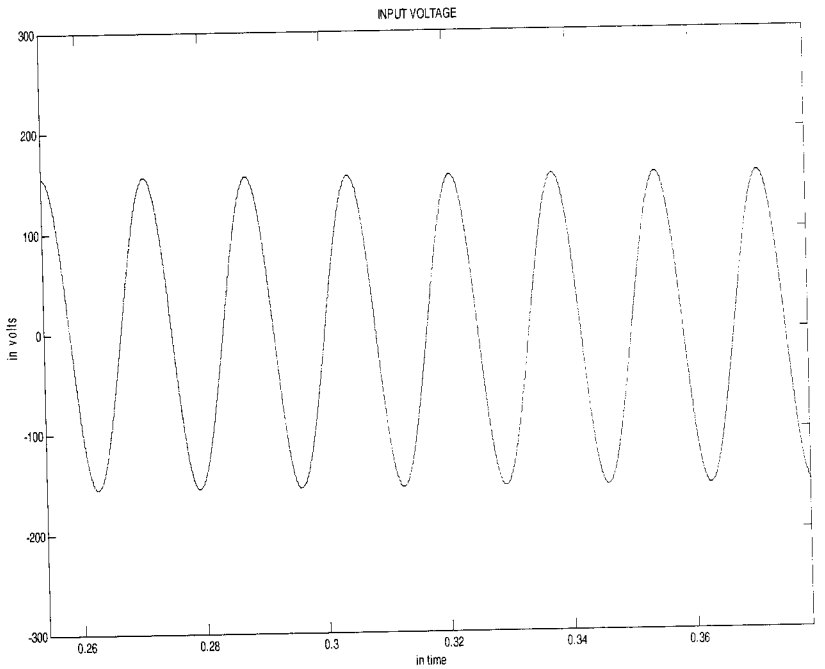


Fig 5.2.1 Input Voltage Waveform

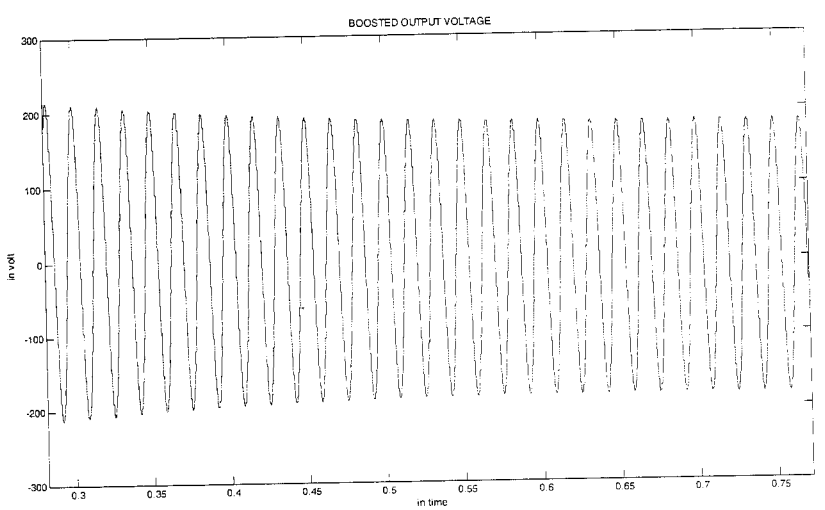


Fig 5.2.2 Boosted Output Voltage Waveform

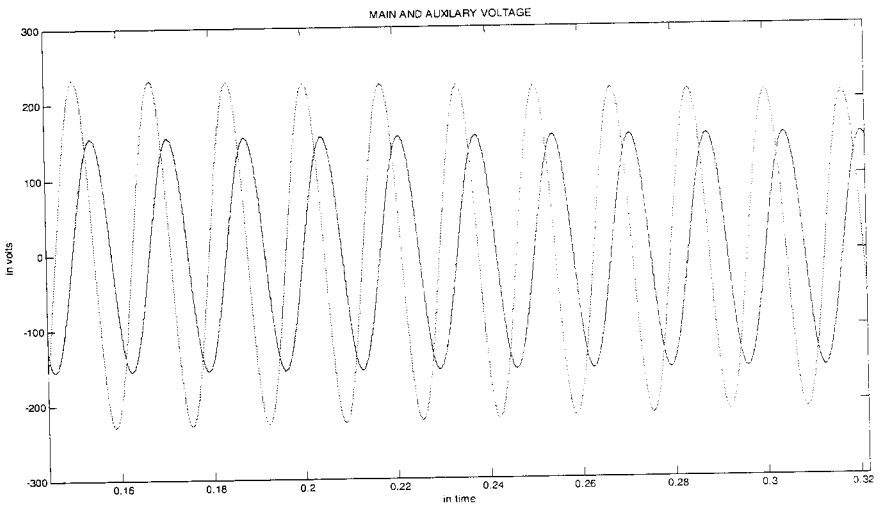


Fig 5.2.3 Main and Auxiliary Voltage Waveform

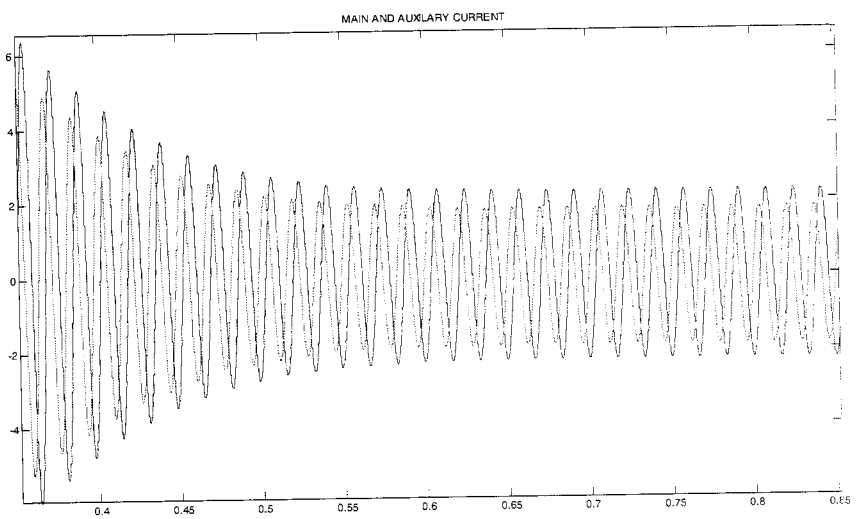


Fig 5.2.4 Main and Auxilary Current Waveform

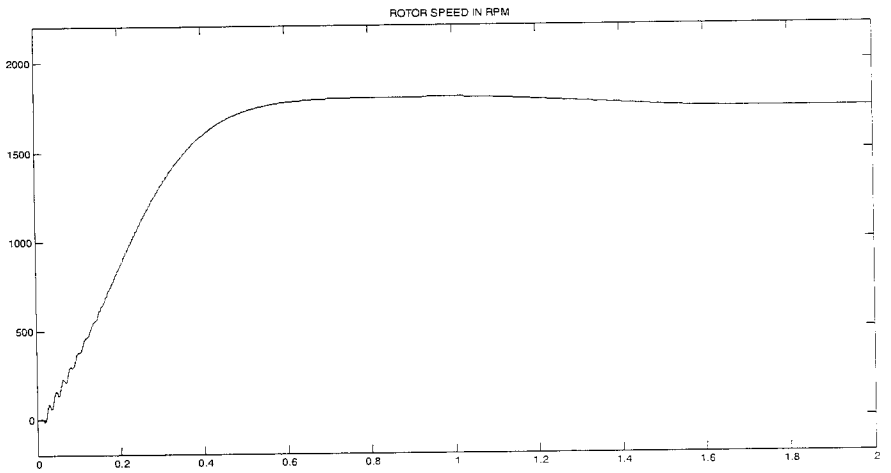


Fig 5.2.5 Rotor Speed Waveform

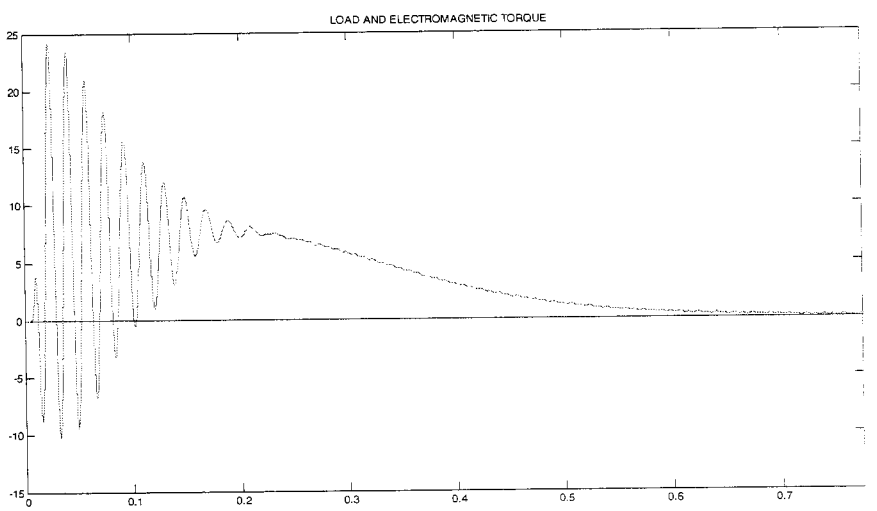


Fig 5.2.6 Torque Waveform

The above simulated output results prove that the given input voltage has been boosted to an appropriate level and also voltage is reduced as in buck operation. Moreover, other parameters like Main and Auxilary Current, Load and Electromagnetic Torque, Speed can also be determined.

Thus simulation result has been verified and tested using an experimental setup which is described in chapter 6.

CHAPTER 6

HARDWARE DESCRIPTION

6.1 IMPEDANCE SOURCE INVERTER UPS MODULE:

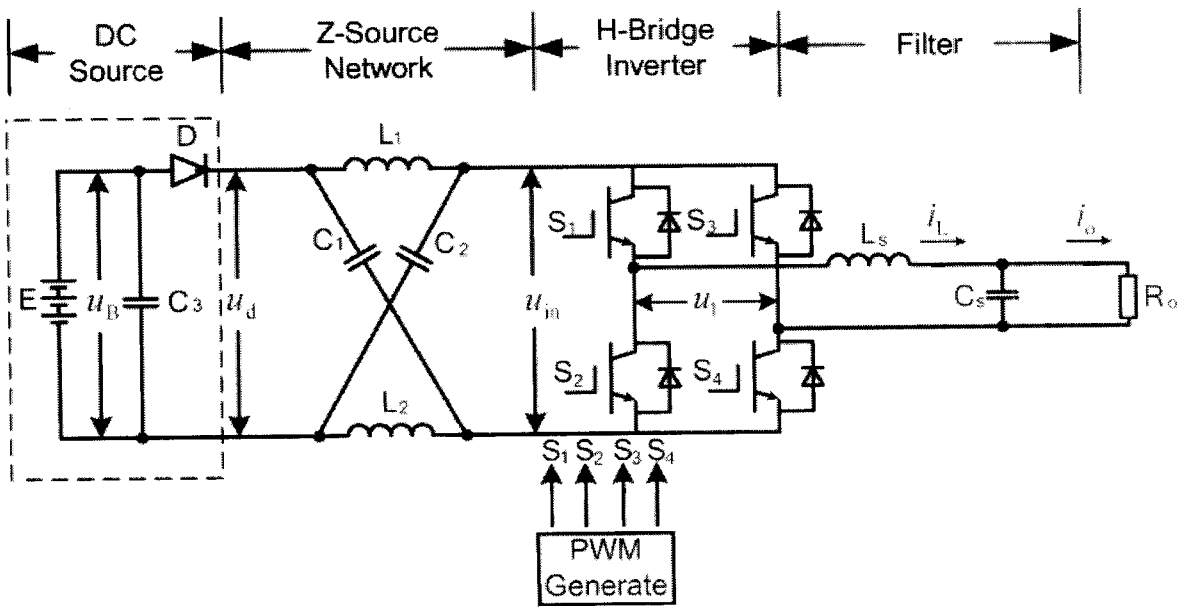


Figure 6.1 Hardware Circuit for Impedance Source Inverter

Figure 6.1 shows the circuit of a single phase impedance source inverter. To minimize the project cost and to reduce the circuit complications, the hardware implementation is done only for a single phase inverter.

The circuit consists of the following blocks

- Input Transformer
- Rectifier
- Impedance Source
- Inverter Bridge
- Power supply circuit
- Driver circuit

6.1.1 Input Transformer

The input transformer is a isolation transformer to isolate the circuit from the input supply surges.

6.1.2 Rectifier

The circuit involves one half controlled rectifier for converting the input ac into dc and the dc output of the rectifier is fed to the next stage via a filtering capacitor.

6.1.3 Impedance Source

In traditional inverters either a capacitor or an inductor is involved in the dc link. In voltage source inverters a capacitor is used where as in the current source inverters an inductor is used. But in this Impedance source inverter both the capacitor and an inductor is involved so that the rectifier output can be boosted as well as bucked as per the requirement. Here the capacitor and the inductor is connected in a manner so as the bridge looks like X . This bridge boosts the rectifier output so that the output of the inverter bridge is maintained as per the requirement.

6.1.4 Inverter Bridge

The circuit involves an single phase inverter which consists four MOSFETs as switching devices. They are named as Q1, Q2, Q3 and Q4.The snubber circuit has resistors and capacitors for protecting the bridge from over voltages and over current. The load used here involves resistor and an inductor. During the positive half cycle, MOSFETs Q1 and Q4 are conducting and MOSFETs Q3 and Q2 conduct during the negative half cycle.

6.1.5 Power Supply Circuit

All electronic circuits works only in low DC voltage, so we need a power supply unit to provide the appropriate voltage supply for their proper functioning .This unit consists of transformer, rectifier, filter & regulator. AC voltage of typically 230v rms

is connected to a transformer voltage down to the level to the desired ac voltage. A diode rectifier that provides the full wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation . A regulator circuit can use this dc input to provide dc voltage that not only has much less ripple voltage but also remains the same dc value even the dc voltage varies somewhat, or the load connected to the output dc voltages changes.

6.1.5.1 Transformer:

A transformer is a static piece of which electric power in one circuit is transformed into electric power of same frequency in another circuit. It can raise or lower the voltage in the circuit, but with a corresponding decrease or increase in current. It works with the principle of mutual induction. In our project we are using a step down transformer to providing a necessary supply for the electronic circuits. Here we step down a 230v ac into 12v ac.

6.1.5.2 Rectifier:

A dc level obtained from a sinusoidal input can be improved 100% using a process called full wave rectification. Here in our project for full wave rectification we use bridge rectifier. From the basic bridge configuration we see that two diodes (say D2 & D3) are conducting while the other two diodes
(D1 & D4) are in off state during the period t = 0 to T/2.Accordingly for the negative cycle of the input the conducting diodes are D1 & D4 .Thus the polarity across the load is the same.

6.1.5.3 Filters:

In order to obtain a dc voltage of 0 Hz, we have to use a low pass filter. So that a capacitive filter circuit is used where a capacitor is connected at the rectifier output& a dc is obtained across it. The filtered waveform is essentially a dc voltage with negligible ripples & it is ultimately fed to the load.

6.1.5.4 Regulators:

The output voltage from the capacitor is more filtered & finally regulated. The voltage regulator is a device, which maintains the output voltage constant irrespective of the

change in supply variations, load variations & temperature changes. Here we use fixed voltage regulator namely LM7805.The IC LM7805 is a +5v regulator which is used for microcontroller.

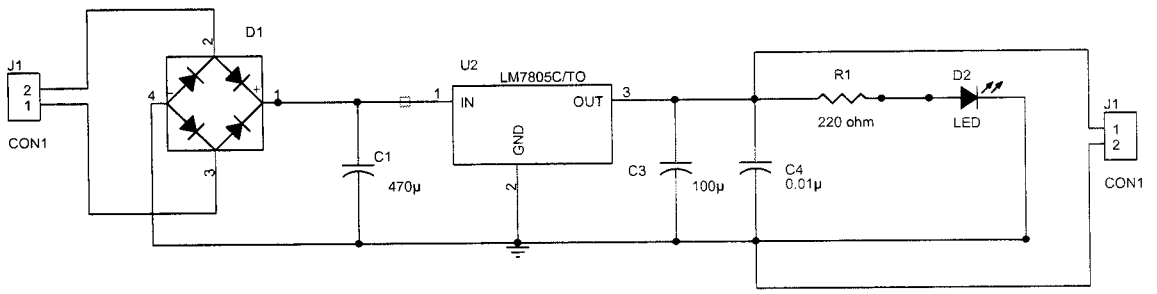


Fig 6.1.1 Circuit Diagram for Power Supply Circuit

6.1.6 Driver circuit:

The driver circuit forms the most important part of the hardware unit because it acts as the backbone of the inverter because it gives the triggering pulse to the switches in the proper sequence. It is used to provide 9 to 20 volts to switch the MOSFET Switches of the inverter. Driver amplifies the voltage from microcontroller which is 5volts. Also it has an Optocoupler for isolating purpose. So damage to MOSFET is prevented.

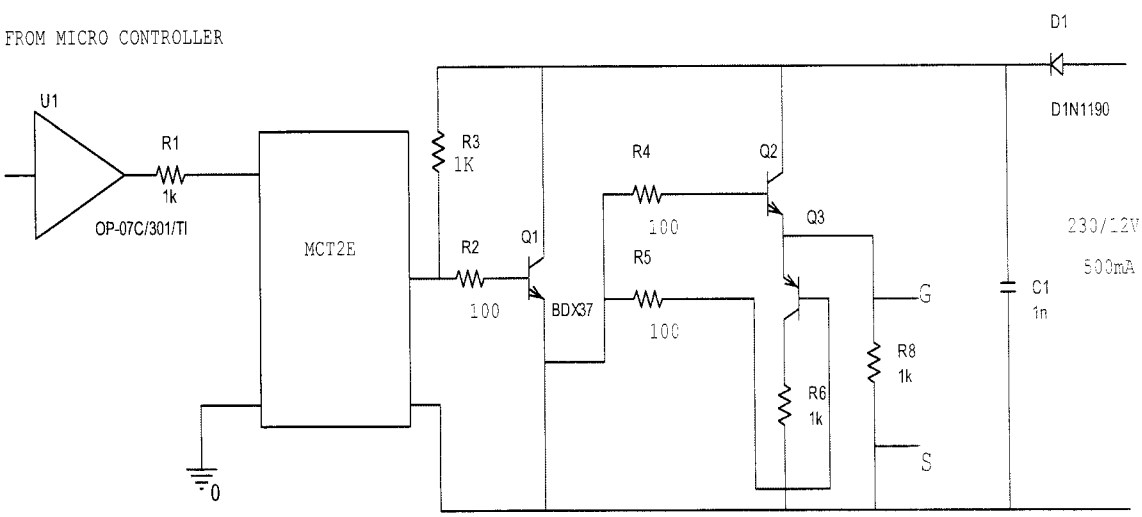


Fig 6.1.2 Driver Circuit diagram

The diagram given above gives the circuit operation of the driver unit. The driver unit contains the following units.

- Optocoupler
- Capacitor
- Supply
- Diode
- Resistor

6.1.6.1 Optocoupler

Optocoupler is also termed as optoisolator. Optoisolator a device which contains a optical emitter, such as an LED, neon bulb, or incandescent bulb, and an optical receiving element, such as a resistor that changes resistance with variations in light intensity, or a transistor, diode, or other device that conducts differently when in the presence of light. These devices are used to isolate the control voltage from the controlled circuit.

Optocoupler not only separates the high voltage input side and the microcontroller but also prevents damage to the microcontroller due to the line voltage transistor. It also reduces the effects of electrical noise common in industrial environments, which cause erratic operation of the microcontroller.

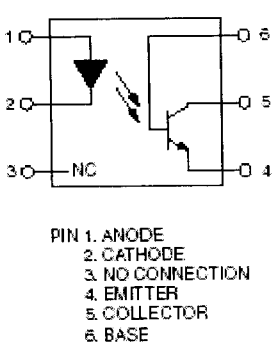


Fig 6.1.3 Pin Details of MC2TE

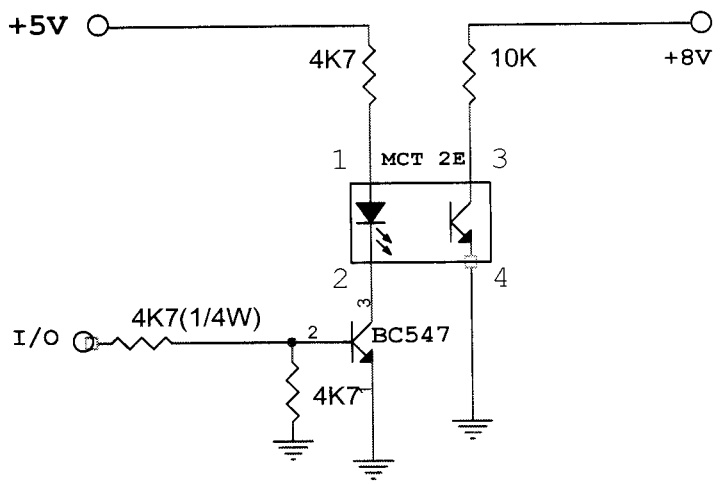


Fig 6.1.4 Circuit representation of Optocoupler

6.2 PULSE WIDTH MODULATION

The advent of the transformer less multilevel inverter topology has brought forth various pulse width modulation (PWM) schemes as a means to control the switching of the active devices in each of the multiple voltage levels in the inverter. The most efficient method of controlling the output voltage is to incorporate pulse width modulation control (PWM control) within the inverters. In this method, a fixed d.c. input voltage is supplied to the inverter and a controlled a.c. output voltage is obtained by adjusting the on and–off periods of the inverter devices. Voltage-type PWM inverters have been applied widely to such fields as power supplies and motor drivers. This is because: (1) such inverters are well adapted to high-speed self turn-off switching devices that, as solid-state power converters, are provided with recently developed advanced circuits; and (2) they are operated stably and can be controlled well.

The PWM control has the following advantages:

(i) The output voltage control can be obtained without any additional components.

(ii) With this type of control, lower order harmonics can be eliminated or minimized along with its output voltage control. The filtering requirements are minimized as higher order harmonics can be filtered easily.

The commonly used PWM control techniques are:

- Sinusoidal pulse-width modulation
- Single-pulse-width modulation
- Multiple-pulse-width modulation
- Modified sinusoidal pulse-width modulation
- Phase-displacement control

The performance of each of these control methods is usually judged based on the following parameters: a) Total harmonic distortion (THD) of the voltage and current at the output of the inverter, b) Switching losses within the inverter, c) Peak-to-peak ripple in the load current, and d) Maximum inverter output voltage for a given DC rail voltage.

From the above all mentioned PWM control methods, the Sinusoidal pulse width modulation (sin PWM) is applied in the proposed inverter since it has various advantages over other techniques. **Sinusoidal PWM inverters provide an easy way to control amplitude, frequency and harmonics contents of the output voltage.**

6.2.1 Sinusoidal Pulse Width Modulation

In the Sinusoidal pulse width modulation scheme, as the switch is turned on and off several times during each half-cycle, the width of the pulses is varied to change the output voltage. Lower order harmonics can be eliminated or reduced by selecting the type of modulation for the pulse widths and the number of pulses per half-cycle. Higher order harmonics may increase, but these are of concern because they can be eliminated easily by filters. The SPWM aims at generating a sinusoidal inverter output voltage without low-order harmonics. This is possible if the sampling frequency is high compared to the fundamental output frequency of the inverter.

Sinusoidal pulse width modulation is one of the primitive techniques, which are used to suppress harmonics presented in the quasi-square wave. In the modulation techniques, there are two important defined parameters: 1) the ratio $P = \omega_c/\omega_m$ known as frequency ratio, and 2) the ratio $M_a = A_m/A_c$ known as modulation index, where ω_c is the reference frequency,

ω_m is the carrier frequency, A_m is reference signal amplitude and A_c is carrier signal amplitude.

6.3 PIC MICROCONTROLLER

16F877A PIC Microcontroller is used for controlling the width of the pulses from PWM generator, by fixing either the frequency or voltage so that the MOSFETs are turned ON and OFF in the desired sequence

6.3.1 The need for micro controller based PWM generation

- Micro controller has inbuilt functions such as timer, ADC, PWM, oscillator which reduce the hardware components used.
- PWM technique used enables the reduction of harmonics
- Wide variation in speed since frequency is used as control parameter.
- Digital circuits used employ a faster response.
- Automatic speed control is achieved since no manual parts all involved.
- The Micro controller IC Chip senses the input speed requirement and gives the output in favor of the input.
- No external commutation circuits are required.

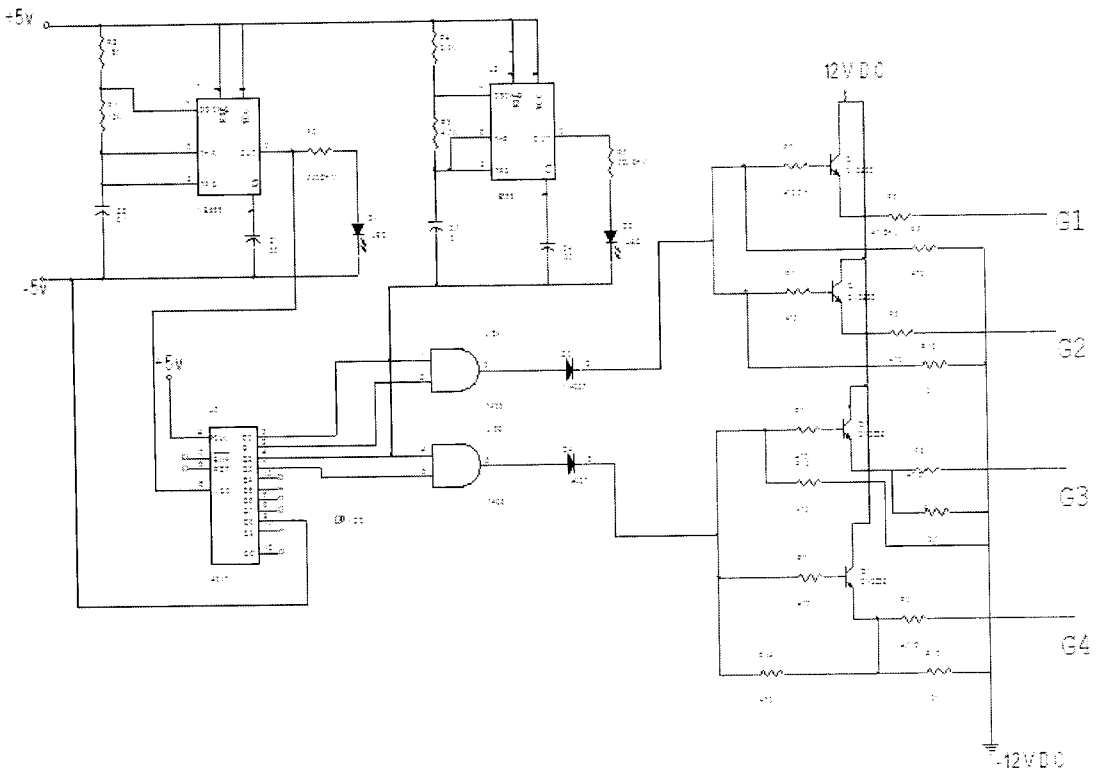


Figure 6.3 PIC 16F877A based control circuit for inverter

Figure 6.3 shows the complete triggering circuit for the single phase impedance source inverter. The outputs G1, G2, G3 and G4 are the gate pulses applied to the MOSFET switches. The sequence of switching is controlled by the microcontroller. The coding for that control is given in appendix A.

6.3.2 Core Features

- High-performance RISC CPU
- Only 35 single word instructions to learn
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory,
  Up to 368 x 8 bytes of Data Memory (RAM)
  Up to 256 x 8 bytes of EEPROM data memory
- Interrupt capability (up to 14 internal/external
- Eight level deep hardware stack

- ❖ Direct, indirect, and relative addressing modes
- ❖ Power-on Reset (POR)
- ❖ Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- ❖ Watchdog Timer (WDT) with its own on-chip RC Oscillator for reliable operation
- ❖ Programmable code-protection
- ❖ Power saving SLEEP mode
- ❖ Selectable oscillator options
- ❖ In-Circuit Serial Programming (ICSP) via two pins
- ❖ Only single 5V source needed for programming capability
- ❖ In-Circuit Debugging via two pins
- ❖ Wide operating voltage range: 2.5V to 5.5V
- ❖ High Sink/Source Current: 25 mA
- ❖ Commercial and Industrial temperature ranges
- ❖ Low-power consumption:

  < 2 mA typical @ 5V, 4 MHz

  20mA typical @ 3V, 32 kHz

  < 1mA typical standby current

6.3.3 Memory Organization

The organization of memory in PIC 16F877A is shown in the following table.

TABLE-6.1 MEMORY OF PIC 16F877

DEVICE	PROGRAM FLASH	DATA MEMORY	DATA EEPROM
PIC 16F877	8K	368 Bytes	256 Bytes

6.3.4 Program Memory Organization

The PIC16f877 devices have a 13-bit program counter capable of addressing 8K *14 words of FLASH program memory. Accessing a location above the physically implemented address will cause a wraparound.

The RESET vector is at 0000h and the interrupt vector is at 0004h.

6.3.5 Data Memory Organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the special functions Registers. Bits RP1 (STATUS<6) and RP0 (STATYUS<5>) are the bank selected bits.

TABLE 6.2 BANK SELECTION

RP1:RP0	Banks
00	0
01	1
10	2
11	3

Each bank extends up to 7Fh (1238 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM.

All implemented banks contain special function registers. Some frequently used special function registers from one bank may be mirrored in another bank for code reduction and quicker access.

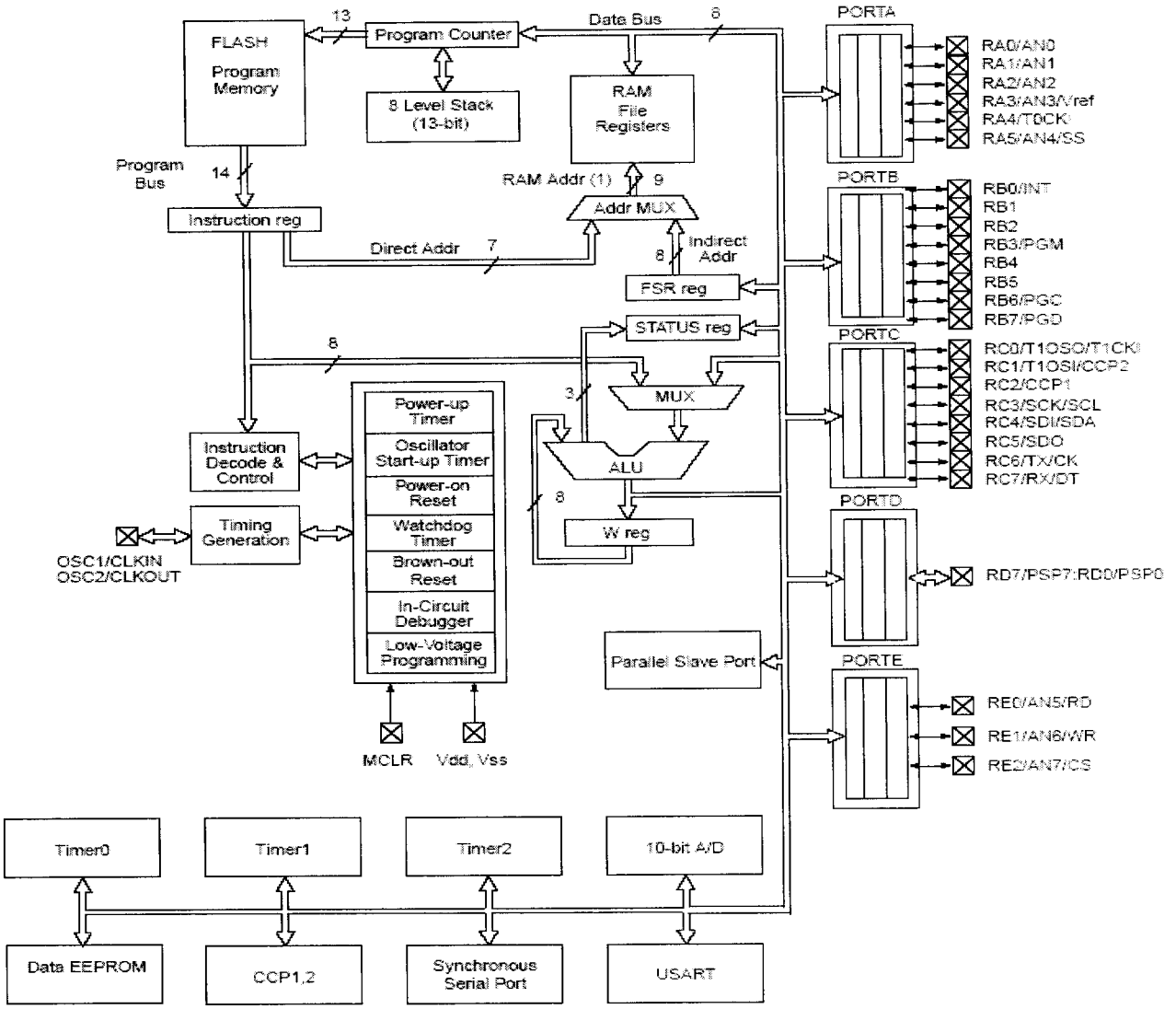
6.3.6 Peripheral Features

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
  - Capture is 16-bit, max resolution is 12.5 ns,
  - Compare is 16-bit, max resolution is 200 ns,
  - PWM max. Resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI. (Master Mode) and I2C. (Master/Slave)
- USART/SCI with 9-bit address detection.
- Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls

These are some of the important features of the peripherals available in PIC16F77A Microcontroller. The next section gives the Architecture and pin details of the controller.

6.3.7 Architecture Of PIC 16F877A

Device	Program Flash	Data Memory	Data EEPROM
PIC16F874	4K	192 Bytes	128 Bytes
PIC16F877	8K	368 Bytes	256 Bytes



Note 1: Higher order bits are from the STATUS register.

Figure 6.4 .Architecture of PIC 16F877A Microcontroller

6.3.8 16F877A PIC Microcontroller Pin Diagram:

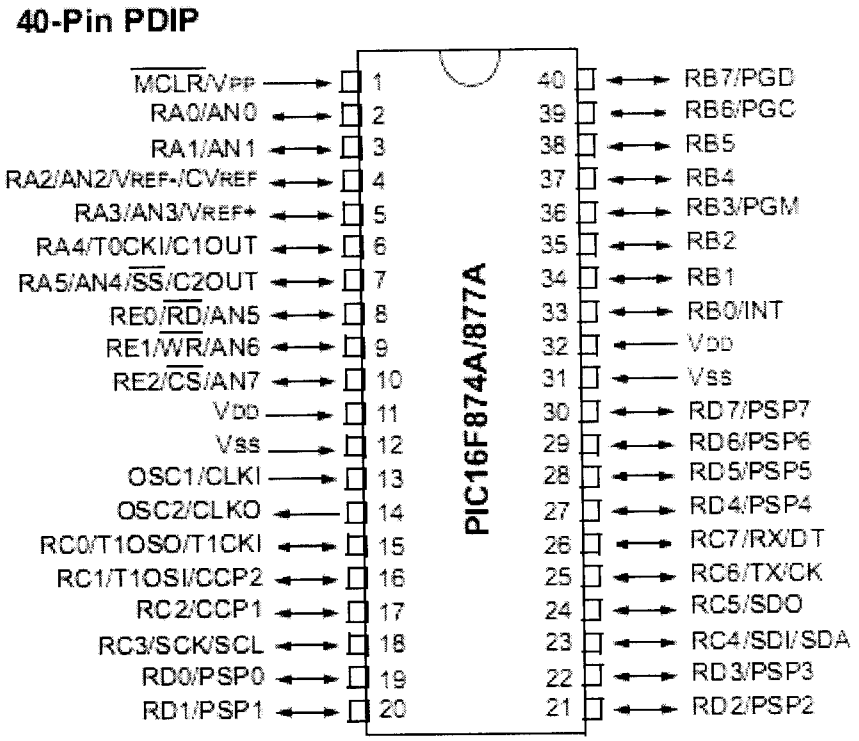


Figure 6.5 Pin diagram of PIC 16F877 Microcontroller

Figure 6.5 shows the pin out diagram of the PIC 16F877 Microcontroller. It is a 40 pin dual inline package (DIP) IC. It has five input / output ports named as Port A, Port B, Port C, Port D and Port E .

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin. The detailed description of the ports are given in Appendix A. Figure 20 gives the pin diagram of the PIC 16F877A Microcontroller

6.4 EXPERIMENTAL SETUP:

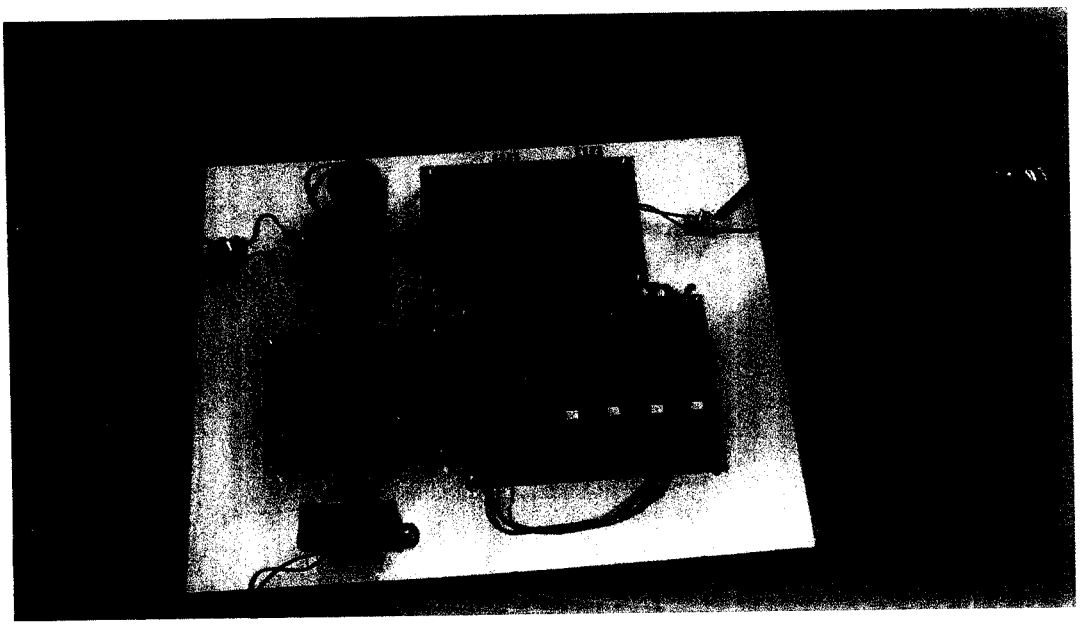


Fig 6.7 Hardware prototype model

6.5 HARDWARE RESULTS

The new impedance source inverter for UPS application is designed and implemented. The hardware is tested with various input voltages to the impedance network and the output voltages are obtained and tabulated. Without modifying the main circuit we can also perform the buck and boost operations individually.

SNO	INPUT VOLTAGE	OUTPUT VOLTAGE
1	50	72
2	50	64
3	50	58

CHAPTER 7

CONCLUSIONS AND SCOPE FOR FUTURE WORK

7.1 CONCLUSION

- A new type of inverter for UPS application has been designed.
- The new Impedance source inverter system provides ride through capability during voltage sags.
- It incorporates single stage power conversion, and doesn't need any additional components and energy storage. Hence component cost is reduced to a greater extent.
- The Impedance source inverter is also suited for fuel cell application and AC electrical drives.

The impedance source technology can be applied to the entire spectrum of power conversion.

7.2 SCOPE FOR FUTURE WORK:

The voltage and current source inverters cannot be operated in shoot through mode. In voltage source inverter the incoming MOSFETs should be turned on, only after the outgoing MOSFETs are turned off completely. Otherwise the devices would be damaged. This introduces a delay in switching and therefore we get a pulsating output waveform.

In current source inverter, the incoming MOSFETs should be turned on, before the outgoing pair is completely turned off. This operation introduces an overlap in switching and hence we get a pulsating output waveform.

In impedance source inverter we are getting a smooth waveform, because shoot through mode is possible. This would be helpful for carrying out the following projects.

- Design of impedance source inverter for torque pulsation free induction motor drives
- Design of impedance source inverter for torque pulsation free synchronous motor drives

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APPENDIX A

16F877 PIC MICROCONTROLLER CODING & DETAILS

Code:

```
#include<pic.h>
#include<stdio.h>
#include"delay.c"

CONFIG(0x3f71);

void main()
{
        TRISC=0x00;
        PORTC=0x00;


        while(1)
        {
//SECTOR-I
                PORTC=0x2A;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x23;
                DelayUs(250);
                DelayUs(167);


                PORTC=0x07;
                DelayUs(250);
                DelayUs(167);
```

```
                PORTC=0x15;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x15;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x07;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x23;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x2A;
                DelayUs(250);
                DelayUs(167);

// SECTOR-II
                PORTC=0x2A;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x0E;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x07;
                DelayUs(250);
                DelayUs(167);
```

```
                PORTC=0x15;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x15;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x07;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x0E;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x2A;
                DelayUs(250);
                DelayUs(167);

//SECTOR-III
                PORTC=0x2A;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x0E;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x1C;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x15;
```

```
                DelayUs(250);
                DelayUs(167);
                PORTC=0x15;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x0C;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x0E;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x2A;
                DelayUs(250);
                DelayUs(167);

//SECTOR-IV
                PORTC=0x2A;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x38;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x1C;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x15;
                DelayUs(250);
                DelayUs(167);
```

```
                PORTC=0x15;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x1C;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x38;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x2A;
                DelayUs(250);
                DelayUs(167);

//SECTOR-V
                PORTC=0x2A;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x38;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x31;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x15;
                DelayUs(250);
                DelayUs(167);
```

```
                PORTC=0x15;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x31;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x38;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x2A;
                DelayUs(250);
                DelayUs(167);

//SECTOR-VI
                PORTC=0x2A;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x23;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x31;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x15;
                DelayUs(250);
                DelayUs(167);

                PORTC=0x15;
```

```
DelayUs(250);
DelayUs(167);
PORTC=0x31;
DelayUs(250);
DelayUs(167);

PORTC=0x23;
DelayUs(250);
DelayUs(167);

PORTC=0x2A;
DelayUs(250);
DelayUs(167);

}
```

APPENDIX B

16F877 PIC MICROCONTROLLER

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P type	Buffer Type	Description
OSC1/CLKIN	13	14	30	I	ST/CMOS[4]	Oscillator crystal or external clock source input.
OSC2/CLKOUT	14	15	31	O	—	Oscillator crystal or clock output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/VPP	1	2	18	I/P	ST	Master clear (reset) input or programming voltage input or high voltage test mode control. This pin is an active low reset to the device.
RA0/AN0	2	3	19	I/O	TTL	PORTA is a bi-directional I/O port.
RA1/AN1	3	4	20	I/O	TTL	RA0 can also be analog input0
RA2/AN2/VREF-	4	5	21	I/O	TTL	RA1 can also be analog input1
RA3/AN3/VREF+	5	6	22	I/O	TTL	RA2 can also be analog input2 or negative analog reference voltage.
RA4/T0CKI	6	7	23	I/O	ST	RA3 can also be analog input3 or positive analog reference voltage.
RA5/SS/AN4	7	8	24	I/O	TTL	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
						RA5 can also be analog input4 or the slave select for the synchronous serial port.
RB0/INT	33	35	8	I/O	TTL/ST[1]	PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB1	34	37	9	I/O	TTL	RB0 can also be the external interrupt pin.
RB2	35	38	10	I/O	TTL	
RB3/PGM	36	39	11	I/O	TTL	RB3 can also be the low voltage programming input
RB4	37	41	14	I/O	TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6/PGC	39	43	16	I/O	TTL/ST[2]	Interrupt on change pin or In-Circuit Debugger pin. Serial programming clock.
RB7/PGD	40	44	17	I/O	TTL/ST[3]	Interrupt on change pin or In-Circuit Debugger pin. Serial programming data.

Pin Out Description

I/O PORTS:

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

PORTA and the TRISA Register

PORTA is a 6-bit wide bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (=1) will make the corresponding PORTA pin an input, i.e., put the corresponding output driver in a Hi-impedance mode. Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output, i.e., put the contents of the output latch on the selected pin.

Reading the PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore a write to a port implies that the port pins are read; this value is modified, and then written to the port data latch. Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers. Other PORTA pins are multiplexed with analog inputs and analog VREF input. The operation of each pin is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register1).

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

PORT A Function

Name	Bit#	Buffer	Function
RA0/AN0	bit0	TTL	Input/output or analog input
RA1/AN1	bit1	TTL	Input/output or analog input
RA2/AN2	bit2	TTL	Input/output or analog input
RA3/AN3/VREF	bit3	TTL	Input/output or analog input or VREF
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0 Output is open drain type
RA5/$\overline{SS}$/AN4	bit5	TTL	Input/output or slave select input for synchronous serial port or analog input

PORTB and the TRISB Register

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input, i.e., put the corresponding output driver in a hi-impedance mode.

Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output, i.e., put the contents of the output latch on the selected pin. Three pins of PORTB are multiplexed with the Low Voltage Programming function; RB3/PGM, RB6/PGC and RB7/PGD. The alternate functions of these pins are described in the Special Features Section. Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>). This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.

b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared. The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature. This interrupt on mismatch feature, together with software configurable pull-ups on these four pins, allow easy interface to a keypad and make it possible for wake-up on key depression

Port B Functions

Name	Bit#	Buffer	Function
RB0/INT	bit0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3/PGM	bit3	TTL	Input/output pin or programming pin in LVP mode. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6/PGC	bit6	TTL/ST(2)	Input/output pin (with interrupt on change) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming clock.
RB7/PGD	bit7	TTL/ST(2)	Input/output pin (with interrupt on change) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

PORT C and the TRISC Register

PORTC is an 8-bit wide bi-directional port. The corresponding data direction register is TRISC. Setting a TRISC bit (=1) will make the corresponding PORTC pin an input, i.e.,

put the corresponding output driver in a hi-impedance mode. Clearing a TRISC bit (=0) will make the corresponding PORTC pin an output, i.e., put the contents of the output latch on the selected pin. PORTC is multiplexed with several peripheral functions(Table-3.5). PORTC pins have Schmitt Trigger input buffers.

When the I2C module is enabled, the PORTC (3:4) pins can be configured with normal I2C levels or with SMBUS levels by using the CKE bit (SSPSTAT <6>).

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify write instructions (BSF, BCF, XORWF) with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

Port C Functions

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input
RC1/T1OSI/CCP2	bit1	ST	Input/output port pin or Timer1 oscillator input or Capture2 input/ Compare2 output/PWM2 output
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I^2C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	bit5	ST	Input/output port pin or Synchronous Serial Port data output
RC6/TX/CK	bit6	ST	Input/output port pin or USART Asynchronous Transmit or Synchro-nous Clock
RC7/RX/DT	bit7	ST	Input/output port pin or USART Asynchronous Receive or Synchro-nous Data

Legend: ST = Schmitt Trigger input

PORT D and TRISD Registers

This section is not applicable to the 28-pin devices. PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

PORTD can be configured as an 8-bit wide microprocessor Port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

Port D Functions

Name	Bit#	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL(1)	Input/output port pin or parallel slave port bit0
RD1/PSP1	bit1	ST/TTL(1)	Input/output port pin or parallel slave port bit1
RD2/PSP2	bit2	ST/TTL(1)	Input/output port pin or parallel slave port bit2
RD3/PSP3	bit3	ST/TTL(1)	Input/output port pin or parallel slave port bit3
RD4/PSP4	bit4	ST/TTL(1)	Input/output port pin or parallel slave port bit4
RD5/PSP5	bit5	ST/TTL(1)	Input/output port pin or parallel slave port bit5
RD6/PSP6	bit6	ST/TTL(1)	Input/output port pin or parallel slave port bit6
RD7/PSP7	bit7	ST/TTL(1)	Input/output port pin or parallel slave port bit7

Legend: ST = Schmitt Trigger input TTL = TTL input
Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffer when in Parallel Slave Port Mode

PORTE and TRISE Register

PORTE has three pins RE0/RD/AN5, RE1/WR/AN6 and RE2/CS/AN7, which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers.

The PORTE pins become control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make sure that the TRISE<2:0> bits are set (pins are configured as digital inputs). Ensure ADCON1 is configured for digital I/O. In this mode the input buffers are TTL.

PORTE pins are multiplexed with analog inputs. When selected as an analog input, these pins will read as '0's. TRISE controls the direction of the RE pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.

Port E Functions

Name	Bit#	Buffer Type	Function
RE0/$\overline{RD}$/AN5	bit0	ST/TTL(1)	Input/output port pin or read control input in parallel slave port mode or analog input: $\overline{RD}$ 1 = Not a read operation 0 = Read operation. Reads PORTD register (if chip selected)
RE1/$\overline{WR}$/AN6	bit1	ST/TTL(1)	Input/output port pin or write control input in parallel slave port mode or analog input: $\overline{WR}$ 1 =Not a write operation 0 =Write operation. Writes PORTD register (if chip selected)
RE2/$\overline{CS}$/AN7	bit2	ST/TTL(1)	Input/output port pin or chip select control input in parallel slave port mode or analog input: $\overline{CS}$ 1 = Device is not selected 0 = Device is selected

Legend: ST = Schmitt Trigger input TTL = TTL input
Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port Mode.

Instruction Set Summary

Each PIC 16f877 instruction is a 14-bit word, divided into an OPCODE which specifies the instruction type and one or more operand which further specify the operation of the instruction. The PIC16F877 instruction set summary in table 12 lists byte-oriented, bit-oriented, and literal and control operations. Table11 shows the opcode Field descriptions.

For byte-oriented instructions, 'f; represents a file register designator and 'd' represents a destination designator. The file register designator speciri4s which file register is to be used by the instruction. The destination designator specified where the result of the operation is to be placed. If'd' is zero, the result is placed in the w register. If'd' is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, which 'f' represents the address of the file in which the bits is located.

For literal and control operations, 'k' represents an eight or eleven bit constant or literal value.

Opcode Field Descriptions

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
PC	Program Counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit

The instruction set is highly orthogonal and is grouped into three basic categories:

- Byte-oriented operations
- Bit-oriented operations
- Literal and control operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 ms. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 ms.

16F877A INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS						
ADDWF	f, d	Add W and f	1	00 0111 dfff ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00 0101 dfff ffff	Z	1,2
CLRF	f	Clear f	1	00 0001 lfff ffff	Z	2
CLRW	-	Clear W	1	00 0001 0xxx xxxx	Z	
COMF	f, d	Complement f	1	00 1001 dfff ffff	Z	1,2
DECF	f, d	Decrement f	1	00 0011 dfff ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00 1011 dfff ffff		1,2,3
INCF	f, d	Increment f	1	00 1010 dfff ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00 1111 dfff ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00 0100 dfff ffff	Z	1,2
MOVF	f, d	Move f	1	00 1000 dfff ffff	Z	1,2
MOVWF	f	Move W to f	1	00 0000 1fff ffff		
NOP	-	No Operation	1	00 0000 0xx0 0000		
RLF	f, d	Rotate Left f through Carry	1	00 1101 dfff ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00 1100 dfff ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00 0010 dfff ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00 1110 dfff ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00 0110 dfff ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS						
BCF	f, b	Bit Clear f	1	01 00bb bfff ffff		1,2
BSF	f, b	Bit Set f	1	01 01bb bfff ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01 10bb bfff ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01 11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS						
ADDLW	k	Add literal and W	1	11 111x kkkk kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11 1001 kkkk kkkk	Z	
CALL	k	Call subroutine	2	10 0kkk kkkk kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00 0000 0110 0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10 1kkk kkkk kkkk		
IORLW	k	Inclusive OR literal with W	1	11 1000 kkkk kkkk	Z	
MOVLW	k	Move literal to W	1	11 00xx kkkk kkkk		
RETFIE	-	Return from interrupt	2	00 0000 0000 1001		
RETLW	k	Return with literal in W	2	11 01xx kkkk kkkk		
RETURN	-	Return from Subroutine	2	00 0000 0000 1000		
SLEEP	-	Go into standby mode	1	00 0000 0110 0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11 110x kkkk kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11 1010 kkkk kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.