DESIGN AND IMPLEMENTATION OF EMBEDDED CONTROLLER FOR THREE PHASE INVERTER

A PROJECT REPORT

Submitted by

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BONAFIDE CERTIFICATE

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CERTIFICATE

This is to certify that the final year B.E.,(Electrical and Electronics Engineering) Students of **KUMARAGURU COLLEGE OF TECHNOLOGY,CHINNAVEDAMPATTI, COIMBATORE-641006** have done their project titled " **DESIGN AND IMPLEMENTATION OF EMBEDDED CONTROLLER FOR THREE PHASE INVERTERS**".

The product has functioned very well as indicated in the project work and we found that the product is useful for manufacturing and marketing. We found the students as intelligent, hard working, sincere and good at analysis. We wish them a bright and prosperous future.

Name of the students

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ABSTRACT

In conventional Digital controllers, the PWM gating signal generation, current control loop for stator current regulation, dead time generation and other computational tasks require high sampling rate to achieve wide bandwidth performance. In most of the domestic inverters the PWM generation is implemented in analog circuits. In this project a three phase Sinusoidal PWM controller in an embedded micro controller is designed and implemented. The output fundamental frequency and the switching frequency can be varied. The prototype of the inverter with driver and opto circuits are designed and implemented to verify the PWM controller in real time. The output of the three phase inverter is tested with an induction motor. The induction motor runs at 25 Hz and 50 Hz. The speed is varied.

ACKNOWLEDGEMENT

The completion of our project can be attributed to the combined efforts made by us and the contribution made in one form or the other by the individuals we hereby acknowledge.

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LIST OF SYMBOLS AND ABBREVIATIONS

NO.	SYMBOLS	ABBREVIATIONS
01	AC	Alternating Current
02	DC	Direct Current
03	PWM	Pulse Width Modulation
04	PIC	Programmable interface control
05	MOSFET	Metal Oxide Semiconductor Field Effect Transistor
06	MC	Micro controller
07	IC	Integrated Circuit
08	DSP	Digital Signal Processing
09	VFD	Variable Frequency Drive
10	ASD	Adjustable Speed Drive
11	ASIC	Application Specific Integrated circuit
12	PLD	Programmable Logic Device
13	CLB	Configurable Logic Block
14	IOB	Input Output Block
15	I/O	Input / Output
16	LUT	Look Up Table
17	SRAM	Static Random Access Memory
18	PCB	Printed Circuit Board
19	CMOS	Complementary metal oxide semiconductor

CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION:

The unpredicted development in industrial drives over the past two decades have resulted from the process developments demanded by the automation industry. This is further augmented with increased speed of modern microprocessors, micro controllers, digital signal processors (DSP), complex programmable logic devices (CPLD), Application Specific Integrated Circuit (ASIC) technology and Field Programmable Gate Array (FPGA) based control techniques used in reduced insulated gate bipolar transistor (IGBT) drive package size coupled with AC motors leads to achievement of multiple machine configuration with minimal process down time. In the conventional drives, the functions like current control loop and PWM generation are still implemented with analog control. This kind of control has an advantage of good dynamic response but suffers by the drawbacks like complexity, limited functions and the difficulty in circuit modification.

Now a day's microcontroller based control in AC drives has become the intensive area of research due to its features of simple circuitry, software control and flexibility to adapt various applications. However, PWM generation and current control loop requires high sampling rate to achieve wide bandwidth performance. Therefore, most computational resources of the controller must be utilized for PWM gating signal generation and the execution of current control loop algorithms .Only a limited time is left to control other functions of the drive.

This project "Embedded based control for three phase Inverter" develops a novel digital circuit realization scheme for the operation of three phase inverters.

1.2 NEED FOR THE PROJECT:

In recent times, variable speed AC Induction motors powered by switching power converters are becoming more and more popular due to the advances in solid state power devices. Switching power converters offer an easy way to regulate both the frequency and magnitude of the voltage and current applied to a motor. As a result much higher efficiency and performance can be achieved by these motor drives with reduced harmonics. The energy that a switching power converter delivers to a motor is controlled by Pulse Width Modulated (PWM) signals applied to the gates of the power transistors. PWM signals are pulse trains with fixed frequency and magnitude and variable pulse width. When a PWM signal is applied to the gate of a power transistor, it causes the output voltage of the inverter to vary according to its turn on time. The inverter converts DC power to AC power at the required frequency and amplitude. The inverter consists of six power MOSFETs that turn on and off in a desired pattern to produce three phase AC output voltage. The control IC is programmed and implemented in Microcontroller to generate PWM gating pulses for the MOSFETs.

In this project we develop a embedded controller for inverter using microcontroller. The output voltage of the inverter is varied by varying the PWM switching frequency of the gating pulses given to the power transistors (MOSFETs) of the inverter. The PWM switching frequency can be varied to a maximum of 10KHz. High switching frequency is achieved which improves the performance by reducing total harmonics distortion and switching loss.

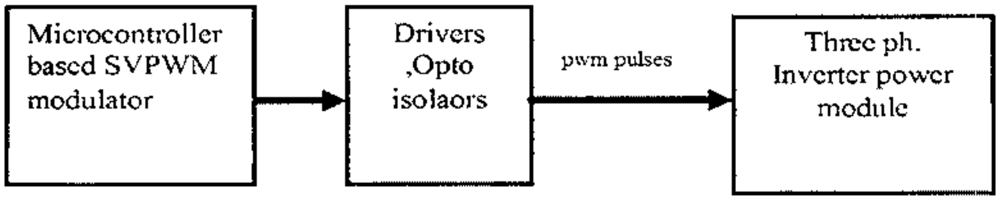

Fig 1.1 System block diagram

1.3 OBJECTIVE:

The main objective of this project is to design and develop Embedded based controller for inverters and to Obtain variable operation voltage and frequency digitally.

1.4 ADVANTAGES OVER THE EXISTING SYSTEM:

Analog control scheme possesses the advantage of fast dynamic response, but suffers the disadvantages of complex circuitry, limited functions, high cost, low processing speed and difficulty in circuit modification. The rapid development in high-performance low-cost microcontrollers has encouraged research on digital PWM control. This control scheme has the advantages of simple circuitry, software control, and flexibility in adaptation to various applications..

- Digital functions make a high scale of integration possible
- Digital technology results in lower cost, high reliability , less floor space and low power consumption.
- This technology offers flexibility and it provides better noise tolerance .

1.5 EXPECTED OUTPUT:

The designed P\/M inverter control IC has been realized using PIC16F877A. Owing to the advantages of digital over analog .Six gate pulses from S1 through S6 from the microcontroller are given to the MOSFET inverter module. The graph shows the six gate pulses S1, S2, S3, S4, S5, S6 and R,Y,B are the 3 phase Inverter output voltage when connected to resistive load.

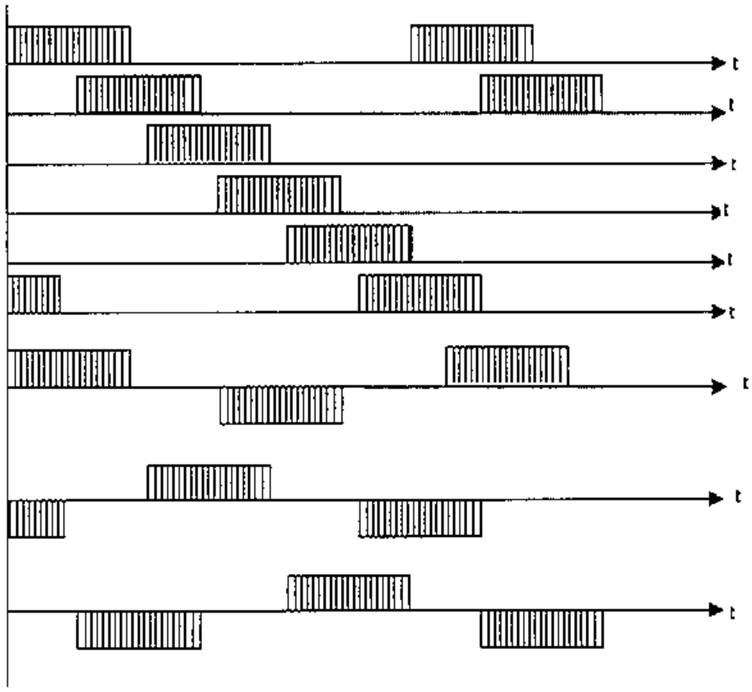

Fig 1.2 Sample output waveform

1.6 ORGANIZATION OF THE REPORT

Chapter 1: Introduction to the project stating the need for this approach, objective and methodology

Chapter 2: PWM Inverter – Gives a brief idea about the types of inverter, their operation, basics of three phase inverter and its modes of conduction, PWM technique types, applications and its advantages.

Chapter 3: Gives the details about the hardware implementation. The isolation circuit, Driver circuit and the power module are described

Chapter 4: Microcontroller – Describes about PIC 16F877, its architecture, design flow and applications. Details the architecture and features of the microcontroller used

Chapter 5: Software code.

Chapter 6: Conclusion – The project done and the scope for future work are discussed.

Appendices: Gives the features and the specification of the ICs and the PIC microcontroller Used.

1.7 METHODOLOGY:

1. Design of SPWM modulator in Embedded -C.
2. The simulation is carried out using MPLAB software.
3. The Implementation is carried out using 8 or 16 bit micro controller.
4. The total hardware consists of inverter power module, driver, opto isolator and embedded controller.

CHAPTER 2

INVERTERS - AN OVERVIEW

2.1 INVERTER BASICS

Introduction

An **inverter** is an electronic circuit for converting direct current (DC) to alternating current (AC). Inverters are used in a wide range of applications, from small switched power supplies for a computer to large electric utility applications to transport bulk power. The "H" bridge inverter and the centre tapped inverter are the two basic circuits for controlled power flow between DC and AC circuits. Alternative DC-AC connections such as the phase controlled rectifier exist but cannot arbitrarily control the power flow and generally require a strong AC supply with which to connect.

They are of two types

1. Single phase inverters
2. Three phase inverters.

Here we are using three phase inverters so lets see a brief description about this inverter

2.2 THREE PHASE INVERTER

2.2.1 Introduction

The inverter consists of three half-bridge units where the upper and lower switches are controlled complimentarily. The three phase voltage source inverter is shown in figure 3.3. As the power device's turn-off time is longer than its turn-on time, some dead-time must be inserted between the turn-off of one transistor of the half-bridge and turn-on of its complementary device. The output voltage is created by a pulse width modulation (PWM) technique. The 3-phase voltage waves are shifted 120° to each other and thus a 3-phase motor can be supplied.

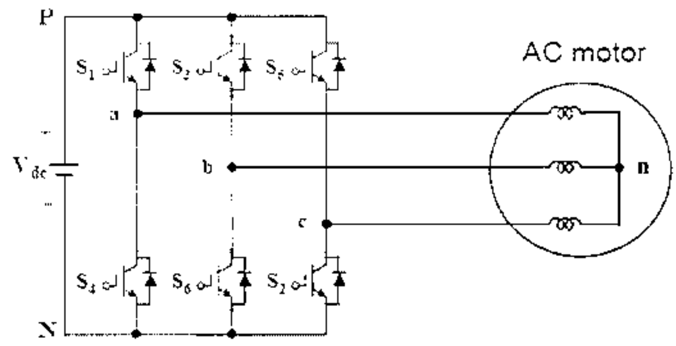

Fig 2.1 Phase Voltage source inverter

2.2.2 Modes of conduction

A three phase output can be obtained from a configuration of six transistors and six diodes as shown in figure 3.4. Two types of control signals can be applied to the transistors.

- 180° conduction
- 120° conduction

180 degree conduction

In this mode each transistor conducts for 180°. Three transistors remain on at any instant of time. When S1 is switched on, terminal *a* is connected to the positive terminal of the dc input voltage. When S4 is switched on, terminal *a* is brought to the negative terminal of the dc source. There are six modes of operation in a cycle with duration of 60° each.

The gating signals are provided such that the switching sequence is S6 S1 S2, S1 S2 S3, S2 S3 S4, S3 S4 S5, S4 S5 S6 and S5 S6 S1 as in figure 3.4. The gating signals are shifted by 60° to obtain three phase balanced voltages as in figure 3.5.

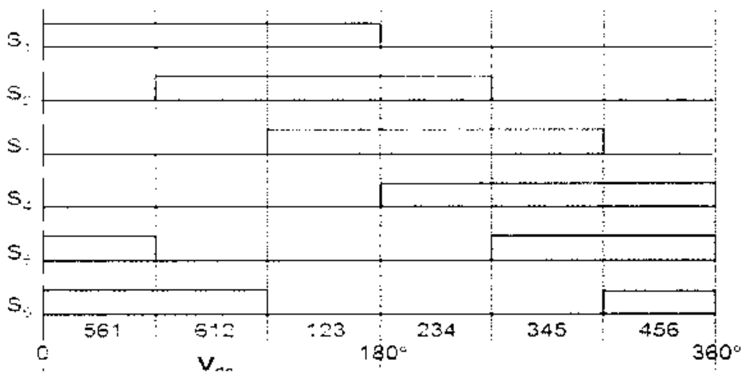

Fig 2.2 Gating signals for 180°conduction

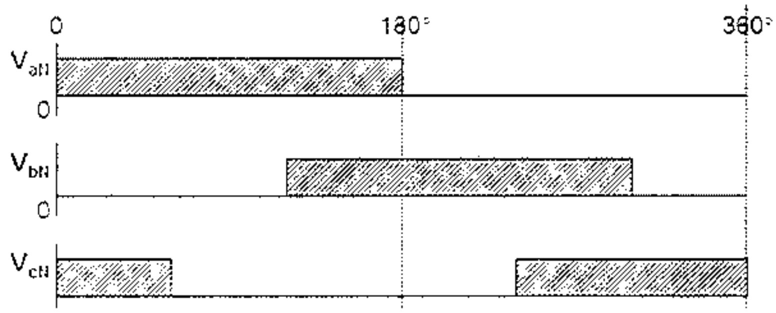

Fig 2.3Voltage waveform for 180°conduction

120 degree conduction

In this mode each transistor conducts for 120 . Three transistors remain on at any instant of time. There are six modes of operation in a cycle with duration of 60° each. The gating signals are provided such that the switching sequence is S6 S1, S1 S2, S2 S3, S3 S4, S4 S5 and S5 S6 as in figure. There is a delay of 30° turning off of S1 and turning on of S4. Thus there is no possibility of short circuit of the dc supply through one upper and one lower transistor.

The voltage waveform is shown in figure.

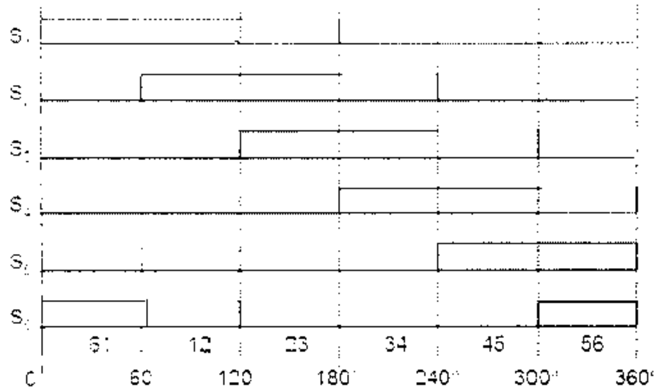

Fig 2.4 Gating signals for 120° conduction

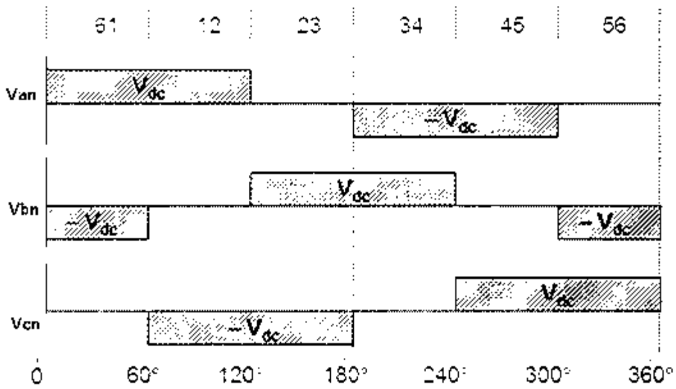

Fig 2.5 Voltage waveform for 120° conduction

2.3 PULSE WIDTH MODULATION

2.3.1 INTRODUCTION

Pulse Width Modulation, abbreviated as PWM, is a modulation technique that generates variable-width pulses to represent the amplitude of an analog input signal. It is a method of transmitting information on a series of pulses. The data that is being transmitted is encoded on the width of these pulses to control the amount of power being sent to a load.

In other words, pulse width modulation is a modulation technique for generating variable width pulses to represent the amplitude of an input analog signal or wave. Using digital pulses we can create some analog value other than just 'high' and 'low' signal levels. Many digital systems are powered by a 5-Volt power supply, so by filtering a signal that has a 50% duty cycle we get an average voltage of 2.5 Volts. Other duty cycles produce any voltage in the range of 0 to 100% of the 'high' voltage, depending upon the PWM resolution. The duty cycle is defined as the percentage of digital 'high' to digital 'low' signals present during a PWM period. The PWM resolution is defined as the maximum number of pulses that can pack into a PWM period. The PWM period is an arbitrarily time period in which PWM takes place. It is chosen to give best results for our particular use. The figure 3.8 shows the PWM pulse generated by comparing the sawtooth carrier and a reference signal.

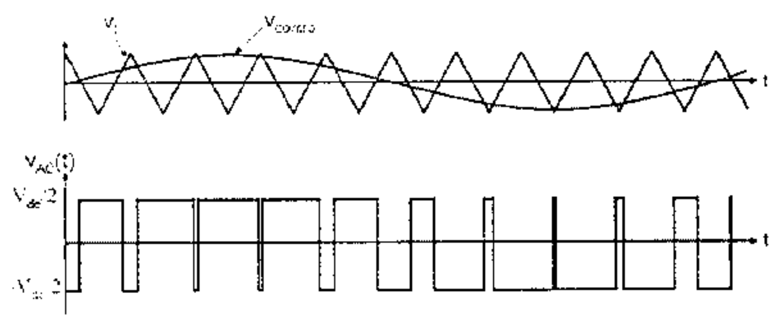

Fig 2.6 Pulse Width Modulation

2.3.2 TYPES OF PULSE WIDTH MODULATION

There are many ways of generating a PWM output such as

- Single pulse width modulation
- Multiple pulse width modulation
- Sinusoidal pulse width modulation
- Space vector pulse width modulation
- Modified pulse width modulation

Multiple PWM

The harmonic content can be reduced by using several pulses in each half-cycle of the output voltage. It is generated by comparing a linear reference signal with a triangular carrier wave. The frequency of reference signal sets the output frequency and the frequency of the carrier determines the number of pulses per half cycle. By varying the on time of the pulses the output voltage can be controlled. This is also known as UNIFORM pulse width modulation.

Sinusoidal PWM

The simplest analog form of generating fixed frequency PWM is by comparison with a linear slope waveform such as a sawtooth. As seen in Fig 3.9 the output signal goes high when the sine wave is higher than the sawtooth. This is implemented using a comparator whose output voltage goes to logic HIGH when the input is greater than the other.

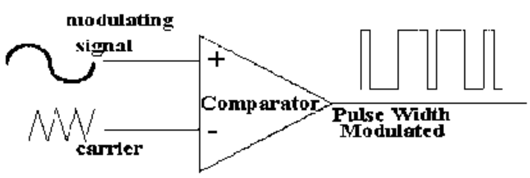

Fig. 2.7 Sine Saw tooth PWM

Space vector PWM

This PWM technique approximates the reference voltage V_{ref} by a combination of the eight switching patterns (V_0 to V_7). The sinusoidal voltage is treated as a constant amplitude vector rotating at constant frequency. The vectors (V_1 to V_6) divide the plane into six sectors (each sector: 60 degrees) as shown in fig 3.10. V_{ref} is generated by two adjacent non-zero vectors and two zero vectors. The switching pattern for a single sector is shown in figure 3.11. S1-S6 are the six power transistors of the inverter. The transistors are switched on and off in the specific pattern to produce the required output.

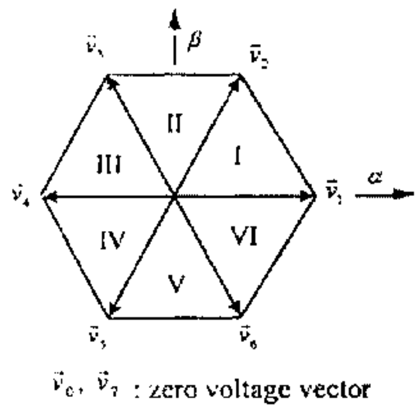

Fig 2.8 Basic switching vector

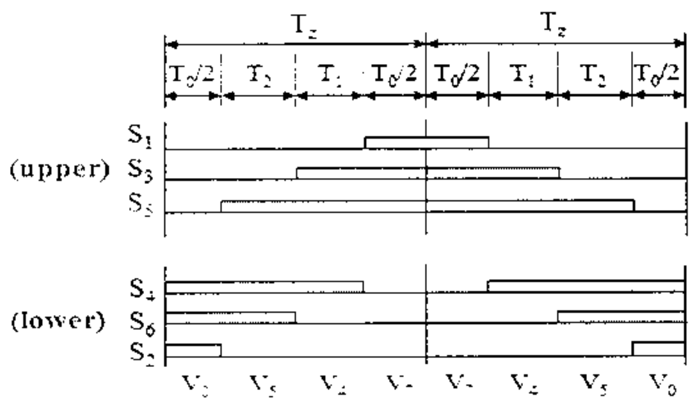

Fig 2.9 Switching pattern for sector-1

2.3.3 APPLICATIONS

The popular applications of pulse width modulation are in power delivery, voltage regulation and amplification and audio effects.

Power delivery

Pulse width modulation is used to reduce the total power delivered to a load without resulting in loss, which normally occurs when a power source is limited by a resistive element. The underlying principle in the whole process is that the average power delivered is directly proportional to the modulation duty cycle. If the modulation rate is high, it is possible to smooth out the pulse train using passive electronic filters and recover an average analog wave form.

Voltage regulation

High frequency pulse width modulation power control systems can be realized using semiconductor switches. Here, the discrete ON or OFF state of the modulation itself can be used to control the switches, thereby controlling the voltage or current across the load. The major advantage with these types of switches is that the voltage drop across it during conducting and non-conducting states is ideally zero. PWM's field of application includes Class D audio amplifiers, DC motor speed control, and light dimmers common in homes. Pulse width modulation is widely used in voltage regulators. It works by switching the voltage to the load with the appropriate duty cycle; the output will maintain a voltage at the desired level.

Audio effects

Pulse width modulation is also exploited in sound synthesis, especially subtractive synthesis, as the process gives a chorus effect or that of slightly detuned oscillators played together. Another application of PWM, as mentioned earlier, is the class D amplifiers, known for better audio clarity alongside its basic function - amplification. The class D amplifier produces a PWM equivalent of the input analog signal, which is in turn fed to the loud speaker after filtering out the carrier wave by sending it through a suitable filter network. Due to the full on/off nature of PWM output, such amplifiers produce less heat than their conventional analog counterparts.

2.3.4ADVANTAGES OF PWM

PWM technique has the following advantages

- Suppresses lower order voltage and current harmonics
- Improved power factor.
- Include a simple drive circuit
- Good start-up characteristics and minimal heat dissipation in the pass transistor
- The signal remains digital all the way from the processor to the controlled system hence no digital-to-analog conversion is needed

2.3.5 PWM CONTROLLER VS. RESISTIVE CONTROLLER

At a 50 percent level, the PWM will use about 50 percent of full power, almost all of which is transferred to the load. A resistive controller at 50 percent load power would consume about 71 percent of full power; 50 percent of the power goes to the load, and the other 21 percent is wasted heating the dropping resistor. It takes a constant trickle of power to operate, so the efficiency improves with higher power loads.

The pulses are at the full supply voltage and will produce more torque in a motor by being able to overcome the internal motor resistances more easily. A resistive speed control will present a reduced voltage to the load, which can cause stalling in motor applications. Finally, in a PWM circuit, common small potentiometers may be used to control a wide variety of loads, whereas large and expensive high power variable resistors are needed for resistive controllers.

Analog control scheme possesses the advantage of fast dynamic response, but suffers the disadvantages of complex circuitry, limited functions, and difficulty in circuit modification. The rapid development in high-performance low-cost microcontroller processors has encouraged research on digital PWM control. This control scheme has the advantages of simple circuitry, software control, and flexibility in adaptation to various applications.

CHAPTER 3

HARDWARE DESCRIPTION

3.1 HARDWARE DESCRIPTION

This chapter describes the hardware model of the developed inverter. Based on the simulation results, a prototype was manufactured and tested to verify the validity of the developed inverter. The figure below shows the complete hardware of the prototype developed.

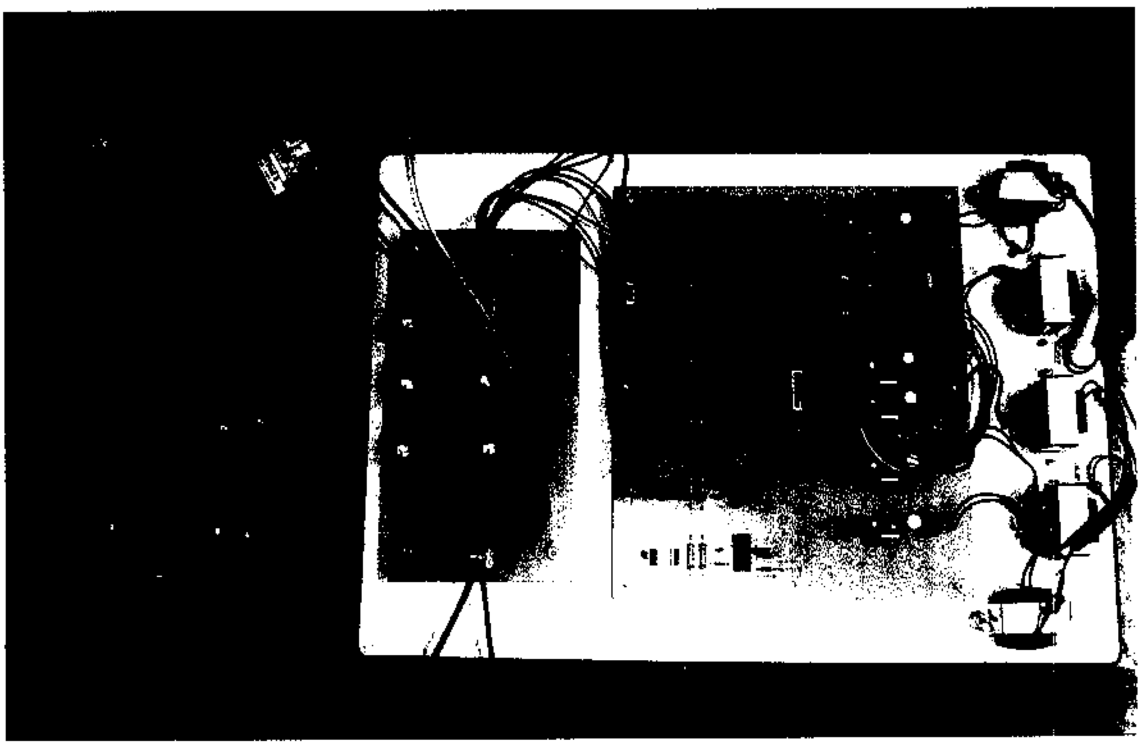

Fig 3.1 Hardware implementation of the circuit

3.2 BLOCK DIAGRAM OF THE DEVELOPED MODEL

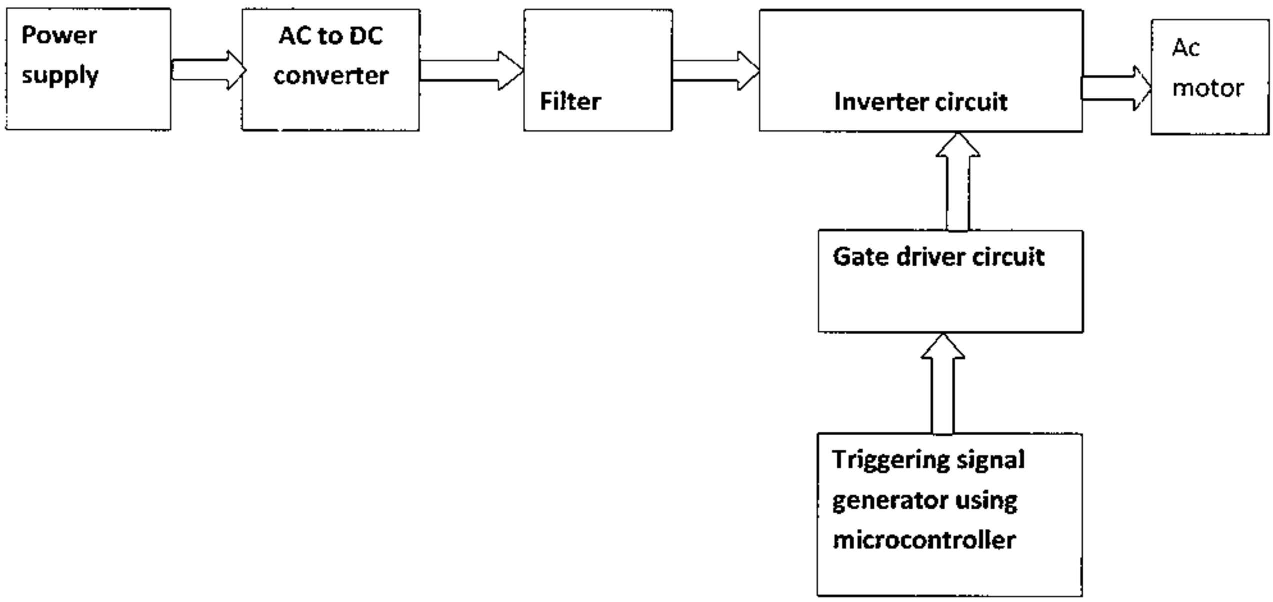

Fig 3.2 Block diagram of the developed prototype.

3.3 DESCRIPTION OF THE BLOCK DIAGRAM

The figure above represents the block diagram of the developed model. The switching signal for the inverter was generated using the microcontroller (mc), Pic 16f877A. First the signal from the mc goes to the optoisolator where electrical isolation takes place, then it is amplified using a buffer CD 4050.This strong signal is given to the MOSFETS and a dc voltage of 12 volts is obtained as an output and this is used to drive the three phase inverter circuit. Similarly there are five more channels and totally six digital pulses are given to the three phase inverter.

3.3.1 Input Source

The electronic circuits work under proper supply voltages. The input source given to the circuit should be of DC voltage. The figure given below represents the input source given to the circuit.

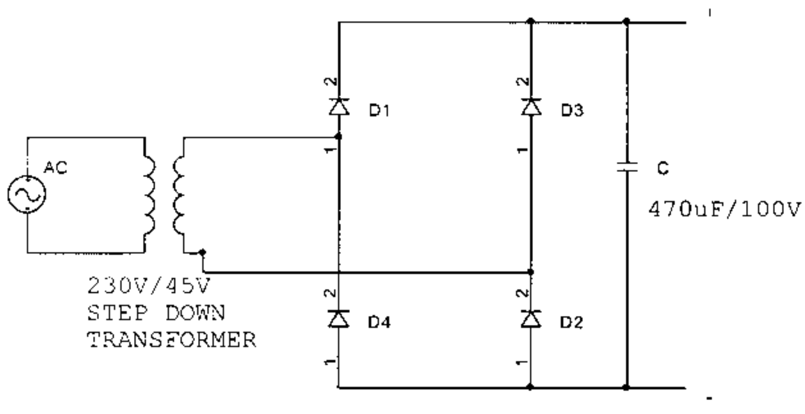

Fig3.3 Representation of Input Source

The transformer is used to step down the voltage. The transformer used is of 230V/45V step down transformer. The bridge circuit which consists of four diodes is available as a module. The module number used here is 68424 International Rectifier (IR).This module is used for rectification purpose. The voltage and the current rating is 600V and 20A respectively. The capacitor is used to filtering the unwanted signals. Thus a dc output voltage is obtained. The output voltage obtained is given to the inverter circuit.

3.3.2 Power Supply circuit for triggering circuit

All electronic circuits works only in low DC voltage, so a proper power an appropriate voltage supply is provided for their proper functioning. Therefore, the power supply circuit for triggering circuit unit consists of transformer, rectifier, filter & regulator. AC voltage of typically 230v is connected to a transformer voltage down to the level to desired ac voltage. A diode rectifier that provides the full wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage is provided. This resulting dc voltage usually has some ripple or ac voltage variation . A regulator circuit can use this dc input to provide dc voltage that not only has much less ripple voltage but also remains the same dc value even when the dc voltage varies some what, or the load connected to the output dc voltages changes. As per our project there are two power supply circuits. Now for microcontroller a regulator of IC LM 7805 is used .Here the output voltage is regulated to be 5v so that it is given as supply to the PIC microcontroller.

In addition to this four other supplies are given. Here 12v is given as supply by using IC LM 7812 regulator which will be discussed later in this report. The general block diagram and the circuit designed for 12v power supply is shown below.

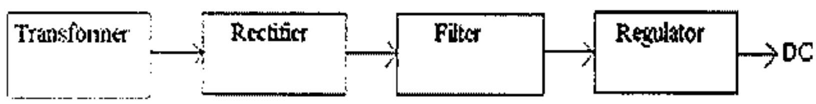

Fig3.4(a) Block diagram of Power Supply circuit .

POWER SUPPLY CIRCUIT :

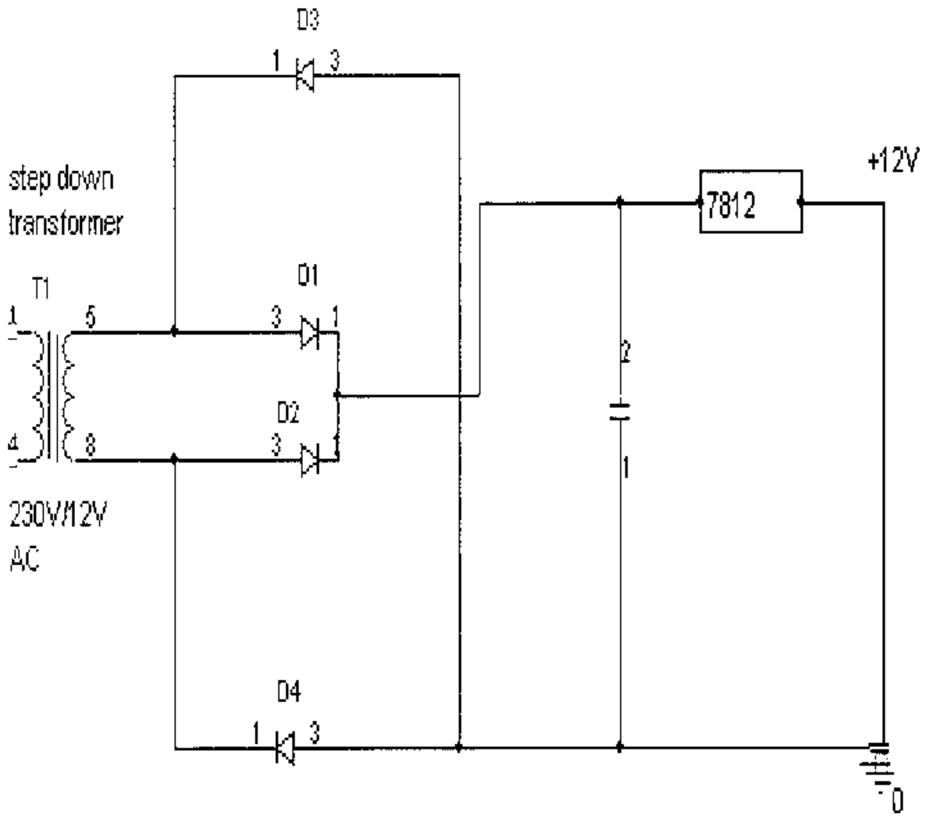

Fig3.4 (b) power supply Circuit .

Transformer

A transformer is a static piece of apparatus in which electric power in one circuit is transformed into electric power of same frequency in another circuit. It can raise or lower the voltage in the circuit, but with a corresponding decrease or increase in current. It works with the principle of mutual induction. Hence a step down transformer is used to provide the necessary supply for the electronic circuits. Here a step down transformer of 230v/12v is used to step down the voltage. Hence, a 230v ac is stepped down to 12v ac voltage.

Rectifier

A dc voltage level obtained from a sinusoidal input can be improved fully using a process called full wave rectification. Therefore the full wave rectification is obtained using Full-wave bridge rectifier. From the basic bridge configuration as shown in fig 6.3(b), it can be observed that during the positive half-cycle of the input voltage, the power is supplied to the load through diodes D1 and D2.During the negative cycle, diodes D3 and D4 conducts. In the bridge rectifier the diodes may be of variable types like 1N4001, 1N4003, 1N4004, 1N4005, 1N4007 etc… can be used. Here the diode used is 1N4007, because it can withstand voltages upto 1000V.

Filters

In order to obtain a dc voltage of 0 Hz, a low pass filter is used. So that a capacitive filter circuit is used where a capacitor is connected at the rectifier output and a dc voltage is obtained across it. The filtered waveform is essentially a dc voltage with negligible ripples and it is ultimately fed to the load.

Regulators

The output voltage from the capacitor is more filtered and finally regulated. The voltage regulator is a device, which maintains the output voltage constant irrespective of the change in supply variations, load variations and temperature changes. In our project we make use of two voltage regulators.Here a fixed voltage regulator namely LM7805 and LM7812 are used. The IC LM7805 is a +5v regulator

which is used for microcontroller and IC LM7812 is used for the mosfets at the driver side.

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point these regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Al-though

designed primarily as fixed voltage regulators devices can be used with external components to obtain adjustable voltages and currents. The LM78XX series is available in an aluminum TO-3 pack-age which will allow over 1.0A load current if adequate heat sinking is provided.

Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissi-pation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating. Considerable effort was expanded to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input by-passing is needed only if the regulator is located far from the filter capacitor of the power supply. For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

Output current in excess of 1A is obtained and it also provides Internal thermal overload protection. No external components are required.Available in the aluminum TO-3 package.

Circuit diagram of LM78XX

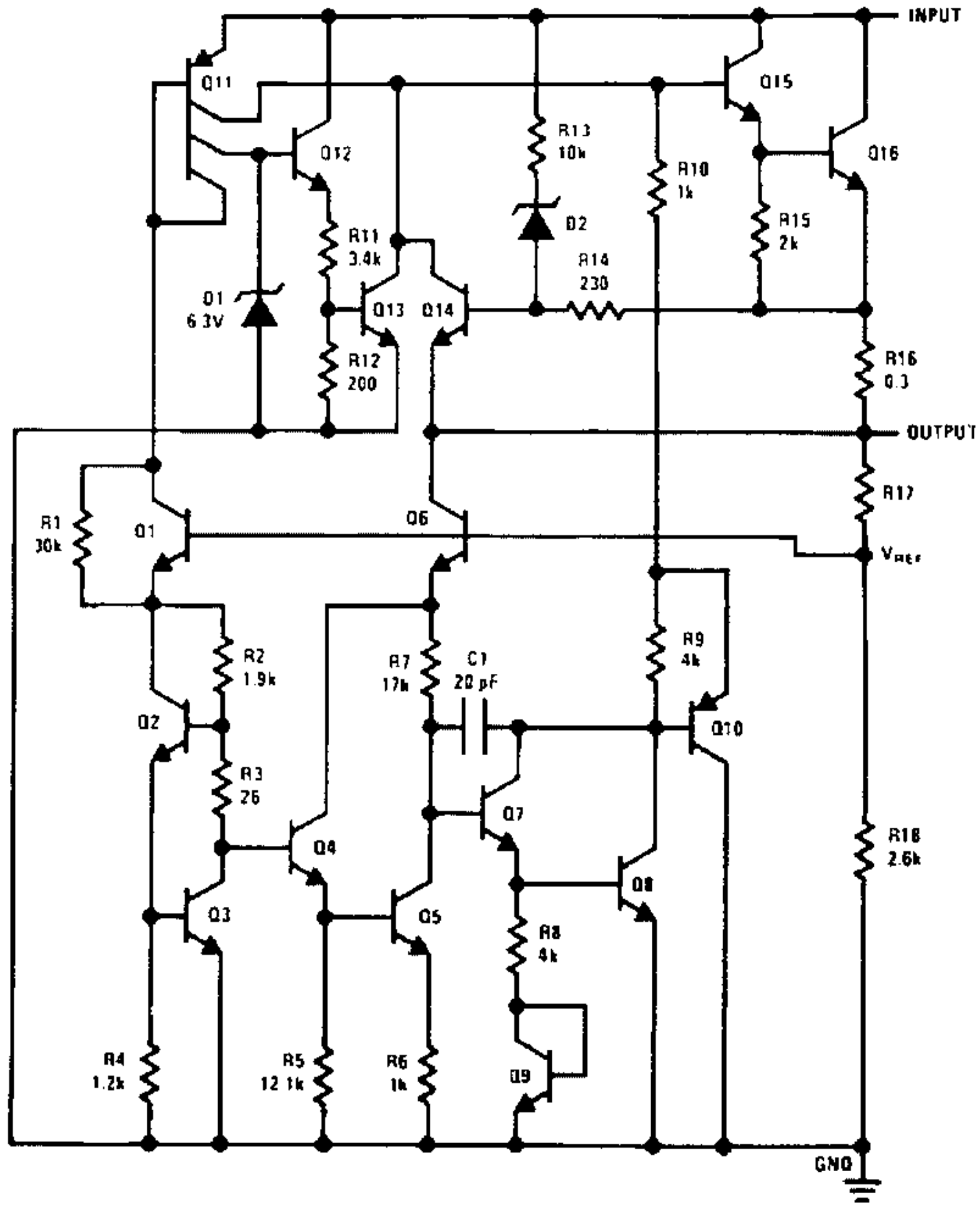

Fig3.5 Circuit diagram of LM78XX

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3.3.3 Optocoupler

Optocoupler is also termed as optoisolator. They are essentially a combination of two distinct devices: an optical transmitter, typically a gallium arsenide LED (light-emitting diode) and an optical receiver such as a phototransistor or light-triggered diac or a resistor that changes resistance with variations in light intensity or other device that conducts differently in the presence of light. These devices are used to isolate the control voltage from the controlled circuit. Optocouplers typically come in a small 6-pin or 8-pin IC package.. The two are separated by a transparent barrier which blocks any electrical current flow between the two, but does allow the passage of light. The basic idea is shown in Fig.6.5, along with the usual circuit symbol for an optocoupler.

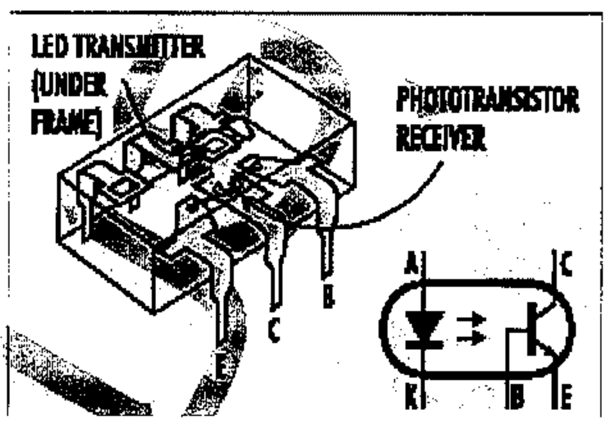


Fig 3.6 Construction of a typical optocoupler and the circuit symbol

Usually the electrical connections to the LED section are brought out to the pins on one side of the package and those for the phototransistor or diac to the other side, to physically separate them as much as possible. This usually allows optocouplers to withstand voltages of anywhere between 500V and 7500V between input and output. Optocouplers are essentially digital or switching devices, so they are best for transferring either on-off control signals or digital data. Analog signals can be transferred by means of frequency or pulse-width modulation. Thus the triggering pulses are given to the inverter circuit.

The optocoupler used in our circuit is SFH615.This features a high current transfer ratio, low coupling capacitance and high isolation test voltage. They employ a GaAs led as emitter which is optically coupled with a silicon planar photo transistor as detector. The components are incorporated in a plastic plug-in DIP-4 package. The coupling devices are designed for signal transmission between two electrically isolated circuits. The potential difference between the circuits to be coupled is not allowed to exceed the maximum permissible reference voltages. The couplers are end stackable in a 2.54 mm and are considered as successor types for the couplers in metal case. Multi couplers can thus easily be implemented and conventional multicouplers can be easily replaced.

FEATURES:

- Isolation test voltage is 2800 volts.
- High current transfer ratio

  At 10 mA : 40-320 %

  At 1 mA : 60 %.
- Fast switching times
- Stable temperature
- Low saturation voltage
- High collector emitter voltage of 70v

3.3.4 Driver Circuit:

The driver circuit forms the most important part of the hardware unit because it acts as the backbone of the inverter. It gives the triggering pulses to the switches in the proper sequence. The signal after being electrically isolated is given to the driver circuit. The diagram given below represents the driver unit.

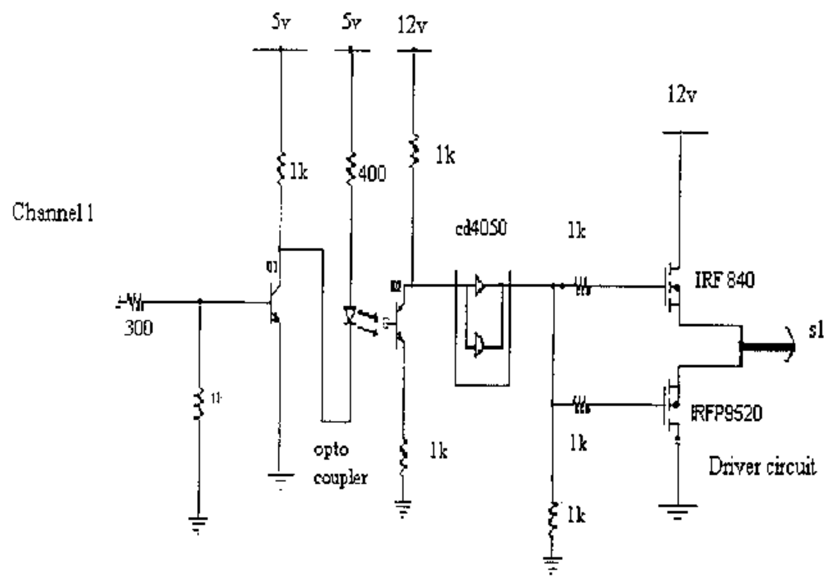


Fig 3.7 Driver circuit.

(Driver circuit for a single channel)

Schematic Diagram of CD4050B:

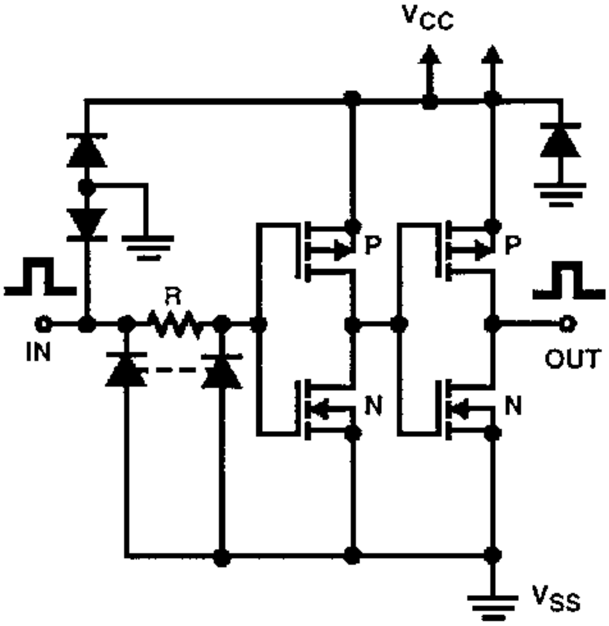


Fig 3.9 Schematic Diagram of CD4050B

CD4050B device is an inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (VCC). The input-signal high level (VIH) can exceed the VCC supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL / TTL converters and can drive directly two DTL/TTL loads. (V CC = 5V, V OL _ 0.4V, and I OL _ 3.3mA.).The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because CD4050B requires only one power supply, they are preferred over the CD4010B and should be used in place of CD4010B in all inverters, current drivers, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation.

MOSFETs

The signal from the buffer amplifier is given to the MOSFET circuit. On top is the N channel IRF 840 and P channel IRFP 9520. When the input is 0v , P channel mosfet conducts which is connected to ground. So there is no output. When the input is 1v, then the N channel mosfet conducts and gives an output voltage of 12 v, which in turn is used to drive the inverter. The output obtained by this manner is sharp.

IRF 840

Symbol of IRF 840.

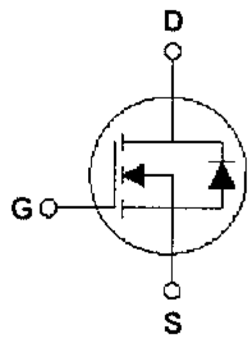


Fig 3.10 Symbol of IRF 840

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, CMOS technology.This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies,power factor correction and electronic lamp ballasts based on half bridge.

Features:

• 8.0A, 500V, rds(on) = 0.8;VGS = 10 V.

• Fast switching.

• 100% avalanche tested.

• Improved dv/dt capability.

IRF9520

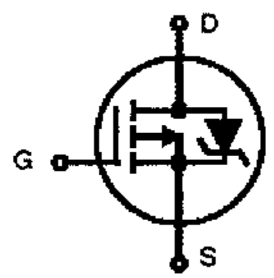


Fig 3.11 Symbol of IRF9520

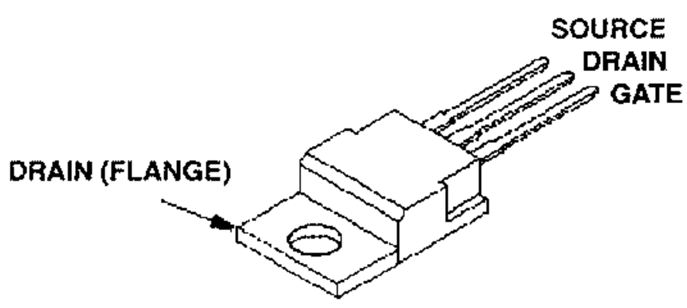


Fig 3.12 IRF9520 packaging.

This advanced power MOSFET is designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are

P-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Features:

- rds(ON) = 0.600 ohm.
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

3.3.5 Inverter Unit

The inverter circuit involves s.x switches. It consists of single DC source. The figure given below represents the inverter circuit. The switches used for the inverter circuit is MOSFET. The number involves IRF P460. There are totally six switches namely s1,s3,s5 on top and s4, s2, s6 at the bottom. A snubber circuit is being provided along with the MOSFETs. The snubber circuit consists of a resistor and a capacitor. The resistor is rated at 100 ohms and the capacitor is rated at 0.1 micro farad. The values of capacitor and resistor are same for all the snubber circuits in the inverter circuit.

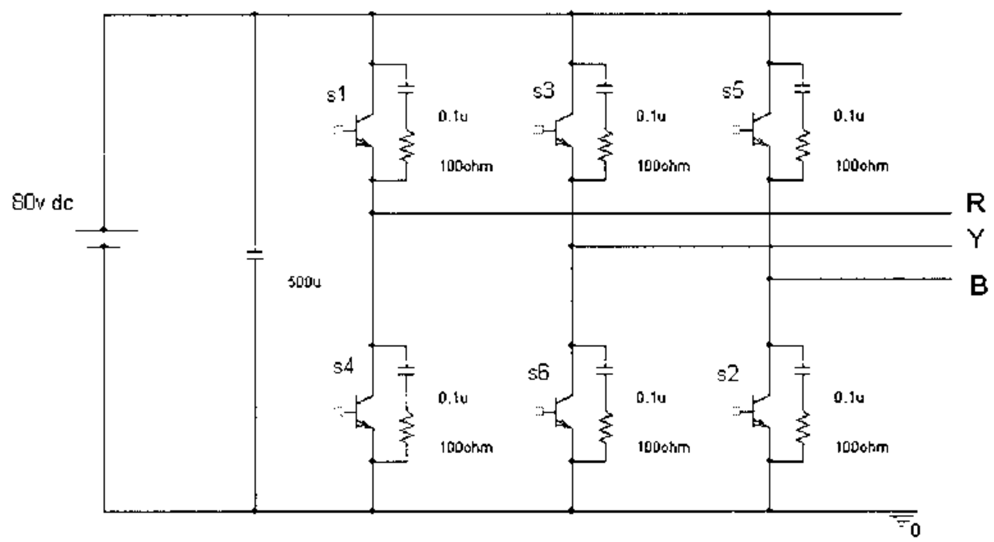


Fig. 3.13 Inverter Circuit

MOSFET

The component that is used as the switch in the inverter unit is the MOSFET which is a voltage controlled device. They are the power semi conductor devices that have a fast switching property with a simple drive requirement.

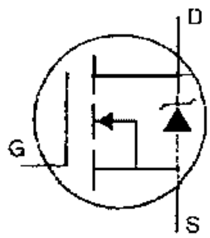


Fig 3.14 (a) MOSFET Switch   Fig 3.14 (b) MOSFET Symbol

V_{dss}= 500 V

Rds (on) = 0.27 ohm

Id= 20 A

This MOSFET provides the designer with the best combination of fast switching, rugged device design, low on-resistance and cost-effectiveness. This package is preferred for commercial and industrial applications where higher power levels are to be handled.

Construction and Operation principle of MOSFET

There are two basic ypes of MOSFETs. They are N Channel depletion type and N Channel enhancement type.

A. N Channel depletion type ***B. N Channel enhancement type***

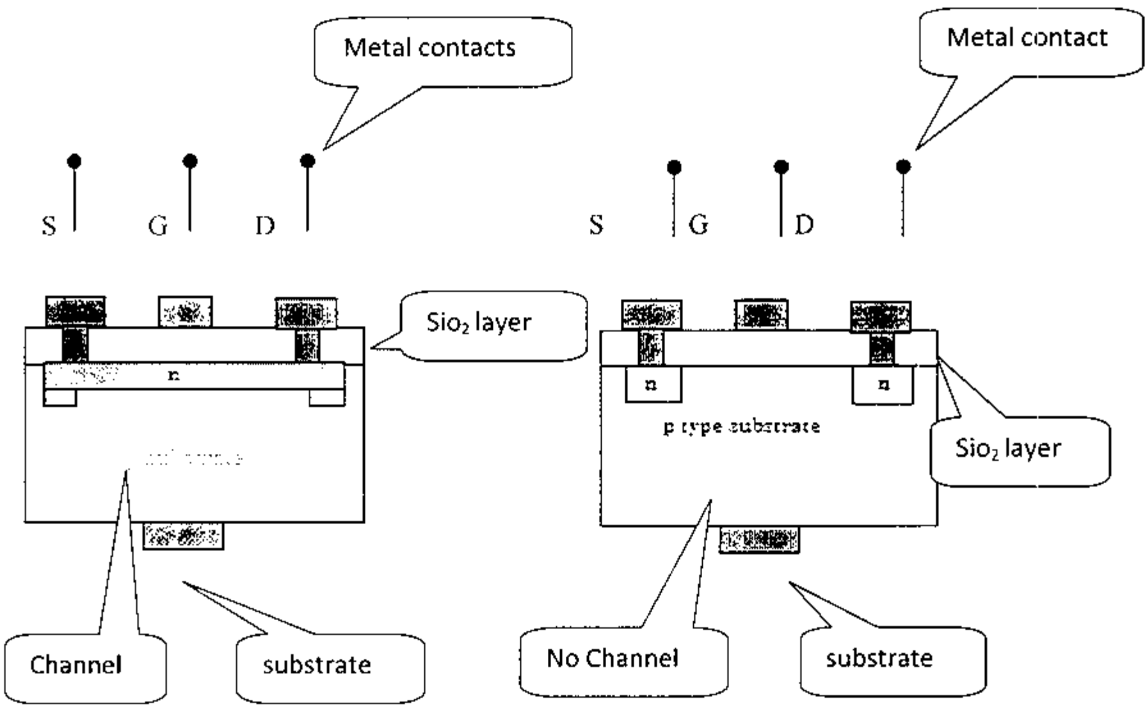


Fig 3.15 A, B MOSFET Types

A.N Channel depletion

The N channel depletion type of MOSFET is constructed with p -Substrate. It has two n doped regions, which forms the drain and source. It has SiO_2 insulating layer between the channel and the metal layer. Thus it has three terminals namely drain source and gate.

With a negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, leaving positive ions in their place. Thereby, the N-channel is depleted of some of its electrons, thus by decreasing the channel conductivity.

When a positive voltage is applied between the gate and source, more electrons are induced in the channel by capacitor action. So there is a flow of current from drain to source. As the gate source voltage increases, the channel gets wider by accumulation of more negative charges and resistance to the channel decreases. Thus more current from flows from drain to source. As there is a current flow through device for zero gate source voltage, it is normally called as ON MOSFET.

B.N Channel Enhancement.

The N channel enhancement MOSFET is similar to the depletion type in the construction except that there is no physical existence of the channel when it is unbiased.

When the positive voltage is applied between the gate and the source, the electrons get accumulated in the channel by capacitive induction in the channel formed out of electrons allowing the flow of current. This channel gets widened as more positive voltage is applied between gate and source. There will not be any condition through the device if the gate source voltage is negative.

As the enhancement type MOSFET conduct only after applying positive gate voltage, it is also called as normally OFF MOSFET. For this reason it becomes easily controllable and is used in power electronics as a switch.

3.3.6 Three- phase Induction Motor

Three-phase AC induction motors are widely used in industrial and commercial applications. These motors are self-starting and use no capacitor, start winding, centrifugal switch or other starting device. They produce medium to high degrees of starting torque.

The power capabilities and efficiency in these motors range from medium to high compared to their single-phase counterparts. Popular applications include grinders, lathes, drill presses, pumps, compressors, conveyors, also printing equipment, farm equipment, electronic cooling and other mechanical duty applications.

They are classified as

- Squirrel cage
- Wound-rotor motors.

Squirrel Cage Motor

A typical squirrel cage rotor construction is shown on the figure 3.4. The cage is constructed from rotor bars (generally copper), typically insulated from and embedded in the rotor body. The bars are then shorted together with end rings at either end. There are no slip rings nor any DC excitation supplied to the rotor. It is a cylindrical not salient.

Almost 90% of the three-phase AC Induction motors are of this type. Here, the rotor is of the squirrel cage type and it works as explained earlier. The power ratings range from one-third to several hundred horse power in the three-phase motors. Motors of this type rated one horsepower or larger, cost less and can start heavier loads than their single-phase counterparts.

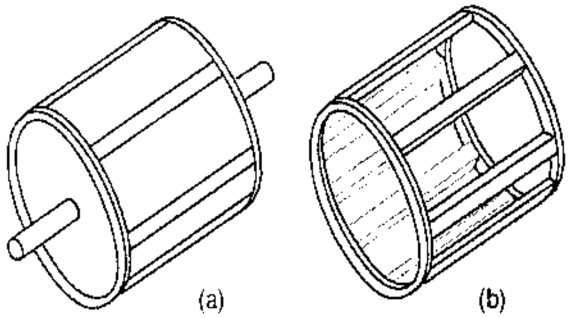


Fig 3.16a) Embedded Squirrel Cage rotor

(b) Conductive Cage removed from rotor

Wound-Rotor Motor

The slip-ring motor or wound-rotor motor is a variation of the squirrel cage induction motor. While the stator is the same as that of the squirrel cage motor, it has a set of windings on the rotor which are not short-circuited, but are terminated to a set of slip rings. These are helpful in adding external resistors and contactors as shown in figure 3.5. The slip necessary to generate the maximum torque (pull-out torque) is directly proportional to the rotor resistance. In the slip-ring motor, the effective rotor resistance is increased by adding external resistance through the slip rings. Thus, it is possible to get higher slip and hence, the pull-out torque at a lower speed. A particularly high resistance can result in the pull-out torque occurring at almost zero speed, providing a very high pull-out torque at a low starting current. As the motor accelerates, the value of the resistance can be reduced, altering the motor characteristic to suit the load requirement. Once the motor reaches the base speed, external resistors are removed from the rotor. This means that now the motor is working as the standard induction motor. This motor type is ideal for very high inertia loads, where it is required to generate the pull-out torque at almost zero speed and accelerate to full speed in the minimum time with minimum current draw.

Here the motor used in our project is 3 phase ac induction motor with an average speed of 1330rpm

PIC 16F877 MICROCONTROLLER

3.4.1 MICROCONTROLLER CORE FEATURES:

High-Performance RISC CPU:

- Only 35 single-word instructions to learn
- All single-cycle instructions except for programbranches, which are two-cycle
- Operating speed: DC – 20 MHz clock input DC – 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory,
  Up to 368 x 8 bytes of Data Memory (RAM),
  Up to 256 x 8 bytes of EEPROM Data Memory
- Pin out compatible to other 28-pin or 40/44-pin
  PIC16CXXX and PIC16FXXX microcontrollers

Analog Features:

- 10-bit, up to 8-channel Analog-to-Digital Converter (A/D)
- Brown-out Reset (BOR)
- Analog Comparator module with:
  - Two analog comparators
  - Programmable on-chip voltage reference (VREF) module
  - Programmable input multiplexing from device inputs and internal voltage reference
  - Comparator outputs are externally accessible

Special Microcontroller Features:

- 100,000 erase/write cycle Enhanced Flash Program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory typical
- Data EEPROM Retention > 40 years
- Self-reprogrammable under software control
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Single-supply 5V In-Circuit Serial Programming
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving Sleep mode
- Selectable oscillator options
- In-Circuit Debug (ICD) via two pin
- Low-power, high-speed Flash/EEPROM technology
- Fully static design
- Wide operating voltage range (2.0V to 5.5V)
- Commercial and Industrial temperature ranges
- Low-power consumption
- Programmable code protection
- Power saving Sleep mode

3.4.2 PIN DIAGRAM:

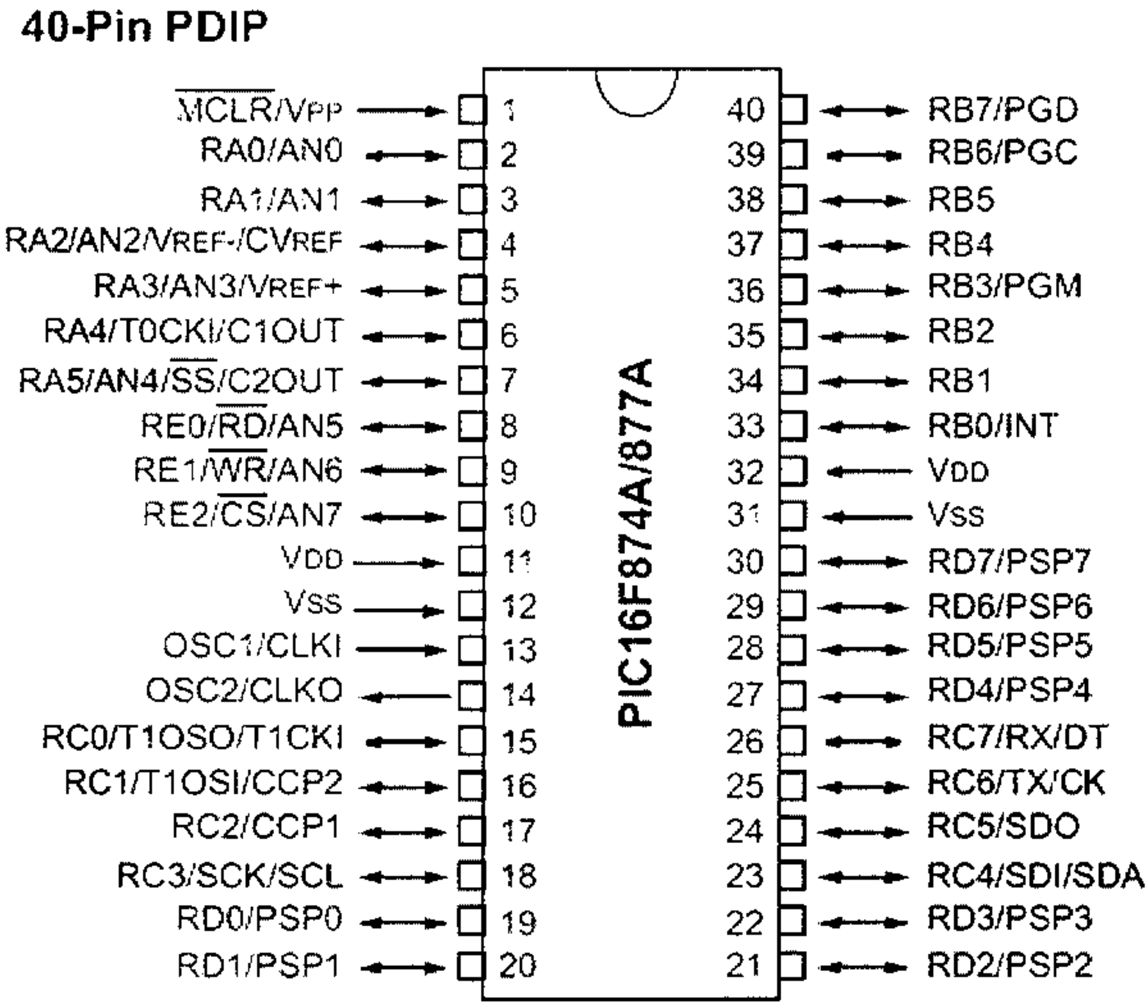


Fig 3.17 Pin diagram of PIC 16F877A

Peripheral Features:

• Timer0: 8-bit timer/counter with 8-bit prescaler

• Timer1: 16-bit timer/counter with prescaler,

can be incremented during Sleep via external crystal/clock

• Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler

• Two Capture, Compare, PWM modules

- Capture is 16-bit, max. resolution is 12.5 ns

- Compare is 16-bit, max. resolution is 200 ns

- PWM max. resolution is 10-bit

• Synchronous Serial Port (SSP) with SPI™

• Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)

with 9-bit address detection

• Parallel Slave Port (PSP) – 8 bits wide with external RD, WR and CS controls

• Brown-out detection circuitry for Brown-out Reset (BOR)

• The PIC16F873A and PIC16F874A have one-half of the total on-chip memory of the PIC16F876A and PIC16F877A

• The 28-pin devices have three I/O ports, while the 40/44-pin devices have five

• The 28-pin devices have fourteen interrupts, while the 40/44-pin devices have fifteen

• The 28-pin devices have five A/D input channels, while the 40/44-pin devices have eight

• The Parallel Slave Port is implemented only on 40/44 pin devises.

3.4.3 MEMORY ORGANIZATION

There are three memory blocks in each of the PIC16F87XA devices. The program memory and datamemory have separate buses so that concurrent access can occur and they are as follows.

Program Memory Organization

The PIC16F87XA devices have a 13-bit program counter capable of addressing an 8K word x 14 bit program memory space. The PIC16F876A/877A devices have 8K words x 14 bits of Flash program memory, while PIC16F873A/874A devices have 4K words x 14 bits. Accessing a location above the physically implemented address will cause a wraparound.

Data Memory Organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 (Status<6>) and RP0 (Status<5>) are the bank select bits.

Table 3.1 Data Memory Organization

RP1 : RP0	BANK
00	0
01	1
10	2
11	3

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank may be mirrored in another bank for code reduction and quicker access.

3.4.4 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly, through the File Select Register (FSR).

I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

PORTA and the TRISA Register

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin). The TRISA register controls the direction of the port pins even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

PORTB and the TRISB Register

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin). Three pins of PORTB are multiplexed with the In-Circuit Debugger and Low-Voltage Programming function: RB3/PGM, RB6/PGC and RB7/PGD. The alternate functions of these pins are described in **"Special Features of the CPU"**.

PORTC and the TRISC Register

PORTC is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISC. Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin). PORTC is multiplexed with several peripheral functions (Table 4-5). PORTC pins have Schmitt Trigger input buffers. When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin.

PORTD and TRISD Registers

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output. PORTD can be configured as an 8-bit wide microprocessor port (Parallel Slave Port) by setting control bit, PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

PORTE and TRISE Register

PORTE has three pins (RE0/RD/AN5, RE1/WR/AN6 and RE2/CS/AN7) which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers. The PORTE pins become the I/O control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make certain that the TRISE<2:0> bits are set and that the pins are configured as digital inputs. Also, ensure that ADCON1 is configured for digital I/O. In this mode, the input buffers are TTL.

3.4.5 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has five inputs for the 28-pin devices and eight for the 40/44-pin devices. The conversion of an analog input signal results in a corresponding 10-bit digital number. The A/D module has high and low-voltage reference input that is software selectable to some combination of VDD, VSS, RA2 or RA3. The A/D converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D clock must be derived from the A/D's internal RC oscillator.

The A/D module has four registers. These registers are:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

The ADCON0 register, shown in Register 11-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 11-2, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be the voltage reference) or as digital I/O.

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 11-2. The source impedance (RS) and the internal sampling switch impedance (RSS) directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD);

see Figure 11-2. **The maximum recommended impedance for analog sources is 2.5 kO.** As the impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

The ADRESH:ADRESL registers contain the 10-bit result of the A/D conversion. When the A/D conversion is complete, the result is loaded into this A/D Result register pair, the GO/DONE bit (ADCON0<2>) is cleared and the A/D interrupt flag bit ADIF is set. The block diagram of the A/D module is shown in Figure 11-1. After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs.

To calculate the minimum acquisition time, Equation 11-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution

1: The reference voltage (VREF) has no effect on the equation since it cancels itself out.
2: The charge holding capacitor (CHOLD) is not discharged after each conversion.
3: The maximum recommended impedance for analog sources is 2.5 kO. This is required to meet the pin
leakage specification

ADCON0 REGISTER (address: 1Fh):

Table 3.2 ADCON0 REGISTER (address: 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0:** Analog Channel Select bits

000 = Channel 0 (AN0)
001 = Channel 1 (AN1)
010 = Channel 2 (AN2)
011 = Channel 3 (AN3)
100 = Channel 4 (AN4)
101 = Channel 5 (AN5)
110 = Channel 6 (AN6)
111 = Channel 7 (AN7)

Note: The PIC16F873A/876A devices only implement A/D channels 0 through 4; the unimplemented selections are reserved. Do not select any unimplemented channels with these devices.

bit 2 **GO/$\overline{DONE}$:** A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)

0 = A/D conversion not in progress

bit 1 **Unimplemented:** Read as '0'

bit 0 **ADON:** A/D On bit

1 = A/D converter module is powered up

0 = A/D converter module is shut-off and consumes no operating current

The ADRESH:ADRESL registers contain the 10-bit result of the A/D conversion. When the A/D conversion is complete, the result is loaded into this A/D Result register pair, the GO/DONE bit (ADCON0<2>) is cleared and the A/D interrupt flag bit ADIF is set. The block diagram of the A/D module is shown in Figure 11-1. After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs.

To determine sample time **"A/D Acquisition Requirements" is used.** After this acquisition time has elapsed, the A/D conversion can be started. To do an A/D Conversion, follow these steps:

1. Configure the A/D module:
    - Configure analog pins/voltage reference and digital I/O (ADCON1)
    - Select A/D input channel (ADCON0)
    - Select A/D conversion clock (ADCON0)
    - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
    - Clear ADIF bit
    - Set ADIE bit
    - Set PEIE bit
    - Set GIE bit
3. Wait the required acquisition time.
4. Start conversion:
    - Set GO/DONE bit (ADCON0)
5. Wait for A/D conversion to complete by either:
    - Polling for the GO/DONE bit to be cleared (interrupts disabled); OR
    - Waiting for the A/D interrupt
6. Read A/D Result register pair (ADRESH:ADRESL), clear bit ADIF if required.
7. For the next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as TAD.A minimum wait of 2TAD is required before next acquisition starts.

CHAPTER 4

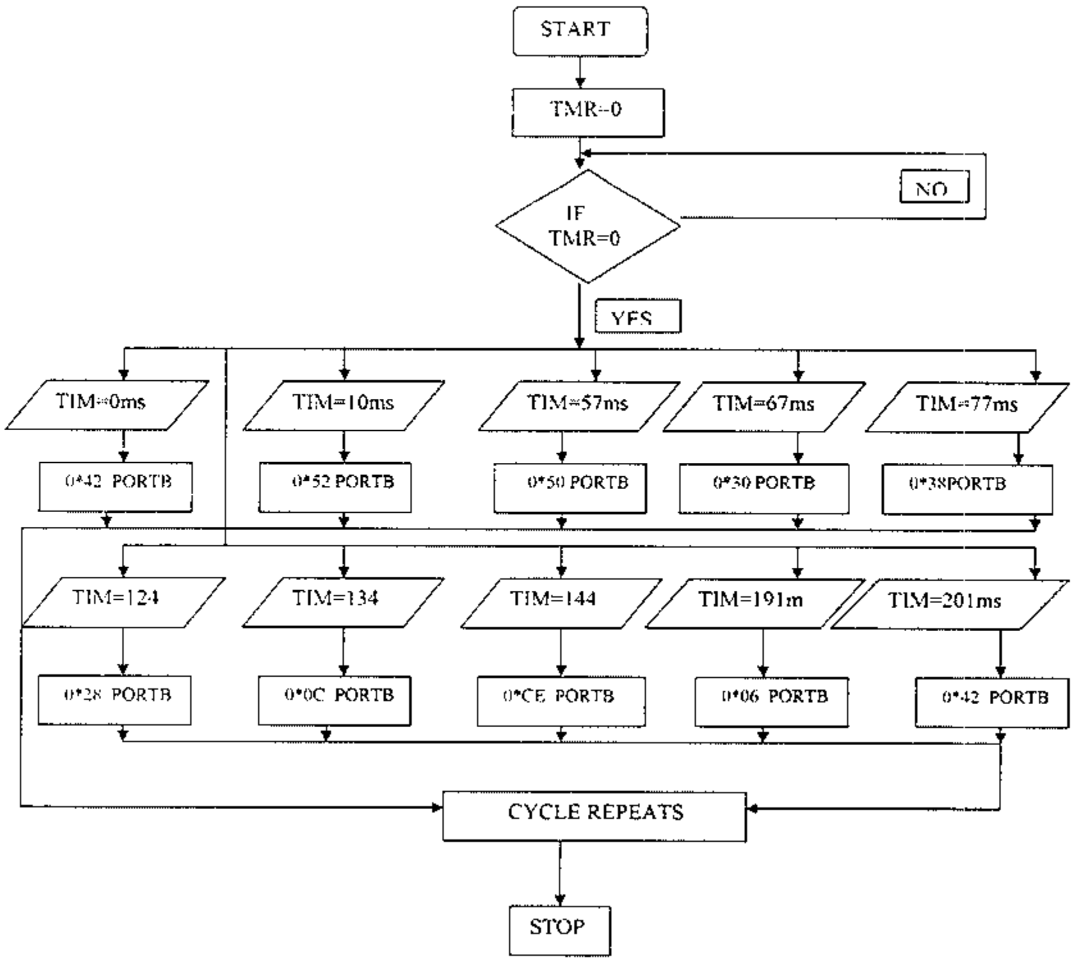
SOFTWARE DETAILS

4.1 FLOWCHART DESCRIPTION:

A simple flow chart is used to explain the program to generate the pwm pulses. The flowchart is explained in simple steps as follows.

- The timer is initially made zero.
- The timing pulse values are randomly generated to be given to the three phase inverter.
- The randomly generated values are 0ms,10ms,57ms,67ms,77ms,124ms.134ms,144ms,191ms,201ms as specified in the switching sequence table.
- The outputs are obtained at port B sequentially for the timings mentioned above.
- They output values are 0*42, 0*52, 0*50, 0*30, 0*38, 0*28, 0*0C, 0*CE, 0*06, 0*42 respectively.
- These values are obtained from the switching sequence tables.
- The cycle repeats again till the power supply is on.

4.2 FLOWCHART:



TMR=TIMER
TIM=SWITHING TIMINGS GENERATED IN PIC16F877A

Fig 4.1 Flowchart to generate pwm pulses

The simulation is done on the MPLAB software. The step by step procedure is given below.

- MPLAB IDE is selected for programming.
- PIC16F877A device is selected.
- HITECH CCS C COMPILER SUITE for PIC controller is selected for compilation of the program.
- Creation of the new project directory is made.
- Program is written using the header file "include<16f877.h> and saved in the **.C** format.
- The file is added to the project directory for compilation and simulation.
- Now the compilation is done.
- A new output window opens which contains the information **"BUILD SUCCESSFUL"** if the program doesn't have any errors.
- After converting it into HEX file format, the program is ready to be simulated.
- Now select the LOGIC ANALYZER window for analysis of the code.
- Select the ports RB1,RB2,RB3,RB4,RB5,RB6 of PIC16F877A as the output ports.
- The crystal oscillator frequency of 4MHZ is selected.
- CCP1 port is also selected if the pulses of 4MHZ crystal oscillator have to be displayed.
- Finally the simulation is done in the logic analyzer and the switching sequence pulses are obtained for the ports mentioned above.

The output generated by running this program in MPLAB software is given below

4.3 OUTPUT FOR 50 HZ

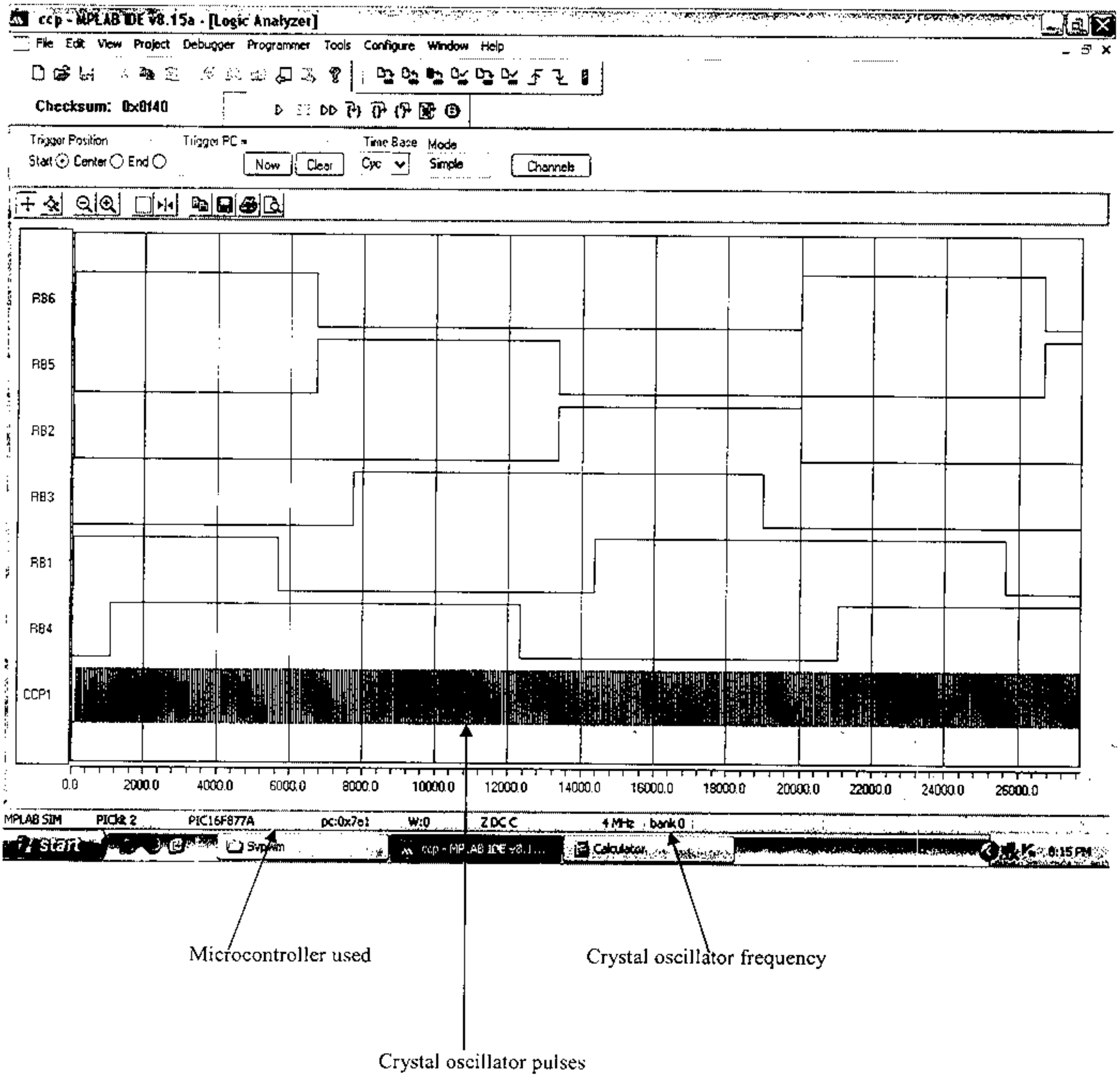


Fig 4.2 output for 50 hz

4.4 OUTPUT FOR 25 HZ

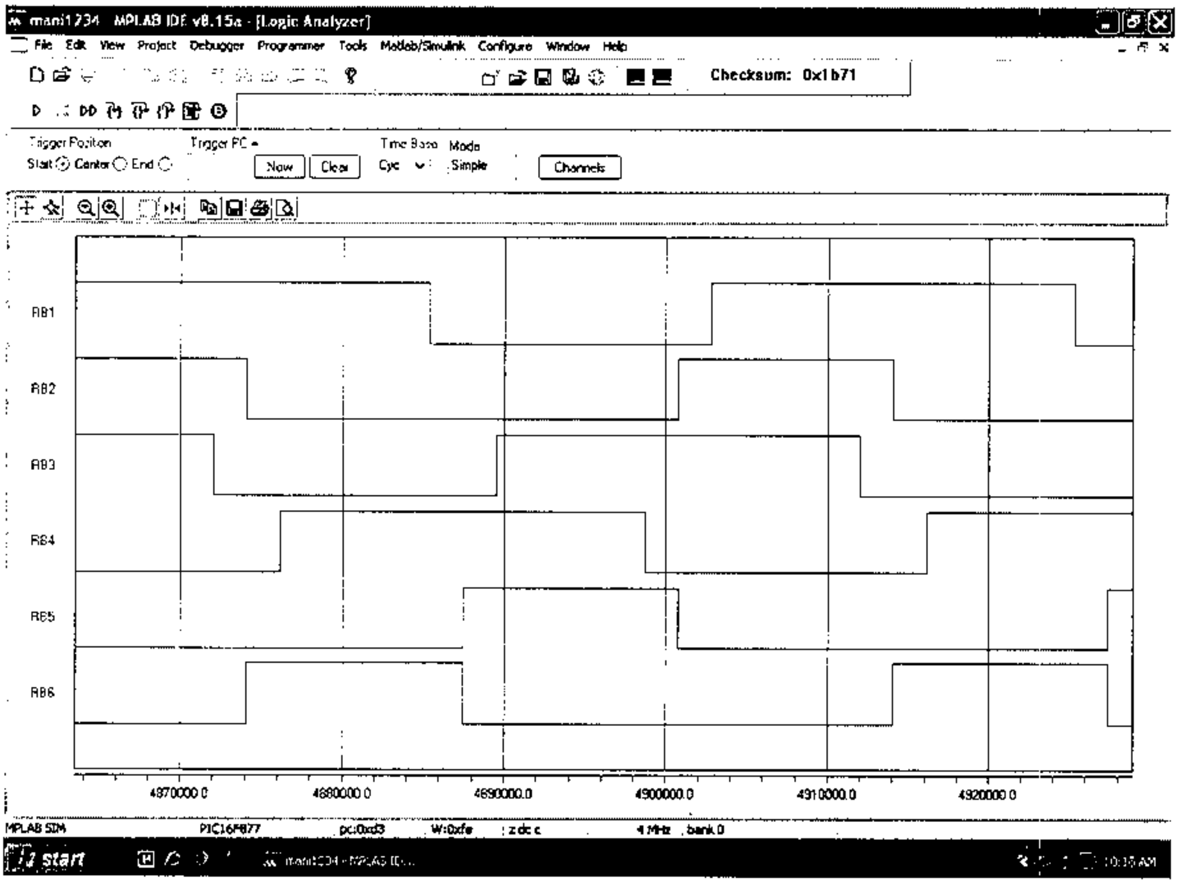


Fig 4.3 output for 25 hz

The figures above show the switching pulses of the inverter. These pulses are generated from the microcontroller. This is the simulation output screen of microcontroller using MPLAB software.

CHAPTER 5

TEST RESULTS

5.1 TEST RESULT

5.2 OUTPUT FOR 50HZ:

IN MOTOR:

Frequency : 50Hz

Motor speed : 1205rpm

IN SCOPE :

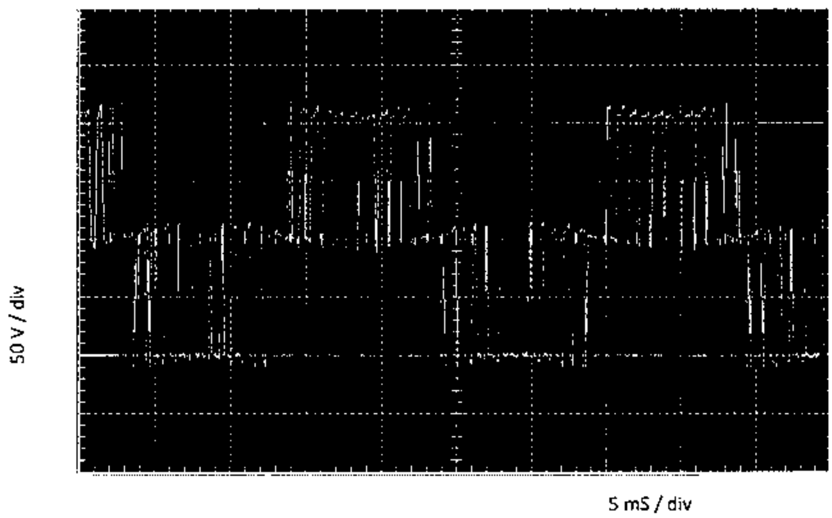


Fig 5.1 Inverter output voltage: U_{R-Y} - Line to line voltage, $f_0 = 50$ Hz

5.3 OUTPUT FOR 25Hz :

IN MOTOR :

Frequency : 25Hz

Motor speed : 700rpm

IN SCOPE :

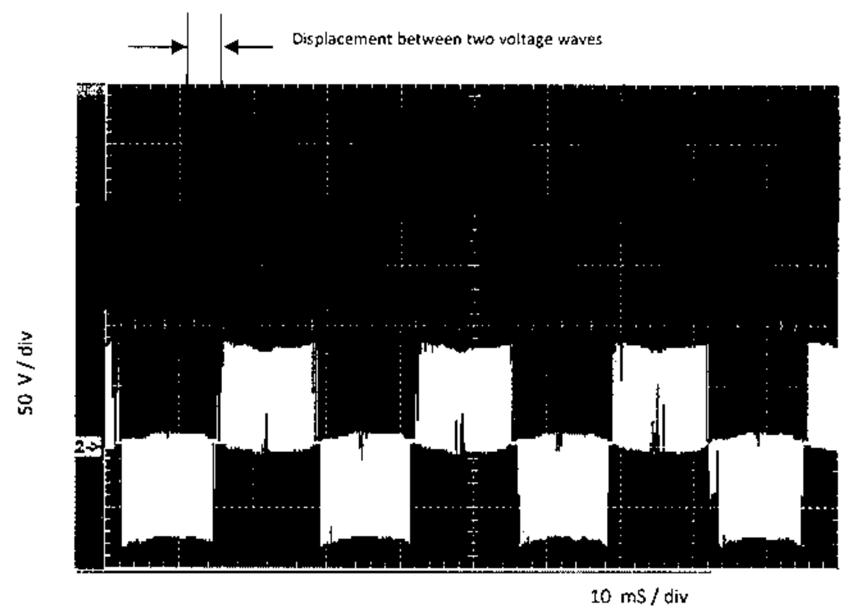


Fig 5.2 Inverter output voltage: U $_{Y-B}$ and U $_{B-R}$ Line to line voltage, f_0 = 25 Hz .

CHAPTER 6

CONCLUSION

CONCLUSION:

In this project a **THREE PHASE INVERTER USING EMBEDDED CONTROLLER** has been designed and implemented. By doing so the disadvantages present in analog based design are overcome. The advantages of the new system are a simple circuitry, reduced system size and minimum cost.

A buffer circuit is used to enhance the signal strength so that the inverter designed can be used for industrial purpose. The PIC 16f877A has the required features for programming in C language. The output of the three phase inverter is shown by running the induction motor at 25 Hz and 50 Hz.

In future this can be enhanced by implementing the same in Digital signal processing (DSP) or by FPGA. This will enhance the speed and efficiency of operation

REFERENCES

REFERENCES:

[1] B.K.Bose, "Power Electronics and ac Drives", Englewood Cliffs, NJ, Prentice-Hall, 1986.

[2] D. M. Bezesky and Scott Kreitzer, "Selecting ASD systems", The NEMA Application Guide for ac Adjustable Speed Drive Systems,IEEE Industry applications magazine, pp.39-49, 2003.

[3] F. Flaabjerg, A. Consoli, J. A. Ferraria and J. D.Van Wyk , "The future of power processing and conversion" *IEEE Trans. on Industry Applications*, Vol. 41, No.1, pp. 3-8 , 2005.

[4] J. Holtz, "Pulse Width Modulation—A survey," *IEEE Trans. on Industry Electronics*, Vol. 39, No. 5, pp. 410–420, 1992.

[5] J. Holtz, "Pulse Width Modulation for Electronic Power Conversion", *Proceeding of the IEEE*, Vol. 82, No. 8, pp. 1194 – 1214, 1994.

[6] A. Videt, P.L. Moigne, N. Idir, P. Baudesson, and X. Cimetière, "A New Carrier-Based PWM Providing Common-Mode-Current Reduction and DC-Bus Balancing for Three-Level Inverters" *IEEE Trans.on Industrial Electronics*, VOL. 54, No. 6, pp-3001,3011, 2007.

[7] Jun Li, A. Q. Huang, Z. Qian, H. Zhao, "A Novel Carrier-based PWM Method for 3-Level NPC Inverter Utilizing Control Freedom Degree", IEEE Proc. of APEC'98, pp.1899-1904,2007.

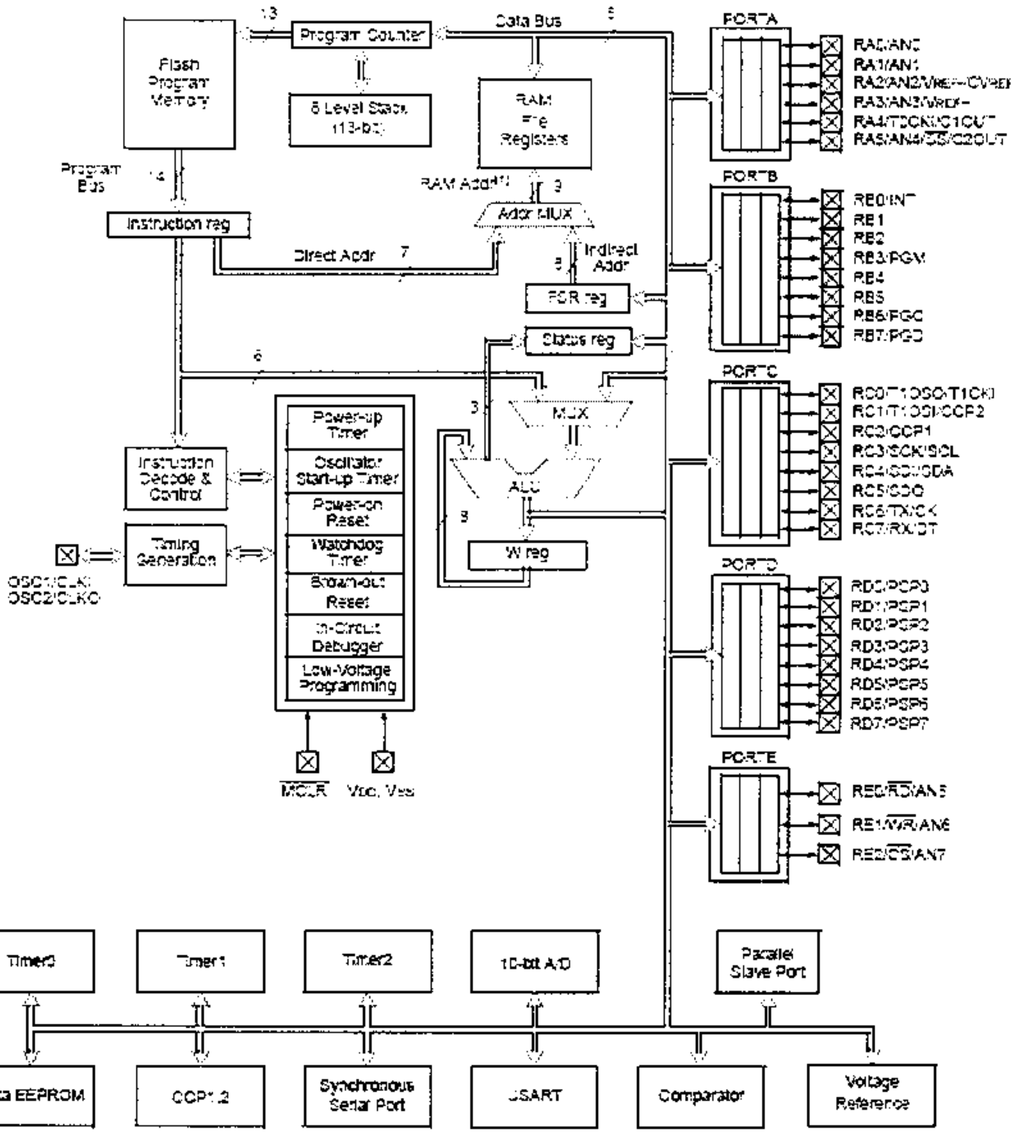
[8] S. Y. R. Hui, I. Oppermann, and S. Sathiakumar, " Microprocessor-Based Random PWM Schemes for DC–AC Power Conversion", *IEEE Trans.on Power Electronics,* Vol. 12, No.2,pp-253-260,1997.

[9] B. Mwinyiwiwa, Z. Wolanski, and B. Ooi, " Microprocessor-Implemented SPWM for Multiconverters with Phase-Shifted Triangle Carriers", *IEEE Trans.on Industry applications,* Vol. 34, NO.3,pp-487-494,1998.

APPENDIX A

APPENDIX A

PIC 16f877A-Architecture



Device	Program Flash	Data Memory	Data EEPROM
PIC16F874A	4K words	192 Bytes	128 Bytes
PIC16F877A	8K words	368 Bytes	256 Bytes

Note 1: Higher order bits are from the Status register.

Fig A.1 PIC 16f877A-Architecture

PIC16F87XA DEVICE FEATURES

Table A.1 PIC16F87XA device features

Key Features	PIC16F873A	PIC16F874A	PIC16F876A	PIC16F877A
Operating Frequency	DC – 20 MHz	DC – 20 MHz	DC – 20 MHz	DC – 20 MHz
Resets (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
Flash Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
EEPROM Data Memory (bytes)	128	128	256	256
Interrupts	14	15	14	15
I/O Ports	Ports A, B, C	Ports A, B, C, D, E	Ports A, B, C	Ports A, B, C, D, E
Timers	3	3	3	3
Capture/Compare/PWM modules	2	2	2	2
Serial Communications	MSSP, USART	MSSP, USART	MSSP, USART	MSSP, USART
Parallel Communications	—	PSP	—	PSP
10-bit Analog-to-Digital Module	5 input channels	8 input channels	5 input channels	8 input channels
Analog Comparators	2	2	2	2
Instruction Set	35 Instructions	35 Instructions	35 Instructions	35 Instructions
Packages	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin PLCC 44-pin TQFP 44-pin QFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin PLCC 44-pin TQFP 44-pin QFN

PIC16F874A/877A PINOUT DESCRIPTION

Table A.2 PIC16F874A/877A pinout description

Pin Name	PDIP Pin#	PLCC Pin#	TQFP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKI	13	14	30	32		ST/CMOS(4)	Oscillator crystal or external clock input.
OSC1					I		Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; otherwise CMOS.
CLKI					I		External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO	14	15	31	33		—	Oscillator crystal or clock output.
OSC2					O		Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO					O		In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	2	18	18		ST	Master Clear (input) or programming voltage (output).
$\overline{MCLR}$					I		Master Clear (Reset) input. This pin is an active low Reset to the device.
VPP					P		Programming voltage input.
							PORTA is a bidirectional I/O port.
RA0/AN0	2	3	19	19		TTL	
RA0					I/O		Digital I/O.
AN0					I		Analog input 0.
RA1/AN1	3	4	20	20		TTL	
RA1					I/O		Digital I/O.
AN1					I		Analog input 1.
RA2/AN2/VREF-/CVREF	4	5	21	21		TTL	
RA2					I/O		Digital I/O.
AN2					I		Analog input 2.
VREF-					I		A/D reference voltage (Low) input.
CVREF					O		Comparator VREF output.
RA3/AN3/VREF+	5	6	22	22		TTL	
RA3					I/O		Digital I/O.
AN3					I		Analog input 3.
VREF+					I		A/D reference voltage (High) input.
RA4/T0CKI/C1OUT	6	7	23	23		ST	
RA4					I/O		Digital I/O – Open-drain when configured as output.
T0CKI					I		Timer0 external clock input.
C1OUT					O		Comparator 1 output.
RA5/AN4/$\overline{SS}$/C2OUT	7	8	24	24		TTL	
RA5					I/O		Digital I/O.
AN4					I		Analog input 4.
$\overline{SS}$					I		SPI slave select input.
C2OUT					O		Comparator 2 output.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

PIC16F874A/877A PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDIP Pin#	PLCC Pin#	TQFP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
							PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI	15	16	32	34		ST	
RC0					I/O		Digital I/O.
T1OSO					O		Timer1 oscillator output.
T1CKI					I		Timer1 external clock input.
RC1/T1OSI/CCP2	16	18	35	35		ST	
RC1					I/O		Digital I/O.
T1OSI					I		Timer1 oscillator input.
CCP2					I/O		Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1	17	19	36	36		ST	
RC2					I/O		Digital I/O.
CCP1					I/O		Capture1 input, Compare1 output, PWM1 output.
RC3/SCK/SCL	18	20	37	37		ST	
RC3					I/O		Digital I/O.
SCK					I/O		Synchronous serial clock input/output for SPI mode.
SCL					I/O		Synchronous serial clock input/output for I²C mode.
RC4/SDI/SDA	23	25	42	42		ST	
RC4					I/O		Digital I/O.
SDI					I		SPI data in.
SDA					I/O		I²C data I/O.
RC5/SDO	24	26	43	43		ST	
RC5					I/O		Digital I/O.
SDO					O		SPI data out.
RC6/TX/CK	25	27	44	44		ST	
RC6					I/O		Digital I/O.
TX					O		USART asynchronous transmit.
CK					I/O		USART1 synchronous clock.
RC7/RX/DT	26	29	1	1		ST	
RC7					I/O		Digital I/O.
RX					I		USART asynchronous receive.
DT					I/O		USART synchronous data.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TIMER0 MODULE

The Timer0 module timer/counter has the following

Features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 9.2 is a block diagram of the Timer0 module and the prescaler shared with the WDT.Additional information on the Timer0 module is available in the PICmicro® Mid-Range MCU Family Reference Manual (DS33023). Timer mode is selected by clearing bit T0CS (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment

is inhibited for the following two instruction cycles.The user can work around this by writing an adjusted value to the TMR0 register. Counter mode is selected by setting bit T0CS (OPTION_REG<5>). In Counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by

the Timer0 Source Edge Select bit, T0SE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge. The prescaler is mutually exclusively shared between the Timer0 module and the Watchdog Timer. The prescaler is not readable or writable.

Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit TMR0IF (INTCON<2>). The interrupt can be masked by clearing bit TMR0IE (INTCON<5>). Bit TMR0IF must be cleared in software by the Timer0

module Interrupt Service Routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from Sleep since the timer is shut-off during Sleep.

BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

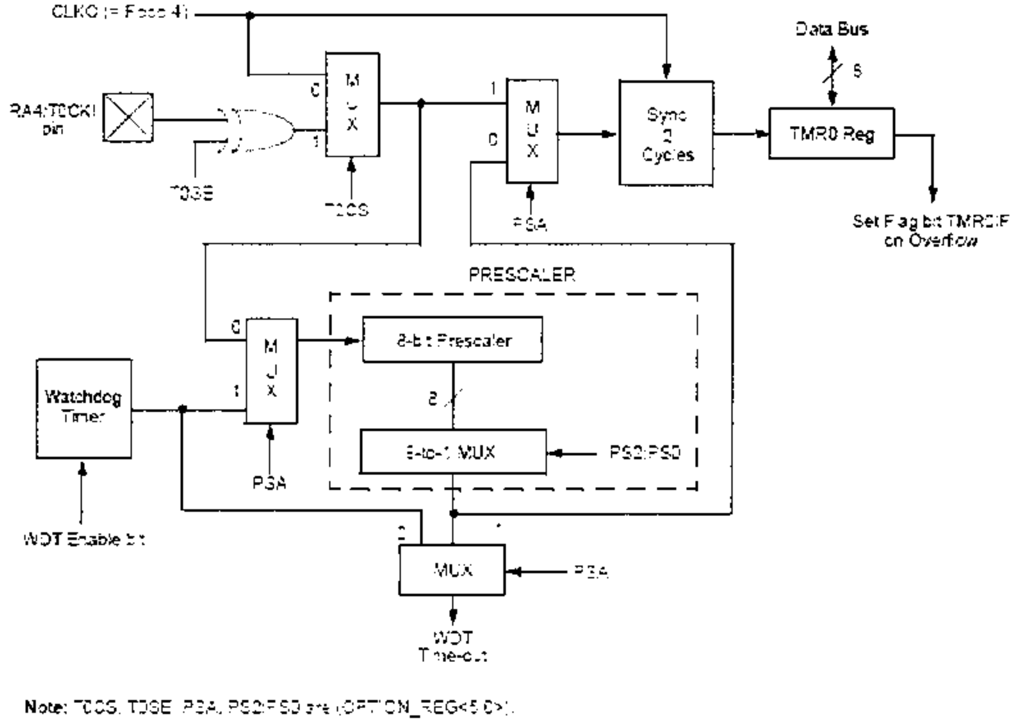


Fig A.2 block diagram of the timer0/wdt prescaler

I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin. Additional information on I/O ports may be found in the

PICmicro™ Mid-Range Reference Manual (DS33023).

PORTA and the TRISA Register

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin

an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations.

Therefore, a write to a port implies that the port pins are read, the value is modified and then written to the port data latch.Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The A4/T0CKI pin is a Schmitt Trigger input and an open-drain output. All other PORTA ins have TTL input levels and full CMOS output drivers.. The operation of each pin is selected by clearing/setting the appropriate control bits in the ADCON1 and/or CMCON registers.The TRISA register controls the direction of the port pins even when they are being used as analog inputs.The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

BLOCK DIAGRAM OF RA3:RA0 PINS

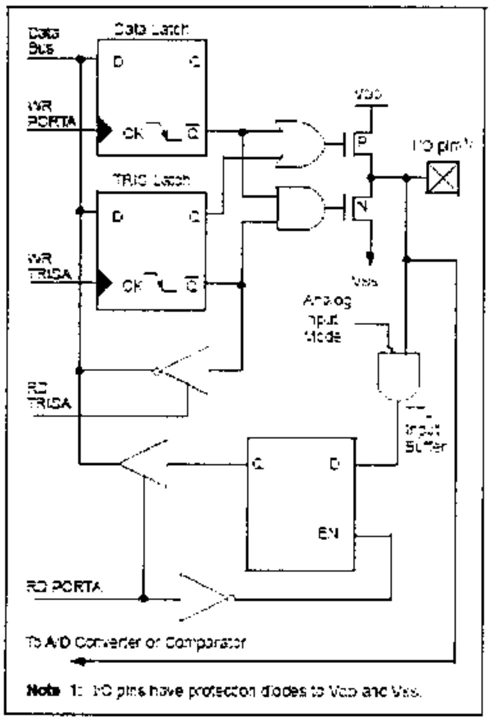
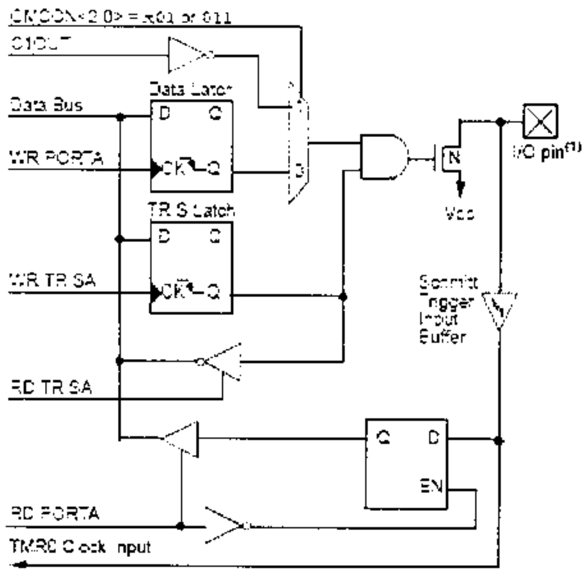


Fig A.3 block diagram of ra3:ra0 pins

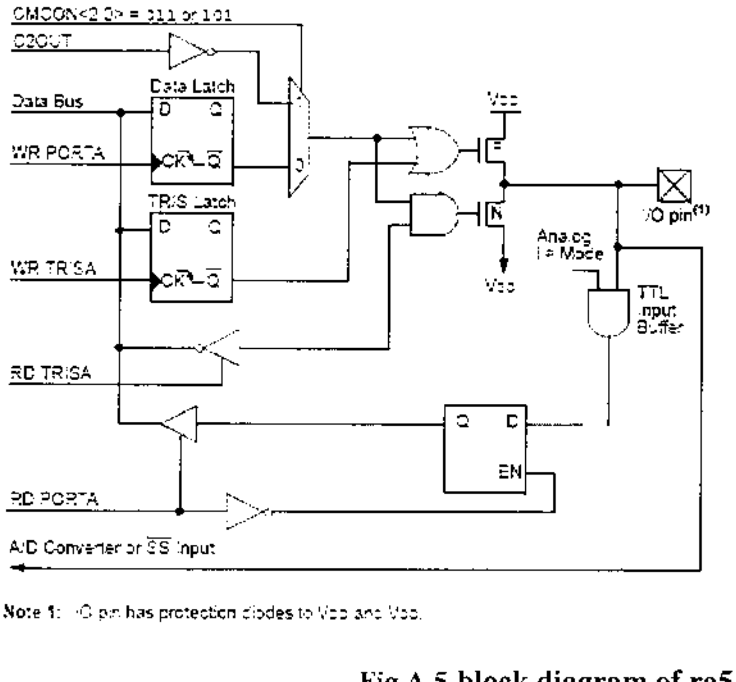
BLOCK DIAGRAM OF RA4/T0CKI PIN



Note 1: I/O pin has protection diodes to Vss only.

Fig A.4 block diagram of ra4/t0cki pin

BLOCK DIAGRAM OF RA5 PIN



Note 1: I/O pin has protection diodes to Vdd and Vss.

Fig A.5 block diagram of ra5 pin

PORTA FUNCTIONS

Table A.3 PORTA functions

Name	Bit#	Buffer	Function
RA0/AN0	bit 0	TTL	Input/output or analog input.
RA1/AN1	bit 1	TTL	Input/output or analog input.
RA2/AN2/VREF-/CVREF	bit 2	TTL	Input/output or analog input or VREF- or CVREF.
RA3/AN3/VREF+	bit 3	TTL	Input/output or analog input or VREF+.
RA4/T0CKI/C1OUT	bit 4	ST	Input/output or external clock input for Timer0 or comparator output. Output is open-drain type.
RA5/AN4/$\overline{SS}$/C2OUT	bit 5	TTL	Input/output or analog input or slave select input for synchronous serial port or comparator output.

Legend: TTL = TTL input, ST = Schmitt Trigger input

SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Table A.4 summary of registers associated with PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--0x 0000	--0u 0000
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
9Ch	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	0000 0111
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	000- 0000
9Fh	ADCON1	ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0	00-- 0000	00-- 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA

Note: When using the SSP module in SPI Slave mode and $\overline{SS}$ enabled, the A/D converter must be set to one of the following modes, where PCFG3:PCFG0 = 0100, 0101, 011x, 1101, 1110, 1111.

PORTB and the TRISB Register

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0)will make the corresponding PORTB pin an output (i.e.,put the contents of the output latch on the selected pin).Three pins of PORTB are multiplexed with the In-Circuit

Debugger and Low-Voltage Programming function:RB3/PGM, RB6/PGC and RB7/PGD.

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

BLOCK DIAGRAM OF RB3:RB0 PINS

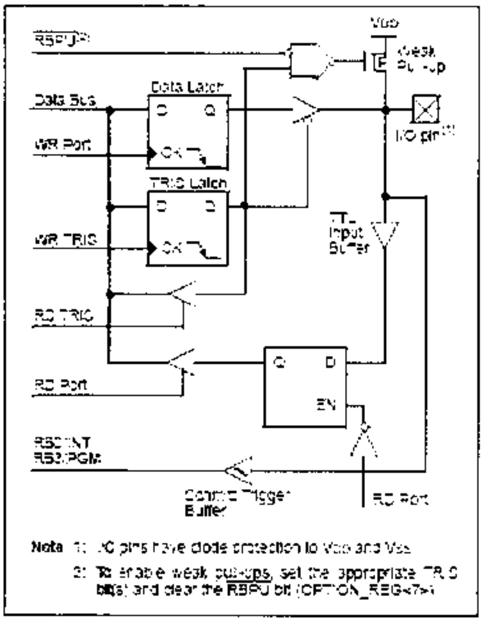


Fig A.6 block diagram of rb3:rb0 pins

BLOCK DIAGRAM OF RB7:RB4 PINS

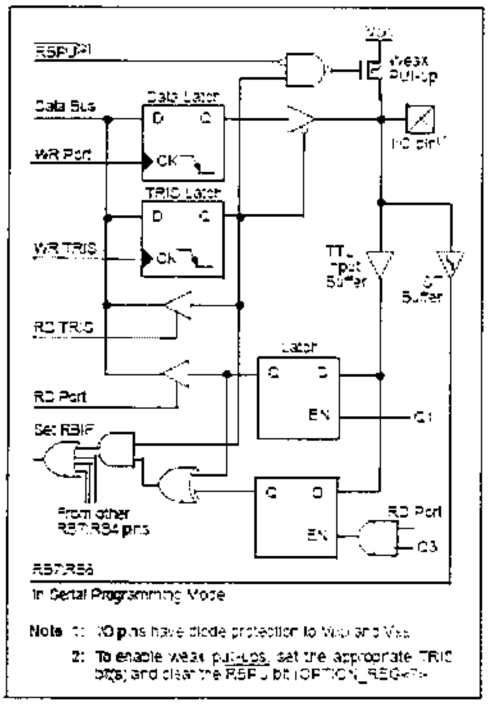


Fig A.7 block diagram of rb7:rb4 pins

PORTB FUNCTIONS

Table A.5 PORTB functions

Name	Bit#	Buffer	Function
RB0/INT	bit 0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit 1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit 2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3/PGM(3)	bit 3	TTL	Input/output pin or programming pin in LVP mode. Internal software programmable weak pull-up.
RB4	bit 4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit 5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6/PGC	bit 6	TTL/ST(2)	Input/output pin (with interrupt-on-change) or in-circuit debugger pin. Internal software programmable weak pull-up. Serial programming clock.
RB7/PGD	bit 7	TTL/ST(2)	Input/output pin (with interrupt-on-change) or in-circuit debugger pin. Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode or in-circuit debugger.

3: Low-Voltage ICSP Programming (LVP) is enabled by default which disables the RB3 I/O function. LVP must be disabled to enable RB3 as an I/O pin and allow maximum compatibility to the other 28-pin and 40-pin mid-range devices.

SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Table A.6 summary of registers associated with PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h, 186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
81h, 181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

BUFFER-CD4050B

Table A.7 Electrical specifications of buffer-CD4050B

DC Electrical Specifications

PARAMETER	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURE (°C)							UNITS
								25			
	V_O (V)	V_{IN} (V)	V_{CC} (V)	-55	-40	85	125	MIN	TYP	MAX	
Quiescent Device Current I_{CC} (Max)	-	0,5	5	1	1	30	30	-	0.02	1	µA
		0,10	10	2	2	60	60		0.02	2	µA
	-	0,15	15	4	4	120	120	-	0.02	4	µA
		0,20	20	20	20	600	600	-	0.04	20	µA
Output Low (Sink) Current I_{OL} (Min)	0.4	0,5	4.5	3.3	3.1	2.1	1.8	2.6	5.2	-	mA
	0.4	0,5	5	4	3.8	2.9	2.4	3.2	6.4	-	mA
	0.5	0,10	10	10	9.6	6.6	5.6	8	16		mA
	1.5	0,15	15	26	25	20	18	24	48	-	mA
Output High (Source) Current I_{OH} (Min)	4.6	0,5	5	-0.81	-0.73	-0.58	-0.48	-0.65	-1.2	-	mA
	2.5	0,5	5	-2.6	-2.4	-1.9	-1.55	-2.1	-3.9	-	mA
	9.5	0,10	10	-2.0	-1.8	-1.35	-1.18	-1.65	-3.0	-	mA
	13.5	0,15	15	-5.2	-4.8	-3.5	-3.1	-4.3	-8.0		mA
Output Voltage Low Level V_{OL} (Max)	-	0,5	5	0.05	0.05	0.05	0.05	-	0	0.05	V
		0,10	10	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0,15	15	0.05	0.05	0.05	0.05	-	0	0.05	V
Output Voltage High Level V_{OH} (Min)		0,5	5	4.95	4.95	4.95	4.95	4.95	5		V
		0,10	10	9.95	9.95	9.95	9.95	9.95	10		V
	-	0,15	15	14.95	14.95	14.95	14.95	14.95	15	-	V
Input Low Voltage V_{IL} Max CD4049UB	4.5	-	5	1	1	1	1	-	-	1	V
	9	-	10	2	2	2	2	-	-	2	V
	13.5		15	2.5	2.5	2.5	2.5			2.5	V
Input Low Voltage V_{IL} Max CD4050B	0.5		5	1.5	1.5	1.5	1.5	-	-	1.5	V
	1		10	3	3	3	3	-	-	3	V
	1.5		15	4	4	4	4	-	-	4	V

Continued

DC Electrical Specifications (Continued)

PARAMETER	TEST CONDITIONS V_O (V)	V_{IN} (V)	V_{CC} (V)	LIMITS AT INDICATED TEMPERATURE (°C) -55	-40	85	125	25 MIN	TYP	MAX	UNITS
Input High Voltage, V_{IH} Min CD4049UB	0.5	-	5	4	4	4	4	4	-	-	V
	1		10	8	8	8	8	8			V
	1.5	-	15	12.5	12.5	12.5	12.5	12.5	-	-	V
Input High Voltage, V_{IH} Min CD4050B	4.5	-	5	3.5	3.5	3.5	3.5	3.5	-	-	V
	9	-	10	7	7	7	7	7			V
	13.5	-	15	11	11	11	11	11	-	-	V
Input Current, I_{IN} Max		0,18	18	±0.1	±0.1	±1	±1		$\pm10^{-5}$	±0.1	µA

AC Electrical Specifications $T_A = 25^oC$, Input $t_r, t_f = 20ns$, $C_L = 50pF$, $R_L = 200k\Omega$

PARAMETER	TEST CONDITIONS V_{IN}	V_{CC}	LIMITS (ALL PACKAGES) TYP	MAX	UNITS
Propagation Delay Time Low to High, t_{PLH} CD4049UB	5	5	60	120	ns
	10	10	32	65	ns
	10	5	45	90	ns
	15	15	25	50	ns
	15	5	45	90	ns
Propagation Delay Time Low to High, t_{PLH} CD4050B	5	5	70	140	ns
	10	10	40	80	ns
	10	5	45	90	ns
	15	15	30	60	ns
	15	5	40	80	ns
Propagation Delay Time High to Low, t_{PHL} CD4049UB	5	5	32	65	ns
	10	10	20	40	ns
	10	5	15	30	ns
	15	15	15	30	ns
	15	5	10	20	ns
Propagation Delay Time High to Low, t_{PHL} CD4050B	5	5	55	110	ns
	10	10	22	55	ns
	10	5	50	100	ns
	15	15	15	30	ns
	15	5	50	100	ns
Transition Time, Low to High, t_{TLH}	5	5	80	160	ns
	10	10	40	80	ns
	15	15	30	60	ns
Transition Time, High to Low, t_{THL}	5	5	30	60	ns
	10	10	20	40	ns
	15	15	15	30	ns

MOSFET-IRF840

Table A.8 Electrical characteristics of mosfet-IRF840

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.55	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	10	μA
		V_{DS} = 400 V, T_C = 125°C	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 4.0 A	--	0.65	0.8	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 4.0 A (Note 4)	--	7.3	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1400	1800	pF
C_{oss}	Output Capacitance		--	145	190	pF
C_{rss}	Reverse Transfer Capacitance		--	35	45	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 8.0 A, R_G = 25 Ω (Note 4, 5)	--	22	55	ns
t_r	Turn-On Rise Time		--	65	140	ns
$t_{d(off)}$	Turn-Off Delay Time		--	125	260	ns
t_f	Turn-Off Fall Time		--	75	160	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 8.0 A, V_{GS} = 10 V (Note 4, 5)	--	41	53	nC
Q_{gs}	Gate-Source Charge		--	6.5	--	nC
Q_{gd}	Gate-Drain Charge		--	17	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	8.0	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	32	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 8.0 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 8.0 A, dI_F / dt = 100 A/μs (Note 4)	--	390	--	ns
Q_{rr}	Reverse Recovery Charge		--	4.2	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 9.0mH, I_{AS} = 8.0A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 8.0A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

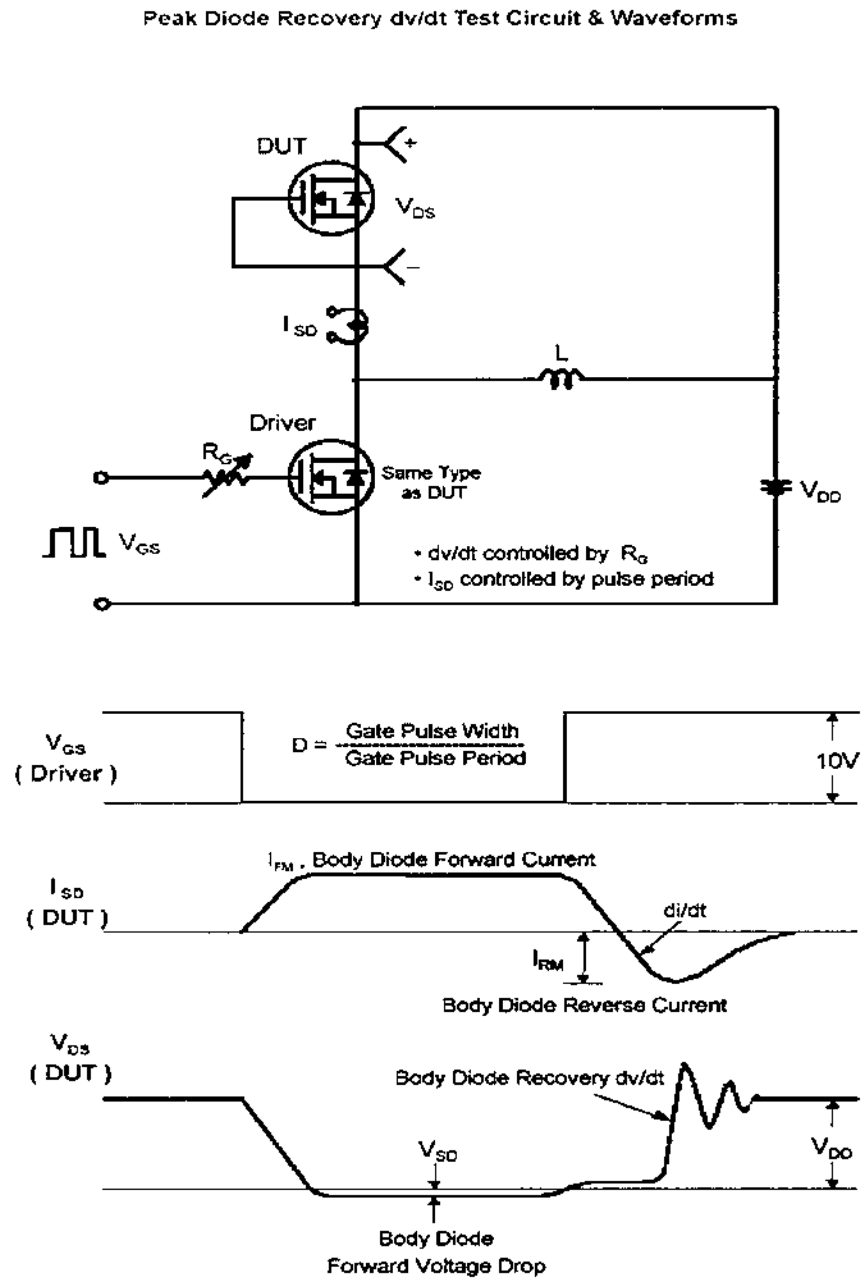


Fig A.8 peak diode recovery dv/dt test circuits and waveforms

MOSFET- IRF9520

Table A.9 Electrical specifications of mosfet- IRF9520

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = -250\mu A$, $V_{GS} = 0V$ (Figure 10)	-100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = -250\mu A$	-2	-	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, $V_{GS} = 0V$	-	-	-25	μA
		$V_{DS} = 0.8$ x Rated BV_{DSS}, $V_{GS} = 0V$ $T_C = 125^oC$	-	-	-250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)\,MAX}$, $V_{GS} = -10V$	-6	-	-	A
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = -3.5A$, $V_{GS} = -10V$ (Figures 8, 9)	-	0.500	0.600	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, $I_D = -3.5A$ (Figure 12)	0.9	2	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 0.5$ x Rated BV_{DSS}, $I_D \approx -6.0A$, $R_G = 50\Omega$, $R_L = 7.7\Omega$ for $V_{DSS} = 50\Omega$ MOSFET Switching Times are Essentially Independent of Operating Temperature	-	25	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	50	100	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	$V_{GS} = -10V$, $I_D = -6A$, $V_{DS} = 0.8$ x Rated BV_{DSS} (Figure 14) Gate Charge is Essentially Independent of Operating Temperature	-	16	22	nC
Gate to Source Charge	Q_{gs}		-	9	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	7	-	nC
Input Capacitance	C_{ISS}	$V_{DS} = -25V$, $V_{GS} = 0V$, f = 1MHz (Figure 11)	-	300	-	pF
Output Capacitance	C_{OSS}		-	200	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Internal Drain Inductance	L_D	Measured From the Contact Screw on Tab To Center of Die; Modified MOSFET Symbol Showing the Internal Devices Inductances	-	3.5	-	nH
		Measured From the Drain Lead, 6mm (0.25in) from Package to Center of Die	-	4.5	-	nH
Internal Source Inductance	L_S	Measured From the Source Lead, 6mm (0.25in) From Header to Source Bonding Pad	-	7.5	-	nH
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	-	3.12	$^oC/W$
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	Typical Socket Mount	-	-	62.5	$^oC/W$

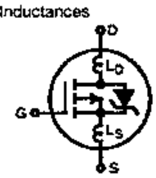
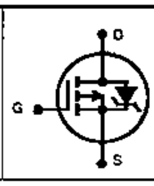


Table A.10 Source to drain diode specifications

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode		-	-	-6.0	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	-24	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_C = 25^oC$, $I_{SD} = -6.0A$, $V_{GS} = 0V$ (Figure 13)		-	-	-1.5	V
Reverse Recovery Time	t_{rr}	$T_J = 150^oC$, $I_{SD} = -6.0A$, $dI_{SD}/dt = 100A/\mu s$		-	230	-	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 150^oC$, $I_{SD} = -6.0A$, $dI_{SD}/dt = 100A/\mu s$		-	1.3	-	μC

NOTES:

2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD} = 25V$, starting $T_J = 25^oC$, $L = 15.4mH$, $R_G = 25\Omega$, peak $I_{AS} = 6.0A$.

Test Circuits and Waveforms

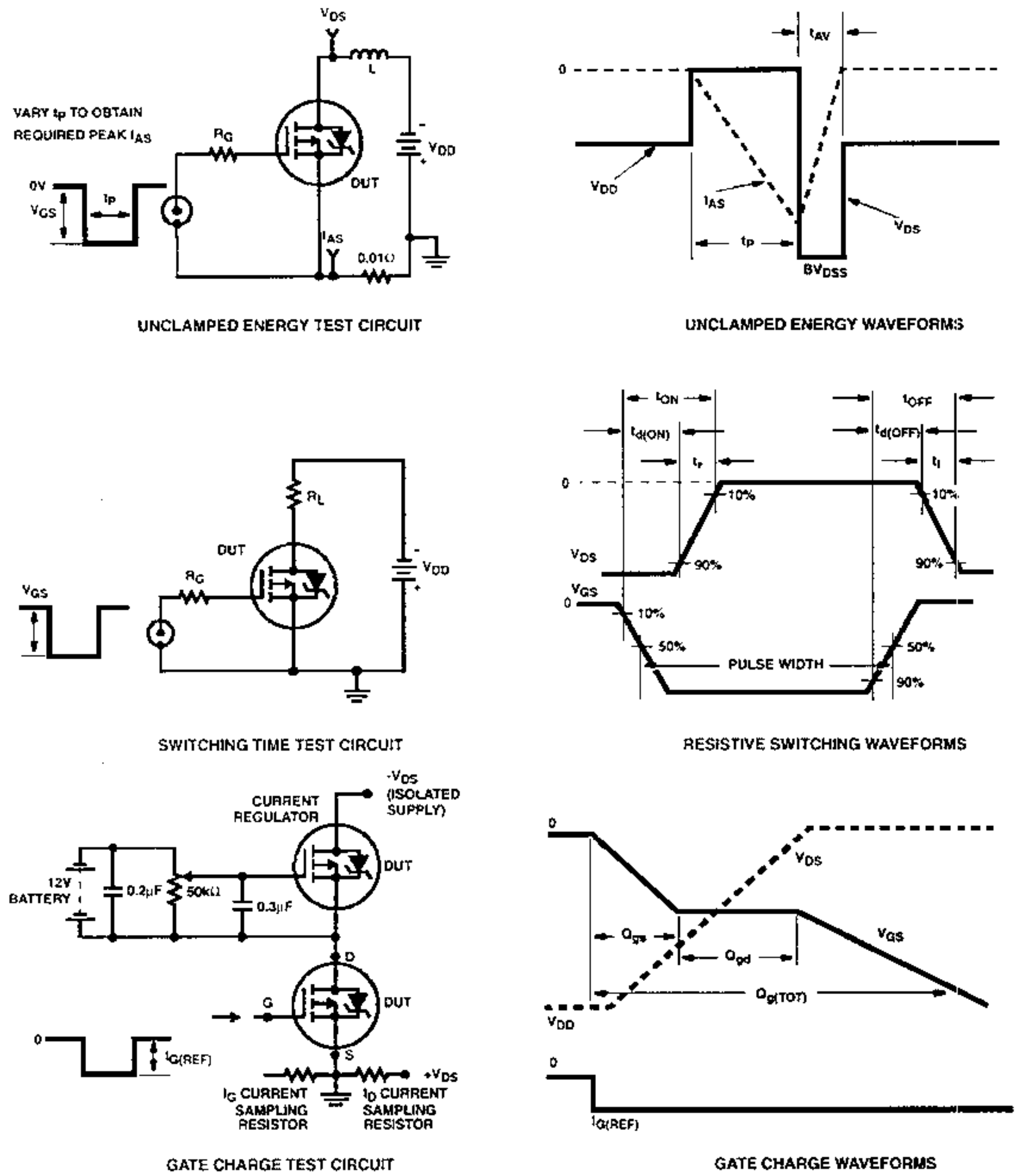


Fig A.9 Test circuits and waveforms of MOSFET- IRF9520

OPTOISOLATOR-SFH615

Maximum Ratings

Emitter (GaAs LED)

Reverse Voltage .... 6 V
DC Forward Current .... 60 mA
Surge Forward Current (t≤10 μs) .... 2.5 A
Total Power Dissipation .... 100 mW

Detector (Silicon Phototransistor)

Collector-Emitter Voltage .... 70 V
Collector Current .... 50 mA
Collector Current (t ≤1 ms) .... 100 mA
Total Power Dissipation .... 150 mW

Optocoupler

Storage Temperature Range .... -55°C to +150°C
Ambient Temperature Range .... -55°C to +100°C
Junction Temperature .... 100°C
Soldering Temperature (max. 10 s)[1] .... 260°C
Isolation Test Voltage[2]
(between emitter and detector referred
to standard climate 23/50 DIN 50014) .... 2800 VDC
Isolation Resistance (V_{IO}=500 V) .... 10^{11} Ω

Notes:

1 Dip soldering minimum clearance from bottom edge of package 1.5 mm. Special soldering conditions apply when through-contacted circuit boards are used. Please request appropriate specification.
2 DC test voltage in accordance with DIN 57883, draft 4/78

Characteristics (T_A=25°C)

Emitter (GaAs LED)			
Forward Voltage (I_F=60 mA)	V_F	1.25 (≤1.65)	V
Breakdown Voltage (I_R=10 μA)	V_{BR}	30 (≥6)	V
Reverse Current (V_R=6 V)	I_R	0.01 (≤10)	μA
Capacitance (V_R=0 V, f=1 MHz)	C_0	25	pF
Thermal Resistance	R_{thJA}	750	K/W
Detector (Silicon Phototransistor)			
Capacitance (V_{CE}=5 V, f=1 MHz)	C_{CE}	6.8	pF
Thermal Resistance	R_{thJA}	500	K/W
Optocoupler			
Collector-Emitter Saturation Voltage (I_F=10 mA, I_C=2.5 mA)	V_{CEsat}	0.26 (≤0.4)	V
Coupling Capacitance	C_K	0.26	pF

The optocouplers are grouped according to their current transfer ratio I_C/I_F at V_{CE}=5 V, marked by dash numbers

	–1	–2	–3	–4	
I_C/I_F (I_F=10 mA)	40–80	63–125	100–200	160–320	%
I_C/I_F (I_F=1 mA)	30 (>13)	45 (>22)	70 (>34)	90 (>56)	%
Collector-Emitter Leakage Current (V_{CE}=10 V) (I_{CEO})	2 (≤50)	2 (≤50)	5 (≤100)	5 (≤100)	nA

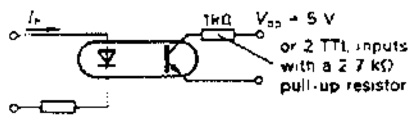
SWITCHING TIMES

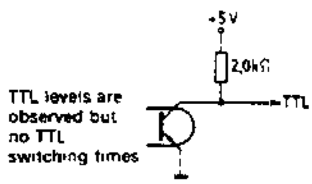
Linear Operation (without saturation)

I_F=10 mA, V_{CE}=5 V, T_A=25°C

Load Resistance	R_L	75	Ω
Turn-On Time	t_{on}	3.0 (≤5.6)	μs
Rise Time	t_r	2.0 (≤4.0)	μs
Turn-Off Time	t_{off}	2.3 (≤4.1)	μs
Fall Time	t_f	2.0 (≤3.5)	μs
Cut-Off Frequency	F_{CO}	250	kHz

Switching Operation (with saturation)





Group		–1 (I_F=20 mA)	–2 and –3 (I_F=10 mA)	–4 (I_F=5 mA)	
Turn-On Time	t_{on}	3.0 (≤5.5)	4.2 (≤8.0)	6.0 (≤10.5)	μs
Rise Time	t_r	2.0 (≤4.0)	3.0 (≤6.0)	4.6 (≤8.0)	μs
Turn-Off Time	t_{off}	18 (≤34)	23 (≤39)	25 (≤43)	μs
Fall Time	t_f	11 (≤20)	14 (≤24)	15 (≤26)	μs
	V_{CEsat}		0.25 (≤0.4)		V

CHARACTERISTICS:

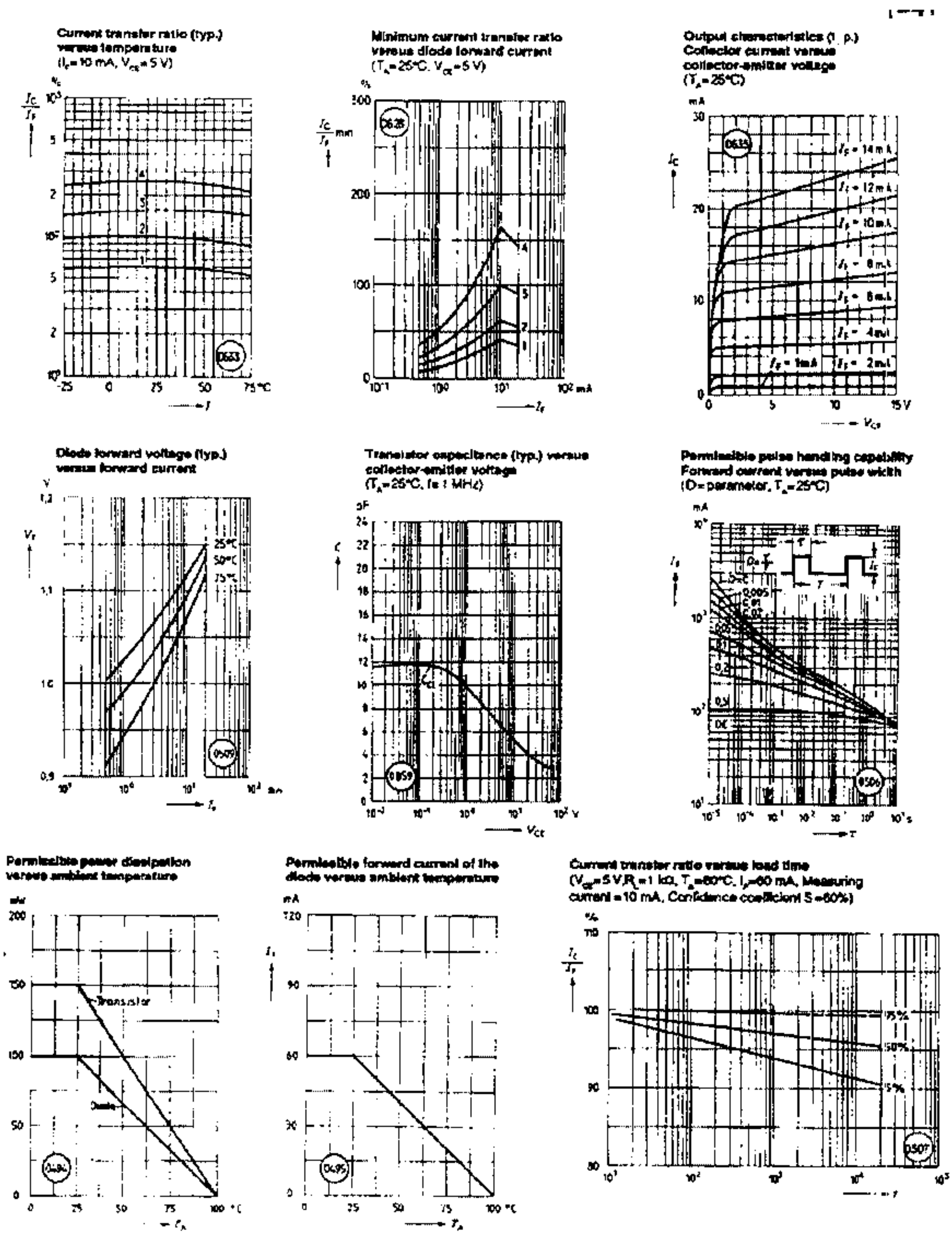


Fig A.10 characteristics of optoisolator-SFH615

APPENDIX B

B.1 CODE FOR GENERATING PWM PULSES:

```
#include<pic.h>

__CONFIG(0x1F71);

void main()

{

        ADCON1=0x06;


        PR2=99;

        CCPR1L=50;

        CCP1CON=0X0C;

        T2CON=0X04;


        TRISD=0X0F;

        TRISC=0X80;

        TRISB=0;

        TRISA=0;

        PORTC=0;

        PORTB=0;


        OPTION=0x87;

        TMR0=0;
```

```
GIE=PEIE=INTE=T0IE=TMR1IE=1;


T1CON =0x01;

TMR1L = 0x00;

TMR1H = 0x00;


if(RD0==1)

{

        while(1)

        {

                PORTB=0x42;

                while(TMR0<8);

                PORTB=0x52;

                while(TMR0<44);


                PORTB=0x50;

                while(TMR0<52);

                PORTB=0x30;

                while(TMR0<60);
```

```
                PORTB=0x38;
                while(TMR0<96);
                PORTB=0x28;
                while(TMR0<104);

                PORTB=0x0c;
                while(TMR0<112);
                PORTB=0x0e;
                while(TMR0<148);
                PORTB=0x06;
                while(TMR0<156);
                TMR0=0;
                        }
            }
if(RD1==1)
{
        while(1)
        {
                PORTB=0x42;
                while(TMR0<4);
                PORTB=0x52;
```

```
            while(TMR0<22);
            PORTB=0x50;
            while(TMR0<26);
            PORTB=0x30;
            while(TMR0<30);
            PORTB=0x38;
            while(TMR0<48);
            PORTB=0x28;
            while(TMR0<52);
            PORTB=0x0c;
            while(TMR0<56);
            PORTB=0x0e;
            while(TMR0<74);
            PORTB=0x06;
            while(TMR0<78);
            TMR0=0;
        }
}
while(1);
}
```

B.2 SWITCHING SEQUENCE FOR 50 HZ

Table B.1 switching sequence for 50 hz

TIMING SEQUENCE		P1	P3	P2	P4	P5	P6		
	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	PORTB OUTPUT VALUES
0	0	1	0	0	0	0	1	0	0*42
10	0	1	0	1	0	0	1	0	0*52
57	0	1	0	1	0	0	0	0	0*50
67	0	0	1	1	0	0	0	0	0*30
77	0	0	1	1	1	0	0	0	0*38
124	0	0	1	0	1	0	0	0	0*28
134	0	0	0	0	1	1	0	0	0*0C
144	0	0	0	0	1	1	1	0	0*CE
191	0	0	0	0	0	1	1	0	0*06
201	0	0	0	0	0	0	1	0	0*42

B.3 SWITCHING SEQUENCE FOR 25 HZ

Table B.2 switching sequence for 25 hz

TIMING SEQUENCE		P1	P3	P2	P4	P5	P6		
	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	PORTB OUTPUT VALUES
0	0	1	0	0	0	0	1	0	0*42
20	0	1	0	1	0	0	1	0	0*52
114	0	1	0	1	0	0	0	0	0*50
134	0	0	1	1	0	0	0	0	0*30
154	0	0	1	1	1	0	0	0	0*38
248	0	0	1	0	1	0	0	0	0*28
268	0	0	0	0	1	1	0	0	0*0C
288	0	0	0	0	1	1	1	0	0*CE
382	0	0	0	0	0	1	1	0	0*06
402	0	0	0	0	0	0	1	0	0*42