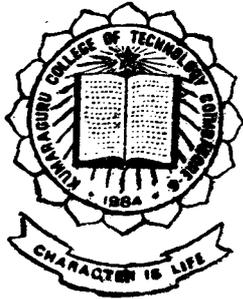


Digital Energy Meter

p - 268

Project Report 1996 - '97



Submitted in partial fulfilment of the requirements for the award of the Degree of
BACHELOR OF ENGINEERING
in Electrical and Electronics Engineering
of the Bharathiar University

Submitted by

K. Vanisri

S. Solai Manohar

E. Bharathi

H. Kamaraj

Guided by

Mr. R. Hari Haran, M.E.,

Department of Electrical and Electronics Engineering
Kumaraguru College of Technology

Coimbatore-641 006

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
Kumaraguru College of Technology
Coimbatore - 641 006.

Certificate

This is to certify that the Project Report entitled

DIGITAL ENERGY METER

has been submitted by

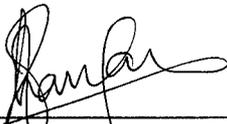
Miss. K. VANISRI
Mr. S. SOLAI MANOHAR
Miss. E. BHARATHI
Mr. U. KAMARAJ

in partial fulfilment for the award of the degree of

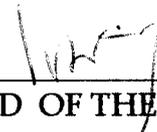
BACHELOR OF ENGINEERING

in Electrical and Electronics Engineering Branch of the Bharathiar University,

during the academic year 1996-97.



GUIDE



HEAD OF THE DEPARTMENT

Date: 9/4/97

Certified that the candidate with University Reg.No: _____ was
examined by us in the project work viva-voce Examination held on _____

INTERNAL EXAMINER

EXTERNAL EXAMINER

CERTIFICATE

This is to certify that the following students of
Kumaraguru College of Technology Coimbatore of branch Electrical,
and Electronics Engineering.

1. E. BHARATHI
2. U. KAMARAJ
3. S. SOLAI MANOHAR
4. K. VANISRI

had undertaken the project "Digital Energy meter" from
Oct '96 to March '97 at our industry and have successfully completed
it.

Their performance during that period was found to good.

We wish them all success.

Place: Coimbatore

Date :

Company Seal

VISAGAN ELECTRONICS PRIVATE LIMITED,
11/72, Thadagam Road, Sivagami Nagar,
Opp: Sivaji Colony,
EDAYARPALAYAM
COIMBATORE-641 025.

External Guide



(N. DHANAKODI)
R&D ENGINEER.

ACKNOWLEDGEMENT

Nature is the controller of things happening in this universe. Similarly whatever happens in this universe or whatever is being done by the people is made to stand upright by a backbone. Just as the backbone is more important for man to stand upright. Whatever we have done as our project is being reinforced with the advice and goodwill of reverent guide MR. R. HARIHARAN, M.E.

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SYNOPSIS

In this project a "DIGITAL ENERGY METER" is designed, fabricated and tested to measure and display the energy consumed by an electrical load. The analog energy meters are inferior to digital ones in terms of accuracy. Solidstate circuits are used in the digital meter. The fundamental measurement is performed by sensing the instantaneous power and hence the average power. By summing the product of power and time for precisely known time period total energy is obtained. The resulting total count is proportional to the unknown energy consumed by the load. Counted energy is displayed in the digital form at the display.

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CHAPTER-1

INTRODUCTION

Opinion remains different on this subject because the world today is quite different and much more important than it was a century ago. If our ancestors would rise from their grave yard they would be wondering to see the marvellous changes brought in by "ELECTRONICS" especially during this century and would really envy us. One of such improvements is our project "DIGITAL ENERGY METER". Nowadays all analogue meters are converted into digital represented by binary digits (bits). A bit may assume either one of two values 1 and 0. Characteristic of a digital system is its manipulation of discrete elements of information. Such discrete elements may be electric impulses, the decimal digits, the letters of an alphabet, arithmetic operations or any other set of meaningful symbols. Discrete elements of information are represented in a digital system by physical quantities called signals. Electrical signals such as voltages and currents are the most common.

The energy meter is one of the most important measuring instrument. Which is used for measuring the energy consumed by a load. To solve this purpose normally analogue meters are used. But we decided to construct a meter by digital means, which will measure and indicates the consumed energy of a load. This eliminates the following errors which are present in the conventional meters.

- a. *Incorrect phase displacement error.*
- b. *Frictional error*
- c. *Creeping*
- d. *Error due to temperature variation*

Also, high voltage causes saturation of iron path and hence proper linearity is lost at higher voltages. They develop more error in course of time due to wear and tear.

The design principles, fabrication methods and test results are presented in this report.

1.1 WORKING PRINCIPLE

This chapter deals with the basic working principle of the digital energy meter using block-diagrammatic representation. The block diagrammatic representation of the digital energy meter is shown in fig 1.1. It consists of wattmeter and energy meter circuits.

1.2 WATTMETER STAGE

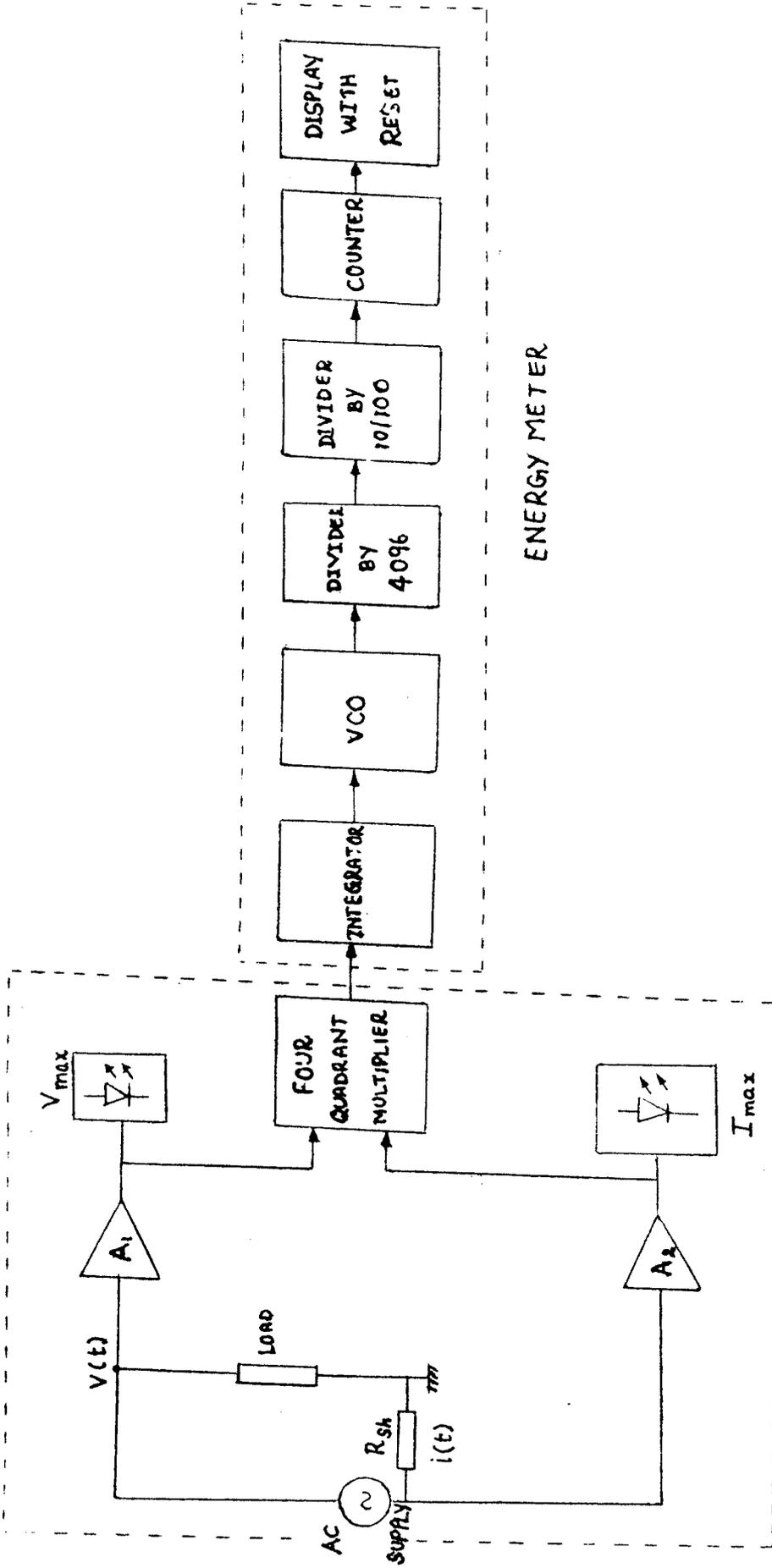
The load power is equal to the mean of the product of the instantaneous voltage across the load and the instantaneous current through it. The main voltage $u(t)$ and the voltage across the resistor R_{shunt} which is developed due to the load current flowing through it are amplified by the input stage amplifiers A1 and A2 as shown in fig-1.1. The output of these

amplifiers are fed to the four quadrant multiplier. The multiplier forms the product of the instantaneous voltage and current and supplies a current as a measure of the instantaneous power $P(t)$. The purpose of the two LED's is to indicate when the wattmeter is being overdriven by an excessive voltage or current.

1.3 ENERGY METER STAGE:

The integrated multiplier output is fed to the voltage controlled oscillator (vco). The VCO provides pulse at its output of which the frequency is directly proportional to its drive current, i.e., the measured power. The VCO output signal is fed to a divider which is divided by 4096, Then the divider output is further divided by 10 or 100 [This increases the measuring range by 10 or 100] which is dependent on the desired meter scale. The dividers are followed by actual counter and the range selector consisting of ranges 1, 10 and 100 which gives the four digit readout.

There is a reset mechanism for resetting the meter to zero.



R_{sh} - Shunt Resistance
 WATTMETER

FIG. 1.1 : BLOCK DIAGRAM REPRESENTATION OF DUAL DIGITAL WATT AND ENERGY METER

CHAPTER-2

DIGITAL ENERGY METER CIRCUIT

This chapter deals with the circuit operation of dual watt and energy meter.

2.1 WATT METER STAGE:

Circuit diagram of this stage is shown in fig 2.1. This stage consists of the following parts,

- 1. Voltage sensing element*
- 2. Current sensing element*
- 3. Protective diodes*
- 4. Operational Amplifiers*
- 5. Over voltage and over current protection*
- 6. Four quadrant multiplier cum integrator*
- 7. Voltage controlled oscillator*

Voltage controlled oscillator which is a part of the circuit containing A4 and A6 is provided to allow for expansion of wattmeter into energymeter.

A voltage divider [R1/R2/R3] reduces the mains voltage to one which is suitable for the wattmeter [mains voltage divided by 60] since the circuit uses 1/8 W resistor and it can only withstand a voltage, two resistors are connected in series to makeup one resistor of the voltage divider. The

measuring current is sensed by the shunt resistor R4. Diodes D1/D2 and D3/D4 are protective elements. If the input signal exceeds 12V the diodes conduct, thus the maximum input voltage is limited to approximately 12V. The input stages consists of A1, A2 and the associated components. Voltage and current senses by the voltage divider and R4 is fed as input of A1 and A2 respectively. The amplification factor of the input op-amp stages can be set 1 or 10. For a factor of 1, the terminals at A and B should be jumpered. The choice of amplification factor also known as slope depends on the load voltage and current.

The output signals of A1 and A2 are fed to the four quadrant multiplier A5, which is the operational Transconductance Amplifier (OTA) IC LMI 3600. OTA amplifies the differential voltage applied to its inputs (pins 13 and 14) and supplies a current at its output (pin 12). The amplification factor is quoted in mA/v and is referred to as "slope". This slope is relatively linear and varies as a function of the current (control) flowing in at pin 16. Thus the OTA multiplies two variables and provides a current as the product. In this case, one variable is the voltage derived from the mains and converted to control current by R2 and R16, and the second variable is the voltage which results from the load current through R4 (Rsh).

Regarding the resistance R4, excessive load current can damage the shunt resistor R4, The power dissipated by this resistor is $P_r = R_4 \times I_{rms}^2$

The load current can be estimated before connecting the meter.

$$I_{rms} = P_{load} / V_{rms} \cdot \cos\theta$$

The value given (0.47 ohms/5w) should be safe for loads upto 350W (mains powered). for higher loads, the value of R4 must be decreased.

The four quadrant multiplier followed by a stage with a virtual earth because the non-inverting input is connected to earth and the voltage difference between non-inverting and inverting inputs of operational amplifiers is assumed to be zero. Integrating network R18/c11 forms the mean or average value of the alternating output current of A5 . Also the next stage VCO circuit can only process an average current, we have to include network R28 / C11. since the VCO circuit can only process positive currents, the watt meter expanded to a kilowatt hour meter will also only be capable of indicating positive power readings. Two LED's are contained in the circuitary of A7 and A8 to indicate over driving. These circuits operate as fullwave rectifiers. Positive voltages are applied via D6 (D6') and negative voltages via the inverting input of the operational amplifier and D7(D7') to transistor stage T2/T3(T2'/T3') If the signal level filtered by C8(C8') is sufficiently high LED D8(D8') lights to indicate that the wattmeter is being overdriven.

2.2 ENERGY METER STAGE:

To know the energy drawn by an appliance from the mains supply over a given period, the power consumed by the appliance in watts have to be multiplied with the time in seconds or hours. This circuit is shown in fig 2.2. The input circuit is fed with the VCO output signal of the wattmeter. The frequency of the VCO signal is in direct proportion to the power measured by the watt meter, the higher the power, the higher the frequency. To convert the wattmeter to an energy meter only the addition of a fairly simple digital counter is needed. This can be simply indicated by the block diagram in fig 2.3. The VCO frequency is first divided by 4096(IC₂). Depending upon the desired meter scale, it is then divided by 10 or 100 this increases the measuring range by 10 and 100, respectively.[IC₃] The dividers are followed by the actual counter IC5 drives a four digit 7 segment display. The decimal points of the display are determined by the position of S₂, the meter range switch. The counter is reset by pressing push button switch S1, at the same time the two dividers IC2 and IC3 are reset to the zero position. To get an indication when the counter has reached its maximum capacity, use is made of its 'carry out' terminal (pin 14). At the moment the counter changes from 9999 to 0000, the logic bit at pin 14 changes from 1 to 0, which causes the capacitor C3 to charge via resistor R5. When the resulting voltage at the clock-input (pin 3) of bi-stable IC4 reaches logic 1, its output Q also becomes 1(+5V). Transistor T1 is then fired and LED D4 lights, indicating that the counter has gone past its maximum at least once. It should

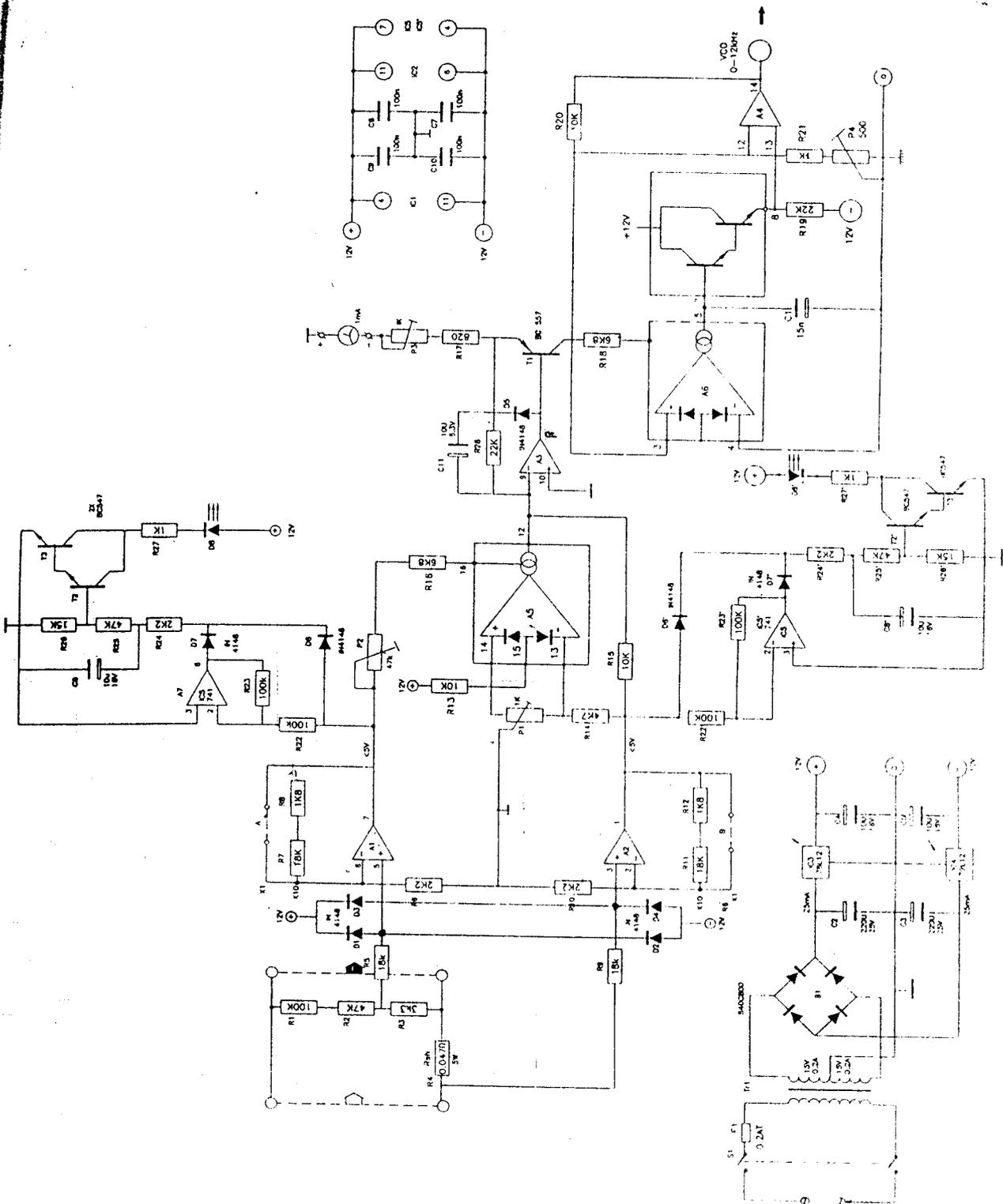


FIG. 2.1 WATTMETER CIRCUIT

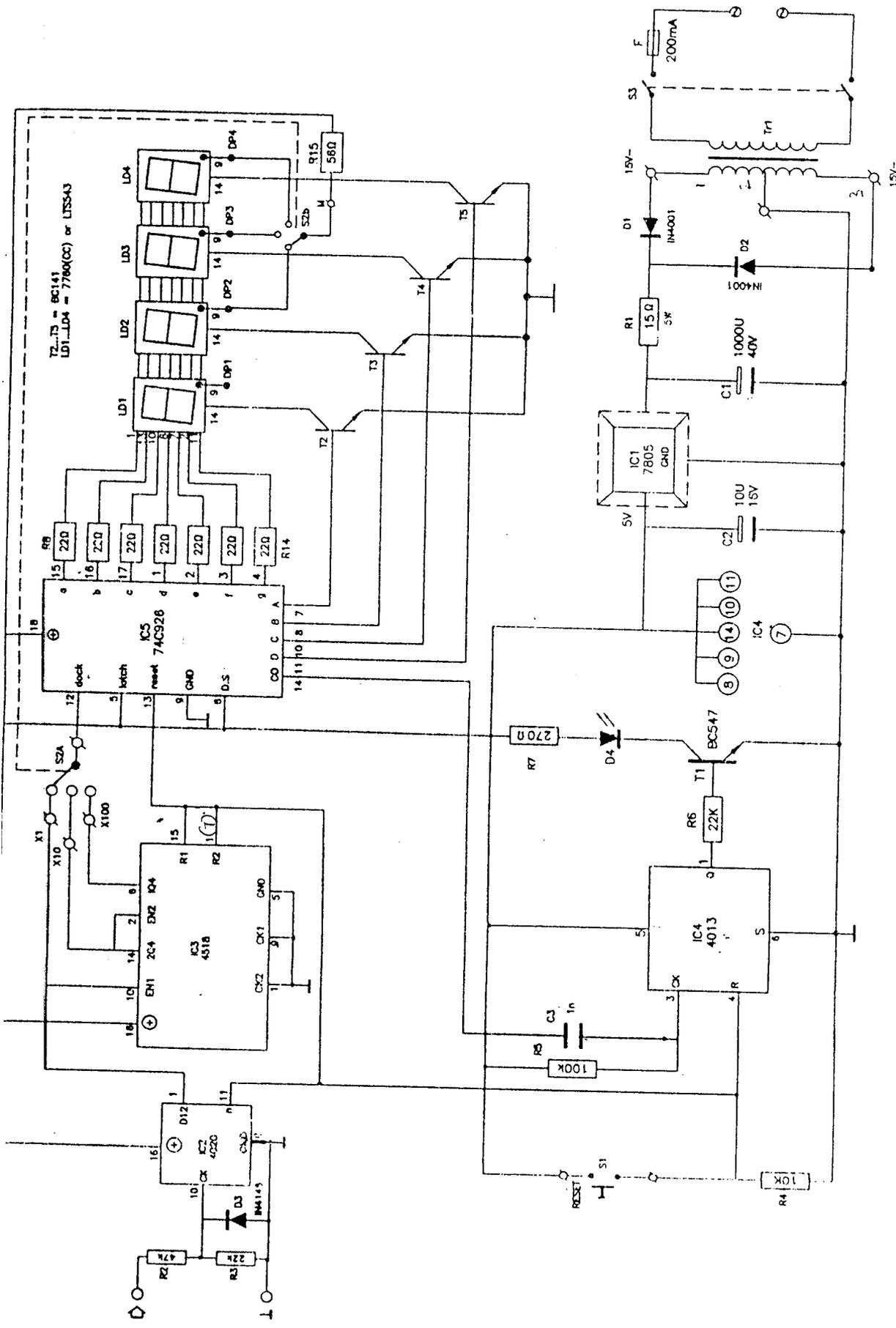


Fig 2-2 ENERGYMETER CIRCUIT

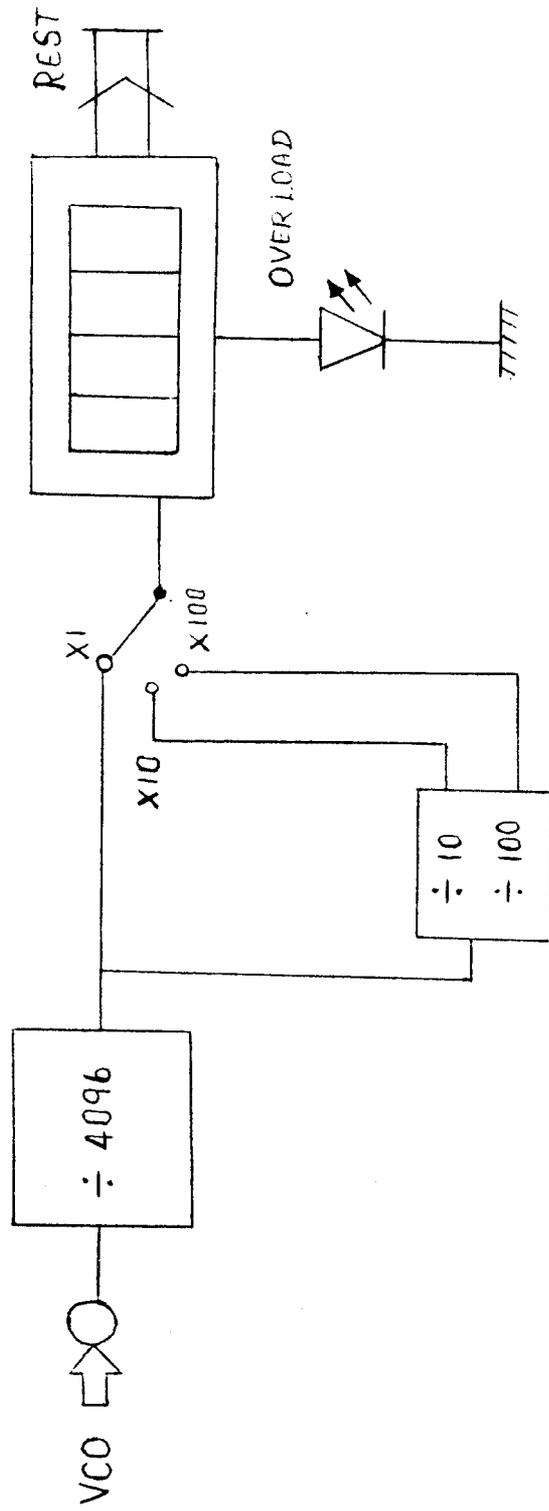


FIG 2.3: BLOCK DIAGRAM OF ENERGY METER STAGE

CHAPTER-3

3.1 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

An OTA is a voltage input current output device such that,

$$\begin{aligned} I_o &= g_m V_{in} \\ &= g_m (V_1 - V_2) \end{aligned}$$

Where,

I_o - Output current in mA.

g_m - Transconductance or gain of OTA

V_1 & V_2 - Input voltages in V.

The unique feature of an OTA is that it is possible to vary g_m over a wide range by means of an external control current. OTA amplifies the differential voltage applied to its inputs and supplies a current at its output. The amplification factor is quoted in mA/v, and is referred to as slope(s).

The equivalent circuit diagram of an OTA configured as a four quadrant multiplier is as shown in fig 3.1. The voltage derived from the mains is designated u_1 and the voltage derived from the load current is designated u_2 . The slope 'S' of the inverting OTA is adjusted with P2. This circuit produces current i_3 which flows to chassis earth (or virtual earth to be more precise). This current, in turn is proportional to the product of u_1 and u_2 . This means that if one of the two factors is zero, no output current will flow because zero multiplied by another value is zero. If the OTA has no u_2 input

signal, this condition is met so there is no gain and therefore no current. The slope is adjusted with P2, so that i_1 plus i_2 is equal to zero when u_1 is zero. According to the rule of nodes, i_3 is then also zero. If neither voltage is zero, an output current i_3 proportional to the product of u_1 and u_2 is produced as a result of the linear characteristic of the OTA. Thus this circuit produces current i_3 which flow to chassis earth from the fig 3.1 the following equations are obtained,

$$i_3 = i_1 + i_2 \text{ [By KCL]} \quad \text{---(3.1)}$$

$$\text{i.e., } i_3 = -(S + S_0) U_1 + U_2 / R_{15} \quad \text{---(3.2)}$$

where,

S_0 - Slope at $u_1 = 0$

$S = ku_1$ where k is a constant

$$i_3 = -[ku_1 + S_0] U_1 + U_2 / R_{15} \quad \text{---(3.3)}$$

$$i_3 = -ku_1 u_2 - S_0 u_2 + u_2 / R_{15} \quad \text{---(3.4)}$$

If P3 is adjusted so that $S_0 = 1/R_{15}$

$$i_3 = -ku_1 u_2$$

$$i_3 = ku_1 u_2 \quad \text{---(3.5)}$$

Thus this current i_3 , in turn is proportional to the product of u_1 and u_2 .

3.2 PURPOSE OF FOUR QUADRANT MULTIPLIER

There are four different situations that can be encountered during the multiplication of alternating voltages, and currents which are listed below as well as shown in fig 3.3

(i) Instantaneous voltage and instantaneous current are simultaneously positive [quadrant-I].

(ii) Instantaneous voltage is negative and instantaneous current is positive [quadrant-II].

(iii) Instantaneous voltage and instantaneous current are simultaneously negative [quadrant-III].

(iv) Instantaneous voltage is positive and the instantaneous current is negative [quadrant-IV].

If the instantaneous power is negative [II and IV] the load returns power to the mains on account of its capacitive or inductive characteristics.

If the load consumes or draws power then the multiplier supplies a positive output current. The load returns power to the mains if the multiplier current is negative.

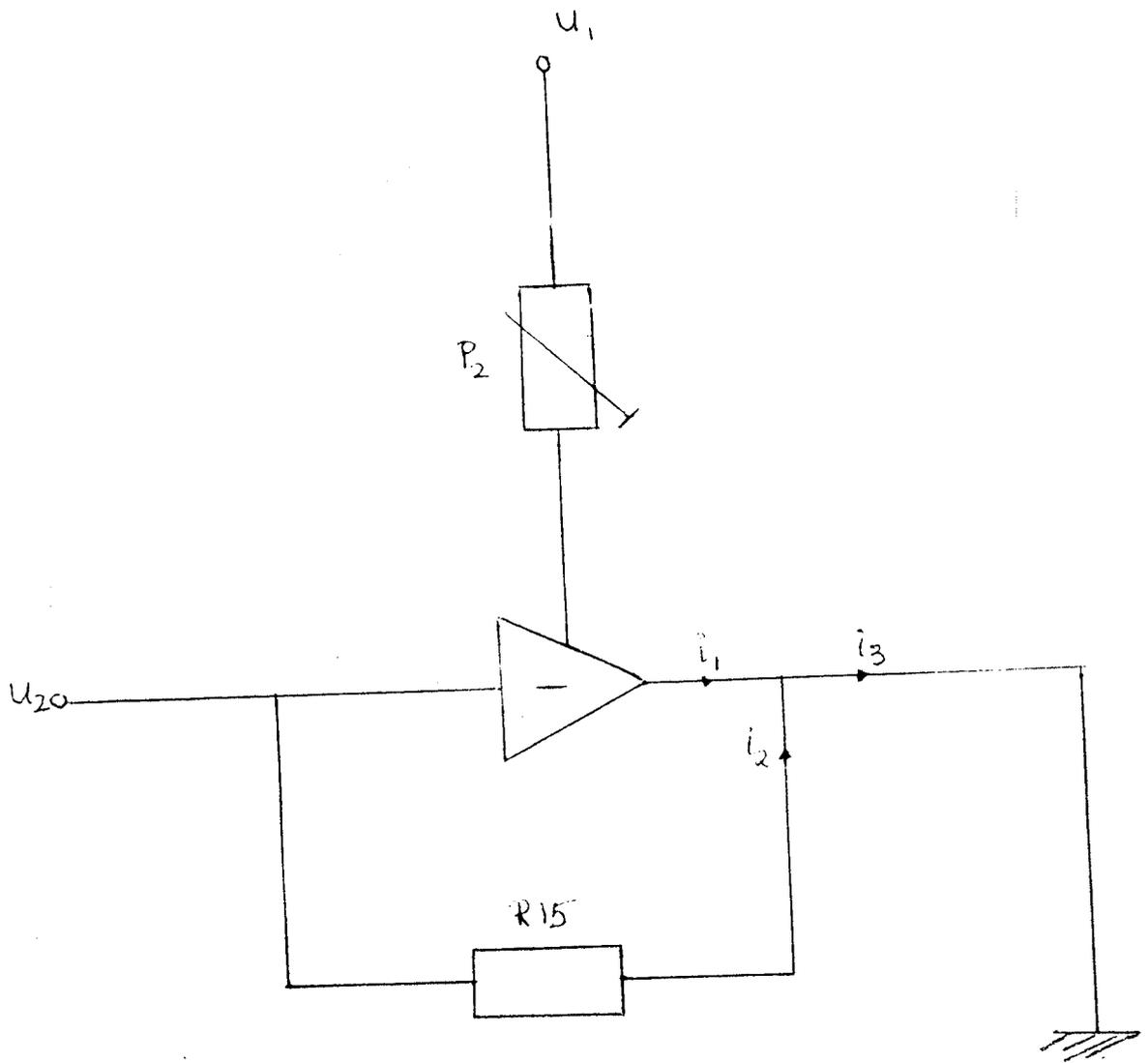


FIG 3.1. EQUIVALENT CIRCUIT DIAGRAM OF AN OTA CONFIGURED AS A 4 QUADRANT MULTIPLIER

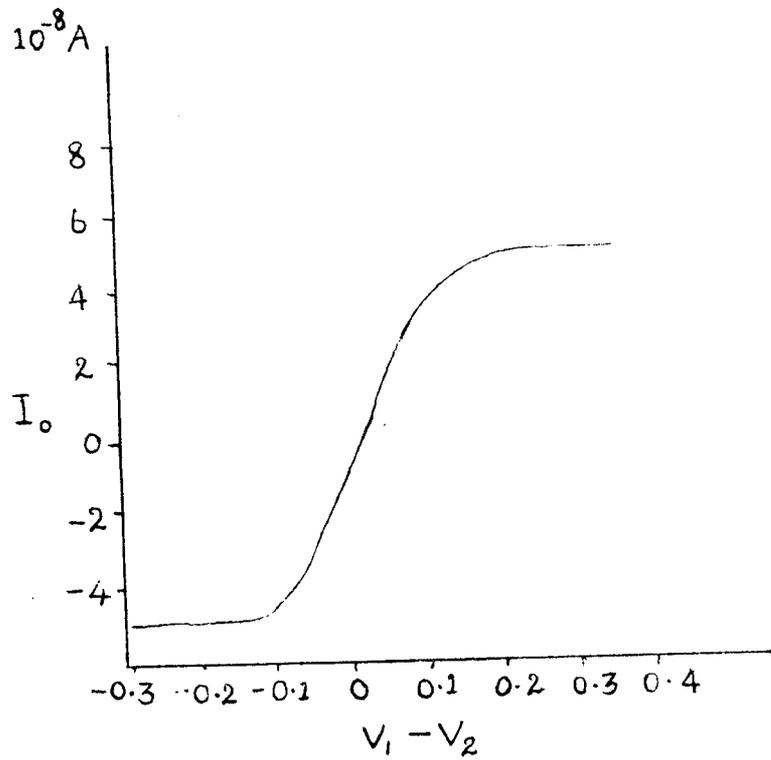


FIG: 3.2 TRANSFER CHARACTERISTICS OF OTA

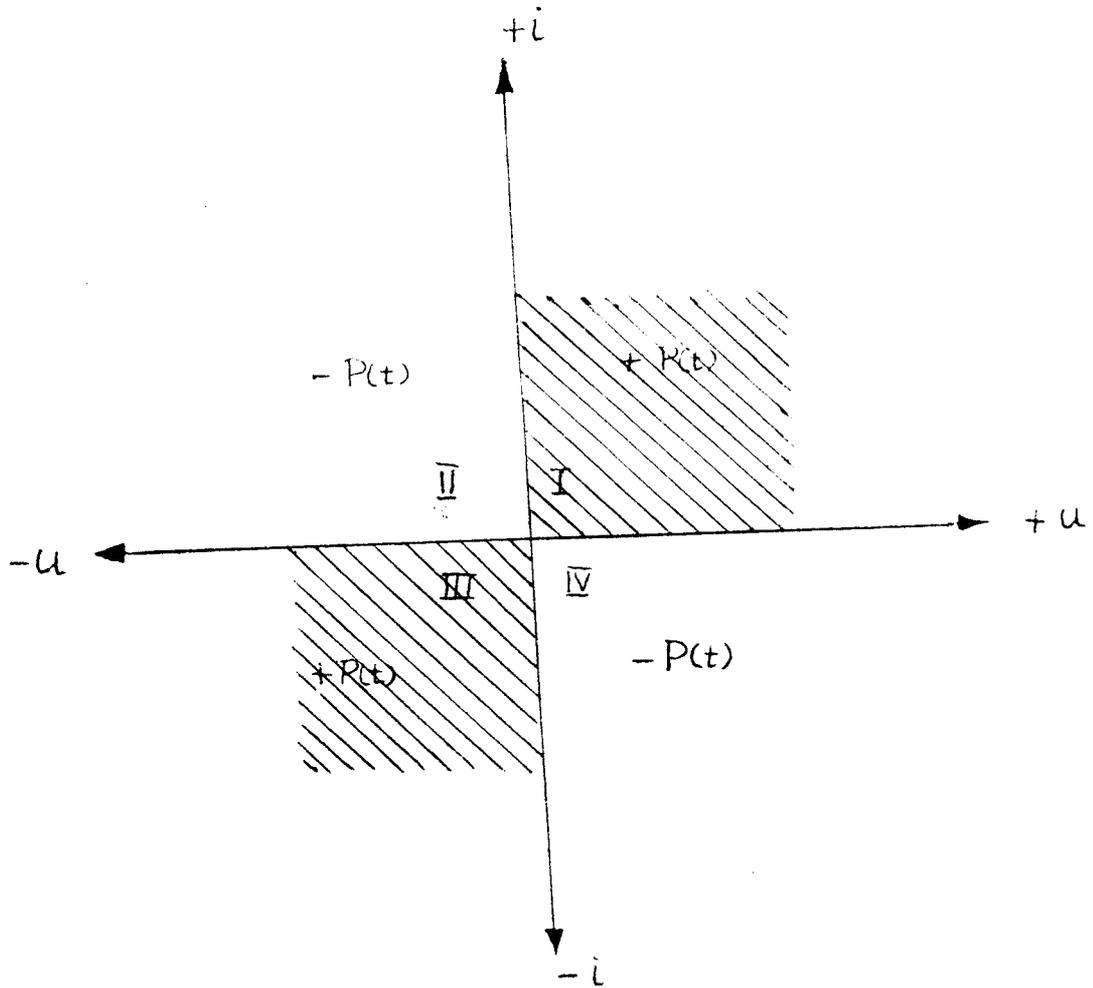


FIG 3-3: FOUR QUADRANT OPERATION

CHAPTER-4

4.1 VOLTAGE CONTROLLED OSCILLATOR

VCO is a free running multivibrator and operates at a set frequency so called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage V_c , to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator" or in short VCO.

The circuit diagram of VCO is shown in fig 4.1. The VCO consists of an OTA[A6] and operational Amplifier[A4] which is connected as a comparator with hysteresis. Dependent on the power consumed, the OTA is fed with a certain drive current. and arranges, in combination with the comparator for the successive charging and discharging of capacitor C1. The output of the comparator therefore consists of a square wave of which the frequency is dependent upon the measured power.

Transistor T1 provides the OTA with drive current. The current from T1 also charges as capacitor C1 in a time which is again dependent upon the measured power. The resulting voltage level across C1 is applied to the input of comparator A4 Via the buffer stage contained in the OTA stage. If this voltage exceeds the upper threshold, the output of the comparator goes negative. At the same instant, the input current (pin 13) of the OTA also

becomes negative, which causes C1 to discharge at a speed, which is dependent upon the drive current at pin 1. In this way the VCO provides a square wave at its output of which the frequency is directly proportional to its drive current that is the measured power. The hysteresis of the comparator and consequently the frequency of VCO can be adjusted by means of potentiometer P4.

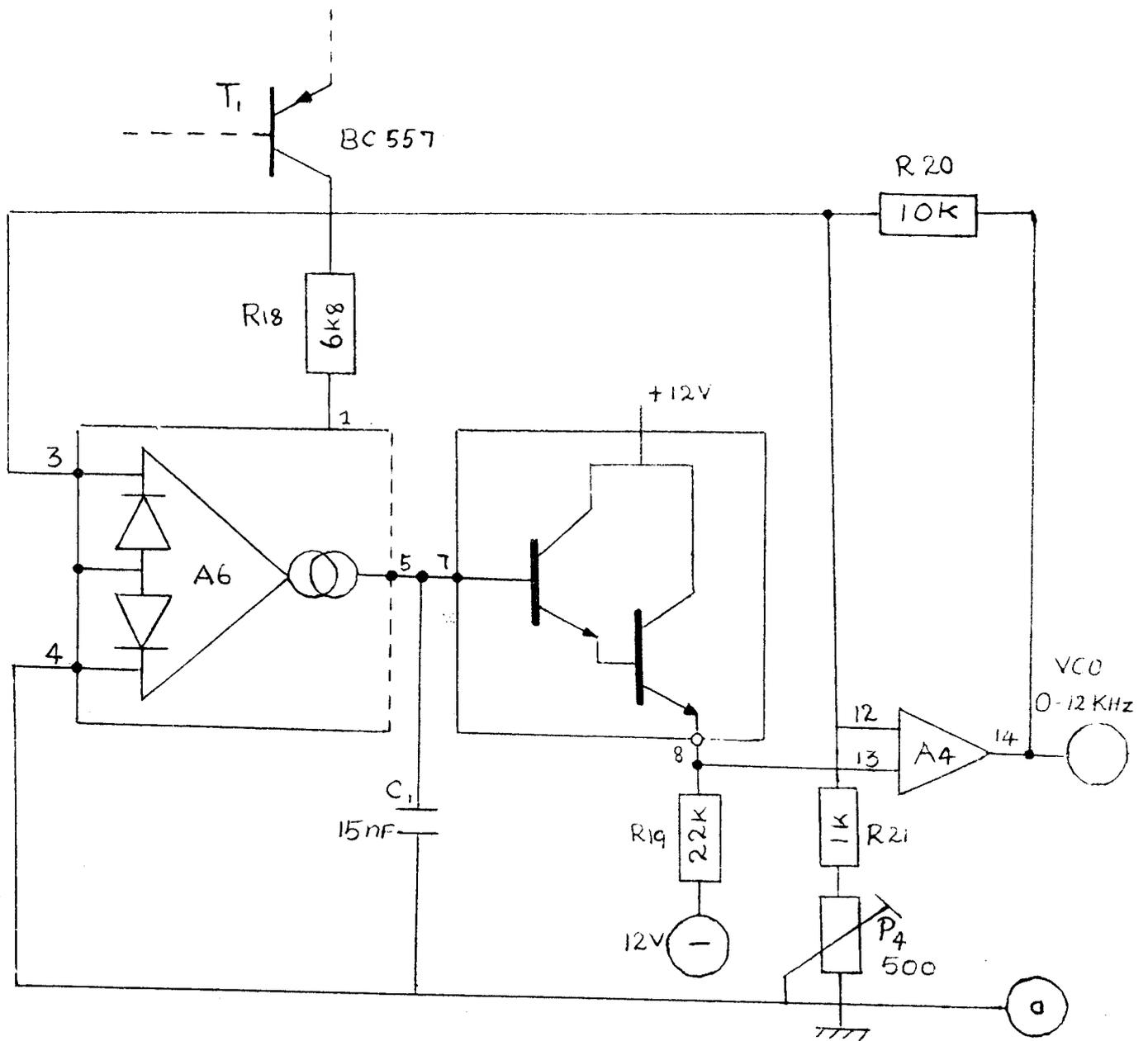


FIG 4-1 VOLTAGE CONTROLLED OSCILLATOR

CHAPTER-5

POWER SUPPLY

For the operation of the circuit, +5v regulated power supply is for energy meter and +12V, -12V for watt meter. The circuit diagram for the +5V, +12V and -12V is as shown in fig 5.1.

To get the power supply +5V, +12V and -12V, a step down transformer of rating 230/ 15-0-15V is used for rectification. the centre tapped secondary of transformer output is applied to the full wave bridge rectifier. The ripple content in the output of rectifier is filtered by capacitors C1 and C2. The regulated output is obtained by using the regulator, IC's IC1 and IC2. The bridge rectifier gives two output voltages with respect to the ground.

5.1 +12V POWER SUPPLY:

The filtered bridge rectifier output is given to the IC1. The IC1 78L12 (IC3 in the watt meter circuit) is a three terminal series pass positive regulator IC. The regulated output with respect to ground gives the +12V power supply (point A to ground in fig 5.1).

5.2 -12V POWER SUPPLY:

The filtered bridge rectifier output is given to the IC2. The IC2 - 79L12 (IC4 in the watt meter circuit) is a three terminal series pass negative

regulator IC. The regulated output with respect to ground gives the -12V power supply.

5.3 +5V POWER SUPPLY:

The filtered output of bridge rectifier is given to the IC3. IC3 - 7805 is a three terminal series pass voltage regulator IC. The point Q to ground in fig 5.1 gives +5V power supply.

5.4 BATTERY BACK UP SUPPLY CIRCUIT:

It is important that the display readout, which indicates the energy consumed should give the display (energy consumed) even when the main supply is failed. Otherwise the reading recorded by the instrument will be disappeared and it is not possible to know the actual energy consumed by the electrical apparatus. To overcome this, a very simple battery back up circuit is used and is as shown in fig 5.1, between the points Q & R. Output from IC3 is +5.7V (because ground is shifted by 0.7V), then it is applied through diode D6. Now the voltage at junction Q is 5V. Four numbers of 1.5V battery is connected in series and this battery set up gives 6VDC and is applied through diodes D7 and D8. The junction Q is formed by connecting the cathodes of D6 and D7. The junction Q is the point or +5V Vcc supply.

5.5 BATTERY BACK UP OPERATION:

When the supply is present, the voltage at junction Q is +6V Vcc and because of forward biased diode D6, Diodes D7 and D8 are reverse biased. So the bridge supplies the load current.

If the mains is absent, no voltage appears at junction Q, because of the absence of bridge output. Now diodes D7 and D8 conduct because they are forward biased. The battery voltage appears at junction Q and this is 4.6V (6-1.4V). The battery supplies the load current.

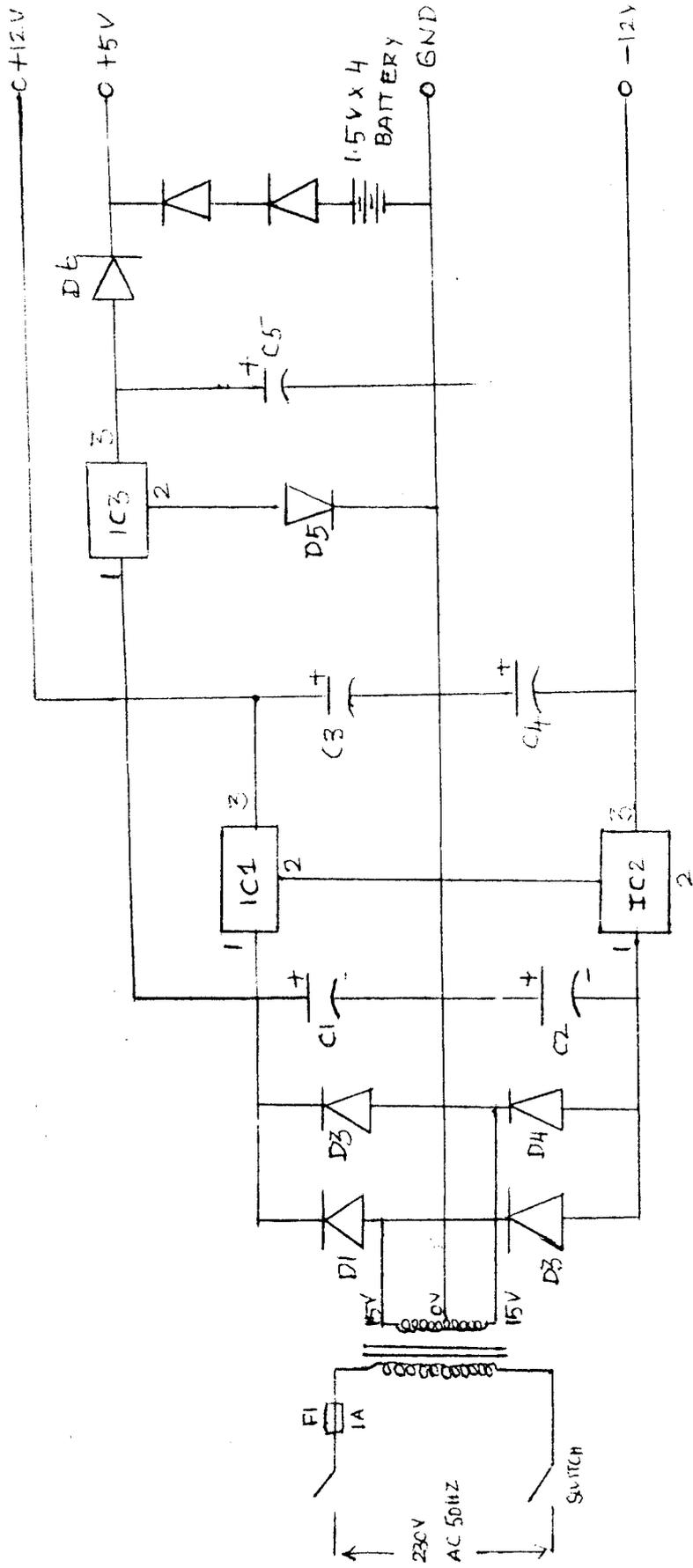


FIG. 5.1 : POWER SUPPLY CIRCUIT

$C_1, C_2 = 1000 \text{ MFD} / 25 \text{ V}$

$C_3, C_4, C_5 = 10 \text{ MFD} / 16 \text{ V}$

TRANSFORMER = 230V / 15-0-15V, 0.7A

IC₁ = 78L12

IC₂ = 79L12

D₁-D₄ = 1N4003

IC₃ = 7805

CHAPTER-6

TESTING AND CALIBERATION

The digital energy meter is fabricated and tested with sub standard meter.

The meter is connected to 230V single phase AC supply. A 40W filament is connected to the meter and the readings are observed after one hour. An error of 1.1% is noted in the readings. The readings are noted after each one hour duration for about four hours and the error is calculated. An average error of 0.9%.

Likewise a 60W bulb is connected to the meter and the readings are observed after one hour and the error is computed as 1.2% .

A 230V single phase induction motor of rating 175 W is connected to the meter and the readings are observed. The motor runs for about three hours and the readings are noted for each one hour. An average error of 1.25% is computed.

CHAPTER-7

CONCLUSION

A digital energy meter has been designed and fabricated. The digital instrument based on electric circuits has several advantages. It is compact and accurate one and draws negligibly small power for its operation. The conventional meter requires certain amount of power from the signal for its operation. All errors whether mechanical or electrical connected with conventional meters are eliminated by incorporating electronic scheme. The digital energy measuring scheme has additional advantage of numerical readout. It reduces human errors such as parallax in reading and increases the human reading speed.

This meter can measure upto 350W for higher loads, the value of R4 must be decreased. The important features of the instrument are given below.

- 1. Set and reset capability*
- 2. Static flip-flop operation retains state indefinitely with clock level either high or low.*
- 3. Medium speed operation - 10khz clock toggle rate of 10V.*
- 4. Maximum input leakage of 1mA at 15 volts*
- 5. 1V - Noise margin (full package temperature range)*
- 6. Battery back-up.*

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APPENDIX - A

IC DETAILS

A1.1ICTLO84

It is a monolithic quadruple JFET input operational amplifier. It has the following characteristics.

- 1. High Input Impedence*
- 2. Continuous short circuit current protection.*
- 3. Wide common mode and differential voltage ranges.*
- 4. No frequency compensation required.*
- 5. Low power consumption.*
- 6. Low latch up.*
- 7. Gain and phase match between amplifiers.*
- 8. Low input bias and offset currents.*

Supply Voltage, Vcc +.....18V

Supply Voltage, Vcc +..... -18V

Input Voltage +/- 15V

Continuous total dissipation at 25 C

free air temp 500 MW

Operating free air temperature0°c to 70°c

Storage temperature range -65°c to 150°c

The pin details of TL084 (JORN dual in line Package Topview) is as shown in fig A1, The connections of operational amplifiers A1-A4 in the Wattmeter circuit is available in a single TL084 IC.

A1.2 A741

It is a general purpose operational amplifier featuring offset voltage null capacitor.

The high common mode input voltage range and the absence of latch up make the amplifier ideal for voltage follower applications. The device is short circuit protected and the internal frequency compensation ensures stability without external components. A741 is characteristics for operation from 0°C to 70°C.

The pin details of MA 741 (JG or PDUAL IN package top view) is shown in fig A2.

A1.3 78 L12 and 79 L12

The ICs 78L12 and 79L12 are three terminal series pass positive and negative voltage regulators. They can be used with power pass elements to make high current voltage regulator. The output current rating is upto 100mA. The pin out details of 78L12 is shown in fig A3 and 79L12 is shown in fig A4.

The two ICs are used to give regulated +12V and -12V supply for the wattmeter circuit.

A14 4020, 14 STAGE BINARY RIPPLE COUNTER:

CD 4020 is a binary ripple counter that counts in the up direction using positive logic.

The reset input is normally held at ground. Every time the clock changes from positive to ground, the counter advances one count. The 1 output divides the input clock by $2^1 = 2$. The 4 output divides the input clock by $2^4 = 16$, upto the 14 output which divides by $2^{14} = 16384$. There are no outputs for the second and 3rd stages.

Making the reset input positive forces all outputs to ground and holds them there until the reset returns to ground. Since this is a ripple counter the output changes in sequential orders. In correct count will result in driving the settling time.

The pin details of CD 4020 is shown in fig A5. Here the 12 output divides the input clock by $2^{12} = 4096$.

A1.5 45 18 DUAL UP COUNTER:

It consists of two identical independent, internally synchronous four stage counters. The counters stages and type-D flipflops, with interchangeable clock and enable negative going transition which is required where cascading multiple stages. Each counter can be cleared by applying a high level on the reset line. It will count out of all undefined stages with in 2 clock periods. These complementary Mos up counters find primary use in multistage synchronous or ripple counting applications requiring low power dissipation and high noise immunity.

fig A6.1 shows the block diagram of SCL 45188 fig A6.2 shows that the truth table of 4518 fig A6.3 shows that the pinout details of 4518 fig A6.4 shows that the timing diagram of 4518.

Features:

Wide supply range = 3.6-15V

High noise immunity = 0.45V

Lower power TTL = Far out of 2 driving

Compatibility 741 or driving 74Ls

6MHZ counting rate at Vdd = 10V

A1.6 4013, DUAL D-FLIP-FLOP:

It has two D flip flops. Each flip flop may be used independently. There are two modes, clocked and direct. In clocked mode, the direct set and reset inputs must remain at ground. The input to the D line divider what the FF is going to do. The actual operation does not happen until the +ve edge of the clock occurs. If D is +ve clocking makes the Q output +ve and Q grounded and Q +ve.

In direct mode, a positive set input forces Q positive and Q to ground. A positive reset input forces Q to ground and Q to positive. Should both set and reset by simultaneously. Positive both Q and Q will also go positive. This is unusually a disallowed state. The last direct input to go to ground will determine the final state of the Q and Q outputs the direct inputs override the clocked inputs.

Each flip flop may be made to binary divide by cross coupling the Q output to the D input. fig A7 the pin details of 4013

1.7.4 DIGIT COUNTERS WITH MULTIPLEXED 7 SEGMENT

OUTPUT DRIVERS (MM 74926)

GENERAL DESCRIPTION:

These CMOS counters of a 4 digit counters, an internal output latch. NPN output sourcing drivers for a 7 segment display, and an internal multiplexing circuitry with four multiplexing outputs. The multiplexing circuit has its own free running oscillators and requires no external clock. The counters advance on negative edge of the clock. A high signal on RESET input will reset the counter to zero, and reset the carry out low. A low signal on the Latch-Enable-Input will latch the number in the counters into the internal output latches. A high signal on the display select input will select the number in the counter to be displayed, a low level signal on the display select will select the number in the output latch to be displayed.

The MM 74C926 is like the MM74925 except that it has a display select and carry out used for cascading counters. The carry out signal goes high at 6000, goes back low at 0000. The pin diagram and logic block diagram are as shown in fig A8.

FEATURES:

- * Wide supply voltage range 3V to 6V*
- * Guaranteed noise margin 1V*
- * High noise immunity 0.4Vcc (typical)*

* High segment sourcing current 40mA

a) $V_{cc} - 1.6 V$ $V_{cc} = 5V$

* Internal multiplexing circuitary.

FUNCTIONAL DESCRIPTION:

Reset - Asynchronous, active high.

Display select - High, displays output of counters

Low, displays output of latch

Latch enable - High flow through condition low, latch condition.

Clock - Negative edge sensitive

Segment output - Current sourcing with 1 mA a) $V_{out} = V_{cc} - 1.6V$ typical.

Also sink capability = 2LTTL loads.

Digital output - Current sourcing with 1mA a) $V_{out} = 1.75V$. Also, sink capability = 2LTTL loads.

Carry out - 2LTTL loads. See carry-out waveforms.

A 1.8 BCD TO SEVEN SEGMENT DECODERS

BCD to 7 segment decoder and driver is a counter which converts the four BCD outputs of the digital counter into seven binary output. This output will be connected to 7 segment display. The decoder circuit conversion of the BCD output to 7 segment display common cathode type (LIS 543) are a,b,c,d,e,f,g

TRUTH TABLE:

Decimal Number	q4	q3	q2	q1	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	1	1	0	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	0	0	1	1

A1.9 LTS 543 SEGMENT LED DISPLAY

The 7 segment LED display (LTS 543) used here is of common cathode type, ie., the cathode of all 7 segment LED's are connected as a,b,c,d,e,f,g. The usual type of LED is of common anode variety requiring 20mA (0.3 inch display size) per segment for full brightness. As the forward drop is 1.7 V only a current limiting resistance of 1500hm is first connected in series with each anode. When only one of the anodes is grounded through the current limiting resistance a current of about 20mA flows in the corresponding PN junction and causes the LED segment to glow.

Fig A10 shows the details of LTS 543. A circuit to transform the BCD output from the counter to 7 segment is required and the truth table for this requirement is given below.

TRUTH TABLE

Q_D	Q_C	Q_B	Q_A	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	0	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	1	0	0	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	0	0	1	1

A 1.10 7805 VOLTAGE REGULATOR +5V

This is a 5V, 750mA voltage regulator IC. It must have a heat sink for high currents. The minimum applied supply voltage must be more than 7 V. The maximum applied voltage at a ripple peak and high line voltage must be less than 12V.

Stand by current drain = 5mA

Fig A9 shows the pinout details of 7805

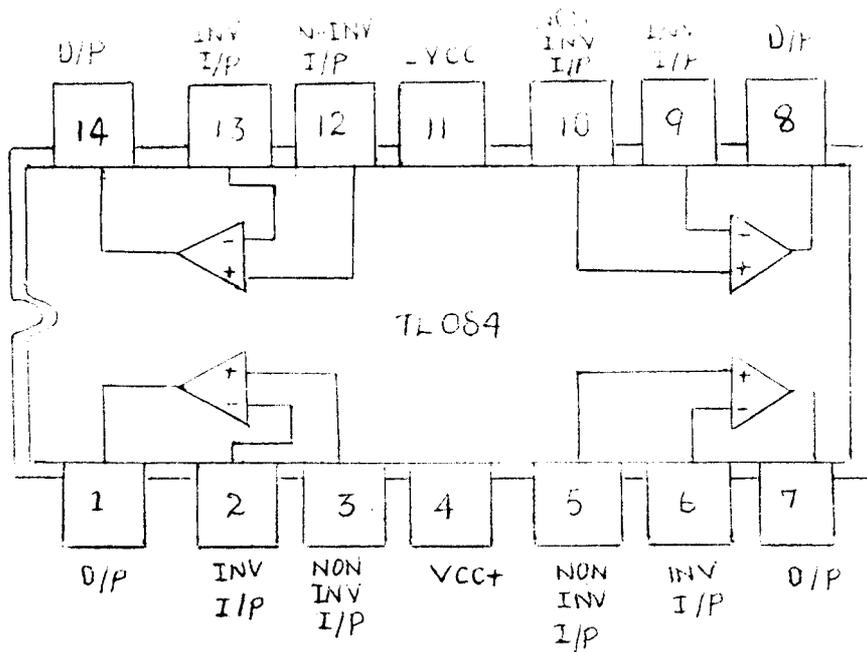


FIG: A1. TL084 QUADRUPLE JFET INPUT OPERATIONAL AMPLIFIER

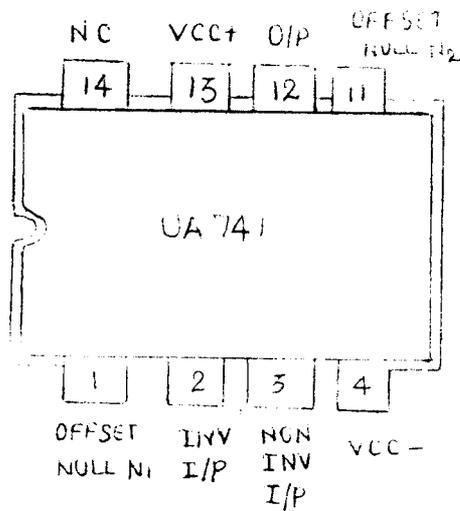
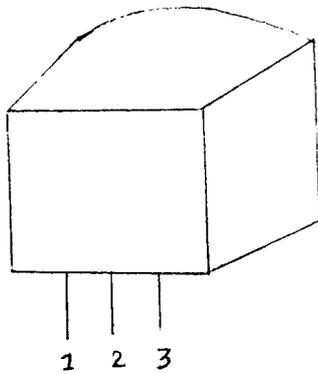
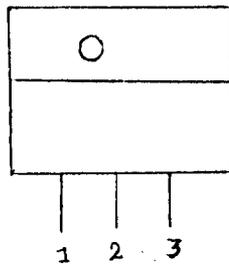


FIG: A2. PIN CONFIGURATION OF UA741 OPERATIONAL AMPLIFIER JG OR P DUAL IN PACKAGE (TOP VIEW)



- 1 - OUTPUT
- 2 - GROUND
- 3 - INPUT

FIG. A₃: PINOUT OF 78L12 - 3 TERMINAL POSITIVE VOLTAGE REGULATOR



- 1 - GROUND
- 2 - INPUT
- 3 - OUTPUT

FIG. A₄: PINOUT OF 79L12 - 3 TERMINAL NEGATIVE VOLTAGE REGULATOR

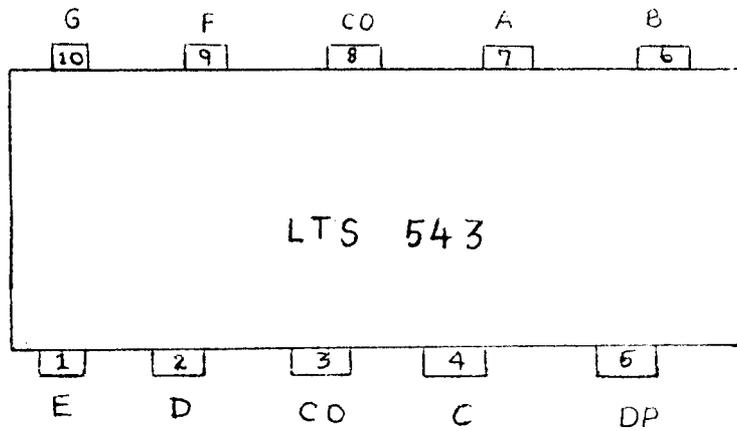


FIG. A₁₀: LTS 543 DISPLAY

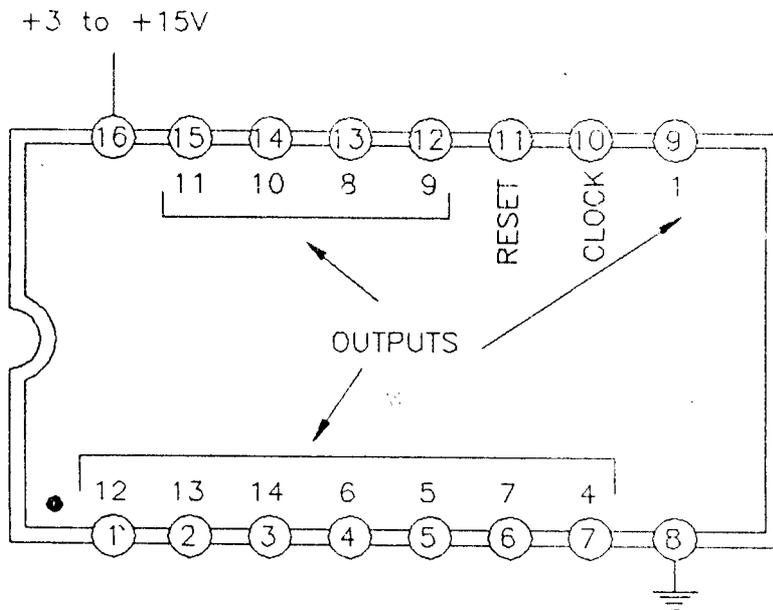
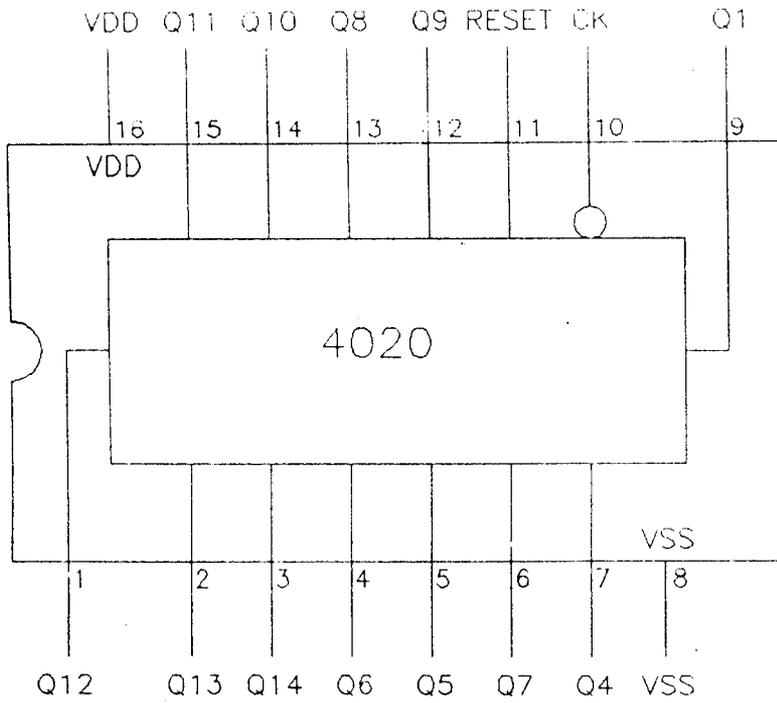


Fig A5 4020, 14 STAGE ($\div 16.384$)
BINARY RIPPLE COUNTER

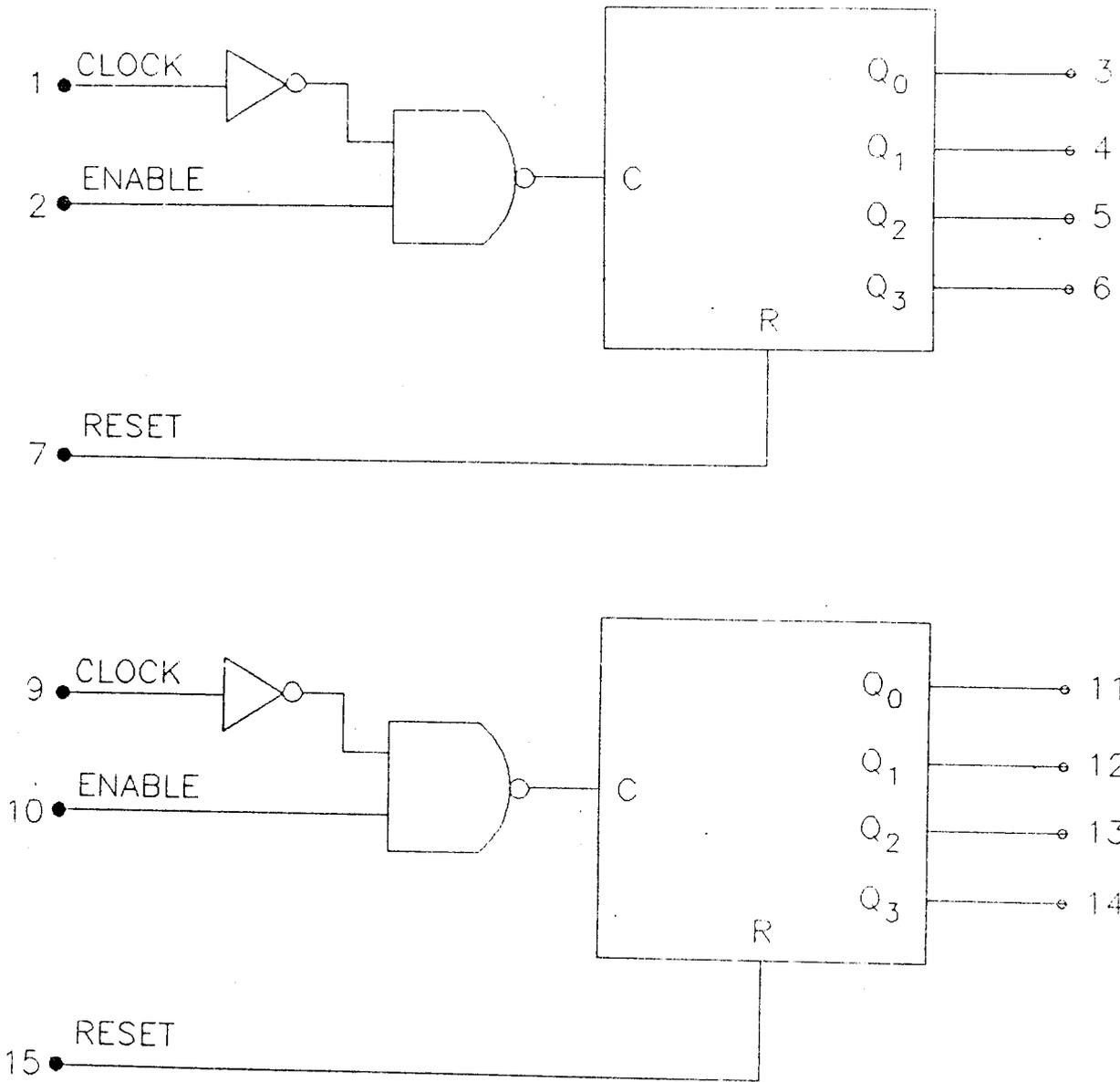


Fig A6.1 Block diagram of 4518 Dual up counter

CLOCK	ENABLE	RESET	ACTION
	0	0	Increment Counter
0		0	Increment Counter
	X	0	No Change
X		0	No Change
	0	0	No Change
1	0	0	No Change
X	X	1	Q ₀ through Q ₃ = 0

Fig A6.2 Truth table of 4518
Dual up counter

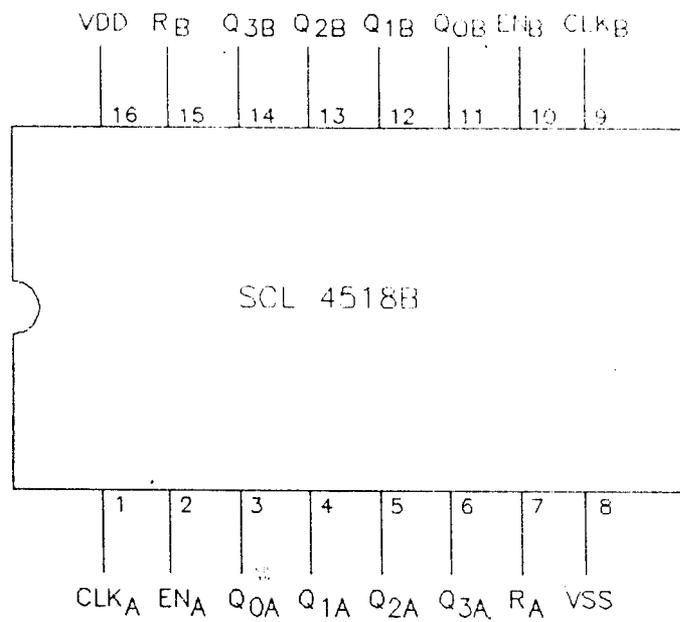


Fig A6.3 4518, Dual up counter

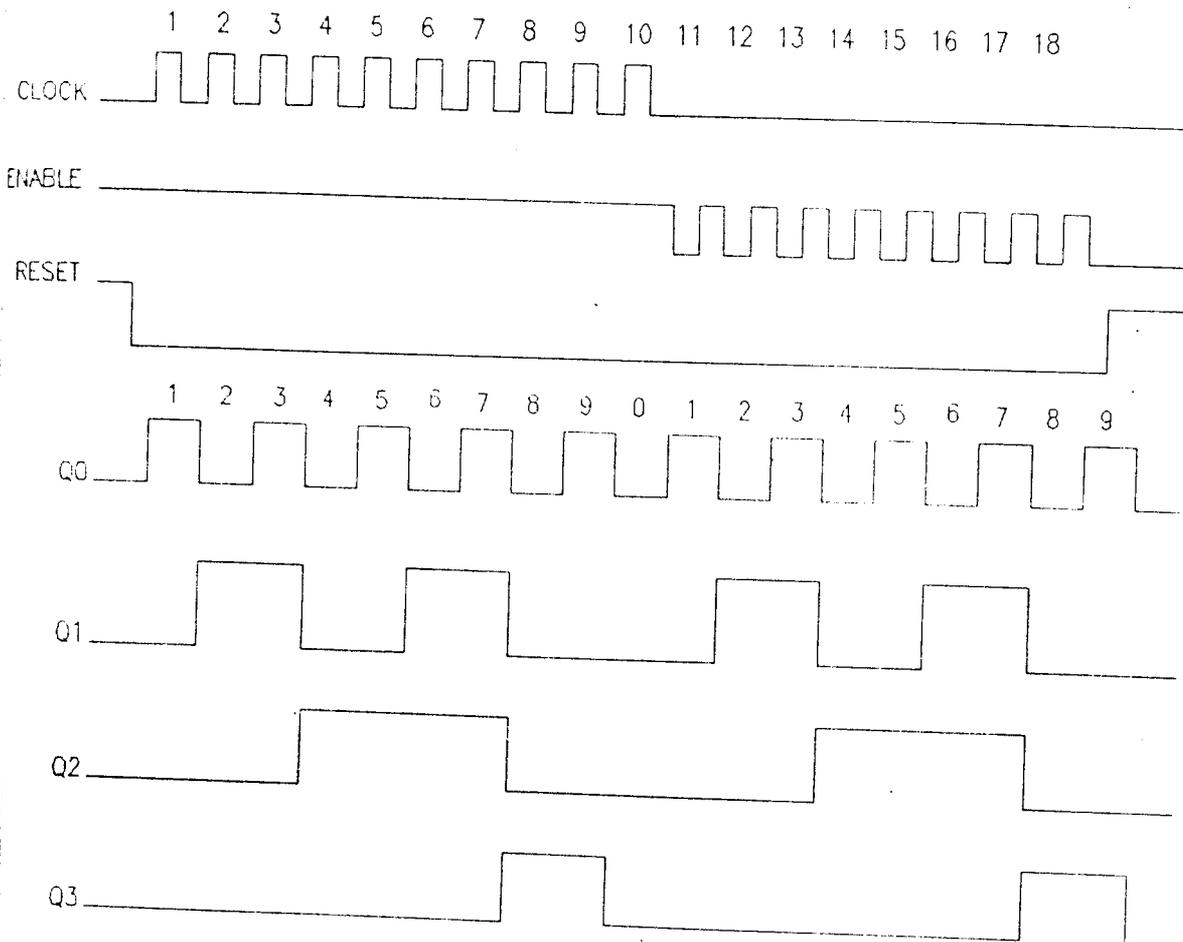


Fig A6.4 Timing Diagram of 4518

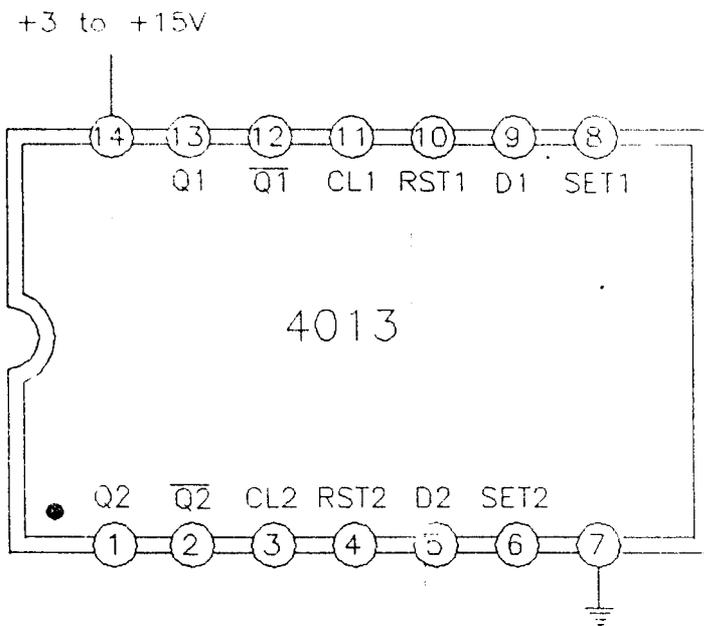
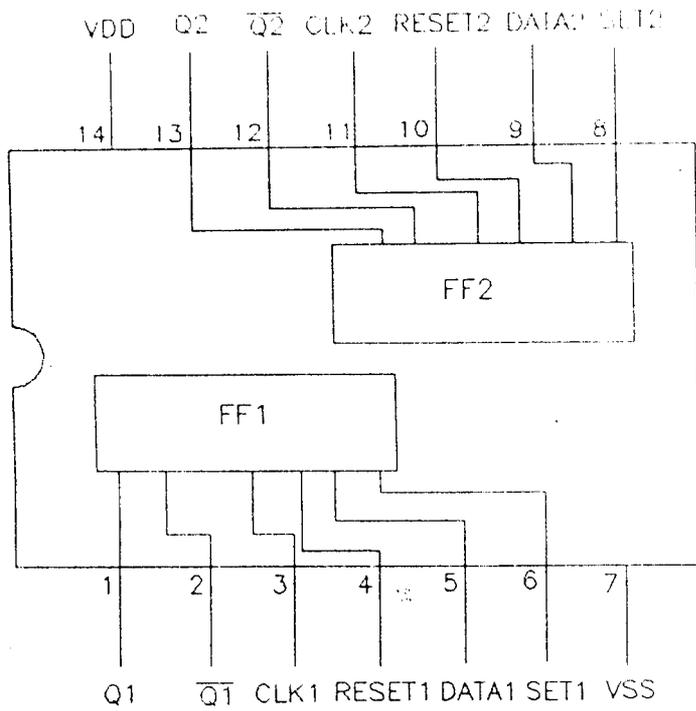


Fig A7 4013, Dual Flip Flop

