Microprocessor Based Yarn Length Controlling System

PROJECT REPORT

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CERTIFICATE

This is to certify that the Project entitled

MICROPROCESSOR BASED YARN LENGTH CONTROLLING SYSTEM

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TO WHOMSOEVER IT MAY CONCERN

This is to certify that the following final year B.E. (E.E.E) students of Kumaraguru College of Technology , Coimbatore have carried out a project work in our organisation from 01-12-1997 to 01-04-1998.

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2 . Mr. RAMESH BABU . J

3 . Mr. SAKTHIVEL . P

4 . Mr. SARAVANAN . N

The title of the Project was " **MICROPROCESSOR BASED YARN LENGTH CONTROLLING SYSTEM".**

During this period , their attendance and conduct were found to be good.

We wish them the very best for a bright future.

Place : Samichetti Palayam
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SYNOPSIS

"TIME AND TIDE WAIT$ FOR NONE". As per the saying, man has conquered everything in the world except time. This project aims to reduce the time involved in the yarn winding process by means of developing a microprocessor based yarn length controlling system.

Till today, no systematic attempt has been made to control the length variation in the winding process of cone winding machines. In the existing method, the length of yarn is controlled by the operator by controlling the diameter of cone and also by weighing each individual cone for obtaining the required weight.

This method yields only approximate length and errors are inevitable. The resulting yarn packages are not uniform in length and it causes more yarn wastage, more machine stoppages, increased cost and decreases the efficiency. Considerable time and cost is saved, if the yarn packages are of equal length.

The project aims at developing a measuring system which includes a microprocessor based controlling unit, sensor unit, cone lifter unit and a monitoring unit which are fitted on a cone winding machine and it is programmed to measure the desired yarn length.

A microprocessor and a programmable counter timer circuit is designed to count exactly the running time of the cone, deleting the knotting time and the time wasted when the cone is idle.

The PCB used incorporates the microprocessor and the necessary peripherals including programmable counter timer. The software caters to our necessities like activating the timer and data manipulation.

CONTENTS

CHAPTER – 1

INTRODUCTION

Cone winding machine is used for winding the yarn on the paper cone. This manually operated machine cannot be used to wind the yarn for a desired length accurately. So, we include a microprocessor based controlling unit with this machine for winding the yarn of a desired length accurately. This microprocessor based yarn length measuring system consists a Microprocessor with keyboard and 7-segment display unit, sensor unit, programmable counter timer, cone lifter and monitoring unit.

Rate of winding on a cone is constant because motor used to wind the yarn will rotate at a constant speed. Therefore, time taken to wind a particular length of yarn is constant, under continuous winding conditions sometimes, interruption to winding occurs due to yarn breakage and running out of the cop, which is being sensed by placing a sensor at shaft of motor to give continuous pulse according to the speed of motor, another sensor is also placed in the passage of yarn, which sends high pulses for continuous yarn passage and low pulse for discontinuous yarn flow between paper cone and cop.

These two pulses are given to an AND gate which produces a pulse when both its inputs go high. This pulse from the AND gate is being counted by a programmable counter timer.

When counter content equals the pre-set Microprocessor count value that corresponds to the desired length, the doff signal is produced and the cone lifter will be actuated. The feeler mechanism lifts the paper cone from the motor shaft.

The pre-set count value will be calculated by Microprocessor using the input length in metres and number of pulses per metre that is given by user using a keyboard. The block diagram representation of "Microprocessor based yarn length controlling system" is given by Figure1.1.

1.1. SIGNIFICANCE OF WINDING:

Weaving which is the final stage in the conversion of fibre to fabric interlaces two sets of yarn, viz., warp and weft. Of these, the warp yarns run longitudinally in the fabric and have to withstand repeated stresses and strains during weaving. The basic aim of warp preparation is therefore to improve the weavability of warp yarns, ie., to improve strength and abrasion resistance of warp yarns.

Warp winding comes first in the sequence of warp preparation and produces wound packages like cones. It serves as a "supply station" for various processes including knitting, dyeing and warping and has therefore to cater to a variety of demands in terms of wound package characteristics.

The main objectives of warp winding are:

- to produce bigger and compactly wound packages.
- to eliminate objectionable yarn faults, and
- to produce suitable wound packages for package dyeing.

The ring bobbins supplied from the spinning department weigh anywhere between 25 and 100 gm depending upon the bobbin size. Such as a small yarn content of the ring bobbins leads to increased creeling frequency and high loss in production in subsequent processes. It is therefore always desired to wind packages weigh far more than ring bobbins (about 1 – 1.5 kg.) and contain longer lengths of yarn.

Warp winding is the only process in warp preparation which handles the yarn individually. Therefore, it is the only stage to eliminate yarn faults easily. Elimination of objectionable yarn faults or what is known as "Yarn Clearing" has therefore received utmost importance in warp winding.

The dye packages should have low and uniform density throughout the package. It is also the object of warp winding to produce suitable wound packages for dyeing as the normal compactly wound packages are found unsuitable for this purpose because, hardness of the package edges and density variations with in the package.

1.2. EXISTING MACHINE:

The process of winding the yarn in textile industries today employs a machine called cone winding machine which is described below:

It contains a motor which is used to carry the drums and the drums are used for guiding the yarn which is from the cop. Drum has slots with various depth that is used for winding the yarn uniformly over the cone.

The feeler mechanism is used to lift the paper cone from the shaft of the motor when yarn is being cut. Motor is always rotating at a constant speed. But for various count of yarn, winding rate will be varying that will be provided by connecting various pulleys to the shaft of the motor and machine. Figure 1.2. shows the cone winding machine.

1.3. WINDING PROCESS:

This process accumulates the yarn over a paper cone form more number of cop.

The yarn is taken from the cop and it is wounded over the cone through the drum. After the cone package reaches a considerable size, it will be weighted then, that will be compared to a predetermined weight. If it is nearer to the predetermined weight, then it will be packed, otherwise the winding process will continue.

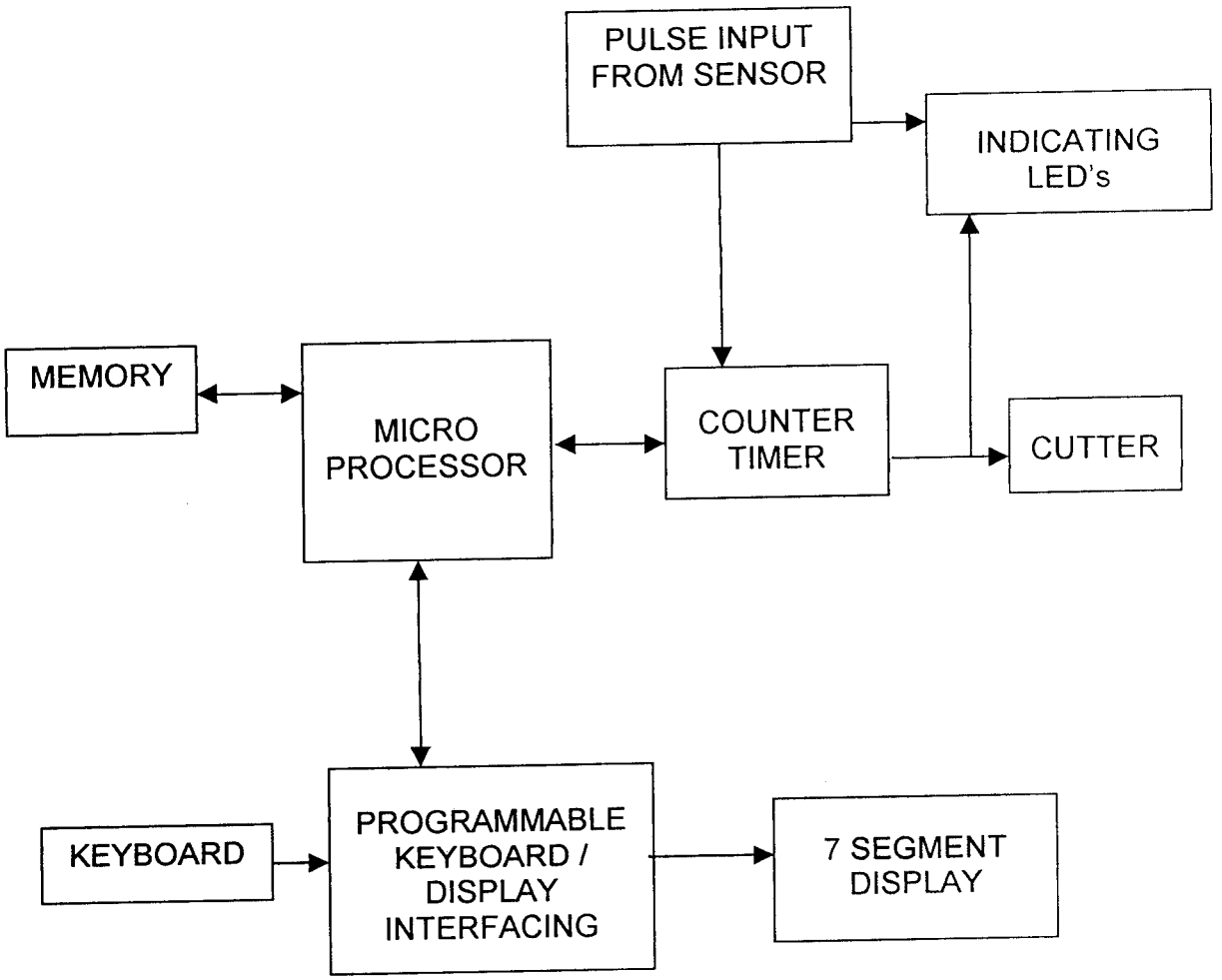


FIG.1.1 BLOCK DIAGRAM OF MICROPROCESSOR BASED YARN LENGTH CONTROLLING SYSTEM.

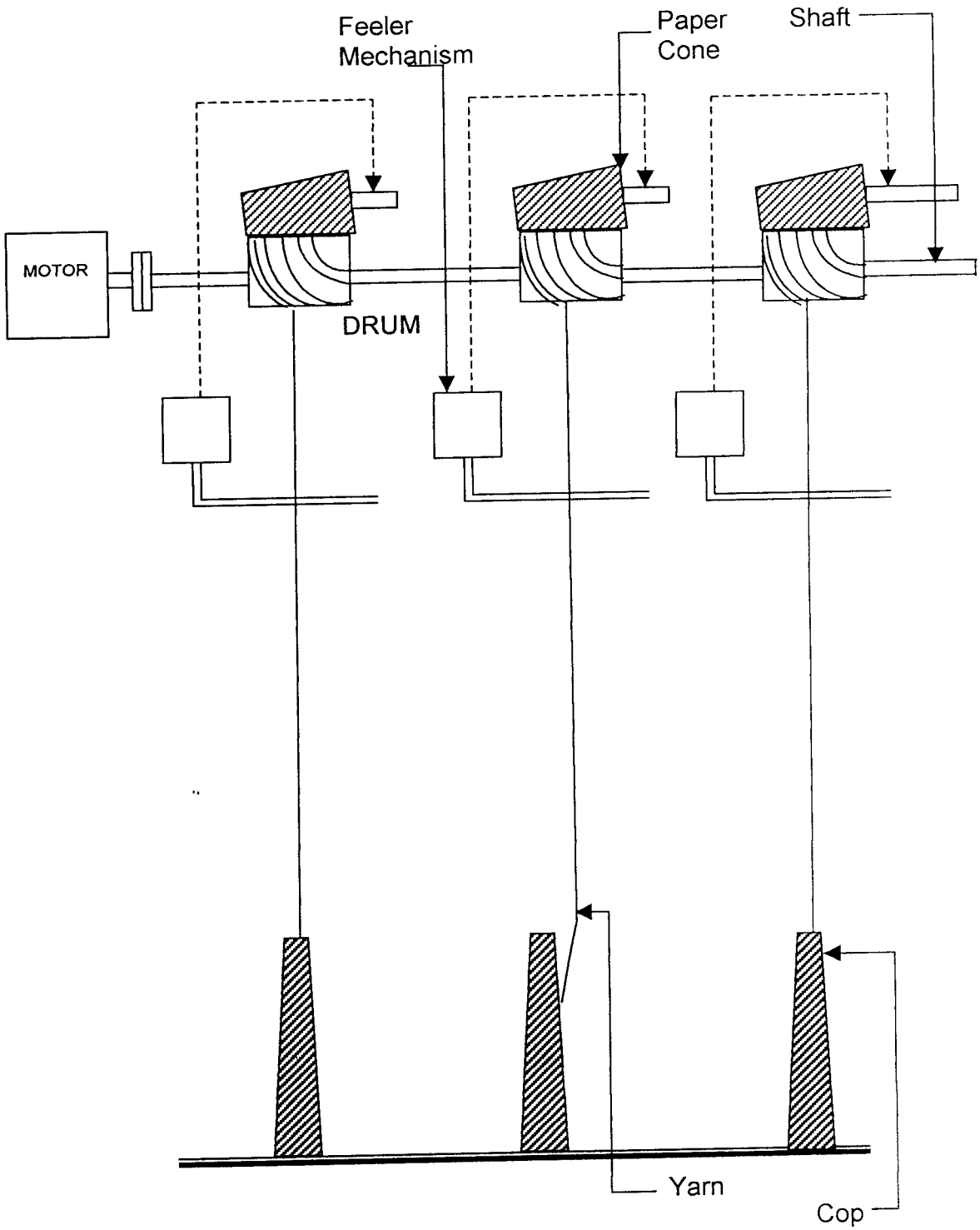


FIG..1.2. CONE WINDING MACHINE

CHAPTER – 2

HARDWARE DETAILS

A cone winding machine with a Microprocessor based length controlling system named as "SEMI-AUTO CONER" which consist of two main parts:

- Accessories to the cone winding machine
- Microprocessor based system.

2.1. ACCESSORIES TO THE CONE WINDING MACHINE.

Additional arrangements are made to measure the speed of motor and also for detection of yarn breakage, cop run out and idleness of yarn using the Inductive proximity sensor and optical sensor respectively. Figure 2.1 shows the Cone Winding Machine with accessories.

2.1.1. Inductive Proximity Sensor:

This sensor is primarily used to find the rate of winding of yarn by the motor.

Inductive proximity sensors are non-contact, solid sate switching devices. They give a control signal when metal is detected within their sensing range.

Operating Principle:

The basic operating principle of an inductive proximity sensor depends upon the damping of an LC oscillator circuit by the sensing of metal.

An High frequency (H.F.) Oscillator generates an alternating electro-magnetic field which radiates through the "active surface" of the proximity sensor. The oscillator output voltage is demodulated and fed via, a trigger circuit to an amplified output stage.

Introduction of an electrically or magnetically conductive material in the region of the 'active surface' will cause the oscillator to become 'damped'. As a result of this damping the oscillator output voltage reduces and at a certain level causes the trigger circuit, and hence the output, to change state. Figure 2.2 shows symbolic diagram of Inductive proximity sensor.

Advantages:

1. Totally solid state with no mechanical parts.
2. High speed switching without contact bounce.
3. Unaffected by vibration
4. Insensitive to aggressive environmental influences such as dirt and moisture.
5. Non-contact switching at low power provides, safe wear free switching function.

DC 3 wire proximity sensor is used to produce pulse according to the rotation of gear wheel which is fitted in motor shaft because it have separate connections for the supply voltage and the output.

2.1.2. Optical Sensor:

This type of sensor senses the discontinuity of yarn flow between the cop and cone.

If the yarn is oscillating in between the 2 diodes, the light wave reaching the photo diodes will be interrupted. This reduces the current flow from the photo diode which is fed as output to the non-inventing comparator. The other output lead of the comparator is maintained at uninterrupt output of photo diode.

When the yarn oscillates, the photo diode will be non-conducting and hence the full voltage is fed as output and hence the output goes high. When the yarn is ideal, the photo diodes conducts which drives the output low.

The monostable multivibration is used to maintain the oscillating output of non-inverting comparator at low or high level. Figure 2.3. shows the circuit diagram of optical sensor.

2.1.3 LIFTER:

Feeler mechanism is used to lift the cone from the rotating shaft when yarn cuts. Yarn will experience a tension when it is being wound. This tension maintains a lever at a height. If, yarn cuts lever will drop down and stop the cam shaft motion which lifts the cone.

In the similar manner, when yarn reaches the predetermined length an electromagnet is actuated which attracts the lever that, causing the lever to drop down. This ceases the rotation of cam shaft which automatically lifts the cone.

2.2, Microprocessor based System:

The purpose of this system is to execute the user's instruction thereby controlling the data transfer and all function from computed result. This system consists of

- Microprocessor.
- Program memory.
- Data memory.
- Programmable keyboard / display interfacing.
- Input / output unit.
- Programmable interval timer.
- Interfacing devices.

The 8085 is an 8 bit general purpose microprocessor capable of addressing 64K memory.

The device has 40 pins, requires +5V single power supply and can operate with 3 MHz single phase clock. The different components of the system are explained in detail in the following chapter.

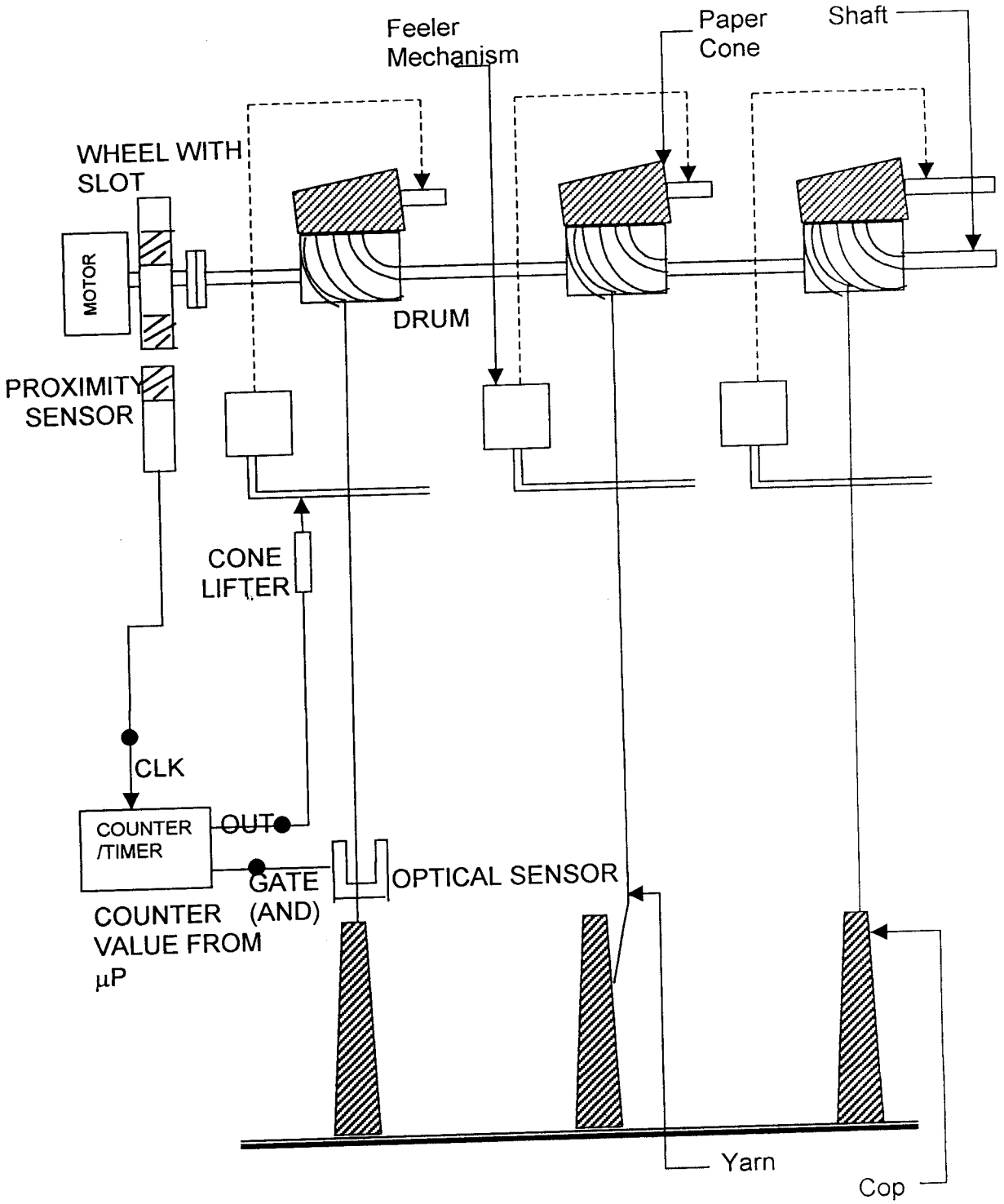
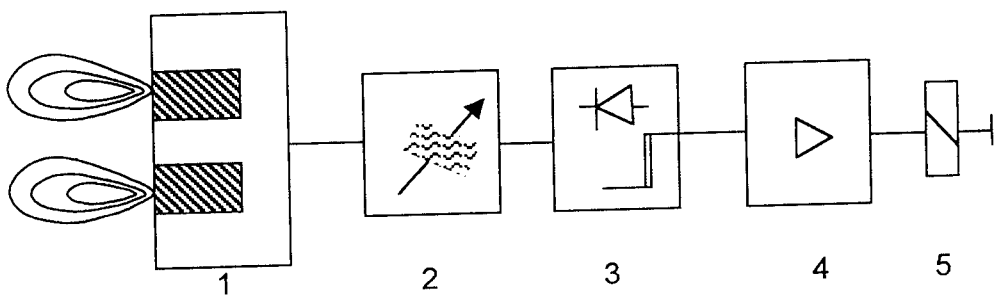


FIG. 2.1. CONE WINDING MACHINE WITH ACESSORIES



1 H.F. Alternating Electro-Magnetic Field

2 H.F. Oscillator with sensing coil

3 Demodulator Trigger Circuit

4 Output Amplifier

5 External Load.

FIG. 2.2. INDUCTIVE PROXIMITY SENSOR

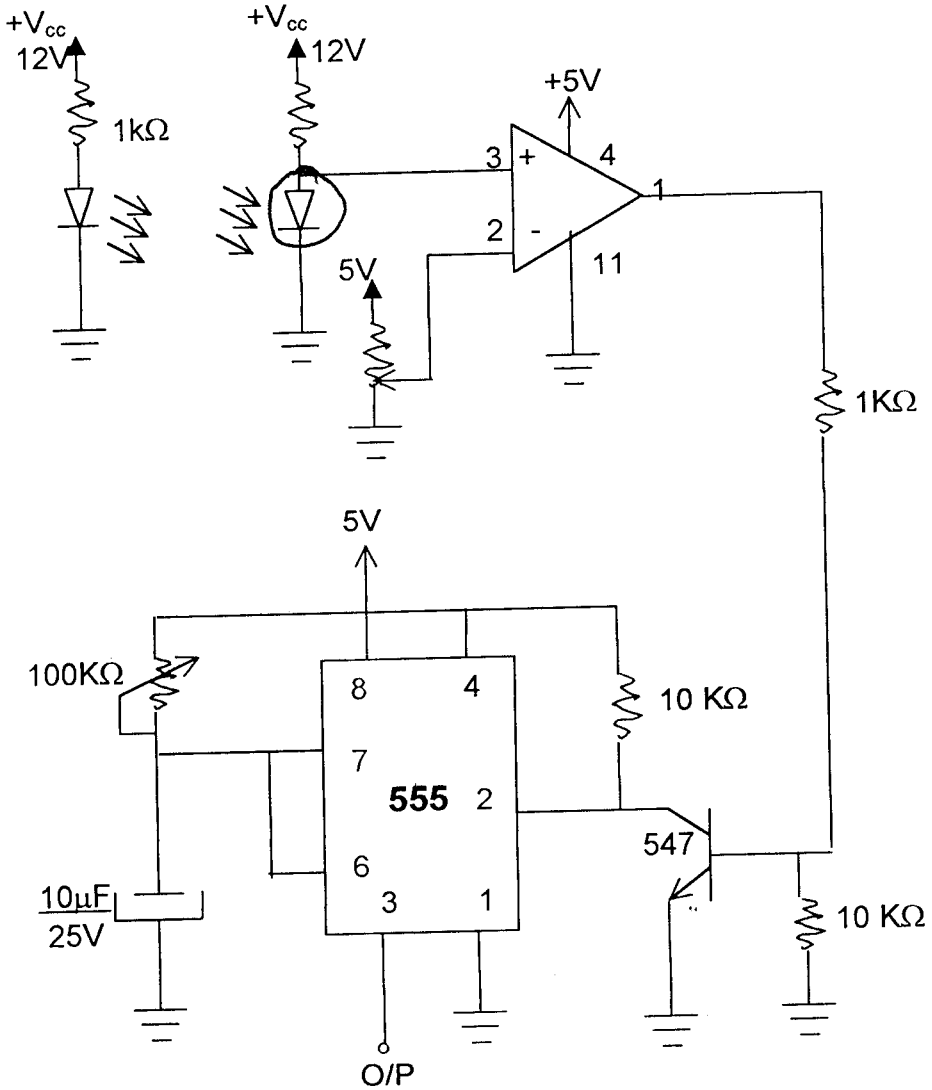


FIG. 2.3. CIRCUIT DIAGRAM OPTICAL OF SENSOR.

CHAPTER – 3

DESCRIPTION OF MICROPROCESSOR BASED SYSTEM

3.1. Microprocessor [8085]

The microprocessor is a semiconductor device consisting of electronic logic circuits manufactured by using either a large scale [LSI] or very-large-scale integration [VLSI] Technique.

It is a multipurpose, programmable logic device that reads binary instructions from a storage device called memory, accepts binary data as input and processes data according to those instructions and provides results as output.

40 pin integrated, Intel 8085 Microprocessor is used for 8 bit data manipulation and it has 16 address lines that can locate 64 KB (2^{16}) of memory. It requires a +5V single power supply, and can operate with a 3MHz single-phase clock.

The 8085 is an enhanced version of its predecessor, the 8080A; its instruction set is upward – compatible with that of the 8080A, means that 8085 instruction set includes all the 8080A instructions plus some

additional ones. programs written for 8080A will be executed by the 8085, but the 8085 and 8080A are not compatible. Figure 3.1. shows the logic pin out of the 8085 Microprocessor.

* All the signals can be classified into six groups.

  - Address bus
  - Data bus
  - Control and status signals
  - Power Supply and frequency signals.
  - Externally initiated signals and
  - Serial I/O ports.

3.1.1. Address Bus:

The 8085 has eight signal lines, A15 – A8, which are unidirectional and used as the high order address bus. Multiplexed Address / Data Bus (AD0 – AD7) will act as a low order address lines (A0 – A7) when Address latch enable (ALE) is high signal.

3.1.2. Data Bus:

Multiplexed address / data bus AD0 – AD7 will act as data bus (D0–D7) when address latch enable (ALE) is low signal.

3.1.3. Control and Status signal:

This group of signals includes two control signals RD and WR, three status signals IO/M, S1, and S0 to identify the nature of the operation, and one special signal ALE to indicate the beginning of the operation.

3.1.4. Power supply and clock frequency:

These signals are

V_{cc}	:	+5volt power supply
V_{ss}	:	Ground reference
X_1, X_2	:	Crystal Oscillator for 6MHz

3.1.5. Externally Initiated signals including interrupts:

The 8085 has five input interrupt signals and one output signal namely

1. INTR (input) – Interrupt request
2. INTA (output) – Interrupt Acknowledge

3. RST 7.5 (Input) - Restart Interrupt
4. RST 6.5 (Input) - Restart Interrupt
5. RST 5.5 (Input) - Restart Interrupt
6. TRAP (Input) – Non-maskable interrupt.

In addition to the interrupts, three pins – RESET, HOLD and READY – accept the externally initiated signals as inputs.

3.1.6. Serial I/O ports:

The 8085 has two signals to implement the serial transmission:

SID (serial input data) and

SOD (serial output data)

* Microprocessor can be separated as follows:

- Arithmetic / Logic unit
- Timing and control unit
- Instruction Register and Decoder
- Register Array
- Other Registers including pointer and counters.

Microprocessor will provide signals to other elements. These signals are conveyed on cables known as highways or bus. Figure 3.2 shows the functional block diagram of 8085 Microprocessor.

3.1.7. The ALU:

The arithmetic logic unit performs the computing functions; it includes

a) The Accumulator

b) The temporary register

c) The arithmetic and logic circuits and

d) Five Flags.

The temporary register is used to hold data during an arithmetic operation. The result is stored in the accumulator and the flags are set or reset according to the result of the operation. There are five flags namely. Sign Flag(s), Zero Flag (z), Auxiliary carry Flag (AC), Parity Flag (P) and Carry Flag (CY)

3.1.8. Timing and Control Unit:

This unit synchronizes all the Microprocessor operations with the clock and generates the control signals are similar to a synchronous pulse in an oscilloscope. The RD and WR signals are synchronous pulses indicating the availability of data on the data bus.

3.1.9. Instruction register and decodes:

The instruction register and decoder are part of the ALU. When an instruction is fetched from memory, it is loaded in the instruction register. The decoder decodes the instruction and establishes the sequence of events of follow. The instruction register is not programmable and cannot be accessed through any instruction.

3.1.10. Register Array:

The 8085 has six general purpose registers to store 8-bit data during a program execution. These registers are named as B, C, D, E, H and L and they can be combined as register pairs – BC, DE and HL to perform some 16 bit operations. Two additional registers W and Z are included in register array.

3.1.11. Other Registers including pointers and counters:

(i) Accumulator (A):

The accumulator is an 8 bit register that is part of the arithmetic unit (ALU). This register is used to store 8 bit data and to perform arithmetic

and logical operations. The result of an operation is stored in the accumulator. The accumulator is also identified and as register A.

(ii) Program Counter (PC):

This 16-bit register is used to sequence the execution of instructions. This register is a memory pointer. Memory locations have 16 – bit address, and that is why this is a 16-bit register. The function of the program counter is to point to the memory address from which the next byte is to be fetched. When a byte is being fetched, the program counter is incremented by one to point to the next memory location.

(iii) Stack pointer (SP):

The stack pointer is a 16 bit register used as a memory pointer to point the starting address of the stack. The stack can be described as a set of memory locations in R/W memory, specified by a programmer in a main program. These memory locations are used to store binary information temporarily during the execution of program.

3.2. Program Memory:

Read only memory (ROM) is used to store programs that do not want alterations. That is once all the faults have been removed from a program. The instruction will probably not need any change. It is unnecessary to hold it in read / write memory (RAM), because it is a volatile memory. So it needs supply to hold the data but ROM is a non-volatile memory. It is simple and also safer than RAM.

The programmable ROM (PROM) on the other hand allow user to do their own field programming of their control memory and a part of the main memory which keeps the monitor program of a single board microcomputer.

A type of ROM known as Erasable PROM (EPROM) allows the user change its contents which can be held for years of routine operation. EPROMS are loaded by PROM Programmer and erased by Ultraviolet light in a safety case. As from above, we refer EPROM as program memory.

3.3. Data memory:

The read/write memory (R/W M) (or) Random Access Memory (RAM) is also known as user memory or data memory. It is used to store user programs and data. In single board microcomputers, the monitor program monitors the Hex keys and stores those instructions and data in the RAM only.

Before, store in to the EPROM we enter all the programs in RAM only because error in the program can be easily rectified in this memory. After, the all correction only program will be stored in the EPROM.

All the data including user inputs and results after the manipulation is to be stored in the RAM memory.

User program is also a data for the single ship microcomputer because it varies according to the user. RAM holds all the user data temporarily to read randomly at any time before switch offing the supply. As from above RAM is known a data memory.

3.4. Programmable Keyboard / display interfacing [8279]:

The 8279 is a hardware approach to interfacing a matrix keyboard and a multiplexed display. The software approach to interfacing a matrix keyboard and a multiplexed display of seven segment LEDs is obtained by writing program to access the input key and also the display a data which includes debounce by delay program. Software approach occupies considerable amount of time in checking the keyboard and refreshing the display.

The trade-offs between the hardware approach and the software approach are producing cost Vs. the processor time and the software development cost. Logic Symbol of 8279 is shown in Figure 3.3.

Four major sections of the 8279 are:

1. Keyboard section
2. Scan section
3. Display section
4. MPU interface section

The functions of these sections are described below:

3.4.1. Keyboard section:

This section has eight lines (RL0 – RL7) that can be connected to eight columns of a keyboard. The keys are automatically debounced, and the keyboard can operate in two modes: two key lock out or N-key rollover.

In the two-key lockout mode, if two keys are pressed almost simultaneously, only the first key is recognized. In the N-key roller mode, simultaneous keys are recognized and their codes are stored in the internal buffer; it can also be set up so that no key is recognized until only one key remains pressed.

The keyboard section also includes 8 x 8 FIFO (first-in-first-out) RAM. The FIFO RAM consists of eight registers that can store eight keyboard entries; each is then read in the order of entries. The status logic keeps tack of the number of entries and provides an IRQ (Interrupt Request) signal when the FIFO is not empty.

3.4.2. Scan Section:

The scan section has a scan counter and four scan lines (SL0 – SL3). These four scan lines can be decoded using a 4 to 16 decoder to generate 16 lines for scanning. These lines can be connected to the row of a matrix keyboard and the digit drivers of a multiplexed display.

3.4.3. Display Section:

The display section has eight output lines divided into two groups A0 – A3 and B0 – B3. These lines can be used, either as a group of eight lines or as two groups of four, in conjunction with the scan lines for a multiplexed display. The display can be blanked by using the BD line. This section includes 16 x 8 display RAM. The MPU can read from or write into any of these registers.

3.4.4. MPU Interface Section:

This section includes eight bi-directional data lines (DB0 – DB7), one interrupt request line (IRQ), and six lines for interfacing, including the buffer address line (A0).

When A0 is high, signals are interpreted as control words or status; when A0 is low signals are interpreted as data. The IRQ line goes high whenever data entries are stored in FIFO. This signal is used to interrupt the MPU to indicate the availability of data.

3.5. INPUT / OUTPUT UNIT:

Input section transfers data and instructions in binary from the outside world to the Microprocessor. Hex-keyboard is to be given input to the Microprocessor. PRI 85 AD kit keyboard consists 16 keys for hexa decimal input, six command keys including EXAM REG, delimiter group key (NEXT, PREV, EXEC) and system operation keys RESET and KBINT keys.

Output section transfer data from Microprocessor to the outside world using 6 seven segment LEDs (Light Emitting Diodes).

Four LED's starting from left is used to display the location of memory (Address) and other Two LEDs is used to display the content of that address.

3.6. PROGRAMMABLE INTERVAL TIMER [8253]:

The 8253 includes three identical 16-bit counters that can be operated independently. It is packed in a 24 pin. DIP and requires a supply +5v power supply.

To operate a counter, a 16 bit count is loaded in its register and on command, begins to decrement the count unit it reaches 0. At the end of the count, it generates a pulse that can be used to actuate the cone lifter. The counter can count the either in binary or BCD. Range of count value will be more when we use binary counter mode compare to BCD counter mode.

Figure 3.4 is the block diagram of the 8254; it includes three counters (0,1, and 2), a data bus buffer, Read / write control logic and a control register. Each counter has two input signals – clock (CLK) and GATE and one output signal – OUT.

Control register

3.6.2. CONTROL WORD REGISTER:

This register is accessed when lines A0 and A1 are at logic 1. It is used to write a command word which specifies the counter to be used, its mode, and either a read or a write operation.

The control word format as follows:

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC-Select counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command

M-Mode:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW – Read / Write:

RW1	RW0	
0	0	Counter Latch Command
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/wrote least significant byte first, then most significant byte.

BCD	
0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't care Bits (X) should be 0 to ensure compatibility with future Intel products.

As mentioned earlier, the 8254 can operate in six different modes, namely.

Mode 0 : Interrupt on terminal count

Mode 1 : Hardware – Retriggerable one-shot

Mode 2 : Rate generator

Mode 3 : Square – wave generator

Mode 4 : Software – Triggered Strobe

Mode 5 : Hardware – Triggered Strobe

In all modes other than Mode 0 counting will be from initial count value when gate being low to high.

In Mode 0 counting will be continued from the decrement value only. So we have chosen Mode 0 for our operation.

3.7 Interfacing devices:

Several types of interfacing devices are necessary to interconnect the component of a bus – oriented system. The devices used in today's microcomputer systems are designed using medium – scale integration (MSI) technology. In addition, tri-state logic devices are essential to proper functioning of bus-oriented system, in which the same bus lines are shared by several components.

3.7.1 BUFFER:

The buffer is a logic circuit that amplifier the current or power. It has one input line and ne output line. The logic level of the output is the same as that of input. The buffer is used primarily to increase the driving capacity of a logic circuit. It is also known as a driver.

We used [74LS244] tristate buffer to amplifier the high order bus lines (A7– A15).

The data bus of a microcomputer system is bidirectional, therefore, it requires a buffer that allows data to flow in both direction. Bidirection buffer 74LS245 is used for data lines (D0 – D7). It is also called as Octal bus transreceiver.

The 74LS245 includes 16 bus drivers (A1 –A8 and B1 – B8), eight for each direction, with tri-state output. The direction of date flow is controlled by the pin DIR (Direction). When DIR is high, data flow from the A bus to the B bus, when it is low, data flow from B to A.

3.7.2. DECODER:

The decoder is a logic circuit that identifies each combination of the signals present at its input. For example, if the input to a decoder has two binary lines, the decodes will have four output lines. The two lines can assume four combinations of input signals – 00, 01, 10, 11 with each combination identified by the output lines 0 to 3.

If the input is 11_2, the output line 3 will be a logic 1, and the orders will remain at logic 0. This is called decoding.

The 74LS138 is called 1 – out of – 8 binary decoders or demultiplexers. It has three input lines and eight active low output lines. It requires three enable inputs; two are active low and one is active high; all three enable lines should be activated so that the device can function as a decoder. If the 74138 is enabled ($G_2A = G_2B=0$ and $G_1 = 1$) and if the input is 101 the output Y_5 will go low, others will remain high.

3.7.3. LATCH

A latch is a D flip-flop and used commonly to interface output devices. When the MPU sends an output, data are available on the data bus for only a few microseconds: therefore, a latch is used to hold data for display.

This octal latch is used to latch 8 bit data. The device (74LS373) includes eight D latches with tristate buffers, and it reaquires two inputs signals, Enable (G) and output control (oc).

The enable is an active high signal connected to the clock input of the flip-flop. When this signal goes low, data are latched from the data bus. The output control signal is active low, and it enables the tri-state buffers to output data to display devices.

Latch (74LS373) is mainly used to demultiplex the multiplexed Address/data lines $AD_0 - AD_7$.

PRI _85 AD system hardware Specifications:

CPU : Intel 8085 with 246 instructions and 3.072 MHz maximum clock rate.

MEMORY:

PRI 85 AD has three sockets (U7, U8, U9) for accepting memory devices.

U7 and U9 are populated and U8 is not populated one. Populated devices in U7 and U9 and option for unpopulated socket are as follows.

Device with socket No.	Address range	Type with capacity
27128 at U7	0000 – 3FFF	16 K EPROM
62256 at U9	8000 – FFFF	32 K RAM
2764 at U8	4000 – 5FFF (or) (6000 – 7 FFF)	8K EPROM
6264 at U8	4000 – 5FFF (or) 6000 – 7FFF	8 K EPROM
27128 AT V8	4000 – 7FFR	16K EPROM
62256 at V8	4000 – 7FFF	16K RAM

Display : 6 – digit, 0.5" seven segment LED display

Keyboard: 32 keys including hexadecimal digits 0 to F

I/O Device:

I./O Device	Name	Port address
8255A:1	Programmable Peripheral Interface	00-03
8255A:2	Programmable Peripheral Interface	40-43
8255A 3	Programmable Peripheral interface	60-63
8255A 4	Programmable peripheral interface	70-73
8253-5	Programmable Interval timer	10-13
8251A:	Programmable communication interface	20-21
8279-5	Programmable keyboard/Display interface	30 –31
8279-A	Programmable interrupt controller	50-51

System power supply:

Supply required for Microprocessor and interfacing device is 5V(±0.1V), 1.2A, options available for outer peripherals is +12V(±1.0v) & 250mA,-12V(±1.0V) & 100mA and 29V(± 2.0V),100mA.

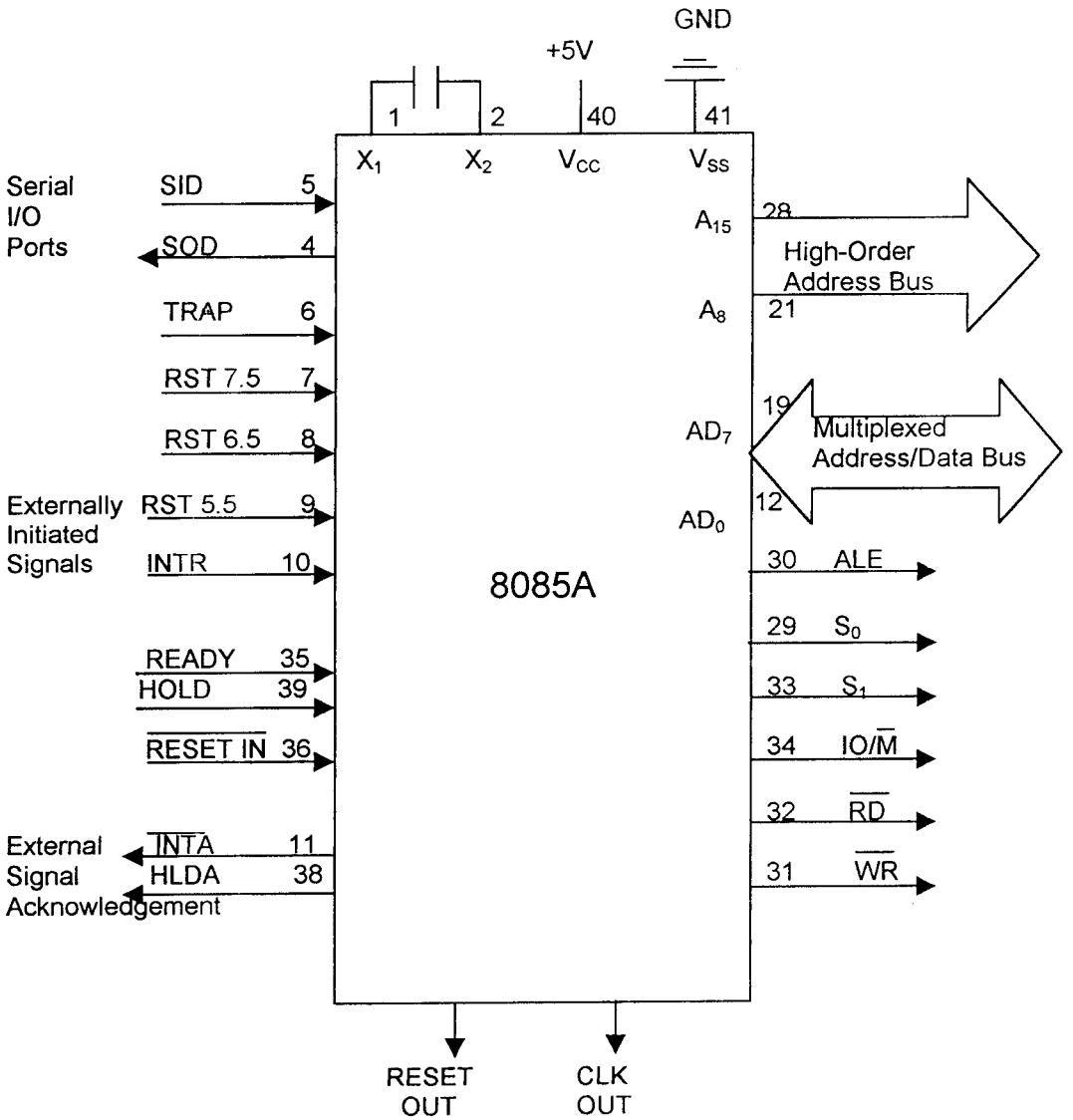


FIG.3.1 LOGIC PINOUT OF 8085

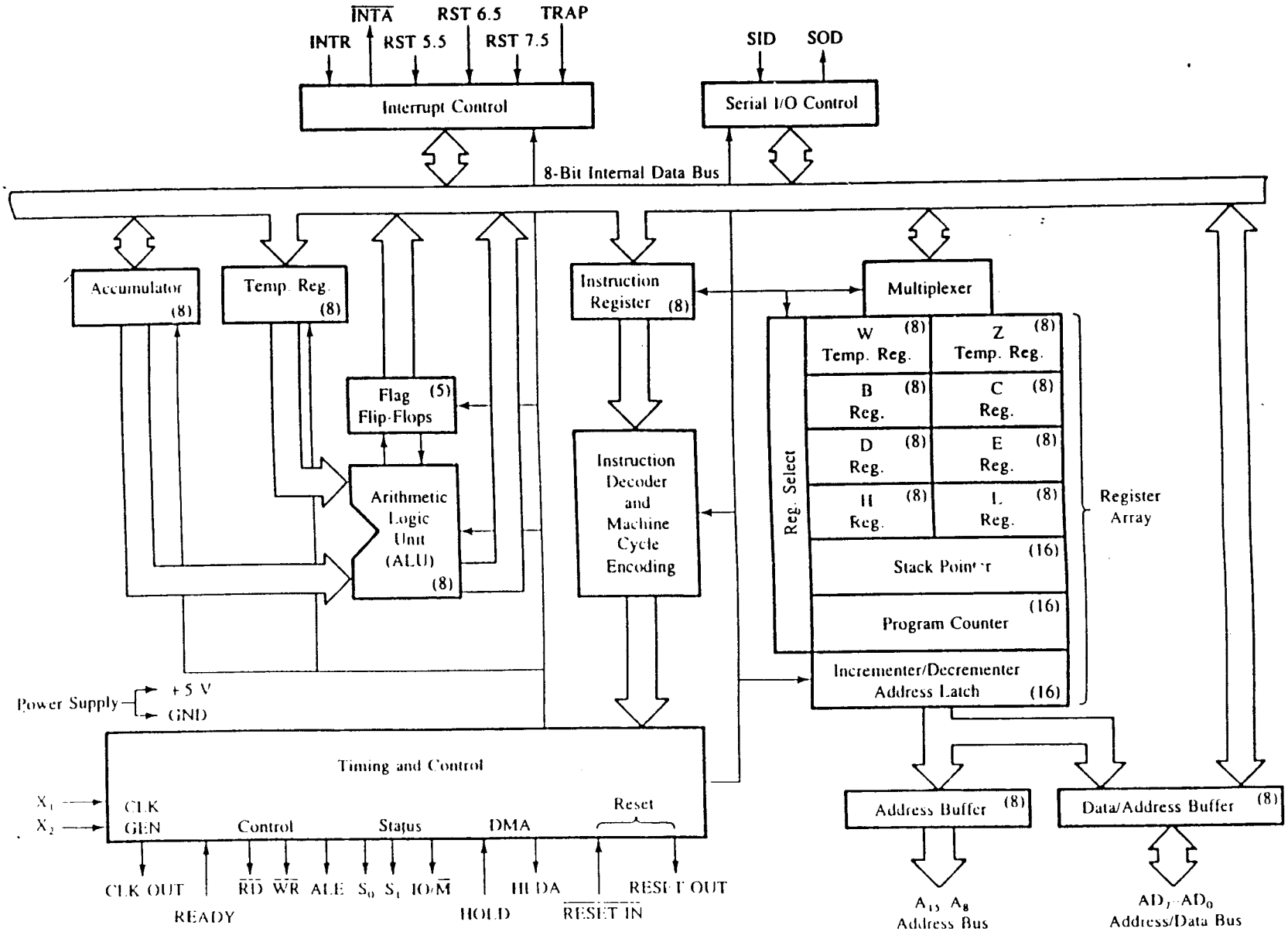


Fig.3.2 Functional Block Diagram of 8085

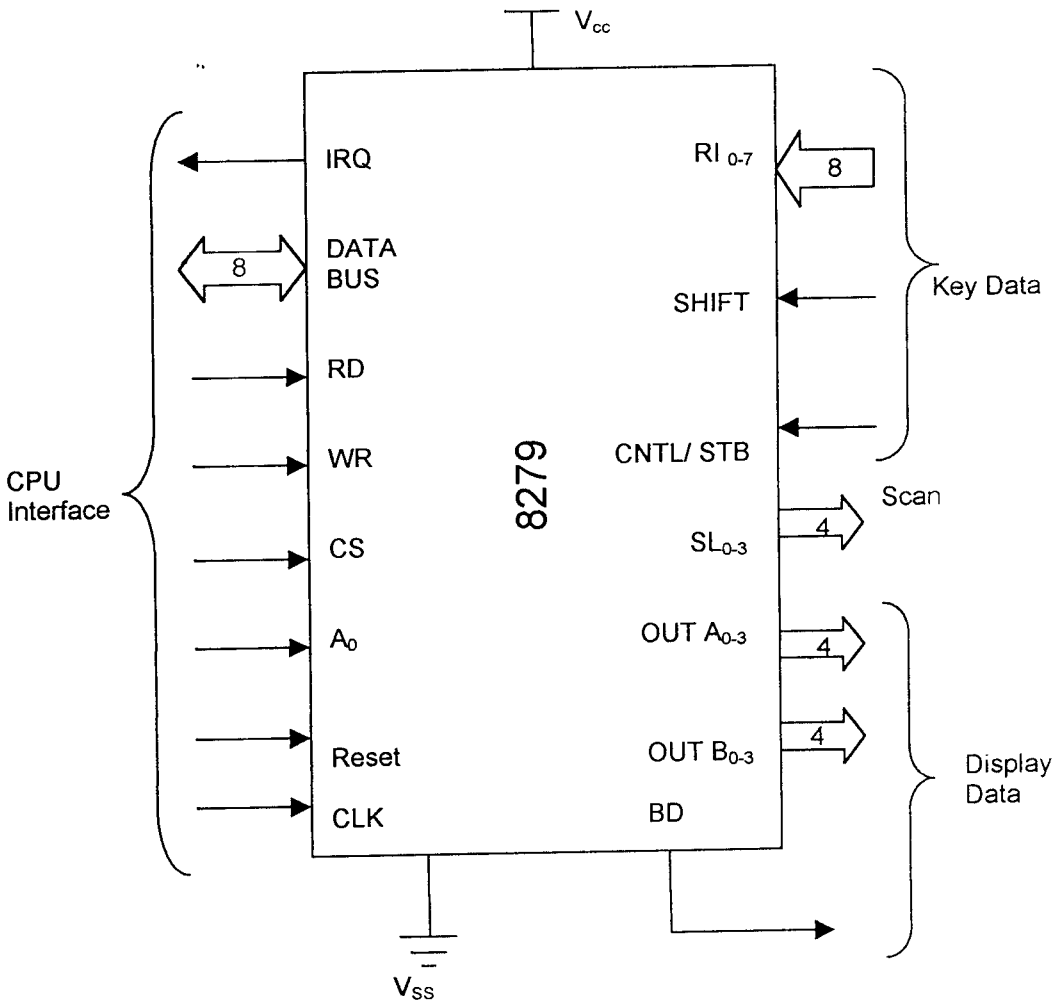


FIG.3.3 LOGIC SYMBOL OF 8279

CHAPTER - 4

SOFTWARE

The software is essential to initiate the various processes that are necessary for hexadecimal conversion, & to actuate the timer. The decimal input by the user is converted into a hexadecimal value and this value is given to a timer which is actuated by a separate control word.

The software is divided into two modules

- Flowchart
- Assembly level program

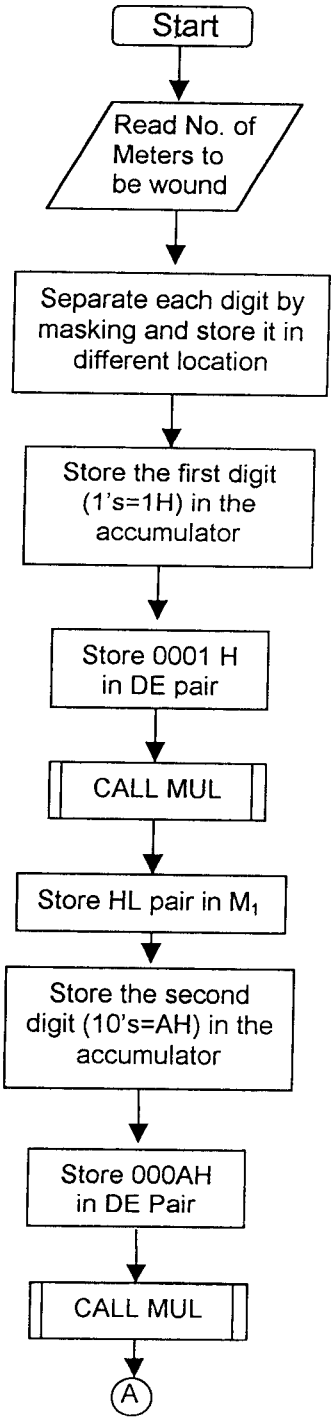
PR185 AD monitor program offers several user-callable routines both in the keyboard and in 7 segment display. We need two routines one for getting input from keyboard and other for display the data in 7 segment.

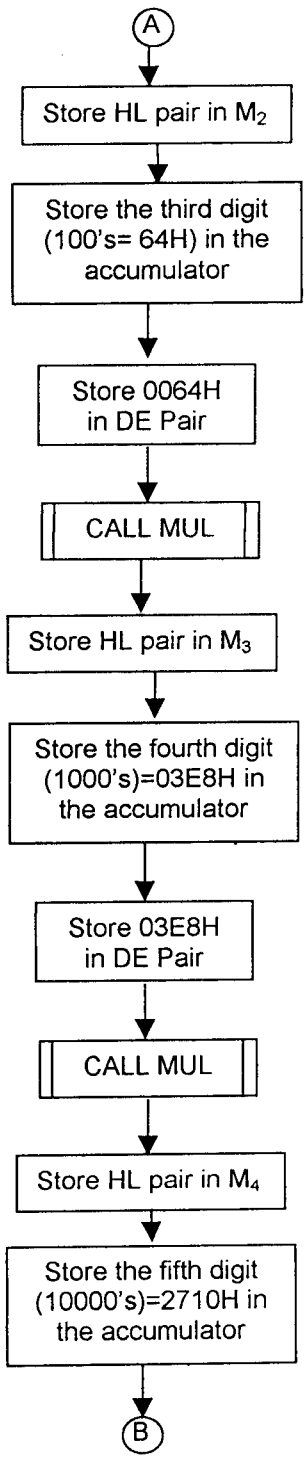
Used routines are

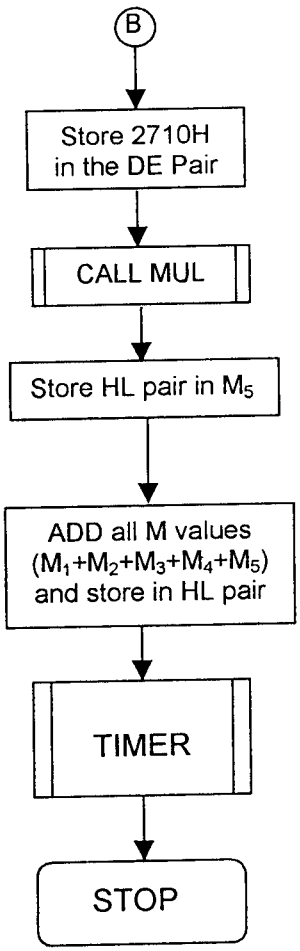
Calling Address	Mnemonic	Function
0514H	RDKBD	Reads keyboard. This routine waits until a character is entered from the system keyboard and upon return, it places the character in the Accumulator
04E3H	OUTPUT	Outputs character to display. The parameters for this routine are as follows. Reg A=1 – Use data field. Reg A=2 – Use Address field. Reg B=1 – Dot at the right edge of the field. Reg B=0 – No dot. Reg HL = Starting Address of character string to be displayed.

4.1. Flow Chart

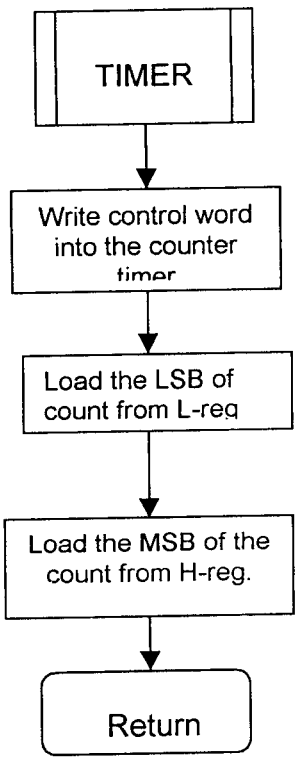
4.1.1 Main Program



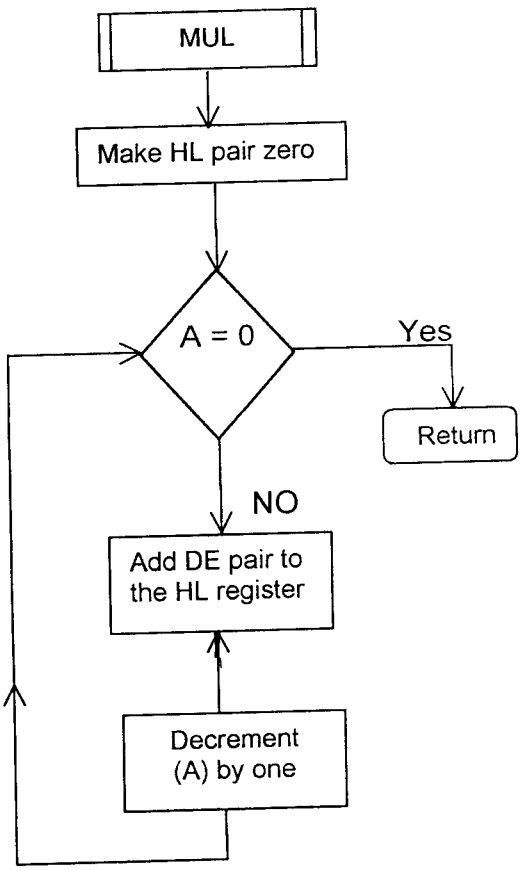

A
Store HL pair in M_2
Store the third digit (100's= 64H) in the accumulator
Store 0064H in DE Pair
CALL MUL
Store HL pair in M_3
Store the fourth digit (1000's)=03E8H in the accumulator
Store 03E8H in DE Pair
CALL MUL
Store HL pair in M_4
Store the fifth digit (10000's)=2710H in the accumulator
B


B
Store 2710H in the DE Pair
CALL MUL
Store HL pair in M_5
ADD all M values (M_1+M_2+M_3+M_4+M_5) and store in HL pair
TIMER
STOP

4.1.2 TIMER SUBROUTINE:



4.1.3 MULTIPLICATION SUBROUTINE:



4.2 ASSEMBLY LANGUAGE PROGRAM:

8000	OE	05		MOV C, 05
8002	21	01	85	LXI H, 8501
8005	CD	14	05	LI: CALL RAKBB
8008	77			MOV M, A
8009	23			INX H
800A	OD			DCR C
800B	C2	05	80	JNZ L1: 8005
800E	C3	00	84	JMP 8400
8400	3E	00		MVI A, 00
8402	06	00		MVI B, 00
8404	21	00	85	LXI H, 8500
8407	CD	E3	04	CALL OUTPUT
840A	3E	01		MVI A, 01
840C	06	00		MVI B, 00
840E	21	04	85	LXI H, 8504
8411	CD	E3	04	CALL OUTPUT
8414	C3	00	81	JMP 8100
8100	3A	01	85	LDA 8501
8103	11	10	27	LXI D, 2710
8106	CD	00	82	CALL MUL
8109	22	50	85	SHLD 8550
810C	3A	02	85	LDA 8502
810F	11	E8	03	LXI D, 03E8
8112	CD	00	82	CALL MUL
8115	22	52	85	SHLD 8552
8118	3A	03	85	LDA 8503
811B	11	64	00	LXI D, 0064

811B	11	64	00	LXI D, 0064
811E	CD	00	82	CALL MUL
8121	22	54	85	SHLD 8554
8124	3A	04	85	LDA 8504
8127	3A	0A	00	LX1 D, 000A
812A	CD	00	82	CALL MUL
812D	22	56	85	SHLD 8556
8130	3A	05	85	LOA 8505
8133	11	01	00	LX1 D, 0001
8136	CD	00	82	CAL MUL
8139	22	58	85	SHLD 8558
813C	2A	50	85	LHLD 8550
813F	EB			XCHG
8140	2A	52	85	LHLD 8552
8143	19			DAD D
8144	EB	X		CHG
8145	2A	54	85	LHLD 8554
8148	19			DAD D
8149	EB			XCHG
814A	2A	5685		LHLD 8556
814D	19			DAD D
814E	EB			XCHG
814F	2A	58	85	LHLD 8558
8152	19			DAD D
8153	22	00	86	SHLD 8600
8156	CD	00	83	CALL TIMER (8300)

SUBROUTINE:TIMER

8300	83	3E	BO	MVI A, BO
8302	D3	13		OUT 13H
8304	7D			MOV A, L
8305	D3	12		OUT 12
8307	7C			MOV A,H
8308	D3	12		OUT 12
830A	76			HLT

SUBROUTINE: MUL

8200	47			MOV B,A
8201	80			ADD B
8202	90			SUB B
8203	21	00	00	LXI H, 0000
8206	CA	OE	82	JZ L2
8209	19			LI; DAD D
820A	EB	05		DCR B
820B	C2	09	82	JNZ LI
820E	C9			L2: RET

CHAPTER -5

TESTING

Microprocessor based Yarn length controlling system is fabricated consisting of Microcomputer, Sensors and cone lifter. These components are tested separately and the whole set up is based over a cone winding machine.

Transmitter and Receiver of optical sensors are tested by using a CRO [Testing Terminal]. Inductive Proximity sensor is checked by using a CRO with an Iron Piece. When the Iron piece is nearer ($\leq$ 3mm) to the sensor tip, it will produce a pulse of 5 volts amplitude, else its output will be at low level.

Electromagnet used for attracting the lever is tested by giving a 12 volts supply from an amplifier

Tested Results of our system, as a whole on Cone Winding for 1kg of yarn package, Machine are as follows:

(* All the length conversion is based on weight and tex)

Count	Tex (gms/ 1000m)	Weight to be wound (gm)	Weight wound by Existing method	Weight wound by New Method	Equivalent length to correspondent to 1kg weight (m)	Length wound by existing method (m)	Length wound by new method (m)	% error of existing method	% error of new method	% of accuracy improved
5	118.108	1000	1072	1034	8466.83	9076.44	8754.69	7.20	3.40	52.98
10	59.054	1000	1051	1023	16933.65	17797.26	17323.123	5.10	2.30	54.90
20	29.527	1000	1032	1013	33867.31	34951.06	34307.58	3.20	1.30	59.37
30	19.685	1000	1013	995	50800.10	51460.90	50546.09	1.30	-0.50	61.5
40	14.763	1000	1020	1007	67736.91	69091.64	68211.07	1.99	0.699	64.87

CHAPTER -6

CONCLUSION

The "Microprocessor based yarn length controlling system" has been designed and fabricated and it is tested on a cone winding machine and its operation is found to be satisfactory.

The machine used for cone wining in textile industries today are time consuming, tedious and involves more manual work. The results thus produced are also not accurate. The modified version of the cone winding machine with the Microprocessor based accessories provided by this project produces a more accurate result.

The advantages of this Microprocessor based yarn length control for cone winding system are as follows.

- Time consumed in yarn winding process is less.
- Accurate winding of yarn to a predetermined weight.
- Yarn package is uniform and quality of winding is better.
- Protection rate is high compared to the conventional method.
- Cost is less at rates affordable by small scale industry.
- requires less man power

FURTHER DEVELOPMENT:

The project can be further developed upon to furnish the following details:

1. Data collection system for cone winding machine by using the same Microprocessor.

2. Automatic twisting by introducing Vacuum Sucker.

3. Muiltiplexing the control for more number of heads.

4. Development of Automatic cone and cop replacement unit.

5. The Microprocessor used for this project, can also be used as centralised setting point for electronic yarn clearing systems and yarn fault classification system.

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9. "VISOLUX" - User manual.

8085AH/8085AH-2/8085AH-1
8-BIT HMOS MICROPROCESSORS

- Single +5V Power Supply with 10% Voltage Margins
- 3 MHz, 5 MHz and 6 MHz Selections Available
- 20% Lower Power Consumption than 8085A for 3 MHz and 5 MHz
- 1.3 μs Instruction Cycle (8085AH); 0.8 μs (8085AH-2); 0.67 μs (8085AH-1)
- 100% Compatible with 8085A
- 100% Software Compatible with 8080A
- On-Chip Clock Generator (with External Crystal, LC or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- Four Vectored Interrupt Inputs (One is Non-Maskable) Plus an 8080A-Compatible Interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64K Bytes of Memory
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The Intel® 8085AH is a complete 8 bit parallel Central Processing Unit (CPU) implemented in N-channel, depletion load, silicon gate technology (HMOS). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085AH (CPU), 8156H (RAM/IO) and 8355/8755A (ROM/PROM/IO)] while maintaining total system expandability. The 8085AH-2 and 8085AH-1 are faster versions of the 8085AH.

The 8085AH incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085AH uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155H/8156H/8355/8755A memory products allow a direct interface with the 8085AH.

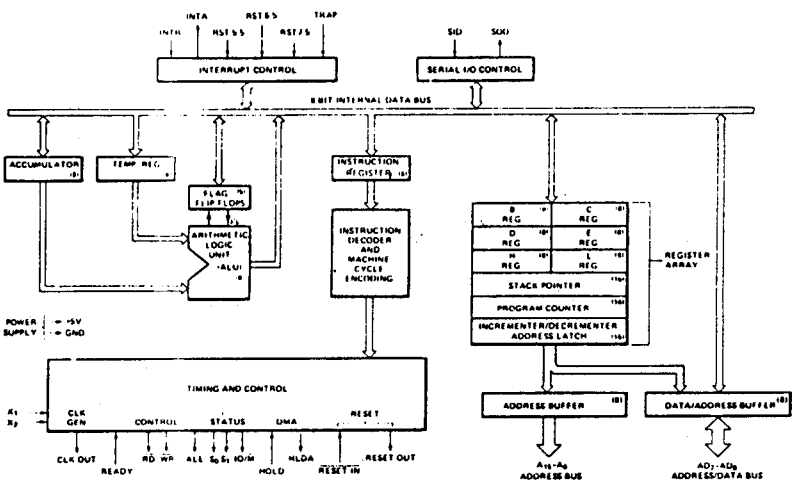


Figure 1. 8085AH CPU Functional Block Diagram

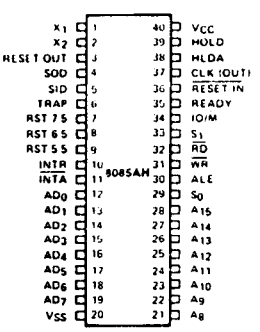


Figure 2. 8085AH Pin Configuration

Table 6. Instruction Set Summary

Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operations Description
MOVE, LOAD, AND STORE									
MOVr1 r2	0	1	D	D	D	S	S	S	Move register to register
MOV M,r	0	1	1	1	0	S	S	S	Move register to memory
MOV r,M	0	1	D	D	D	1	1	0	Move memory to register
MVI r	0	0	D	D	D	1	1	0	Move immediate register
MVI M	0	0	1	1	0	1	1	0	Move immediate memory
LXI B	0	0	0	0	0	0	0	1	Load immediate register Pair B & C
LXI D	0	0	0	1	0	0	0	1	Load immediate register Pair D & E
LXI H	0	0	1	0	0	0	0	1	Load immediate register Pair H & L
STAX B	0	0	0	0	0	0	1	0	Store A indirect
STAX D	0	0	0	1	0	0	1	0	Store A indirect
LDAX B	0	0	0	0	1	0	1	0	Load A indirect
LDAX D	0	0	0	1	1	0	1	0	Load A indirect
STA	0	0	1	1	0	0	1	0	Store A direct
LDA	0	0	1	1	1	0	1	0	Load A direct
SHLD	0	0	1	0	0	0	1	0	Store H & L direct
LHLD	0	0	1	0	1	0	1	0	Load H & L direct
XCHG	1	1	1	0	1	0	1	1	Exchange D & E, H & L Registers
STACK OPS									
PUSH B	1	1	0	0	0	1	0	1	Push register Pair B & C on stack
PUSH D	1	1	0	1	0	1	0	1	Push register Pair D & E on stack
PUSH H	1	1	1	0	0	1	0	1	Push register Pair H & L on stack
PUSH PSW	1	1	1	1	0	1	0	1	Push A and Flags on stack
POP B	1	1	0	0	0	0	0	1	Pop register Pair B & C off stack
POP D	1	1	0	1	0	0	0	1	Pop register Pair D & E off stack
POP H	1	1	1	0	0	0	0	1	Pop register Pair H & L off stack
POP PSW	1	1	1	1	0	0	0	1	Pop A and Flags off stack
XTHL	1	1	1	0	0	0	1	1	Exchange top of stack, H & L
SPHL	1	1	1	1	1	0	0	1	H & L to stack pointer
LXI SP	0	0	1	1	0	0	0	1	Load immediate stack pointer
INX SP	0	0	1	1	0	0	1	1	Increment stack pointer
DCX SP	0	0	1	1	1	0	1	1	Decrement stack pointer
JUMP									
JMP	1	1	0	0	0	0	1	1	Jump unconditional
JC	1	1	0	1	1	0	1	0	Jump on carry
JNC	1	1	0	1	0	0	1	0	Jump on no carry
JZ	1	1	0	0	1	0	1	0	Jump on zero
JNZ	1	1	0	0	0	0	1	0	Jump on no zero
JP	1	1	1	1	0	0	1	0	Jump on positive
JM	1	1	1	1	1	0	1	0	Jump on minus
JPE	1	1	1	0	1	0	1	0	Jump on parity even
JPO	1	1	1	0	0	0	1	0	Jump on parity odd
PCHL	1	1	1	0	1	0	0	1	H & L to program counter
CALL									
CALL	1	1	0	0	1	1	0	1	Call unconditional
CC	1	1	0	1	1	1	0	0	Call on carry
CNC	1	1	0	1	0	1	0	0	Call on no carry

Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operations Description
CZ	1	1	0	0	1	1	0	0	Call on zero
CNZ	1	1	0	0	0	1	0	0	Call on no zero
CP	1	1	1	1	0	1	0	0	Call on positive
CM	1	1	1	1	1	1	0	0	Call on minus
CPE	1	1	1	0	1	1	0	0	Call on parity even
CPO	1	1	1	0	0	1	0	0	Call on parity odd
RETURN									
RET	1	1	0	0	1	0	0	1	Return
RC	1	1	0	1	1	0	0	0	Return on carry
RNC	1	1	0	1	0	0	0	0	Return on no carry
RZ	1	1	0	0	1	0	0	0	Return on zero
RNZ	1	1	0	0	0	0	0	0	Return on no zero
RP	1	1	1	1	0	0	0	0	Return on positive
RM	1	1	1	1	1	0	0	0	Return on minus
RPE	1	1	1	0	1	0	0	0	Return on parity even
RPO	1	1	1	0	0	0	0	0	Return on parity odd
RESTART									
RST	1	1	A	A	A	1	1	1	Restart
INPUT/OUTPUT									
IN	1	1	0	1	1	0	1	1	Input
OUT	1	1	0	1	0	0	1	1	Output
INCREMENT AND DECREMENT									
INR r	0	0	D	D	D	1	0	0	Increment register
DCR r	0	0	D	D	D	1	0	1	Decrement register
INR M	0	0	1	1	0	1	0	0	Increment memory
DCR M	0	0	1	1	0	1	0	1	Decrement memory
INX B	0	0	0	0	0	0	1	1	Increment B & C registers
INX D	0	0	0	1	0	0	1	1	Increment D & E registers
INX H	0	0	1	0	0	0	1	1	Increment H & L registers
DCX B	0	0	0	0	1	0	1	1	Decrement B & C
DCX D	0	0	0	1	1	0	1	1	Decrement D & E
DCX H	0	0	1	0	1	0	1	1	Decrement H & L
ADD									
ADD r	1	0	0	0	0	S	S	S	Add register to A
ADC r	1	0	0	0	1	S	S	S	Add register to A with carry
ADD M	1	0	C	0	0	1	1	0	Add memory to A
ADC M	1	0	0	0	1	1	1	0	Add memory to A with carry
ADI	1	1	0	0	0	1	1	0	Add immediate to A
ACI	1	1	0	0	1	1	1	0	Add immediate to A with carry
DAD B	0	0	0	0	1	0	0	1	Add B & C to H & L
DAD D	0	0	0	1	1	0	0	1	Add D & E to H & L
DAD H	0	0	1	0	1	0	0	1	Add H & L to H & L
DAD SP	0	0	1	1	1	0	0	1	Add stack pointer to H & L
SUBTRACT									
SUB r	1	0	0	1	0	S	S	S	Subtract register from A
SBB r	1	0	0	1	1	S	S	S	Subtract register from A with borrow
SUB M	1	0	0	1	0	1	1	0	Subtract memory from A
SBB M	1	0	0	1	1	1	1	0	Subtract memory from A with borrow
SUI	1	1	0	1	0	1	1	0	Subtract immediate from A
SBI	1	1	0	1	1	1	1	0	Subtract immediate from A with borrow

Table 6. Instruction Set Summary (Continued)

Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operations Description
LOGICAL									
ANA r	1	0	1	0	0	S	S	S	And register with A
XRA r	1	0	1	0	1	S	S	S	Exclusive OR register with A
ORA r	1	0	1	1	0	S	S	S	OR register with A
CMP r	1	0	1	1	1	S	S	S	Compare register with A
ANA M	1	0	1	0	0	1	1	0	And memory with A
XRA M	1	0	1	0	1	1	1	0	Exclusive OR memory with A
ORA M	1	0	1	1	0	1	1	0	OR memory with A
CMP M	1	0	1	1	1	1	1	0	Compare memory with A
ANI	1	1	1	0	0	1	1	0	And immediate with A
XRI	1	1	1	0	1	1	1	0	Exclusive OR immediate with A
ORI	1	1	1	1	0	1	1	0	OR immediate with A
CPI	1	1	1	1	1	1	1	0	Compare immediate with A
ROTATE									
RLC	0	0	0	0	0	1	1	1	Rotate A left
RRC	0	0	0	0	1	1	1	1	Rotate A right
RAL	0	0	0	1	0	1	1	1	Rotate A left through carry
RAR	0	0	0	1	1	1	1	1	Rotate A right through carry

Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operations Description
SPECIALS									
CMA	0	0	1	0	1	1	1	1	Complement A
STC	0	0	1	1	0	1	1	1	Set carry
CMC	0	0	1	1	1	1	1	1	Complement carry
DAA	0	0	1	0	0	1	1	1	Decimal adjust A
CONTROL									
EI	1	1	1	1	1	0	1	1	Enable Interrupts
DI	1	1	1	1	0	0	1	1	Disable Interrupt
NOP	0	0	0	0	0	0	0	0	No-operation
HLT	0	1	1	1	0	1	1	0	Halt
NEW 8085A INSTRUCTIONS									
RIM	0	0	1	0	0	0	0	0	Read Interrupt Mask
SIM	0	0	1	1	0	0	0	0	Set Interrupt Mask

NOTES:
1. DDS or SSS: B 000, C 001, D 010, E011, H.100 L 101, Memory 110, A 111.
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.

intel

8279/8279-5
PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

- Simultaneous Keyboard Display Operations
- Scanned Keyboard Mode
- Scanned Sensor Mode
- Strobed Input Entry Mode
- 8-Character Keyboard FIFO
- 2-Key Lockout or N-Key Rollover with Contact Debounce
- Dual 8- or 16-Numerical Display
- Single 16-Character Display
- Right or Left Entry 16-Byte Display RAM
- Mode Programmable from CPU
- Programmable Scan Timing
- Interrupt Output on Key Entry
- Available in EXPRESS
  —Standard Temperature Range
  —Extended Temperature Range

The Intel® 8279 is a general purpose programmable keyboard and display I/O interface device designed for use with Intel® microprocessors. The keyboard portion can provide a scanned interface to a 64-contact key matrix. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the hall effect and ferrite variety. Key depressions can be 2-key lockout or N-key rollover. Keyboard entries are debounced and strobed in an 8-character FIFO. If more than 8 characters are entered, overrun status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The 8279 has 16X8 display RAM which can be organized into dual 16X4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

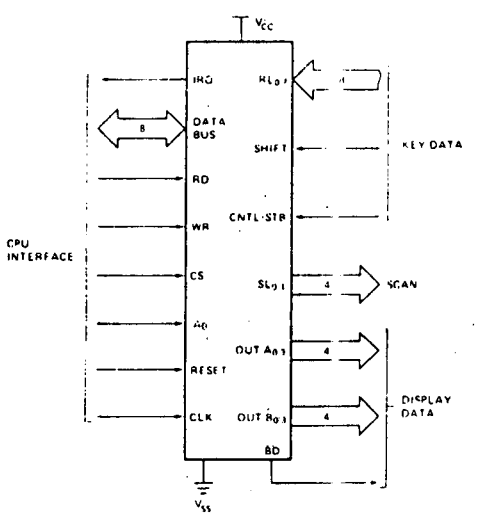


Figure 1. Logic Symbol

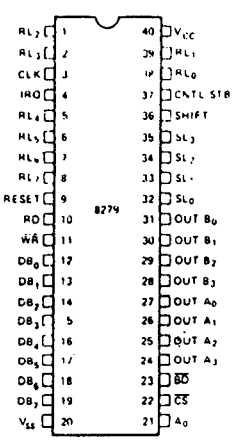
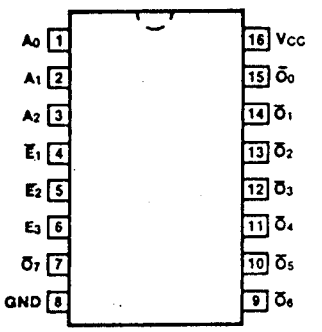


Figure 2. Pin Configuration

54S/74S138
54LS/74LS138
1-OF-8 DECODER/DEMULTIPLEXER

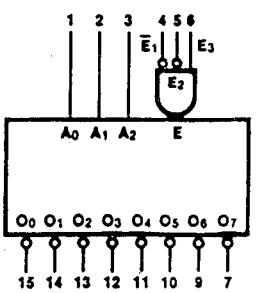
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '138 is a high speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three '138 devices or to a 1-of-32 decoder using four '138 devices and one inverter. The '138 is fabricated with the Schottky barrier diode process for high speed.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **DEMULTIPLEXING CAPABILITY**
- **MULTIPLE INPUT ENABLE FOR EASY EXPANSION**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S138PC, 74LS138PC		9B
Ceramic DIP (D)	A	74S138DC, 74LS138DC	54S138DM, 54LS138DM	6B
Flatpak (F)	A	74S138FC, 74LS138FC	54S138FM, 54LS138FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_2$	Address Inputs	1.25/1.25	0.5/0.25
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)	1.25/1.25	0.5/0.25
E_3	Enable Input (Active HIGH)	1.25/1.25	0.5/0.25
$\overline{O}_0 - \overline{O}_7$	Outputs (Active LOW)	25/12.5	10/5.0 (2.5)

54LS/74LS245

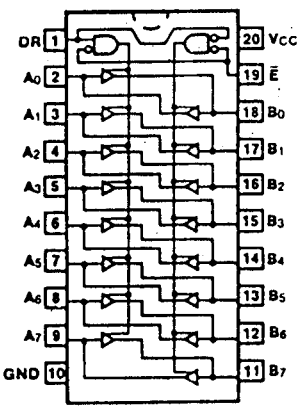
OCTAL BUS TRANSCEIVER

(With 3-State Outputs)

DESCRIPTION — The 'LS245 is an octal bus transmitter/receiver designed for 8-line asynchronous 2-way data communication between data busses. Direction input (DR) controls transmission of data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input ($\overline{E}$) can be used to isolate the busses.

- **HYSTERESIS INPUTS TO IMPROVE NOISE IMMUNITY**
- **2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION**
- **INPUT DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS245PC		9Z
Ceramic DIP (D)	A	74LS245DC	54LS245DM	4E
Flatpak (F)	A	74LS245FC	54LS245FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	0.5/0.125
Outputs	75/15 (7.5)

TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	DR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

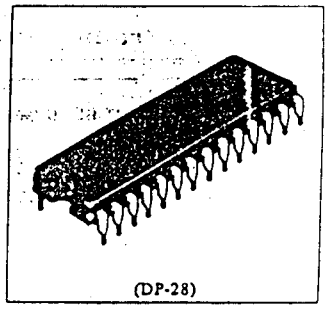
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

HM6264P-10, HM6264P-12, HM6264P-15

8192-word x 8-bit High Speed Static CMOS RAM

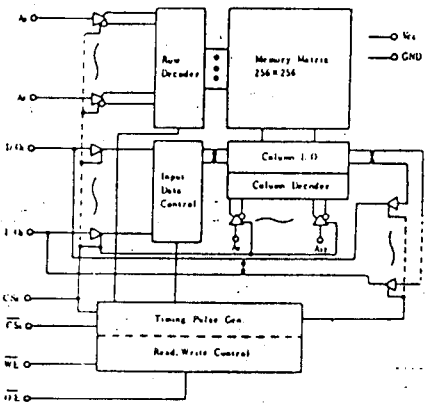
■ FEATURES

- Fast access Time — 100ns/120ns/150ns (max.)
- Low Power Standby — Standby: 0.1mW (typ.)
  Low Power Operation — Operating: 200mW (typ.)
- Single +5V Supply
- Completely Static Memory..... No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

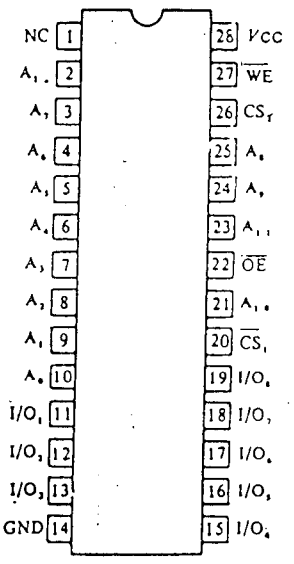


(DP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns: −3.0V

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

x : Don't care.

2732A provide a trace to pin 26

PIN NAMES

A_0-A_{12}	ADDRESSES
$\overline{CE}$	CHIP ENABLE

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}