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ADVANCED HORN TESTING SYSTEM

By

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Certificate

BONAFIDE CERTIFICATE

This is to be certified that this project report " **Advanced Horn Testing System**" is the bonafied work of **"Deepak.C, Dinesh Babu.D, Gopi.M, Balaji.K** " who carried out the project work under my supervision.

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ROOTS INDUSTRIES INDIA LIMITED

RIL/HRD/4403/11 14.04.2011

PROJECT CERTIFICATE

This is to certify that **Mr.K.Balaji,(Roll No.0710107302) Final Year Electronics and Communication Engineering** Student of **Kumaraguru College of Technology** has done a Project work on **"Advanced Horn Testing System"** in our organisation from **December 2010 to April 2011.**

for **ROOTS INDUSTRIES INDIA LIMITED**

(Dr.Kavidasan)
DIRECTOR

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(Dr.Kavidasan)
DIRECTOR

Abstract

ABSTRACT

The main aim of our project is to provide advanced horn testing environment. The venue of our project is Roots Industries India Limited, Coimbatore. Horn testing and tuning mainly focuses on the design specifications set by the Government. It involves measuring of current, frequency and sound pressure level when predefined voltages are applied to the horn. The present testing mechanism which is done manually is prone to errors and also time consuming. Thus we go for the advanced testing and tuning methodology. This involves automated testing system which utilizes the LabVIEW, a graphical development environment for controlling instruments and data acquisition. The advanced design technique involves the specification need for calibration and adaptive control measures. The threshold value mainly depends on the product type based on which the preset voltages are applied to the testing chamber over which the horn is placed. In this different range of voltages is applied in a fixed interval (Which is programmable) and the corresponding Voltage, Frequency, Current and dB are recorded and compared with the parameter of Horn under test. For different testing voltages corresponding key parameters are measured and analyzed via LabVIEW programming. If the horn didn't meet the requirement tuning is done.

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LIST OF ABBREVIATIONS

LabVIEW	Laboratory Virtual Instrumentation Engineering Workbench
VI	Virtual Instrumentation
PCI	Peripheral Component Interconnect
PXI	PCI eXtensions for Instrumentation
TTL	Transistor–transistor logic
NI	National Instruments
SPL	Sound Pressure Level
LED	Light Emitting Diode
AC	Alternating current
DC	Direct current
CMOS	Complementary metal–oxide–semiconductor
DAQ	Data Acquisition

Chapter 1

1. INTRODUCTION

1.1 STUDY OF THE EXISTING SYSTEM

The Horn production unit follows a sequence of manufacturing processes like,

- Self tapping screw insertion
- Spool assembly
- Pointer holder assembly
- Diaphragm assembly & tightening
- Horn pre crimping & final crimping
- Air gap measuring & adjusting
- Terminal connector binding & Mounting bracket assembling
- Horn testing & tuning

Once the manufacturing completes, there is a need for testing the horn in order to check whether they meet the specifications that are set by the government.

Horn testing involves measuring of current, frequency and sound pressure level in dB by applying different voltages to the horn. At present the measurements are made manually by applying different voltages and noting down the values and checking it manually by comparing it with the government specifications.

1.1.1 DISADVANTAGES OF THE EXISTING SYSTEM

- This system is time consuming.
- The repetition of same work at regular intervals cause human fatigue.
- There is a chance of occurring errors during the time of testing.

1.2 FEATURES OF THE PROPOSED SYSTEM

The horn testing is performed by utilizing LabVIEW software for controlling instruments and data acquisition. The advanced design techniques focuses over the specification needed for calibration and adaptive control measures. The threshold value mainly depends on the horn model, based on which the preset voltages are applied to the testing chamber over which the horn is placed. For different testing voltages, corresponding key parameters are calibrated via LabVIEW programming. If the horn meets the required parameters the testing will be completed by indicating PASS/FAIL result.

Whenever the horn fails to meet the required parameters then tuning is done and again it is subjected to undergo test.

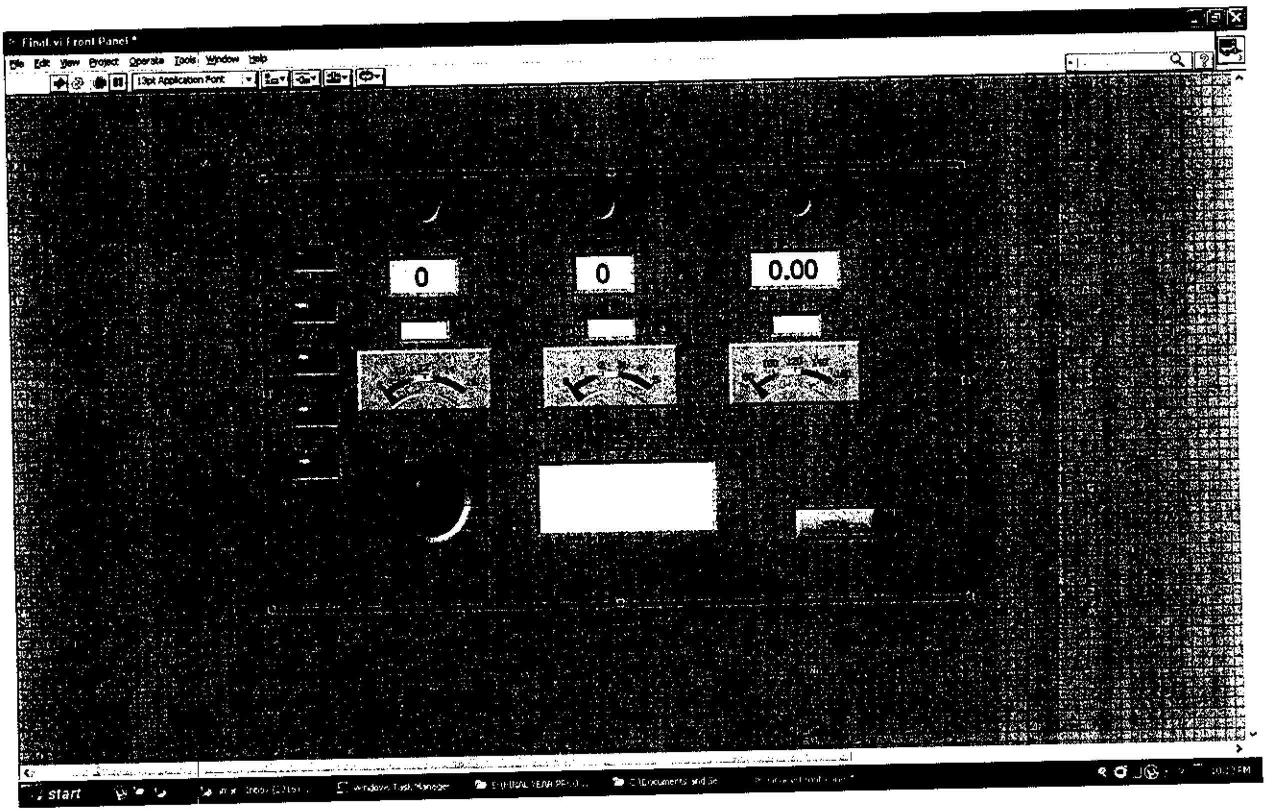


Fig. 1 Front Panel

1.3 LabVIEW SOFTWARE

LabVIEW (Laboratory Virtual Instrumentation Engineering Workbench) is a platform and development environment for a visual programming language from National Instruments.

The purpose of such programming is automating the usage of processing and measuring equipment in any laboratory setup. LabVIEW is commonly used for data acquisition, instrument control, and industrial automation on a variety of platforms including Microsoft Windows, various versions of UNIX, Linux, and Mac OS X.

1.3.1 DATAFLOW PROGRAMMING

The programming language used in LabVIEW is a dataflow programming language. Execution is determined by the structure of a graphical block diagram on which the programmer connects different function-nodes by drawing wires. These wires propagate variables and any node can execute as soon as all its input data become available.

Since this might be the case for multiple nodes simultaneously, Graphical programming is inherently capable of parallel execution. Multi-processing and multi-threading hardware is automatically exploited by the built-in scheduler, which multiplexes multiple OS threads over the nodes ready for execution.

1.3.2 GRAPHICAL PROGRAMMING

LabVIEW ties the creation of user interfaces called front panels into the development cycle. LabVIEW programs/subroutines are called virtual instruments (VIs).

Each VI has three components:

- Block diagram
- Front panel
- Connector panel

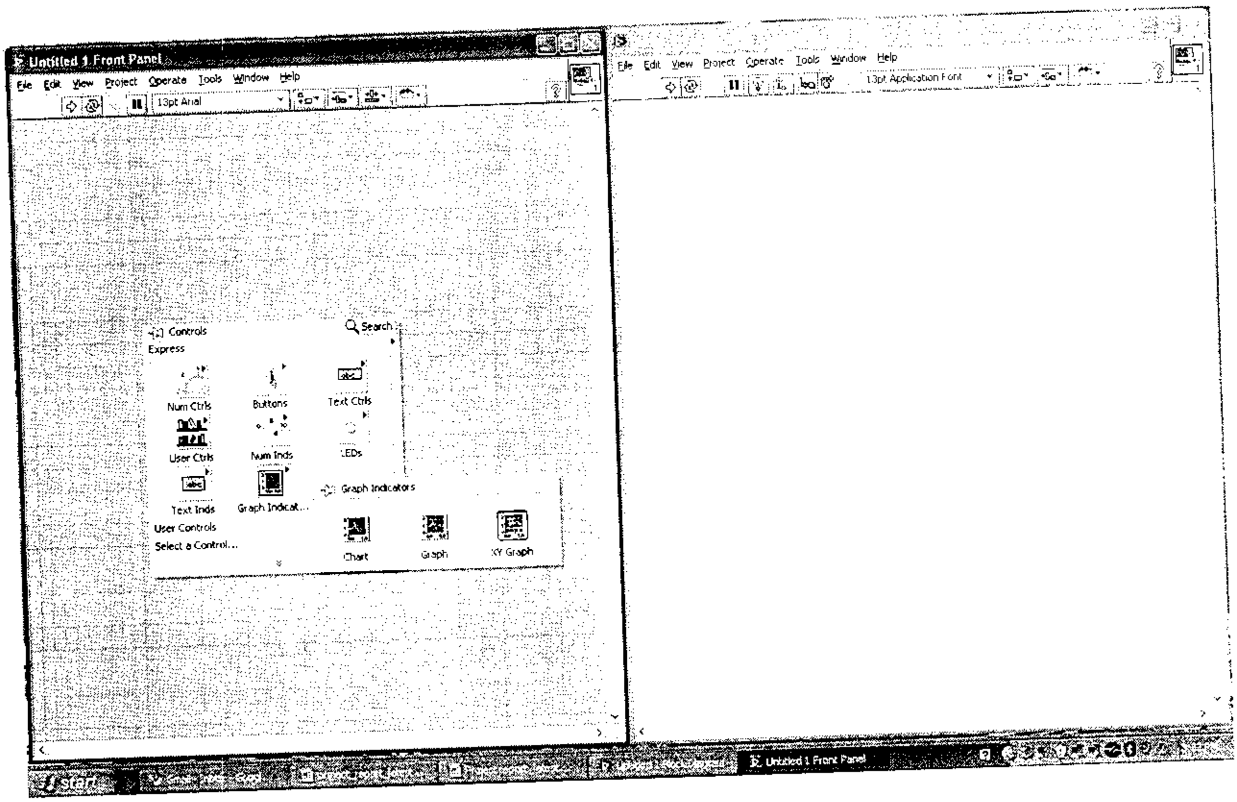


Fig. 2 Front Panel with controls

Controls and indicators on the front panel allow an operator to input data into or extract data from a running virtual instrument. However, the front panel can also serve as a programmatic interface.

Thus a virtual instrument can either be run as a program, with the front panel serving as a user interface, or, when dropped as a node onto the block diagram, the front panel defines the inputs and outputs for the given node through the connector panel. This implies each VI can be easily tested before being embedded as a subroutine into a larger program.

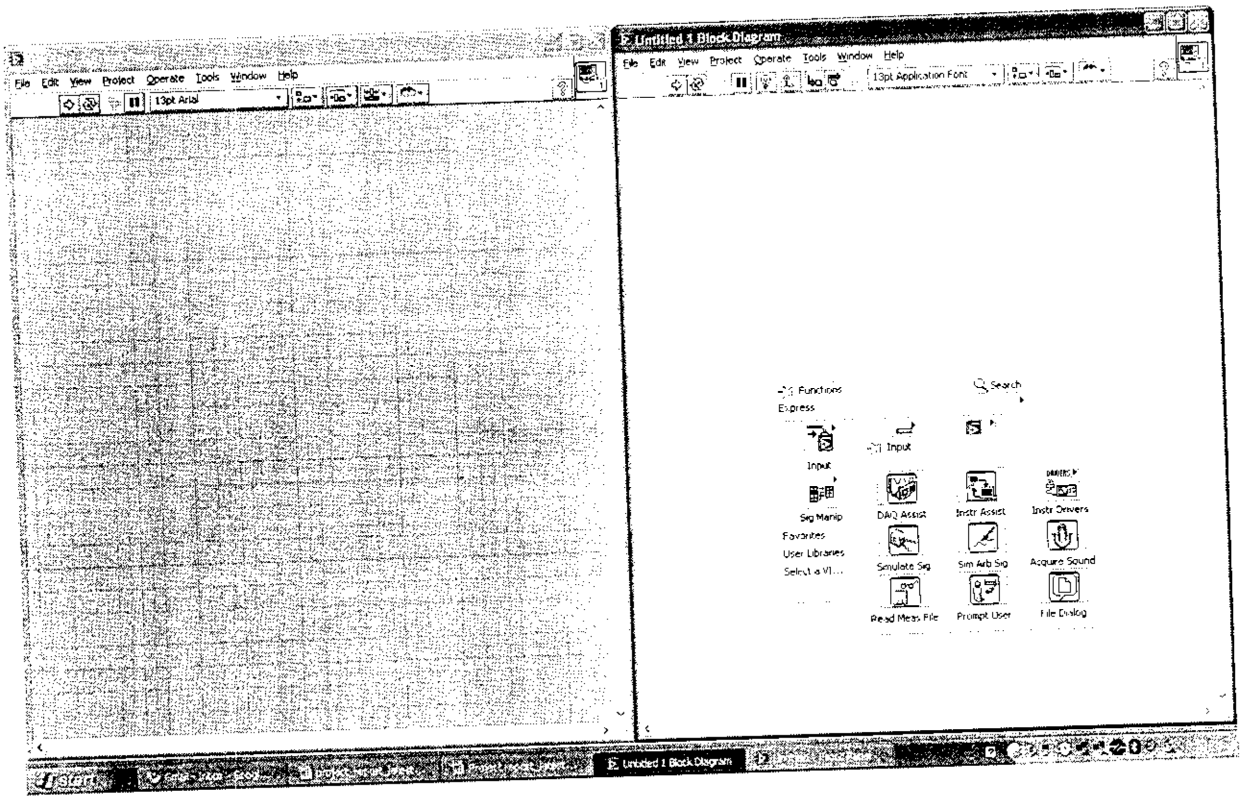


Fig. 3 Block Diagram with functions

The graphical approach also allows non-programmers to build programs by dragging and dropping virtual representations of lab equipment with which they are already familiar. The LabVIEW programming environment, with the included examples and the documentation, makes it simple to create small applications.

For complex algorithms or large-scale code, it is important that the programmer possess an extensive knowledge of the special LabVIEW syntax and the topology of its memory management.The most advanced LabVIEW development systems offer the possibility of building stand-alone applications.

Furthermore, it is possible to create distributed applications, which communicate by a client/server scheme, and are therefore easier to implement due to the inherently parallel nature of LabVIEW.

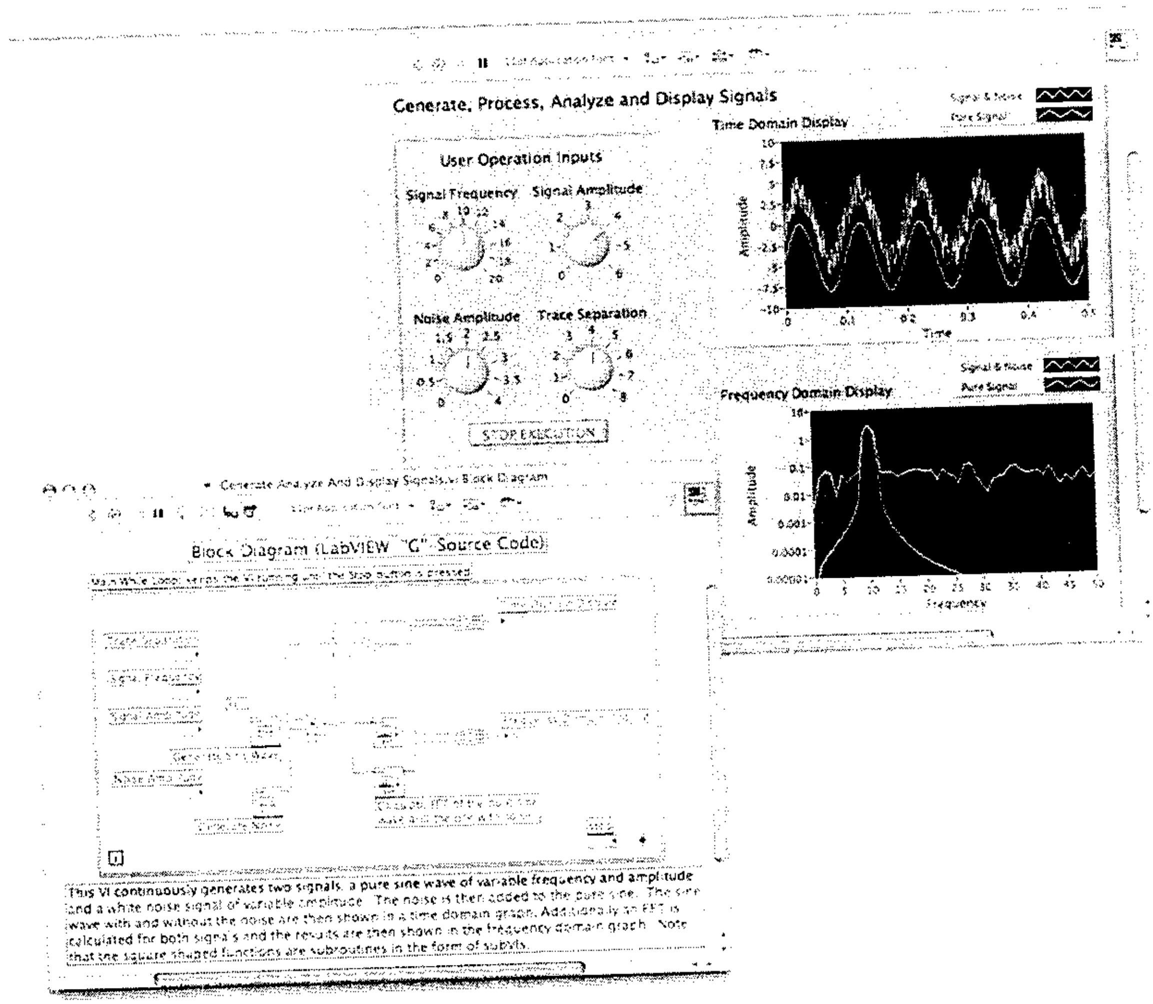


Fig. 4 Screenshot of a simple LabVIEW program

The image above is an illustration of a simple LabVIEW program showing the dataflow source code in the form of the block diagram in the lower left frame and the input and output variables as graphical objects in the upper right frame.

The two are the essential components of a LabVIEW program referred to as a Virtual Instrument VI.

1.3.3 INTERFACING

Drivers and abstraction layers for many different types of instruments and buses are included or are available for inclusion. These present themselves as graphical nodes. The abstraction layers offer standard software interfaces to communicate with hardware devices. The provided driver interfaces saving the program development time.

The sales pitch of National Instruments is, therefore, that even people with limited coding experience can write programs and deploy test solutions in a reduced time frame when compared to more conventional or competing systems.

A new hardware driver topology (DAQmxBase), which consists mainly of Graphical coded components with only a few register calls through NI Measurement Hardware Driver Development Kit functions, provides platform independent hardware access to numerous data acquisition and instrumentation devices. The DAQmxBase driver is available for LabVIEW on Windows, Mac OS X and Linux platforms.

1.3.4 CODE COMPILATION

In terms of performance, LabVIEW includes a compiler that produces native code for the CPU platform. The graphical code is translated into executable machine code by interpreting the syntax and by compilation. The LabVIEW syntax is strictly enforced during the editing process and compiled into the executable machine code when requested to run or upon saving. In the latter case, the executable and the source code are merged into a single file.

The executable runs with the help of the LabVIEW run-time engine, which contains some precompiled code to perform common tasks that are defined by the Graphical language. The run-time engine reduces compile time and also provides a consistent interface to various operating systems, graphic systems, hardware components, etc.

The run-time environment makes the code portable across platforms. Generally, LabVIEW code can be slower than equivalent compiled C code, although the differences often lie more with program optimization than inherent execution speed.

1.3.5 LARGE LIBRARIES

Many libraries with a large number of functions for data acquisition, signal generation, mathematics, statistics, signal conditioning, analysis, etc., along with numerous graphical interface elements are provided in several LabVIEW package options.

The number of advanced mathematic blocks for functions such as integration, filters, and other specialized capabilities usually associated with data capture from hardware sensors is immense. In addition, LabVIEW includes a text-based programming component called MathScript with additional functionality for signal processing, analysis and mathematics.

1.3.6 CODE RE-USE

The fully modular character of LabVIEW code allows code reuse without modifications: as long as the data types of input and output are consistent, two sub VIs are interchangeable. The LabVIEW Professional Development System allows creating stand-alone executables and the resultant executable can be distributed an unlimited number of times. The run-time engine and its libraries can be provided freely along with the executable.

A benefit of the LabVIEW environment is the platform independent nature of the graphical code, which is (with the exception of a few platform-specific functions) portable between the different LabVIEW systems for different operating systems (Windows, Mac OS X and Linux). National Instruments is increasingly focusing on the capability of deploying LabVIEW code onto an increasing number of targets including devices like Phar Lap or VxWorks OS based LabVIEW Real-Time controllers, FPGAs, PocketPCs, PDAs, and Wireless sensor network nodes.

1.3.7 RUNTIME ENVIRONMENT

Compiled executables produced by the Application Builder are not truly standalone in that they also require that the LabVIEW run-time engine be installed on any target computer on which users run the application.

The use of standard controls requires a runtime library for any language and all major operating system suppliers supply the required libraries for common languages such as C.

However, the runtime required for LabVIEW is not supplied with any operating system and is required to be specifically installed by the administrator or user. This requirement can cause problems if an application is distributed to a user who may be prepared to run the application but does not have the inclination or permission to install additional files on the host system prior to running the executable.

1.4 DATA ACQUISITION

Data acquisition involves gathering signals from measurement sources and digitizing the signals for storage, analysis, and presentation on a PC. Data acquisition systems come in many different PC technology forms to offer flexibility. It can be choose from PCI, PXI, PCI Express, PXI Express, PCMCIA, USB, wireless, and Ethernet data acquisition for test, measurement, and automation applications.

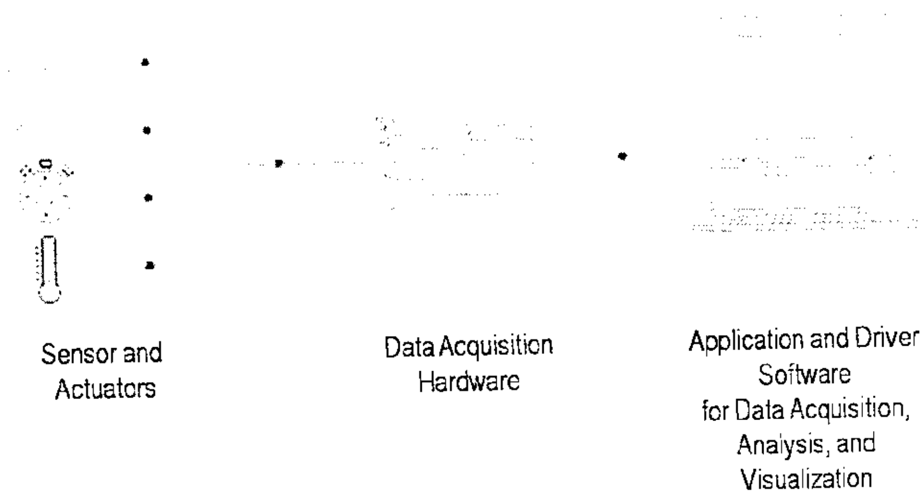


Fig. 5 Data Acquisition System

A basic data acquisition system consists of following five components

- Transducers and sensors
- Signals
- Signal conditioning

- DAQ hardware
- Driver and application software

1.4.1 SIGNALS

The transducer converts physical phenomena into measurable signals. However, different signals need to be measured in different ways. For this reason, it is important to understand the different types of signals and their corresponding attributes. Signals can be categorized into two groups:

- Analog
- Digital

1.4.2 ANALOG SIGNALS

An analog signal can exist at any value with respect to time. A few examples of analog signals include voltage, temperature, pressure, sound, and load.

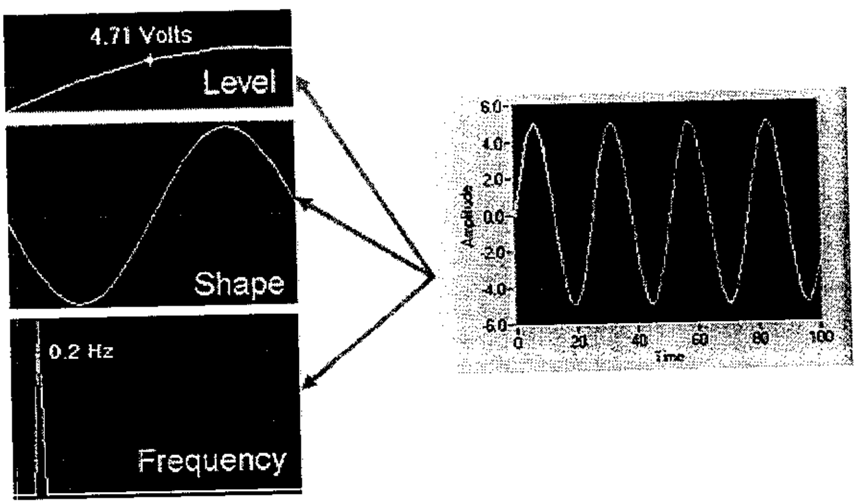


Fig. 6 Primary Characteristics of an Analog Signal

1.4.3 LEVEL

Analog signals can take on any value; the level gives vital information about the measured analog signal. The intensity of a light source, the temperature in a room, and the pressure inside a chamber are all examples that demonstrate the importance of the level of a signal.

While measuring the level of a signal, the signal generally does not change quickly with respect to time. The accuracy of the measurement, however, is very important. A data acquisition system that yields maximum accuracy to help with analog level measurements must be choosen.

1.4.4 SHAPE

Some signals are named after their specific shapes sine, square, sawtooth, and triangle. The shape of an analog signal can be as important as the level because by measuring the shape of an analog signal, analyzing the signal, including peak values, DC values, and slope.

Signals where shape is of interest generally change rapidly with respect to time, but system accuracy is still important. The analysis of heartbeats, video signals, sounds, vibrations, and circuit responses are some applications involving shape measurements.

1.4.5 FREQUENCY

All analog signals can be categorized by their frequencies. Unlike the level or shape of the signal, you cannot directly measure frequency. The signal is analyzed using software to determine the frequency information. This analysis is usually done using an algorithm known as the Fourier transform.

When frequency is the most important piece of information, the need to the both accuracy and acquisition speed is considered. The condition that stipulates this speed is known as the Nyquist Sampling Theorem.

Speech analysis, telecommunication, and earthquake analysis are some examples of common applications where the frequency of the signal must be known.

1.4.6 Digital Signals

A digital signal cannot take on any value with respect to time. Instead, a digital signal has two possible levels: high and low. Digital signals generally conform to certain specifications that define the characteristics of the signal. They are commonly referred to as transistor-to-transistor logic.

TTL specifications indicate a digital signal to be low when the level falls within 0 to 0.8 V, and the signal is high between 2 and 5 V. The useful information that you can measure from a digital signal includes the state and the rate.

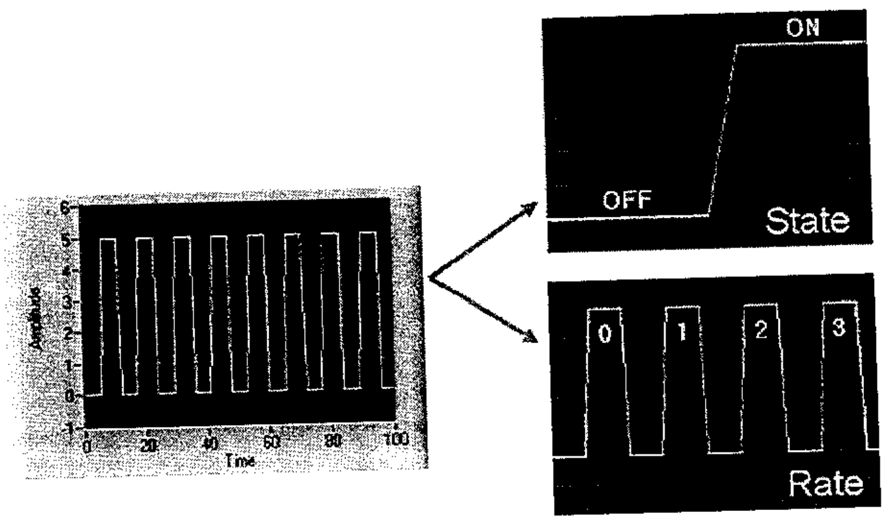


Fig. 7 Primary Characteristics of a Digital Signal

1.4.7 STATE

Digital signals cannot take on any value with respect to time. The state of a digital signal is essentially the level of the signal - on or off, high or low. Monitoring the state of a switch - open or closed - is a common application showing the importance of knowing the state of a digital signal.

1.4.8 RATE

The rate of a digital signal defines how the digital signal changes state with respect to time. An example of measuring the rate of a digital signal includes determining how fast a motor shaft spins.

Unlike frequency, the rate of a digital signal measures how often a portion of a signal occurs. A software algorithm is not required to determine the rate of a signal.

1.4.9 SIGNAL CONDITIONING

Sometimes transducer generates signals too difficult or too dangerous to measure directly with a data acquisition device. For instance, when dealing with high voltages, noisy environments, extreme high and low signals, or simultaneous signal measurement, signal conditioning is essential for an effective data acquisition system. It maximizes the accuracy of a system, allows sensors to operate properly, and guarantees safety.

It is important to select the right hardware for signal conditioning. From both modular and integrated hardware options can be choosed and use of signal conditioning accessories in a variety of applications including the following:

- Amplification
- Attenuation
- Isolation
- Sensor excitation
- Multiplexing
- Bridge completion
- Simultaneous sampling

1.4.10 DATA ACQUISITION HARDWARE

Data acquisition hardware acts as the interface between the computer and the outside world. It primarily functions as a device that digitizes incoming analog signals so that the computer can interpret them.

Other data acquisition functionality includes the following:

- Analog input/output
- Digital input/output
- Counter/timers
- Multifunction - a combination of analog, digital, and counter operations on a single device

National Instruments offers several hardware platforms for data acquisition. The most readily available platform is the desktop computer. NI provides PCI DAQ boards that plug into any desktop computer.

In addition, NI makes DAQ modules for PXI/CompactPCI, a more rugged modular computer platform specifically for measurement and automation applications.

For distributed measurements, the NI Compact FieldPoint platform delivers modular I/O, embedded operation, and Ethernet communication. For portable or handheld measurements, National Instruments DAQ devices for USB and PCMCIA work with laptops or Windows Mobile PDAs.

In addition, National Instruments has launched DAQ devices for PCI Express, the next-generation PC I/O bus, and for PXI Express, the high-performance PXI bus.

1.4.11 DRIVER AND APPLICATION SOFTWARE

DRIVER SOFTWARE

Software transforms the PC and the data acquisition hardware into a complete data acquisition, analysis, and presentation tool. Without software to control or drive the hardware, the data acquisition device does not work properly. Driver software is the layer of software for easily communicating with the hardware. It forms the middle layer between the application software and the hardware.

Driver software also prevents a programmer from having to do register-level programming or complicated commands to access the hardware functions. NI offers two different software options:

- NI-DAQmx driver and additional measurement services software
- NI-DAQmx Base driver software

With the introduction of NI-DAQmx, National Instruments revolutionized data acquisition application development by greatly increasing the speed at which you can move from building a program to deploying a high-performance measurement application.

The DAQ Assistant, included with NI-DAQmx, is a graphical, interactive guide for configuring, testing, and acquiring measurement data. With a single click, you can even generate code based on your configuration, making it easier and faster to develop complex operations.

Because the DAQ Assistant is completely menu-driven, you make fewer programming errors and drastically decrease the time from setting up your data acquisition system to taking your first measurement.NI-DAQmx Base offers a subset of NI-DAQmx functionality on Windows and Linux, Mac OS X, Windows Mobile, and Windows CE.

APPLICATION SOFTWARE

The application layer can be either a development environment in which you build a custom application that meets specific criteria, or it can be a configuration-based program with preset functionality. Application software adds analysis and presentation capabilities to driver software.

To choose the right application software, evaluate the complexity of the application, the availability of configuration-based software that fits the application, and the amount of time available to develop the application. If the application is complex or there is no existing program, use a development environment.

Chapter 2

2. PROJECT OVERVIEW

2.1 TESTING CHAMBER

The Testing Chamber is where the testing of horn is done. Here the horn is subjected to test for the various horn parameters. The following are the test parameters:

- Current measured in Amps
- Frequency measured in Hz
- Sound pressure level measured in dB

The horns that are manufactured must rely on certain specifications. These specifications are mandatory and hence it must be met in order to use the horn in the automobiles. The following are the specifications given by the Government:

Optimum Operating Range of Voltage	Current in amps		SPL in dB		Frequency	
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum
12 V	-	4.0	80	118	310	360

Table No.1 Government specifications

Generally in all automobiles the voltage applied to the horn will be 12 volts. But in the test chamber various voltages ranging from 9 volts to 15 volts are applied and the parameters are analyzed.

The LabVIEW software used in this system will acquire the signals. The horn test parameters frequency, Sound pressure level, Current and applied voltage are read from the horn through the National Instruments Multi function card and it is compared with the pre set values of current, frequency and sound pressure level values for different voltages. Once the testing is complete, the result for the test will be displayed by showing Pass/Fail message.

2.2 BLOCK DIAGRAM

The main components of the Horn Testing system contains a power supply unit, signal isolation panel, leakage current tester, DAQ card connector and DAQ card- PCI 6221.

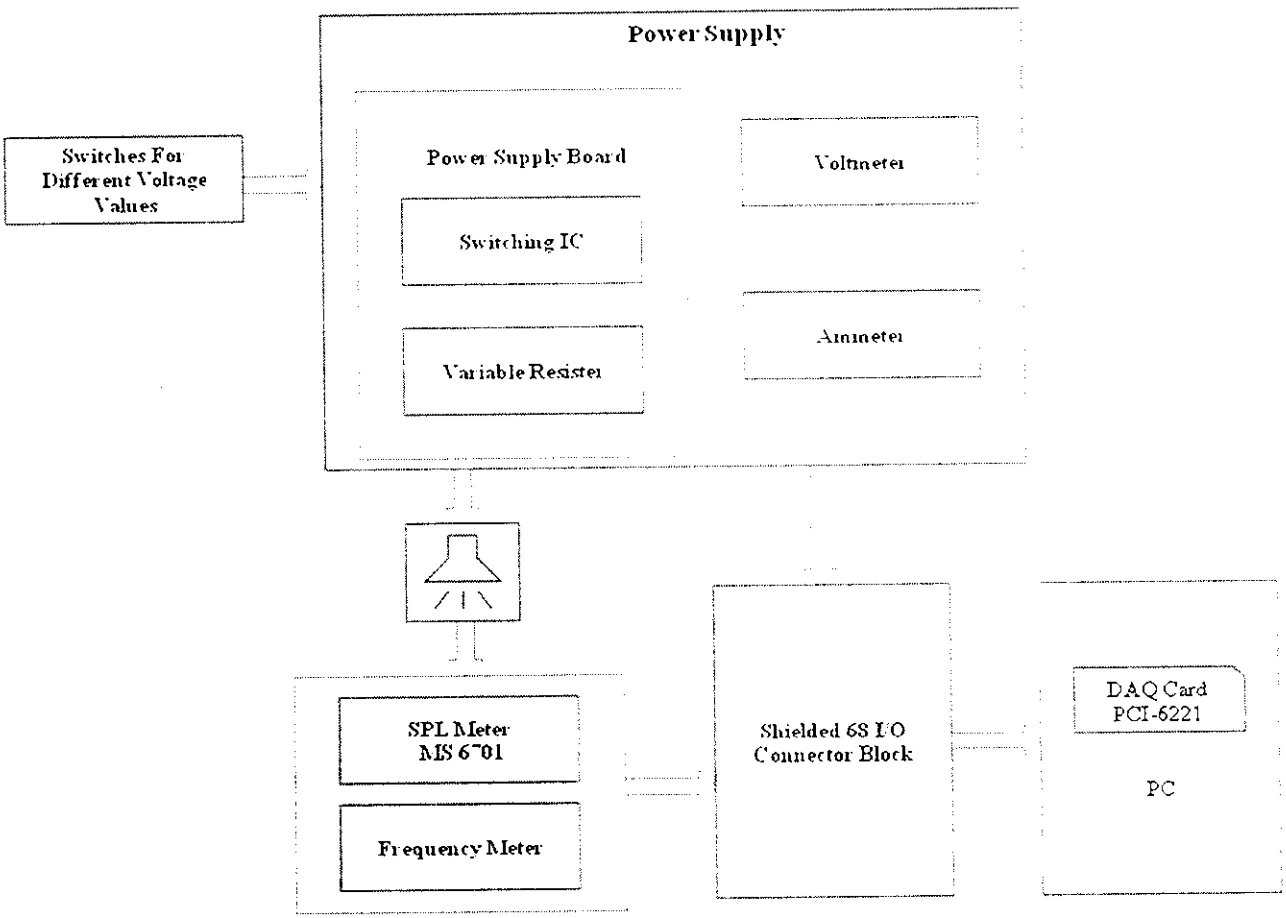


Fig. 8 Block Diagram

In this process of testing horn the compatible type is Electrical horn. In this there are three mode of testing is possible. The three modes include 6V, 12V and 24V mode of which 12 V mode is most commonly used. The main part of testing unit is the Power supply board to which a switch box is connected. This switch box configuration is completely integrated with the PSB where Once the mode of testing is chosen the High and Low limit for the corresponding mode is obtained, then the multiple voltages for the switch box is chosen between this range and this can be set to the switch box. Thus each of the six switches is set with specific voltage and this can adjust based on the need by adjusting the Variable Resistor (Trimpod). In the present testing condition, five switches are chosen with 9V, 10V, 12V, 13V and 14.5V respectively.

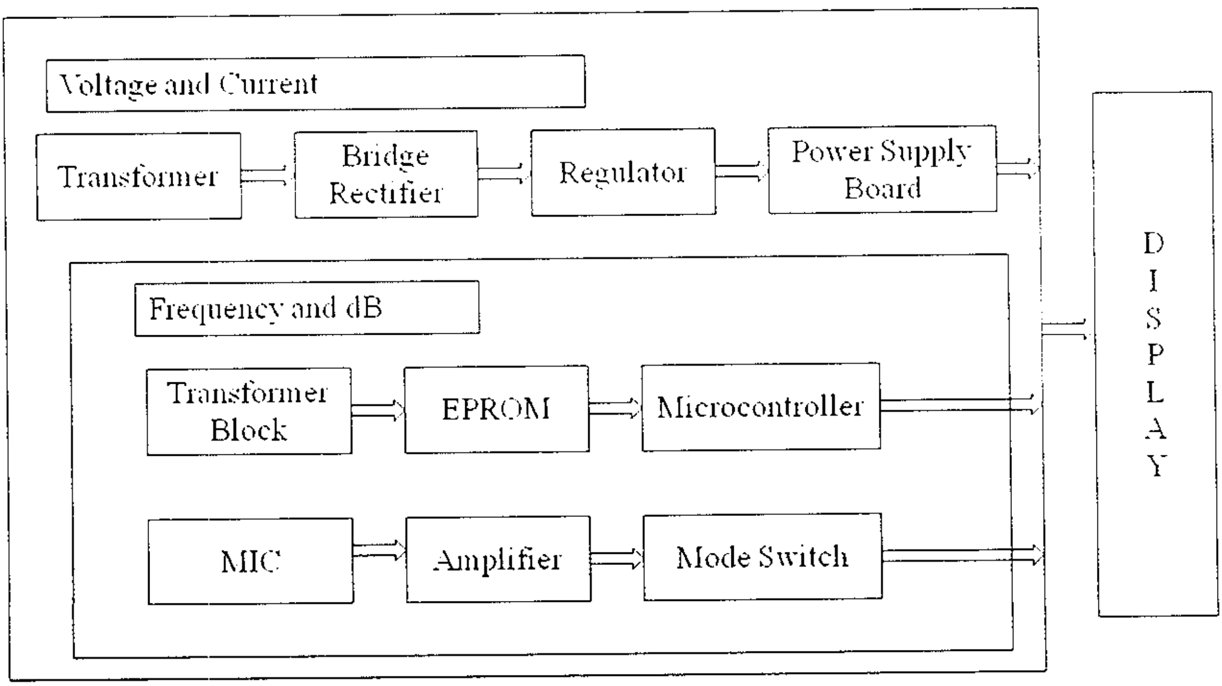


Fig. 9 Block Diagram of Hardware units

Once these voltages are set in switch box, the horn can be mounted and the terminals are connected to the power supply. For each switch pressed during the time of testing this signal is passed to the relay inside the PSB and this switch on the horn. For each horn voltage measured the corresponding current is measured across the shunt resistance.

The Sound Pressure level can be measured using the SPL meter. This unit consists of a MIC, Amplifier and Mode selection unit. The sound from the horn is received through the MIC. This analog signal is amplified and the corresponding voltage is fed to the SCB 68 I/O connector block. In order to receive proper sound from the horn without environmental noise, the SPL meter should be kept in a glass chamber. This improves the precision of the testing system.

The signals from various measuring devices are sent to the SCB 68 I/O connector block. These are acquired by the DAQ card 6221 as analog signals and these signals should not exceed the maximum voltage of 5V.

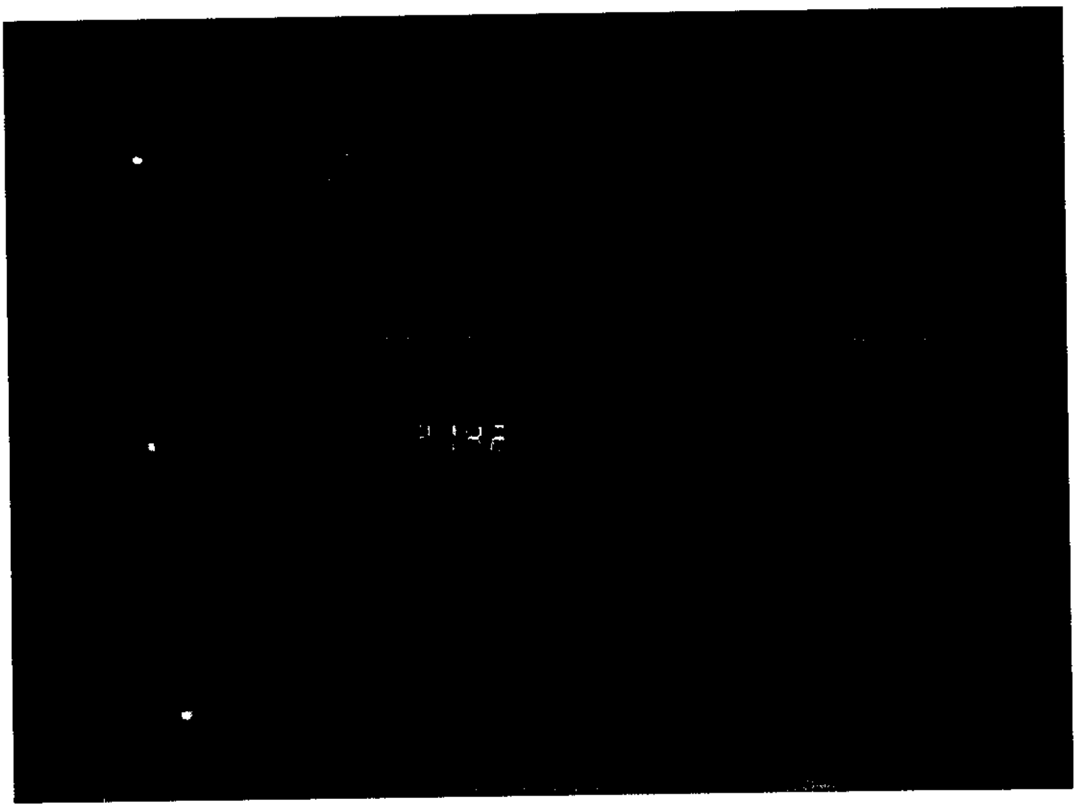
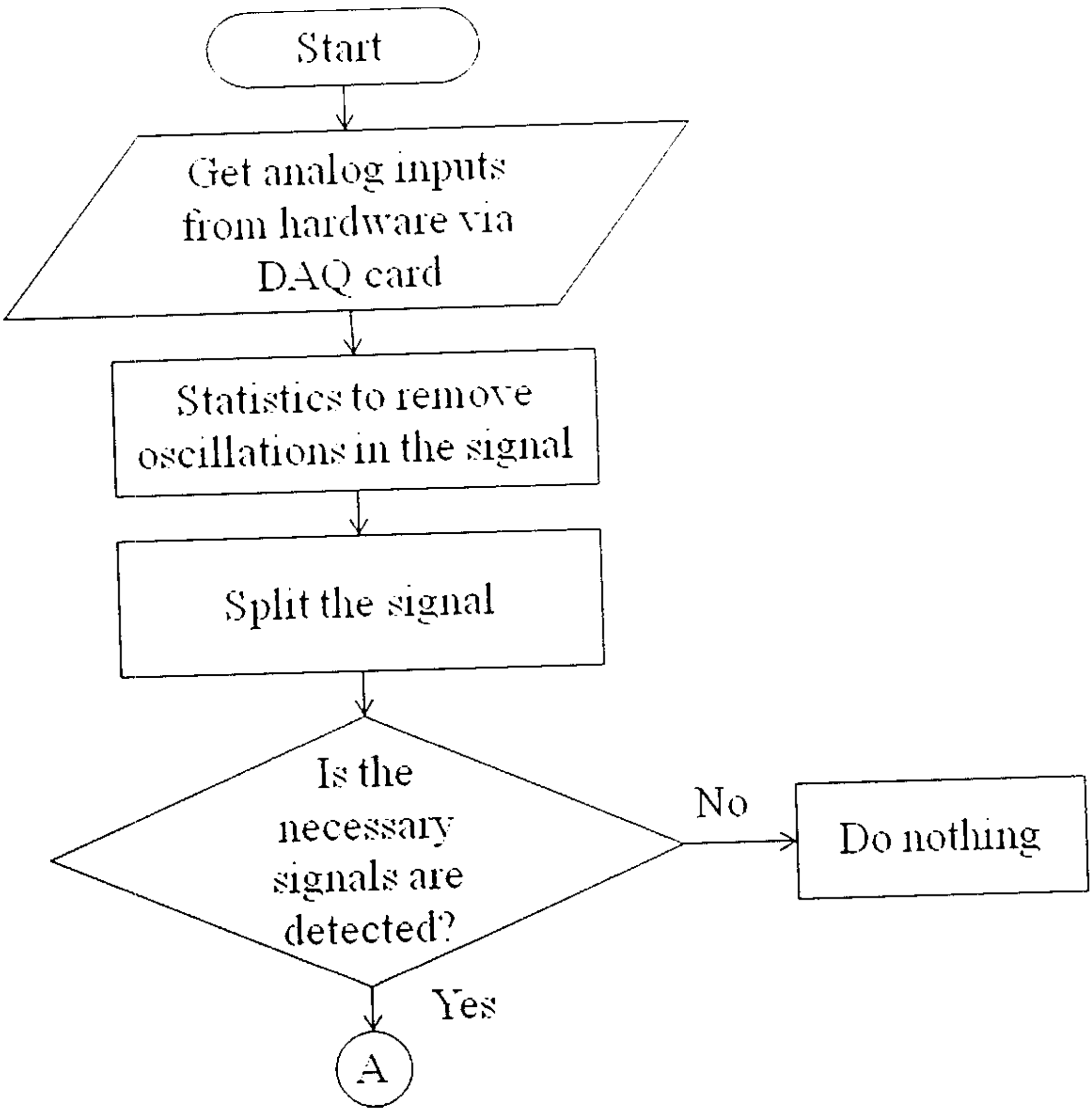
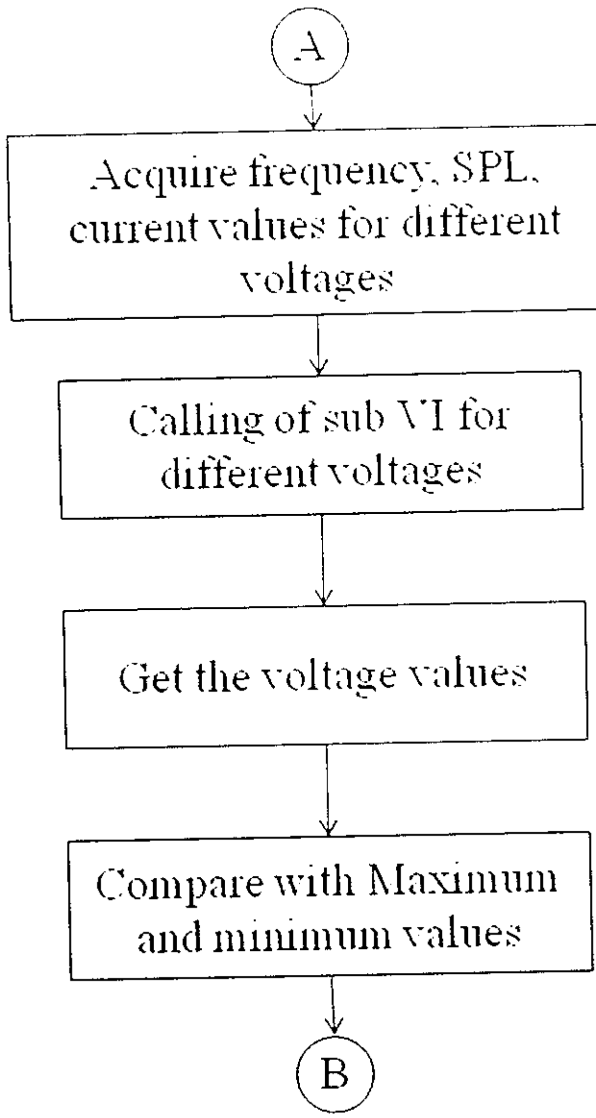


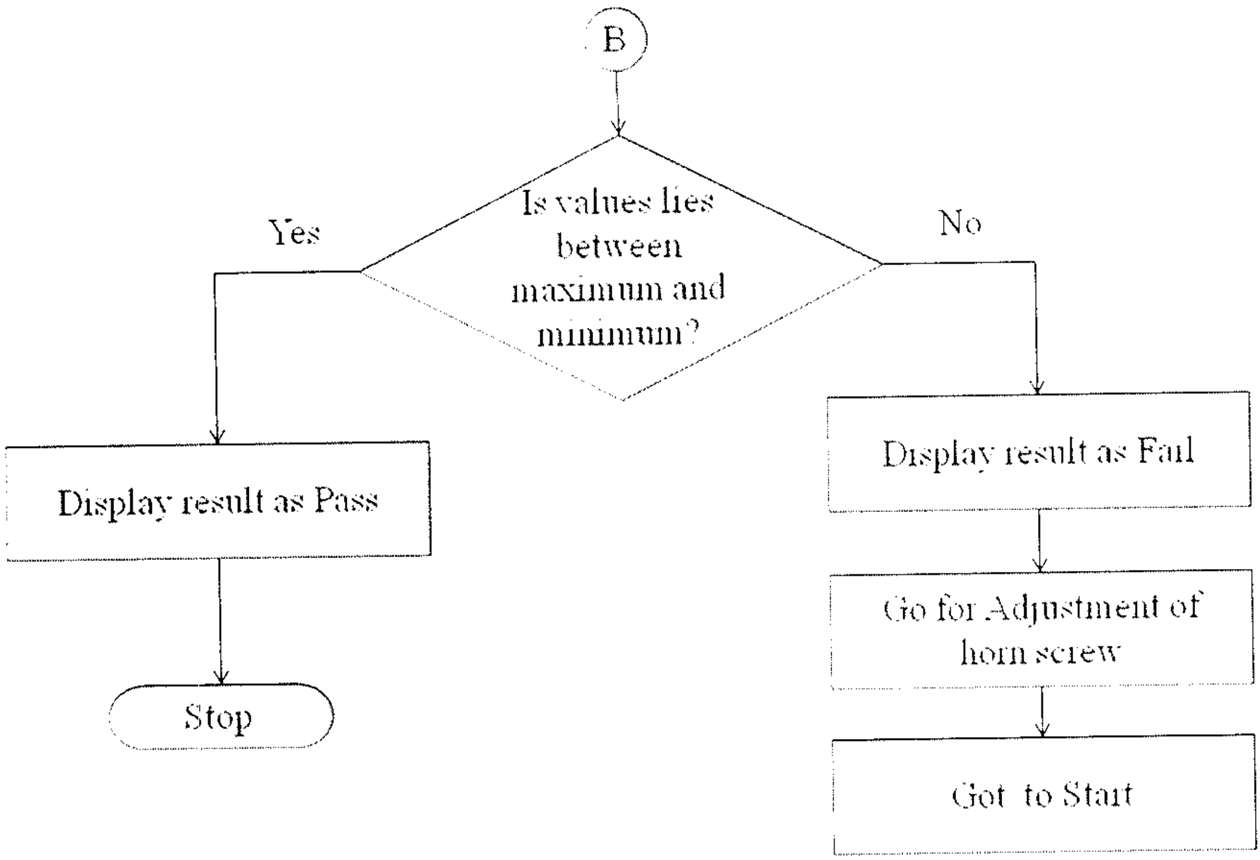
Fig. 10 Real Time Hardware units

2.3 FLOWCHART

The following flowchart represents the overall mechanism of the testing system.




A
Acquire frequency, SPL, current values for different voltages
Calling of sub VI for different voltages
Get the voltage values
Compare with Maximum and minimum values
B


B
Is values lies between maximum and minimum?
Yes
No
Display result as Pass
Stop
Display result as Fail
Go for Adjustment of horn screw
Got to Start

Chapter 3

3. HARDWARE DETAILS

3.1 DC REGULATED POWER SUPPLY

Power supplies are designed to convert high voltage AC mains electricity to a suitable low voltage supply for electronic circuits and other devices.

A power supply can by broken down into a series of blocks, each of which performs a particular function.

For example a regulated supply

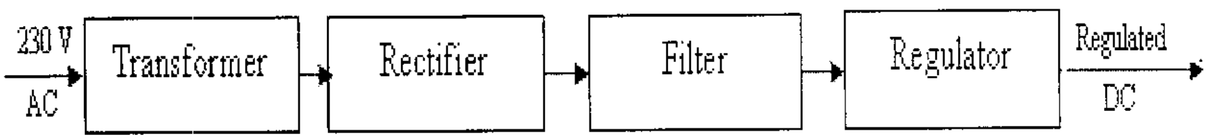


Fig. 11 Regulated Power supply

Each of the blocks is described in more detail below:

- Transformer - Steps down high voltage AC mains to low voltage AC.
- Rectifier - Converts AC to DC, but the DC output is varying.
- Filter-Filters the DC from varying greatly to a small ripple.
- Regulator - Eliminates ripple by setting DC output to a fixed voltage.

3.1.1 TRANSFORMER

The low voltage AC output is suitable for lamps, heaters and special AC motors. It is not suitable for electronic circuits unless they include a rectifier and a smoothing capacitor.

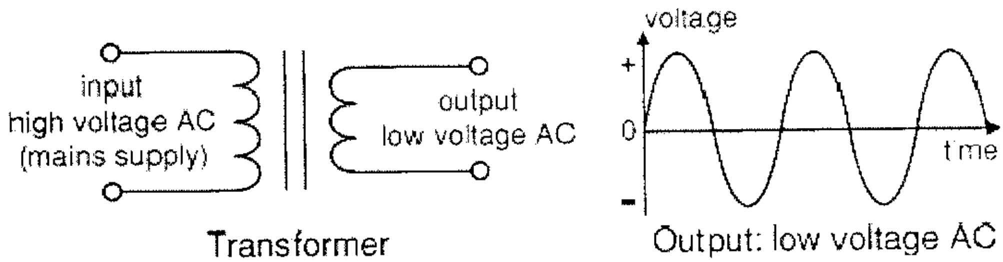


Fig. 12 Transformer

3.1.2 TRANSFORMER + RECTIFIER

The varying DC output is suitable for lamps, heaters and standard motors. It is not suitable for electronic circuits unless they include a smoothing capacitor.

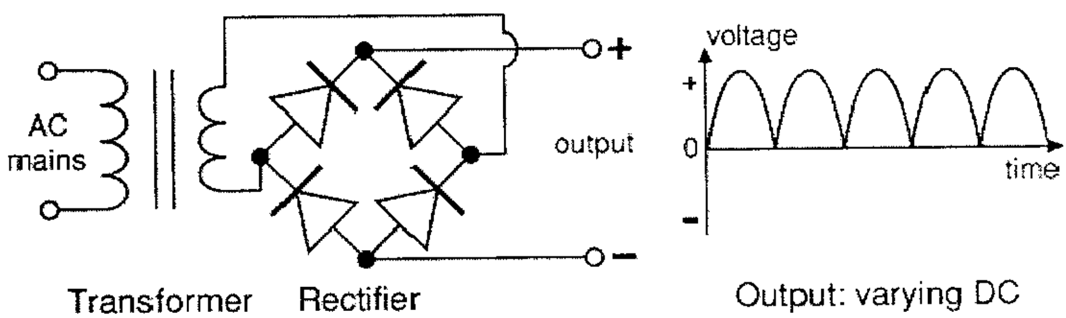


Fig. 13 Transformer with Rectifier

3.1.3 TRANSFORMER + RECTIFIER + FILTER

The smooth DC output has a small ripple. It is suitable for most electronic circuits.

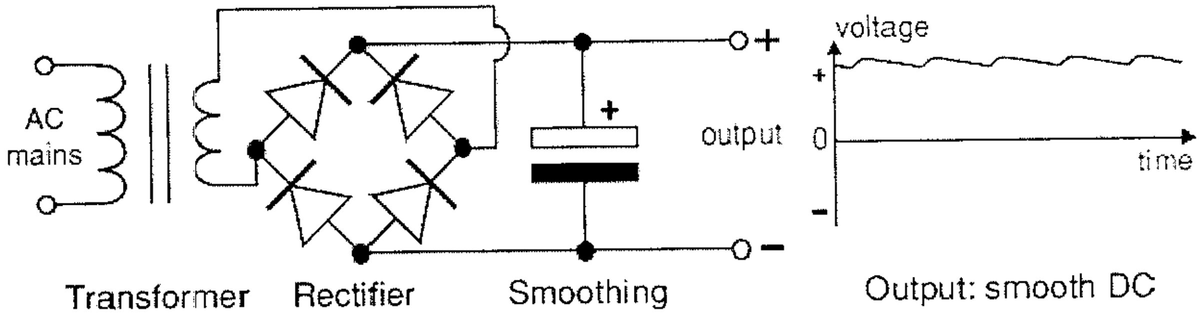


Fig. 14 Transformer with Rectifier and Filter

3.1.4 TRANSFORMER + RECTIFIER + FILTER+ REGULATOR

The regulated DC output is very smooth with no ripple. It is suitable for all electronic circuits.

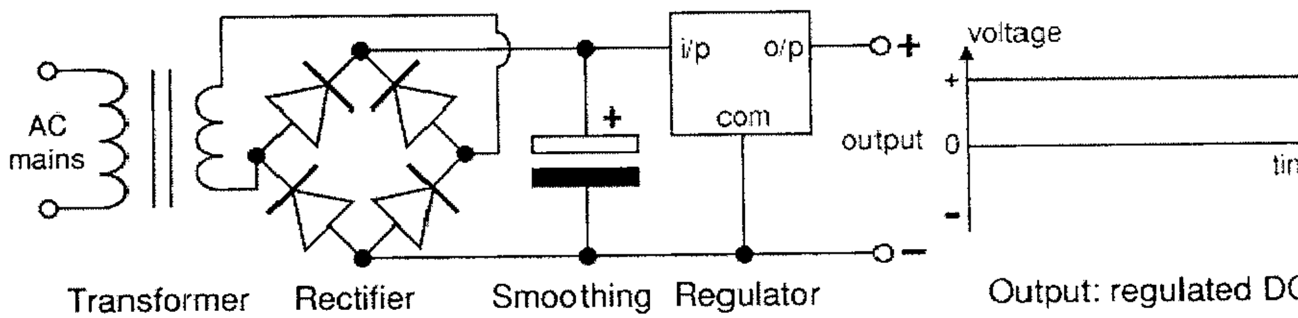


Fig. 15 Transformer with Rectifier, Filter and Regulator

3.1.5 TRANSFORMER

Transformers convert AC electricity from one voltage to another with little loss of power. Transformers work only with AC and this is one of the reasons why mains electricity is AC. Step-up transformers increase voltage, step-down transformers reduce voltage. Most power supplies use a step-down transformer to reduce the dangerously high mains voltage (230V in UK) to a safer low voltage.

The input coil is called the primary and the output coil is called the secondary. There is no electrical connection between the two coils; instead they are linked by an alternating magnetic field created in the soft-iron core of the transformer. The two lines in the middle of the circuit symbol represent the core. Transformers waste very little power so the power out is (almost) equal to the power in. Note that as voltage is stepped down current is stepped up.

The ratio of the number of turns on each coil, called the turn's ratio, determines the ratio of the voltages. A step-down transformer has a large number of turns on its primary (input) coil which is connected to the high voltage mains supply, and a small number of turns on its secondary (output) coil to give a low output voltage.

3.1.6 RECTIFIER

There are several ways of connecting diodes to make a rectifier to convert AC to DC. The bridge rectifier is the most important and it produces full-wave varying DC. A full-wave rectifier can also be made from just two diodes if a centre-tap transformer is used, but this method is rarely used now that diodes are cheaper. A single diode can be used as a rectifier but it only uses the positive (+) parts of the AC wave to produce half-wave varying DC.

3.1.7 BRIDGE RECTIFIER

A bridge rectifier can be made using four individual diodes, but it is also available in special packages containing the four diodes required. It is called a full-wave rectifier because it uses the entire AC wave (both positive and negative sections). 1.4V is used up in the bridge rectifier because each diode uses 0.7V when conducting and there are always two diodes conducting, as shown in the diagram below.

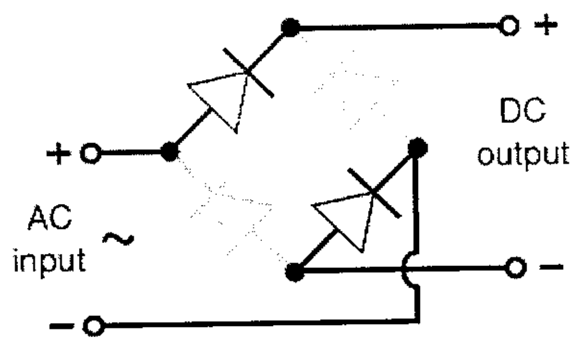


Fig. 16 Bridge Rectifier

Bridge rectifiers are rated by the maximum current they can pass and the maximum reverse voltage they can withstand (this must be at least three times the supply RMS voltage so the rectifier can withstand the peak voltages). Please see the Diodes page for more details, including pictures of bridge rectifiers.

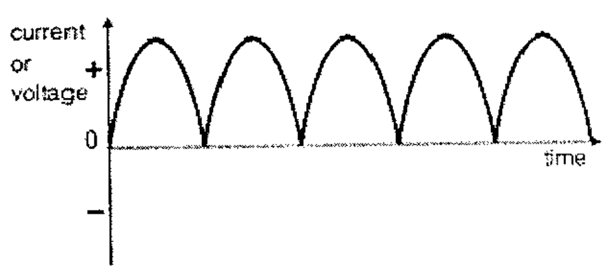


Fig. 17 Bridge Rectifier output waveform

3.1.8 SINGLE DIODE RECTIFIER

A single diode can be used as a rectifier but this produces half-wave varying DC which has gaps when the AC is negative. It is hard to smooth this sufficiently well to supply electronic circuits unless they require a very small current so the smoothing capacitor does not significantly discharge during the gaps. Please see the Diodes page for some examples of rectifier diodes.

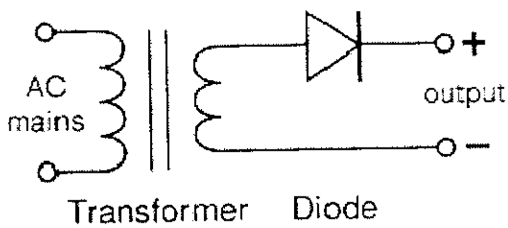


Fig. 18 Single Diode Rectifier

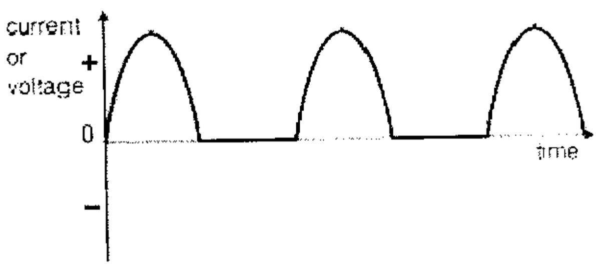


Fig. 19 Single Diode Rectifier output waveform

3.1.9 FILTERING

Smoothing is performed by a large value electrolytic capacitor connected across the DC supply to act as a reservoir, supplying current to the output when the varying DC voltage from the rectifier is falling. The diagram shows the unsmoothed varying DC (dotted line) and the smoothed DC (solid line).

The capacitor charges quickly near the peak of the varying DC, and then discharges as it supplies current to the output.

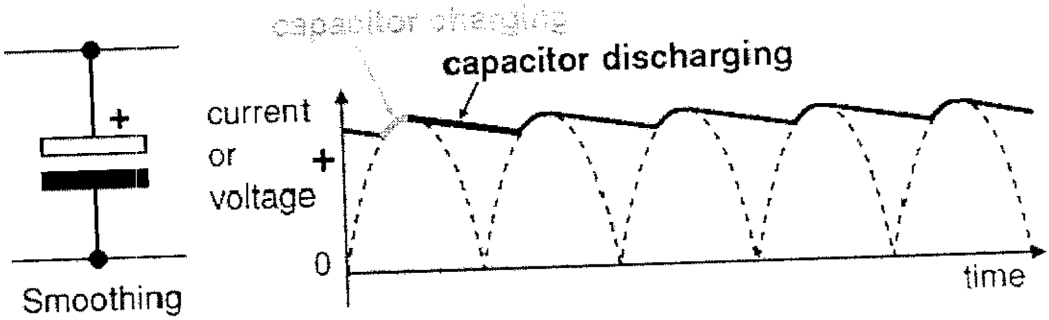


Fig. 20 Filter and its output waveform

Smoothing is not perfect due to the capacitor voltage falls a little as it discharges, giving a small ripple voltage. For many circuits a ripple which is 10% of the supply voltage is satisfactory and the equation below gives the required value for the smoothing capacitor. A larger capacitor will give fewer ripples. The capacitor value must be doubled when smoothing half-wave DC.

3.1.10 REGULATOR

Voltage regulator ICs are available with fixed (typically 5, 12 and 15V) or variable output voltages. They are also rated by the maximum current they can pass. Negative voltage regulators are available, mainly for use in dual supplies. Most regulators include some automatic protection from excessive current ('overload protection') and overheating ('thermal protection').

Many of the fixed voltage regulator ICs has 3 leads and look like power transistors, such as the 7805 +5V 1A regulator shown on the right. They include a hole for attaching a heat sink if necessary. For low current power supplies a simple voltage regulator can be made with a resistor and a zener diode connected in reverse as shown in the diagram. Zener diodes are rated by their breakdown voltage V_Z and maximum power P_Z (typically 400mW or 1.3W).

The resistor limits the current (like an LED resistor). The current through the resistor is constant, so when there are no output current all the current flows through the zener diode and its power rating P_Z must be large enough to withstand this.

Choosing a zener diode and resistor

- The zener voltage V_Z is the output voltage required
- The input voltage V_S must be a few volts greater than V_Z (this is to allow for small fluctuations in V_S due to ripple)
- The maximum current I_{MAX} is the output current required plus 10%
- The zener power P_Z is determined by the maximum current: $P_Z > V_Z \times I_{MAX}$
- The resistor resistance: $R = (V_S - V_Z) / I_{MAX}$
- The resistor power rating: $P > (V_S - V_Z) \times I_{MAX}$

3.2 FREQUENCY METER

The frequency counter has to count the number of cycles per second of an incoming signal. Hence we need a device to count. In electronics circuits, counter ICs are available for counting. These IC's can count the input pulses. The count is given as coded output from the IC (in binary form or BCD form). The count must be converted into decimal digit to be understood by human beings. More number of IC's can be cascaded to increase the number of digits.

The number of digits required for the counter to display the count value depends on the application and the accuracy needed. In our design we use a single 4 bit BCD high-speed CMOS counter chips. One chip is used for one digit and we use 7 similar ICs to get seven digit counter. Also we use CMOS decoder IC to decode the BCD output of the counter to drive 7 segment displays.

Since the counter can count only digital pulses, we need to convert the incoming signal wave to digital pulse or we should obtain one pulse for every input wave. Hence we need a special circuit to shape the input wave into a square wave of same frequency and amplitude confined to the TTL signal levels. A signal conditioning section is needed for this purpose.

The input Signal-conditioning section consists of the following stages.

1. Amplifier or attenuation stage
2. TTL level converter stage

Besides the above initial stages, sometimes a few more additional stages such as input protection stages, filter stages, etc are can be found in some designs. The input whose frequency is to measure is given to the input stage consisting of the above and the output of this stage is the square pulses. Now the square pulses are given to the counter to count the number of pulses for a fixed duration. If the duration is 1 second, then the counter displays a value that equals to the number of cycles per second, now if we want to measure a frequency of say 20MHz, the counter should display 20000000. This means the counter should have 8 digits to display. Now the resolution of the counter (minimum change of frequency that can be displayed) is 1Hz. If we do not require that much of resolution, we can reduce the number of digits.

For example, if we are counting the input cycles for duration of 0.1 seconds, the display shows 2000000. Now if we put decimal points after two digits from the left of the display, the frequency can be read in MHz, in both cases, the resolution for the later being 10Hz. The time for which the counter is counting is called as gating time and if the gating is says 1 milli second; we get a display with resolution of 1 kHz. A frequency counter must always count the input frequency and display frequency. This means there should be an arrangement to count the input for a fixed time, display the reading.

While displaying the reading, the counter should clear again to read input again. Then only we get a continuous reading that displays the correct frequency at all times. A control circuit is needed to achieve this. The function of the control circuit to generate the following signals.

1. Clear the counter for refreshing
2. Provide a precision gating signal to allow the input pulses to the counter circuit
3. Latch the count value to decode and display
4. Repeat the above steps continuously to get a continuous reading

The control circuit must operate with precision timing. This is achieved by deriving all timing signals from a crystal oscillator or time base circuit. The accuracy of the counter solely depends on the stability and accuracy of the time base circuit.

3.2 F-V CONVERTER LM2017

3.2.1 FEATURES

- Tachometer has built-in hysteresis with either differential input or ground referenced input
- Built-in zener on LM2917
- Ground referenced tachometer is fully protected from damage due to swings above VCC and below ground

3.2.2 ADVANTAGES

- Output swings to ground for zero frequency input. Easy to use
- $VOUT = f_{IN} \times VCC \times R_1 \times C_1$
- Zener regulator on chip allows accurate and stable frequency to voltage or current conversion (LM2917)

3.2.2 APPLICATIONS

- Horn control
- Frequency to voltage conversion (tachometer)

3.3 SOUND PRESSURE LEVEL METER

This Digital Sound Level Meter is an instrument to measure Sound Pressure Level in decibels (dB). MS6701 is featured with wide measuring range (30 ~ 130 dB), Bar-Graph Indication, A/C frequency weighting, Fast / Slow response and Maximum Hold function. The meter also provides a windscreen to filter-out unwanted signals. MS6701is a portable, easy to use and handy instrument for sound quality control in office, home, school and construction site. The meter has wide range of applications such as noise pollution studies, research and other industrial use.

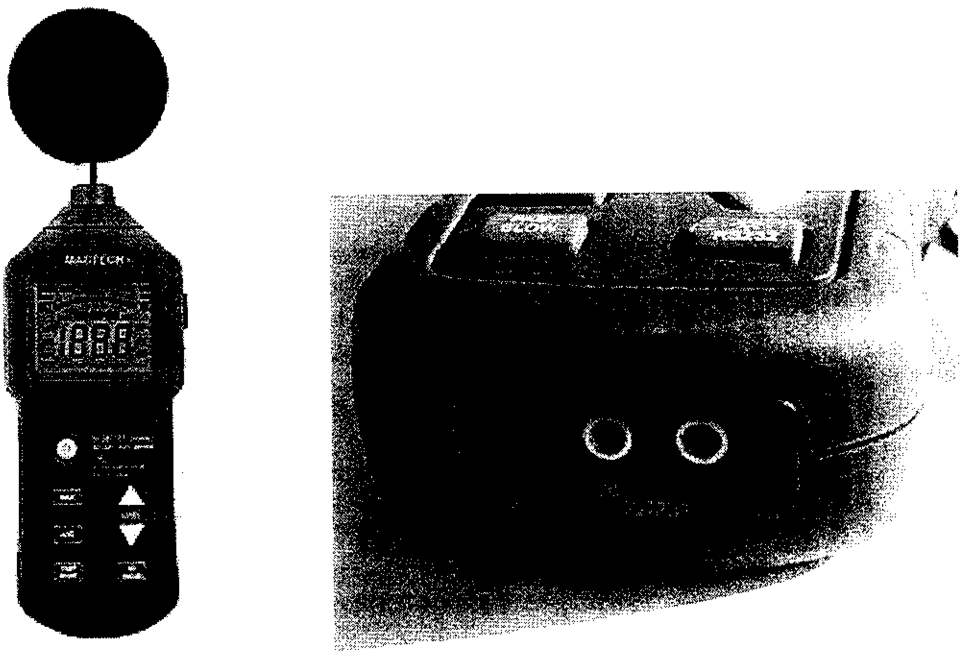


Fig. 21 Digital sound level meter MS6701

3.3.1 METER SPECIFICATIONS

- Wide Measuring Range: 30 ~ 130 dB
- Maximum hold function
- Large LCD screen with 4 digits reading
- Sound Level: 30 ~ 130 dB with Level selecting button switches
    1. Level 1: 30 ~ 80 dB
    2. Level 2: 40 ~ 90 dB
    3. Level 3: 50 ~ 100 dB
    4. Level 4: 60 ~ 110 dB
    5. Level 5: 70 ~ 120 dB
    6. Level 6: 80 ~ 130 dB
    7. Level 7: 30 ~ 130 dB

3.3.2 FEATURES

- LCD digital display
- Analog bar indicator
- Wide dynamic range
- Auto/Manual range
- Fast/Slow response selectable
- MAX value hold function
- A/C weighting selection
- Date and time display

- AC/DC auxiliary output
- Memory function
- RC232C interface
- Computer record graph software
- Back light
- Low power indication
- Measurement range: 30dB ~ 130dB
- Accuracy: ±2dB
- Resolution: 0.1dB
- Display: 3 $^{1/2}$ digitals
- Sample rate: 2 times/s
- Frequency range: 30Hz ~ 8kHz
- Memory function: 16000 records
- Over range indication "UNDER" or "OVER"
- Low power indication
- Battery voltage 6 x 1.5V (AAA)

3.4 NI CARD - PCI 6221

3.4.1 OVERVIEW

The National Instruments PCI-6221 is a low-cost multifunction M Series data acquisition (DAQ) board optimized for cost-sensitive applications. Also consider the high-speed M Series devices for 5X faster sampling rates or the high-accuracy M Series devices for 4X resolution and superior measurement accuracy.

Low-cost M Series devices incorporate advanced features such as the NI-STC 2 system controller, NI-PGIA 2 programmable amplifier, and NI-MCal calibration technology to increase performance and accuracy.

The specifications are,

- Two 16-bit analog outputs; 24 digital I/O; 32-bit counters
- Traceable calibration certificate and more than 70 signal conditioning options
- Correlated DIO (8 clocked lines, 1 MHz)
- NI-MCal calibration technology for increased measurement accuracy
- Select high-speed M Series for 5X faster sampling rates or high-accuracy M Series for 4X resolution.
- NI-DAQmx driver software and NI LabVIEW SignalExpress LE interactive data-logging software

3.4.2 DRIVER SOFTWARE

M Series devices work with multiple operating systems using three driver software options including NI-DAQmx, NI-DAQmx Base, and the Measurement Hardware DDK. Browse the information in the Resources tab to learn more about driver software or download a driver. M Series devices are not compatible with the Traditional NI-DAQ (Legacy) driver.

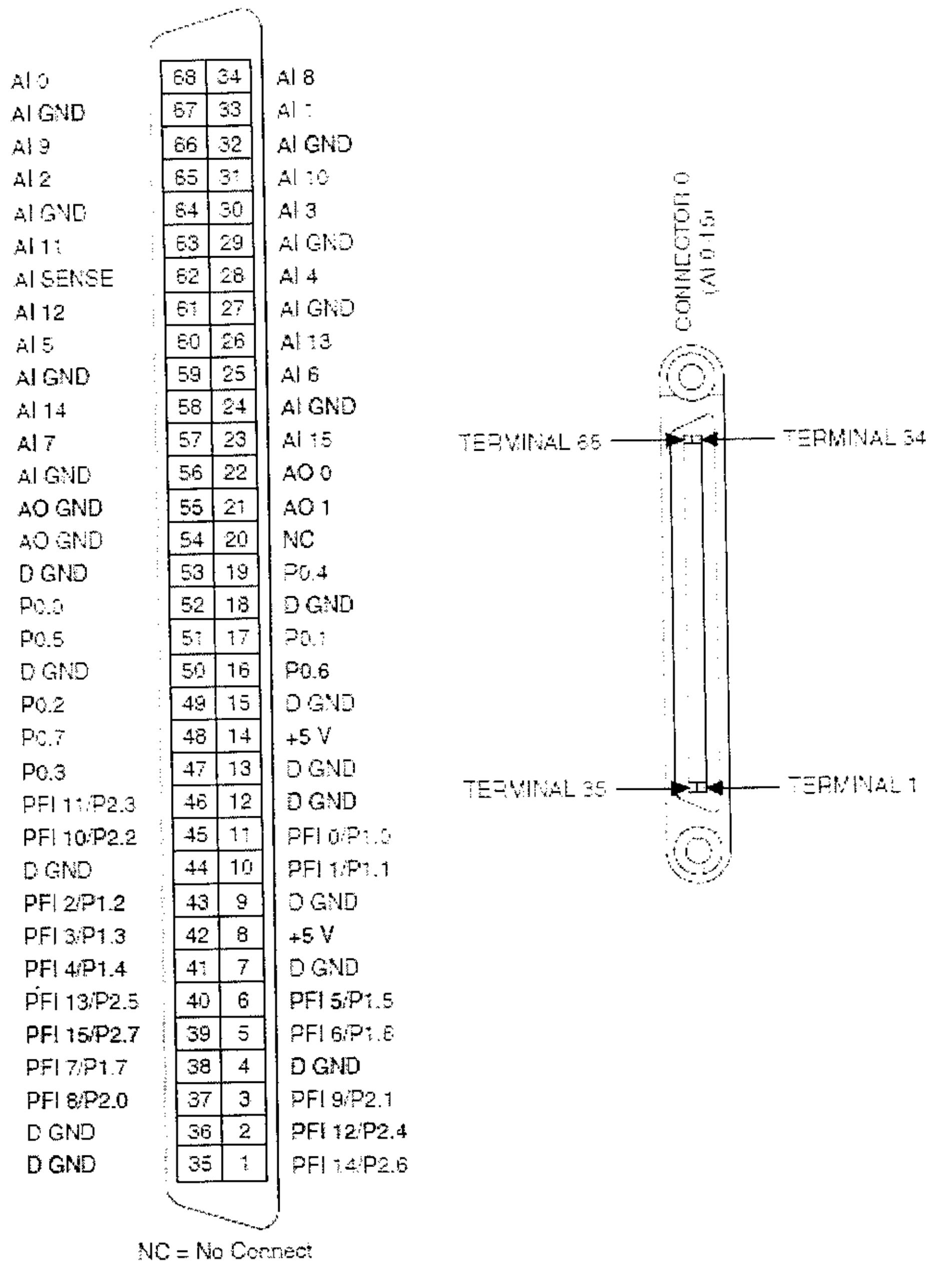


Fig. 22 Pin out diagram of PCI 6221

3.4.3 APPLICATION SOFTWARE

Every M Series data acquisition device includes a copy of NI LabVIEW SignalExpress so you can quickly acquire, analyze, and present data without programming. In addition to LabVIEW SignalExpress, M Series data acquisition devices are compatible with the following versions (or later) of NI application software – LabVIEW 7.x, LabWindow/CVI 7.x, or Measurement Studio 7.x; or LabVIEW with the LabVIEW Real-Time Module 7.1. M Series data acquisition devices are also compatible with Visual Studio .NET, C/C++, and Visual Basic 6.

3.4.4 INSTALLATION PROCEDURES

INSTALL THE NI DRIVER SOFTWARE

- Install NI-DAQ software from the CD and follow the instructions given by the setup

Note: NI-DAQ software to be installed before hardware installation

INSTALL THE NI HARDWARE

The NI 6221 fits in any PCI system slot in the computer. However, to achieve best noise Performance, leave as much room as possible between the NI 6221 and other devices. The following are general installation instructions, but consult the computer user manual or technical reference manual for specific instructions and warnings.

Note Follow the guidelines in the computer documentation for installing plug-in hardware.

1. Power off and unplug the computer.
2. Remove the cover.

3. Make sure there are no lighted LEDs on the motherboard. If any are lit, wait until they go out before continuing the installation.
4. Remove the expansion slot cover on the back panel of the computer.
5. Insert the NI 6221 into a PCI system slot. Gently rock the device to ease it into place. It may be a tight fit, but do not force the device in to place.
6. If required, screw the mounting bracket of the device to the back panel rail of the computer.
7. Visually verify the installation. Make sure the device is not touching other devices or components and is fully inserted into the slot.
8. Replace the cover.
9. Plug in and power on the computer.

The NI 6013/6014 is now installed. You are now ready to configure the device.

3.4.5 CONFIGURING THE CARD

1. There should be an icon for the Measurement and Automation Explorer on the desktop. Click on it to run the program. Select the PCI 6221 Card.
2. Click on Self-Test. It should pass.

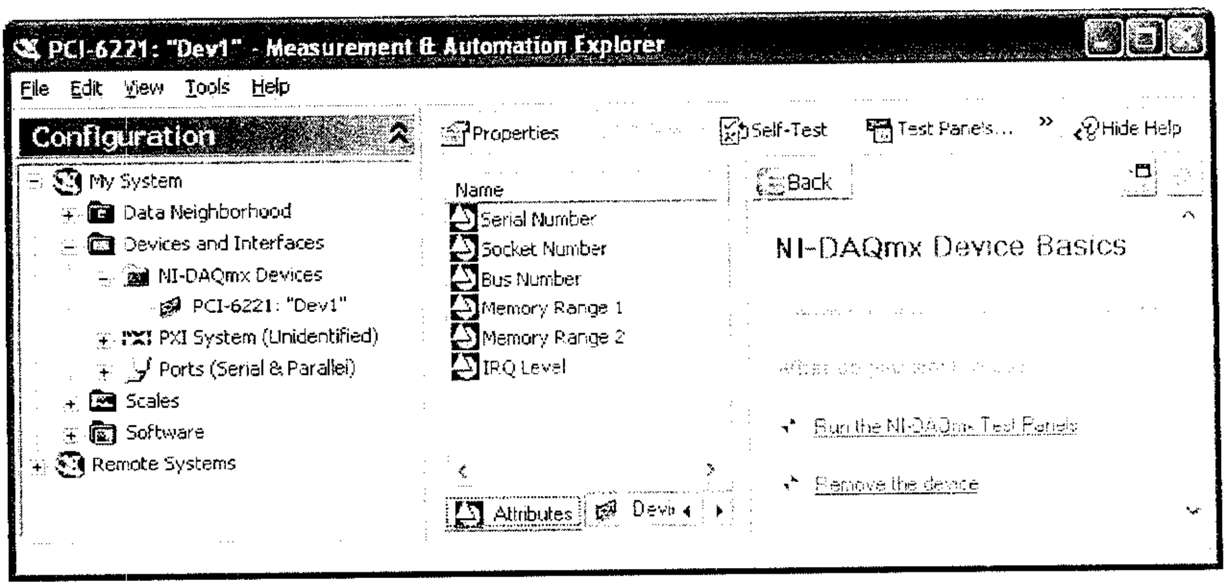


Fig. 23 Configuring the Card

3.5 Shielded I/O Connector Block

The NI SCB-68 is a shielded I/O connector block for interfacing I/O signals to plug-in data acquisition (DAQ) devices with 68-pin connectors. Combined with the shielded cables, the SCB-68 provides rugged, very low-noise signal termination.

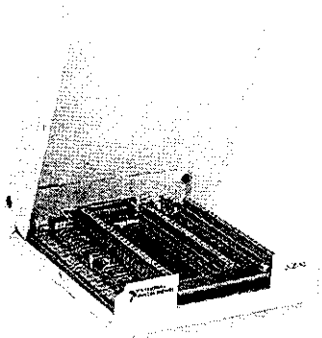


Fig. 24 Shielded I/O Connector Block for DAQ Devices with 68-Pin Connectors

It is compatible with single- and dual-connector NI X Series and M Series devices with 68-pin connectors. The connector block is also compatible with most NI E, B, S, and R Series DAQ devices.

- Shielded I/O connector block for use with 68-pin X, M, E, B, S, and R Series DAQ devices
- Screw terminals for easy I/O connections or for use with the CA-1000
- 2 general-purpose breadboard areas
- Onboard cold-junction compensation sensor for low-cost thermocouple measurements
- For highly accurate thermocouple measurements use SCC or SCXI signal conditioning

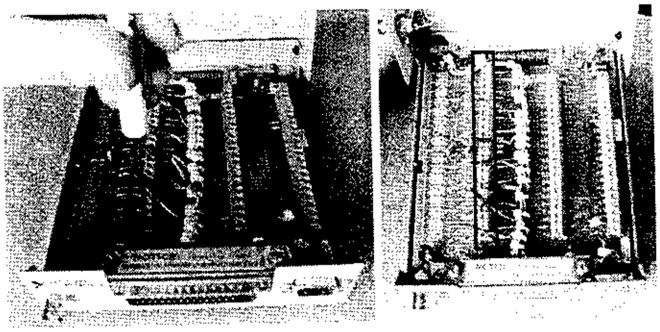


Fig. 25 Connections in Shielded I/O Connector Block

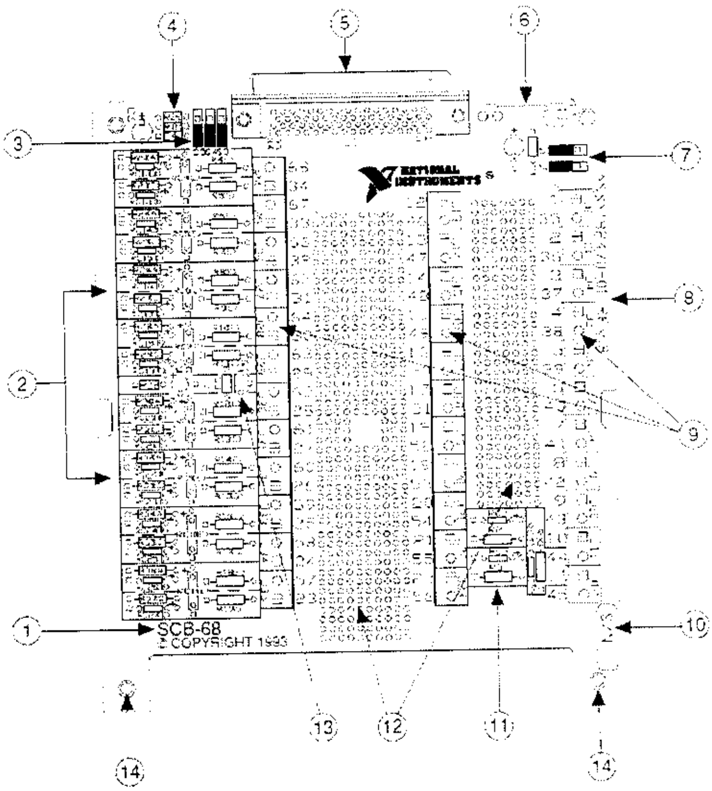


Fig. 26 IMAQ SCB-68 Terminal Block Parts Locator Diagram

1 Product Name

2 Pads for Analog Input Conditioning

3 Switches S3, S4, and S5

4 R20 (see fuse and power)

5 68-Pins I/O Connector

6 Fuse (0.8 A)

7 Switches S1 and S2

8 Assembly Number and Revision Letter

9 Screw Terminals

10 Serial Numbers

11 RC Filters and Attenuators for DACO, DAC1, and Ext. Trig.

12 Breadboard Areas

13 Cold-Junction Compensation Temperature Sensor (not used)

14 Board Mount Screws

3.6 CONNECTION DETAILS

PIN NO	SIGNAL NAME	SWITCH NO	DAQ PIN NO
1	DIO 0	PS Switching O/p 1	52
2	DIO 1	PS Switching O/p 2	17
3	DIO 2	PS Switching O/p 3	49
4	DIO 3	Solenoid o/p to punch result	47
5	DIO 4	Test Start PB	19
6	DIO 5	PS Switching enable o/p	51
7	DI GND		5

Table No. 2 Supply switching connection details (9 Pin D types)

PIN NO	SIGNAL NAME	DESCRIPTION	DAQ PIN NO
1	AICH 0	CURRENT I/P	68
3	AICH 0	VOLTAGE I/P	33
5	AICH 0	SPARE	28
8,9	AIGND		27

Table No. 3 Analog Connection details for V & I (9 Pin D Type)

PIN NO	SIGNAL NAME	DESCRIPTION	DAQ PIN NO
1	AICH 2	FREQ. I/P	65
3	AICH 3	SPL I/P	30
5	AICH 5	SPARE	6
8,9	AIGND		59

Table No. 4 Frequency/dB Unit

PIN NO	SIGNAL NAME	DESCRIPTION	DAQ PIN NO
1	DIO 6	HV ON o/p	16
3	DIO 7	HV/Body Insulation STATUS/ Read i/p	48
5	DI GND		15

Table No. 5 High Voltage Unit

Chapter 4

4.1 LabVIEW SOFTWARE

Step 1: Getting DAQ Assistant

Click,

Functions →Input →DAQ Assist

After selecting DAQ Assistant the function block will be initialized.

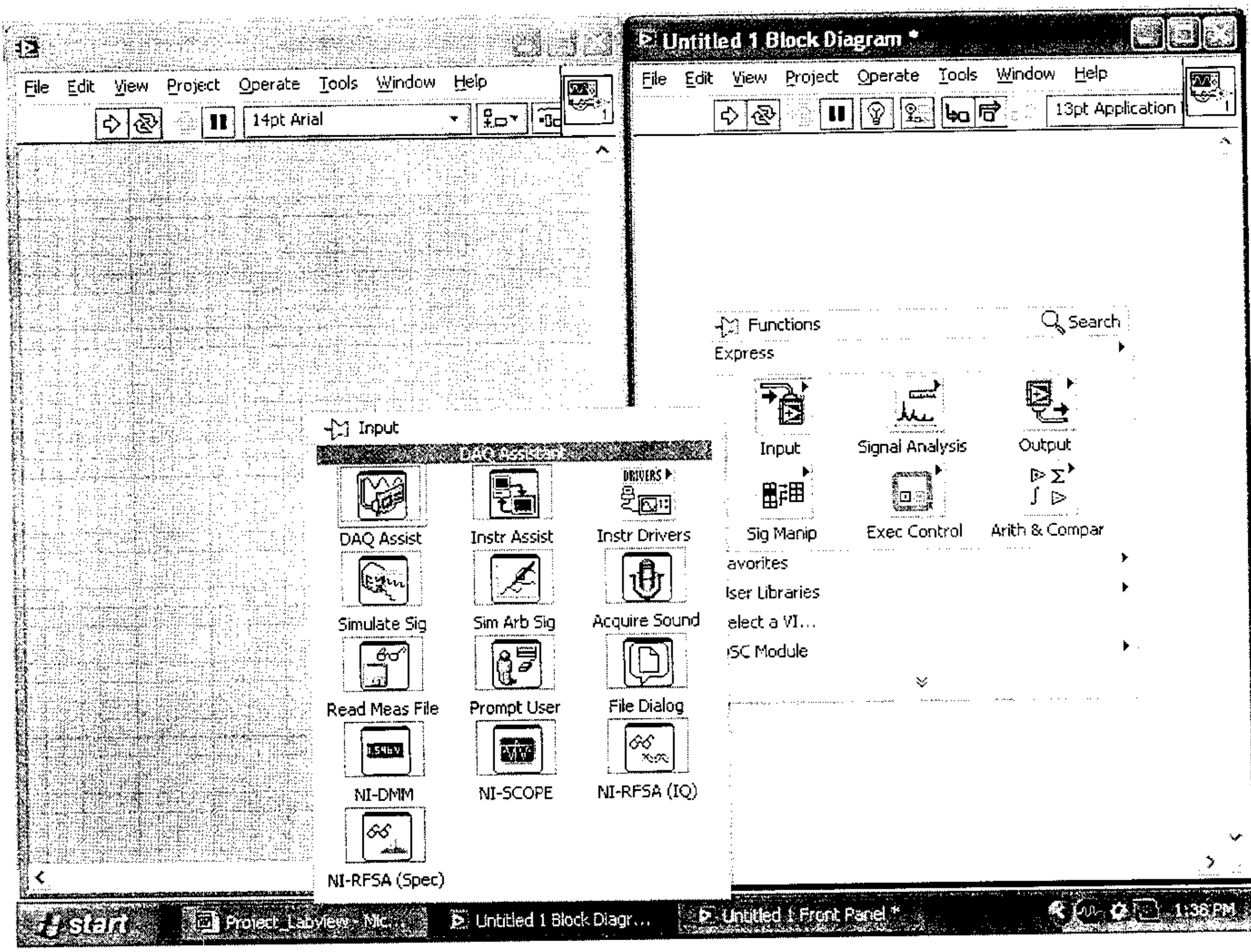


Fig. 27 DAQ Assistant

Step 2: Selecting the measurement type

DAQ Assistant acquires analog signals from the hardware.

In the Create New Express Task window click,

Acquire Signals→ Analog Input→Voltage

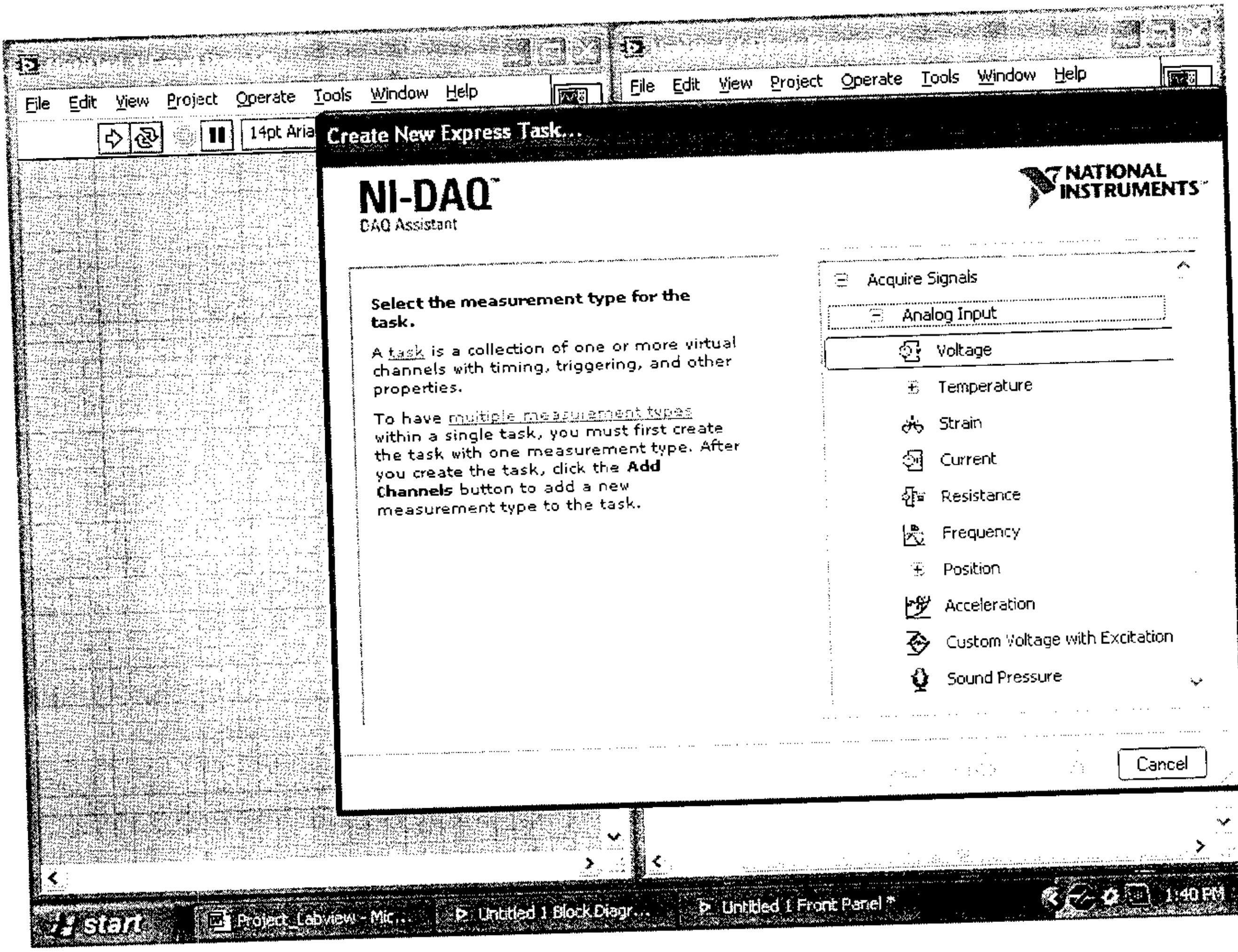


Fig. 28 New Express Task

Step 3: Assigning Physical channels

For the required analog input signals the various channels are allocated.

In the Supported Physical Channel tab select the channels such as ai0, ai1, ai2 and ai3.

Click Finish.

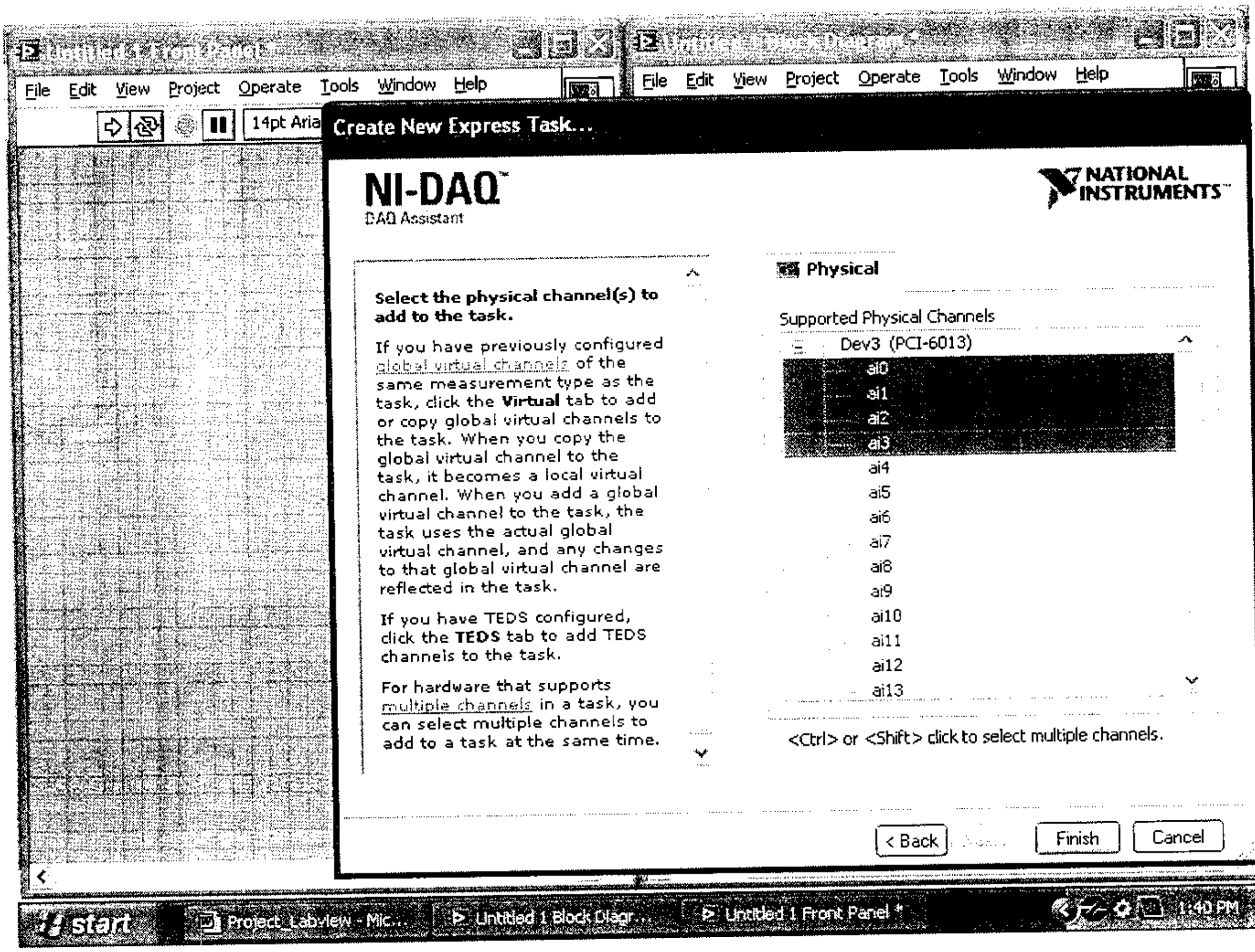


Fig. 29 Physical Channel Selection

Step 4: Selecting channels and specifying signal input range.

For the each channel specify the signal input range scaled units and Terminal Configuration.

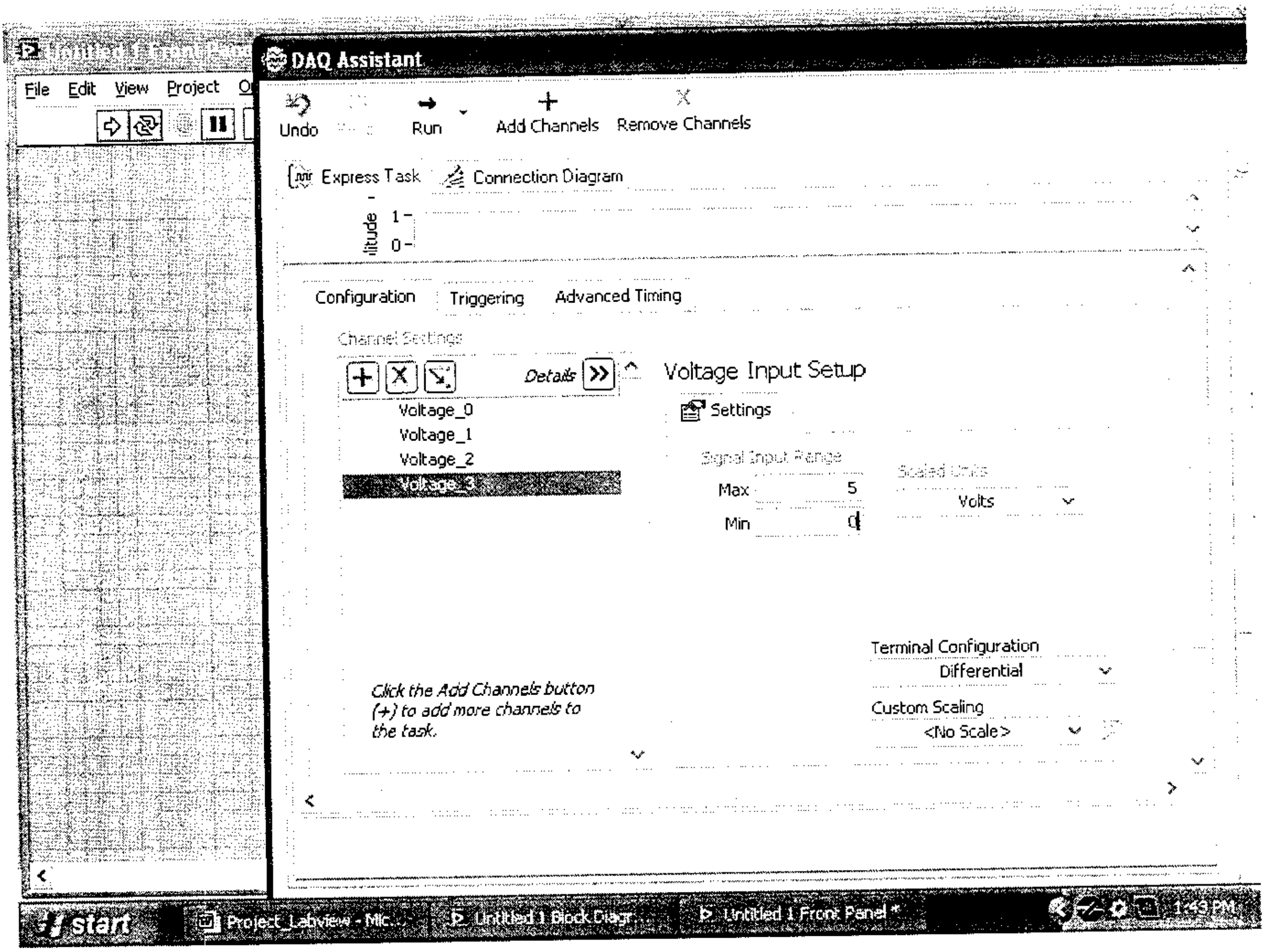


Fig. 30 Express Task Configuration

Then click OK to build the DAQ Assistant.

Step 5: Stabilization of Signals

Statistics performs statistical calculations on time domain or scalar data. Also it minimizes the oscillations of the acquiring signals.

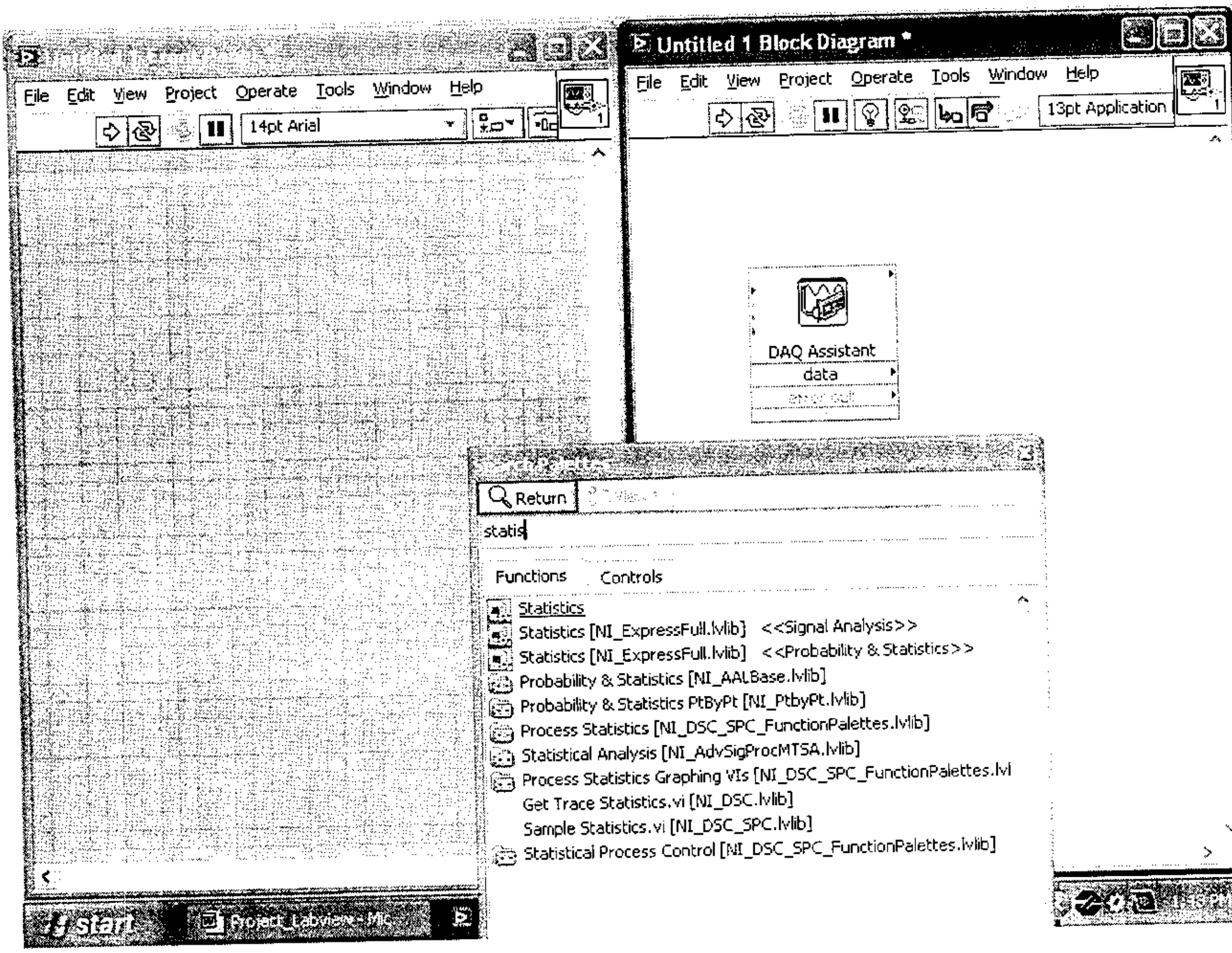


Fig. 31 Statistics Window

Step 6: Configuring Statistics

In the configuring statistics window select Arithmetic Mean as the statistical calculations.

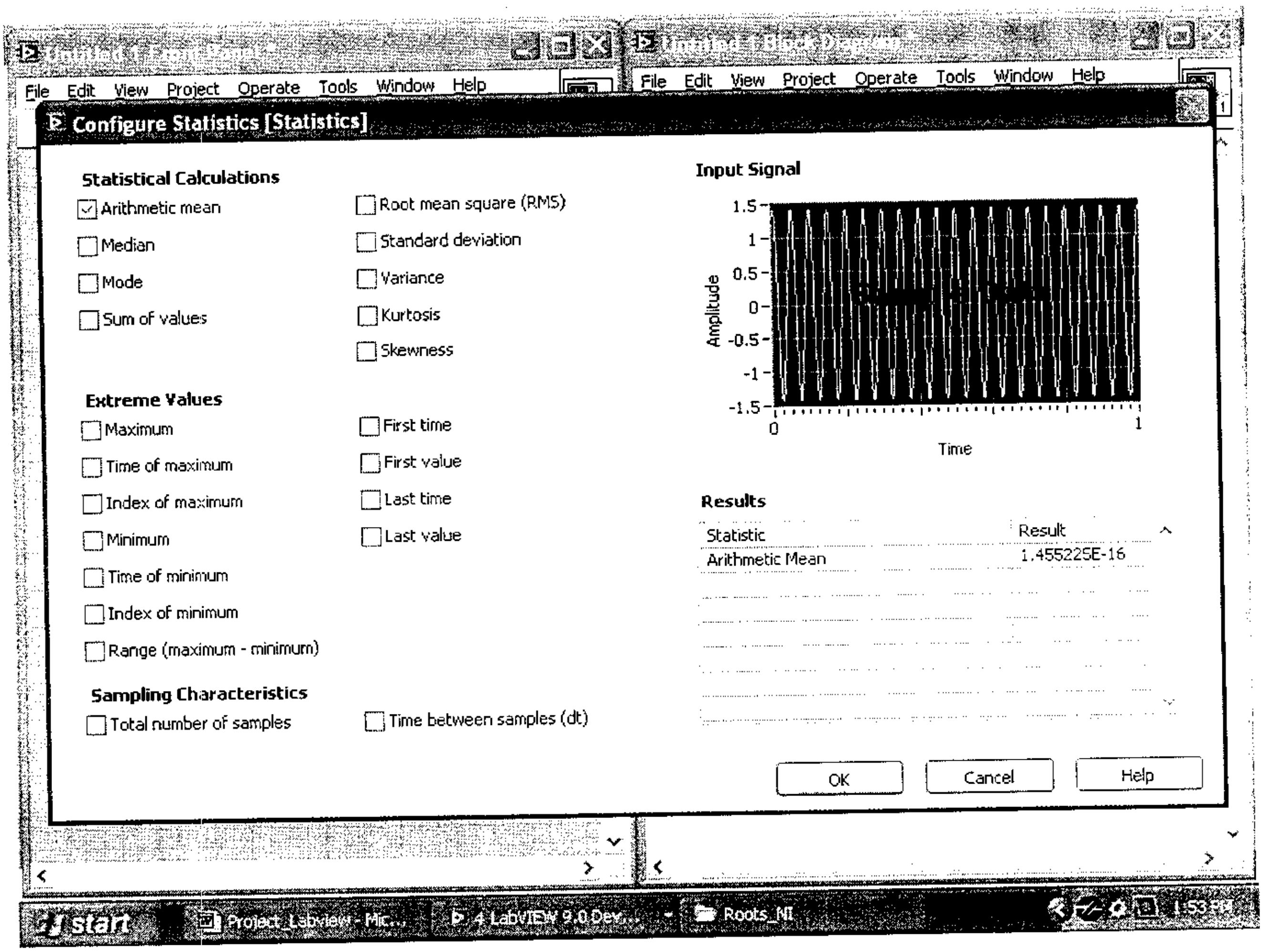


Fig. 32 Configuring Statistics

Step 7: Assigning Numeric control for four parameters

The numeric controls are added to acquire the voltage values and the correct voltage values are calibrated by multiplying factor.

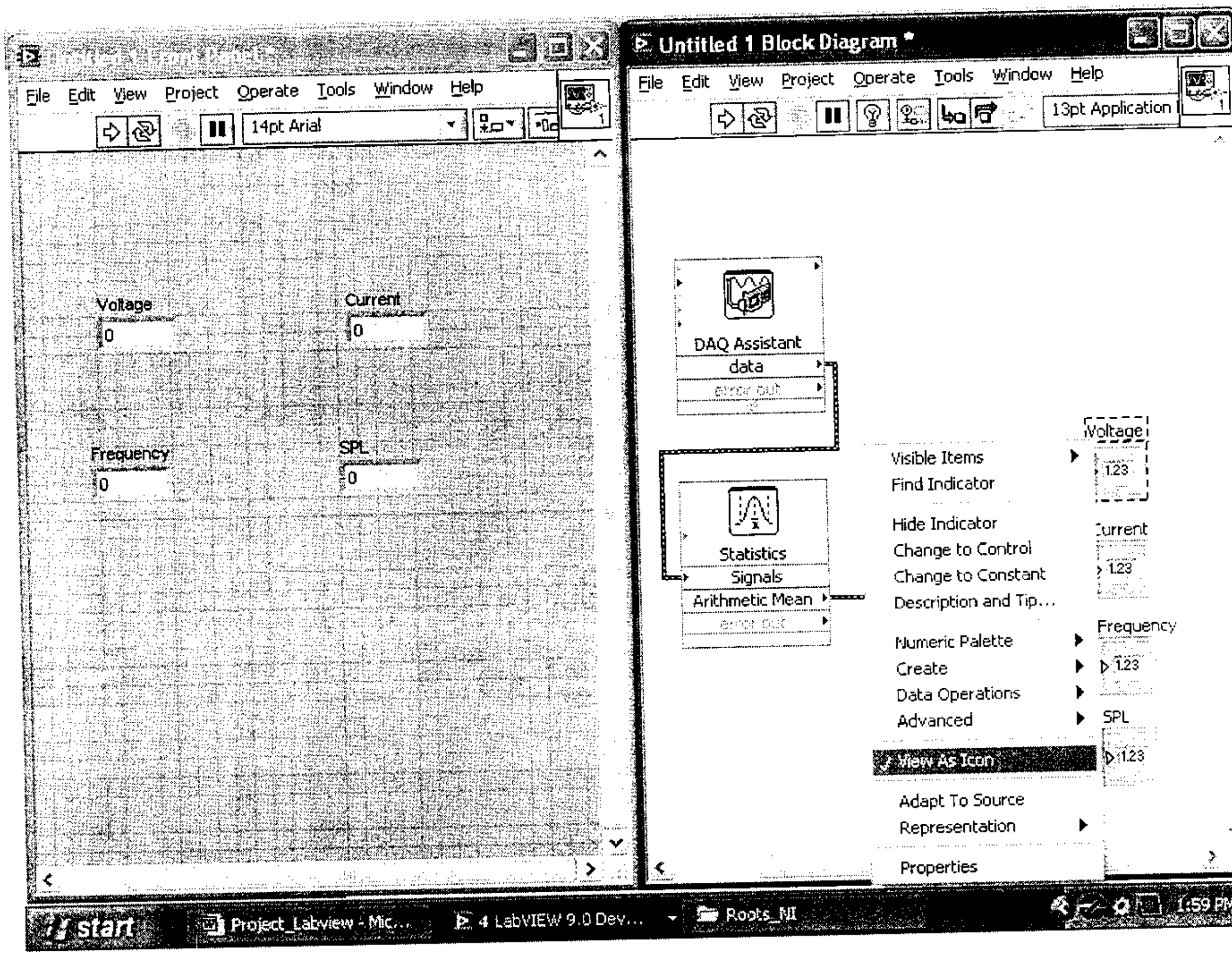


Fig. 33 Numeric controls

Step 8: Building sub VI

For the comparision of the acquired signals with minimum and maximum values of current, voltage and sound pressure levels the aub VI is build.

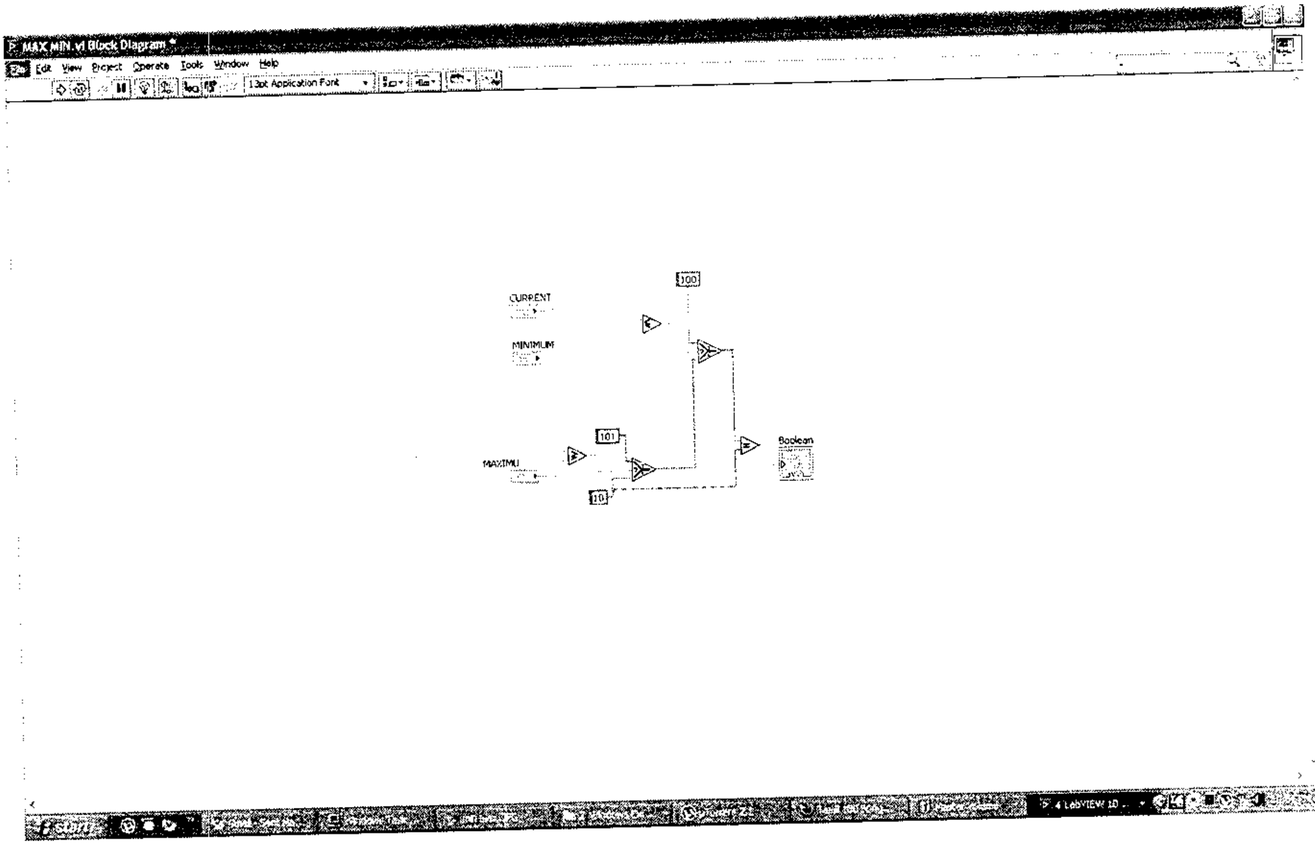


Fig. 34 Building Sub VI for Max and Min Values

This Sub VI helps to compare the horn parameters with the specified range of values. It also diplays the result using LED when the acquired signal is within the range.

Here the Select Block returns the value wired to the T input or F input, depending on the value of S. If S is True, this function returns the value wired to T. If S is False, this function returns the value wired to false.

Step 9: Building sub VI for displaying the result as PASS/FAIL.

Greater Or Equal Fuction returns TRUE if x is greater than or equal to y. otherwise, this function returns FALSE. The comparision mode of this function can be changed.

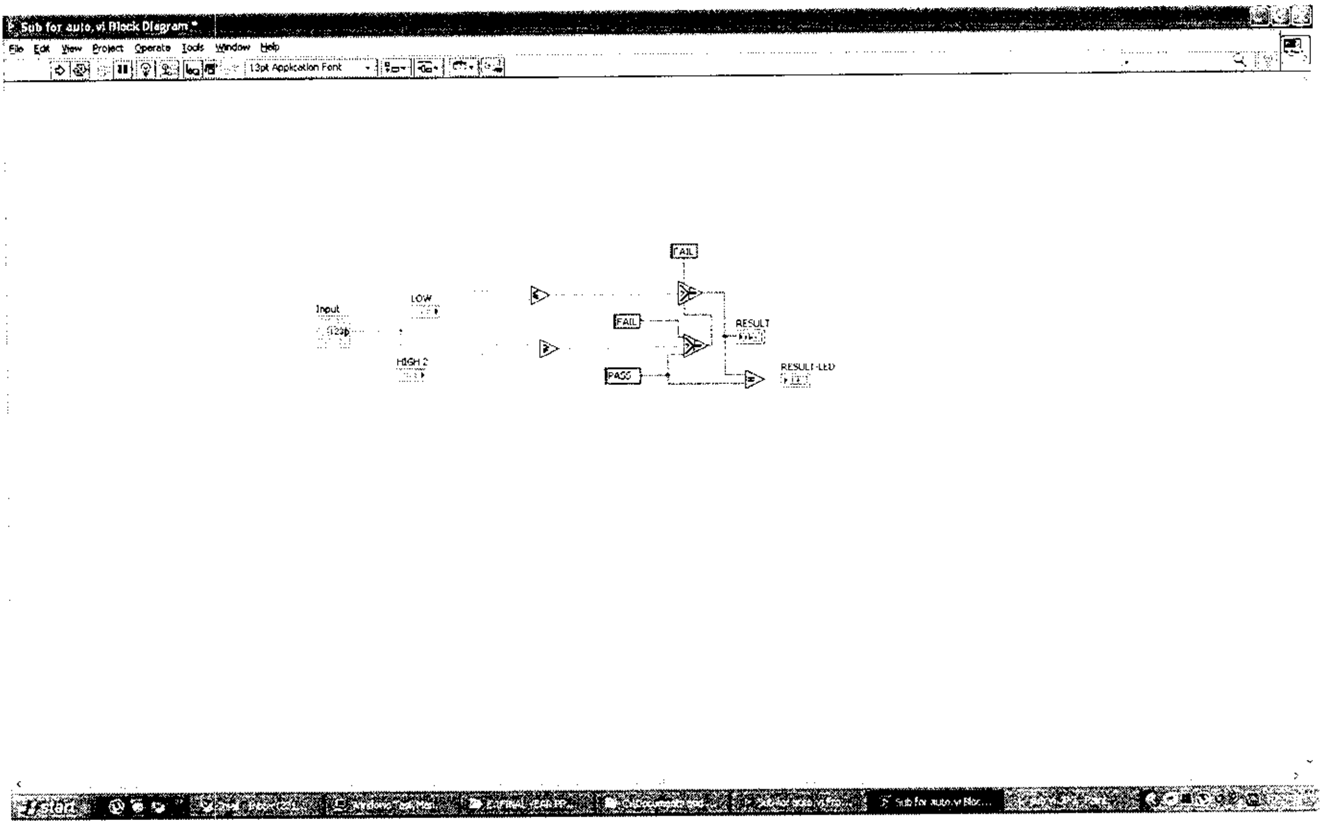


Fig. 35 Building Sub VI for Result

Less Or Equal Block Function returns TRUE if x is less than or equal to y. otherwise, this function returns FALSE. The comparision mode of this function can be changed.

Step 10: Final block diagram which includes all necessary blocks. The end result can be displayed by checking all the range of values.

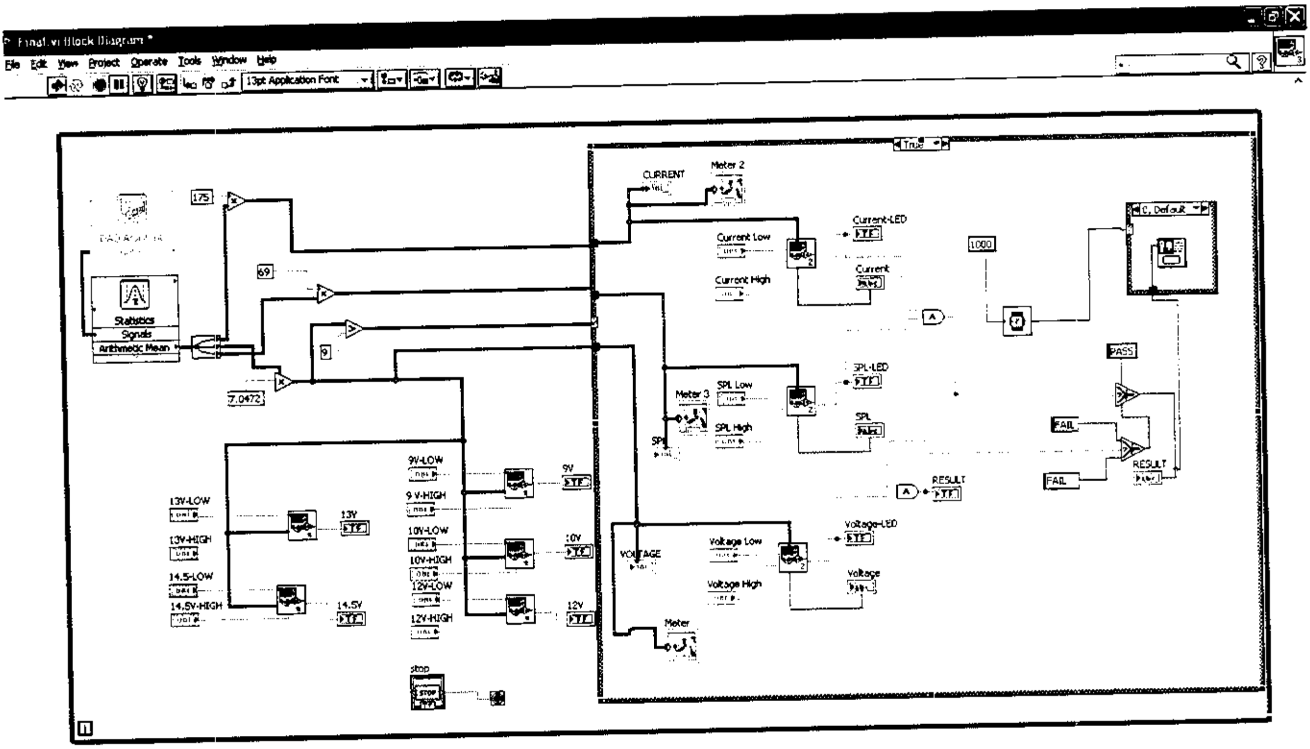


Fig. 36 Final Block Diagram

While Loops

Similar to a Do Loop or a Repeat-Until Loop in text-based programming languages, a While Loop, executes until a condition is met. The While Loop executes the sub diagram until the conditional terminal, an input terminal, receives a specific Boolean value.

Case Structures

Only one sub diagram is visible at a time, and the structure executes only one case at a time. An input value determines which sub diagram executes. The

Case structure is similar to case statements or if...then...else statements in text-based programming languages.

Time Delay

This block waits the specified number of milliseconds and returns the value of the millisecond timer. Wiring a value of 0 to the "milliseconds to wait" input forces the current thread to yield control of CPU.

4.2 FINAL FRONT PANEL

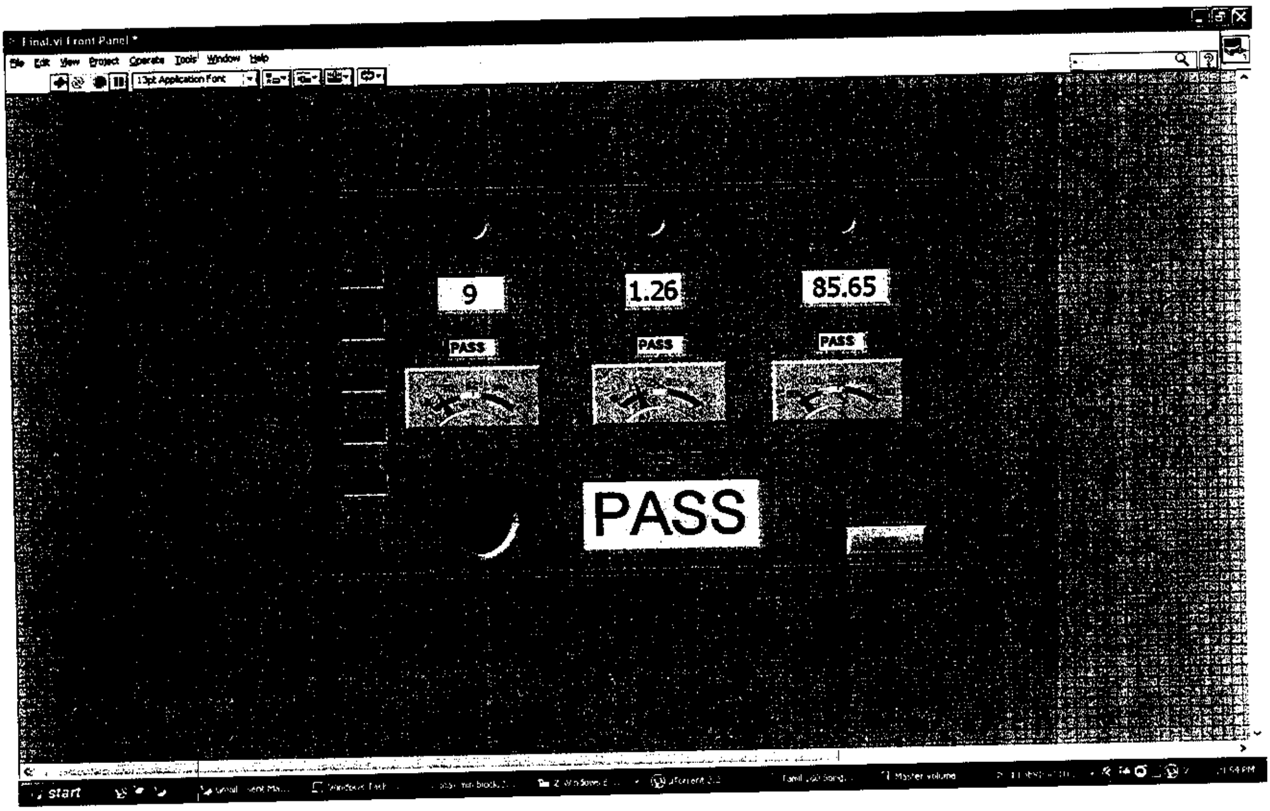


Fig. 37 Final Front Panel

Chapter 5

5. CONCLUSIONS

This project is mainly concerned about the time efficiency and data accuracy. The major technical difficulty in the earlier system was that, repetition of same work at regular intervals cause human fatigue and chance of occurring errors during the time of testing are high. This is now overcome by the use of LabVIEW software which has its unique feature of data acquisition and maintenance. Also LabVIEW is basically a graphical programming language in which the user can set up the program to manipulate and store data. The implementation of program using LabVIEW is very simple which in turn reduces the coding errors.

5.1 Future Scope

Advanced Horn Testing System can be extended by adding the "Auto Test" feature in which the voltage switching and the horn parameter measurements are sequenced automatically that reduces the process time much more. This feature enhances the test system by reducing the error occurring at the time of manual voltage switching.

Also this project will provide an option of database management that enables the direct access to each and every other details of the horn by just entering its model number.

Appendices

Appendix 1

NI 622*x* Specifications

Specifications listed below are typical at 25 °C unless otherwise noted. Refer to the *M Series User Manual* for more information about NI 622*x* devices.

> このドキュメントの日本語版については、[illegible]を参照してください。
> (For a Japanese language version, go to [illegible])

Analog Input

Number of channels	
NI 6220/6221	8 differential or 16 single ended
NI 6224/6229	16 differential or 32 single ended
NI 6225	40 differential or 80 single ended
ADC resolution	16 bits
DNL	No missing codes guaranteed
INL	Refer to the *AI Absolute Accuracy Table*
Sampling rate	
Maximum	250 kS/s single channel, 250 kS/s multi-channel (aggregate)
Minimum	No minimum
Timing accuracy	50 ppm of sample rate
Timing resolution	50 ns
Input coupling	DC
Input range	±10 V, ±5 V, ±1 V, ±0.2 V
Maximum working voltage for analog inputs (signal + common mode)	±11 V of AI GND
CMRR (DC to 60 Hz)	92 dB

Input impedance	
Device on	
AI+ to AI GND	>10 GΩ in parallel with 100 pF
AI– to AI GND	>10 GΩ in parallel with 100 pF
Device off	
AI+ to AI GND	820 Ω
AI– to AI GND	820 Ω
Input bias current	±100 pA
Crosstalk (at 100 kHz)	
Adjacent channels	–75 dB
Non-adjacent channels	–90 dB[1]
Small signal bandwidth (–3 dB)	700 kHz
Input FIFO size	4,095 samples
Scan list memory	4,095 entries
Data transfers	
PCI/PXI devices	DMA (scatter-gather), interrupts, programmed I/O
USB devices	USB Signal Stream, programmed I/O

[1] For USB-6225 devices, channel AI <0..15> crosstalk to channel AI <64..79> is –71 dB; applies to channels with 64-channel separation, for example, AI (*x*) and AI (*x* + 64).

NATIONAL INSTRUMENTS

Overvoltage protection (AI <0..79>, AI SENSE, AI SENSE 2)

Device on ....±25 V for up to two AI pins

Device off ....±15 V for up to two AI pins

Input current during overvoltage condition ....±20 mA max/AI pin

Settling Time for Multichannel Measurements

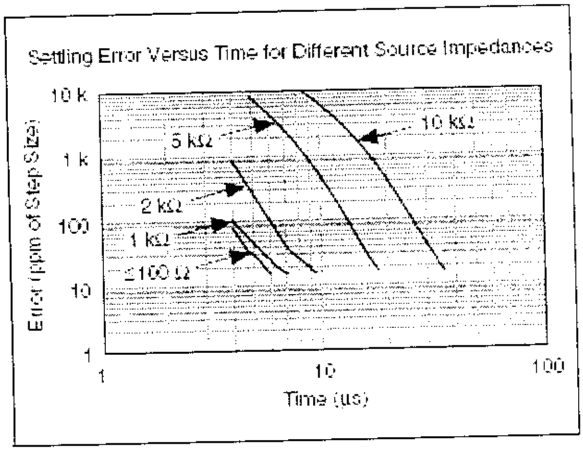
Accuracy, full scale step, all ranges

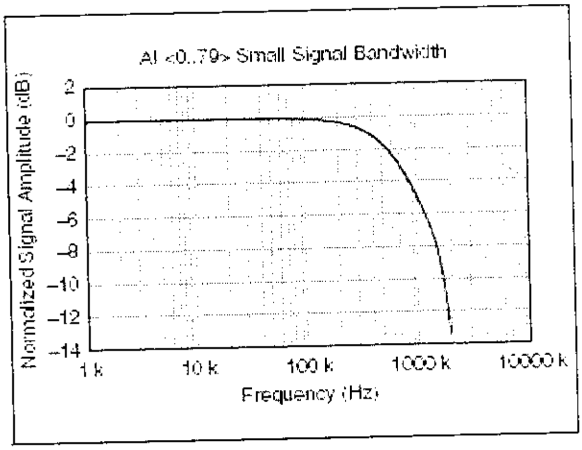
±90 ppm of step (±6 LSB) ....4 µs convert interval

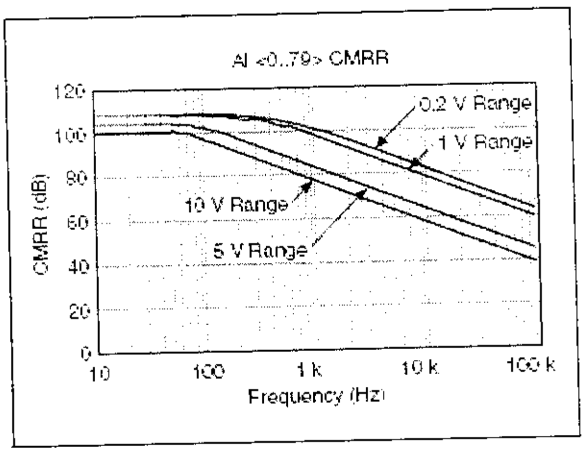
±30 ppm of step (±2 LSB) ....5 µs convert interval

±15 ppm of step (±1 LSB) ....7 µs convert interval

Typical Performance Graphs







Analog Output

Number of channels
- NI 6220/6224 0
- NI 6221/6225 2
- NI 6229 4

DAC resolution .... 16 bits

DNL .... ±1 LSB

Monotonicity .... 16 bit guaranteed

Maximum update rate
- 1 channel .... 833 kS/s
- 2 channels .... 740 kS/s per channel
- 3 channels .... 666 kS/s per channel
- 4 channels .... 625 kS/s per channel

Timing accuracy .... 50 ppm of sample rate

Timing resolution .... 50 ns

Output range .... ±10 V

Output coupling .... DC

Output impedance .... 0.2 Ω

Output current drive .... ±5 mA

Overdrive protection .... ±25 V

Overdrive current .... 10 mA

Power-on state .... ±20 mV[1]

Power-off glitch .... 400 mV for 200 ms

Output FIFO size .... 8,191 samples shared among channels used

Data transfers
- PCI/PXI devices .... DMA (scatter-gather), interrupts, programmed I/O
- USB devices .... USB Signal Stream, programmed I/O

AO waveform modes:

- Non-periodic waveform
- Periodic waveform regeneration mode from onboard FIFO
- Periodic waveform regeneration from host buffer including dynamic update

Settling time, full scale step 15 ppm (1 LSB) .... 6 μs

Slew rate .... 15 V/μs

Glitch energy
- Magnitude .... 100 mV
- Duration .... 2.6 μs

Calibration (AI and AO)

Recommended warm-up time .... 15 minutes

Calibration interval .... 1 year

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[1] For all USB-6221/6229 Screw Terminal devices, when powered on, the analog output signal is not defined until after USB configuration is complete.

AI Absolute Accuracy Table

Nominal Range		Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Random Noise, σ (µVrms)	Absolute Accuracy at Full Scale[1] (µV)	Sensitivity[2] (µV)
Positive Full Scale	Negative Full Scale									
10	–10	75	25	5	20	57	76	244	3,100	97.6
5	–5	85	25	5	20	60	76	122	1,620	48.8
1	–1	95	25	5	25	79	76	30	360	12.0
0.2	–0.2	135	25	5	80	175	76	13	112	5.2

AbsoluteAccuracy = Reading · (GainError) + Range · (OffsetError) + NoiseUncertainty

GainError = ResidualAIGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)

OffsetError = ResidualAIOffsetError + OffsetTempco · (TempChangeFromLastInternalCal) + INL_Error

$$NoiseUncertainty = \frac{RandomNoise \cdot 3}{\sqrt{100}}$$ For a coverage factor of 3 σ and averaging 100 points.

[1] Absolute accuracy at full scale on the analog input channels is determined using the following assumptions:

TempChangeFromLastExternalCal = 10 °C

TempChangeFromLastInternalCal = 1 °C

number_of_readings = 100

CoverageFactor = 3 σ

For example, on the 10 V range, the absolute accuracy at full scale is as follows:

GainError = 75 ppm + 25 ppm · 1 + 5 ppm · 10 GainError = 150 ppm

OffsetError = 20 ppm + 57 ppm · 1 + 76 ppm OffsetError = 153 ppm

$$NoiseUncertainty = \frac{244\ \mu V \cdot 3}{\sqrt{100}}$$ NoiseUncertainty = 73 µV

AbsoluteAccuracy = 10 V · (GainError) + 10 V · (OffsetError) + NoiseUncertainty AbsoluteAccuracy = 3,100 µV

[2] Sensitivity is the smallest voltage change that can be detected. It is a function of noise.

Accuracies listed are valid for up to one year from the device external calibration.

General-Purpose Counter/Timers

Number of counter/timers 2

Resolution .... 32 bits

Counter measurements .... Edge counting, pulse, semi-period, period, two-edge separation

Position measurements .... X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding

Output applications .... Pulse, pulse train with dynamic updates, frequency division, equivalent time sampling

Internal base clocks......................... 80 MHz, 20 MHz, 0.1 MHz

External base clock frequency .... 0 MHz to 20 MHz

Base clock accuracy .... 50 ppm

Inputs .... Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down

Routing options for inputs .... Any PFI, RTSI, PXI_TRIG, PXI_STAR, analog trigger, many internal signals

FIFO.. 2 samples

Data transfers

PCI/PXI devices .... Dedicated scatter-gather DMA controller for each counter/timer; interrupts; programmed I/O

USB devices .... USB Signal Stream, programmed I/O

Frequency Generator

Number of channels 1

Base clocks .... 10 MHz, 100 kHz

Divisors .... 1 to 16

Base clock accuracy .... 50 ppm

Output can be available on any PFI or RTSI terminal.

Phase-Locked Loop (PLL)

Number of PLLs 1

Reference signal .... PXI_STAR, PXI_CLK10, RTSI <0..7>

Output of PLL .... 80 MHz Timebase; other signals derived from 80 MHz Timebase including 20 MHz and 100 kHz Timebases

External Digital Triggers

Source .... Any PFI, RTSI, PXI_TRIG, PXI_STAR

Polarity .... Software-selectable for most signals

Analog input function...................... Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase

Analog output function.................... Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase

Counter/timer functions.................... Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down

Digital waveform generation (DO) function .... Sample Clock

Digital waveform acquisition (DI) function.................................. Sample Clock

Device-To-Device Trigger Bus

PCI devices .... RTSI <0..7>[1]

PXI devices .... PXI_TRIG <0..7>, PXI_STAR

USB devices .... None

Output selections .... 10 MHz Clock; frequency generator output; many internal signals

Debounce filter settings .... 125 ns, 6.425 μs, 2.56 ms, disabled; high and low transitions; selectable per input

Bus Interface

PCI/PXI devices .... 3.3 V or 5 V signal environment

USB devices .... USB 2.0 Hi-Speed or full-speed[2]

DMA channels (PCI/PXI devices) .... 6, analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1

USB Signal Stream (USB devices) .... 4, can be used for analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1

All PXI-622x devices support one of the following features:

- May be installed in PXI Express hybrid slots
- Or, may be used to control SCXI in PXI/SCXI combo chassis

Table 1. PXI/SCXI Combo and PXI Express Chassis Compatibility

M Series Device	M Series Part Number	SCXI Control in PXI/SCXI Combo Chassis	PXI Express Hybrid Slot Compatible
PXI-6220	191332B-04	No	Yes
PXI-6221	191332B-03	No	Yes
	191332B-13	Yes	No
PXI-6224	191332B-02	No	Yes
PXI-6225	192227A-01	No	Yes
PXI-6229	191332B-01	No	Yes
	191332B-11	Yes	No
Earlier versions of PXI-6220/6221/6224/6229	191332A-0x	Yes	No

Power Requirements

Current draw from bus during no-load condition[3]

+5 V .... 0.02 A[4]

+3.3 V .... 0.25 A[4]

+12 V .... 0.15 A

Current draw from bus during AI and AO overvoltage condition[3]

+5 V .... 0.02 A[4]

+3.3 V .... 0.25 A[4]

+12 V .... 0.25 A

Caution USB-622x devices must be powered with NI offered AC adapter or a National Electric Code (NEC) Class 2 DC source that meets the power requirements for the device and has appropriate safety certification marks for country of use.

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[1] In other sections of this document, *RTSI* refers to RTSI <0..7> for PCI devices or PXI_TRIG <0..7> for PXI devices.

[2] If you are using a USB M Series device in full-speed mode, device performance will be lower and you will not be able to achieve maximum sampling/update rates.

[3] Does not include P0/PFI/P1/P2 and +5 V terminals.

[4] PCI-6221 (37-pin) devices do not use +3.3 V from the bus. The 3.3 V current draw, shown in the *Power Requirements* section, comes from the +5 V instead.

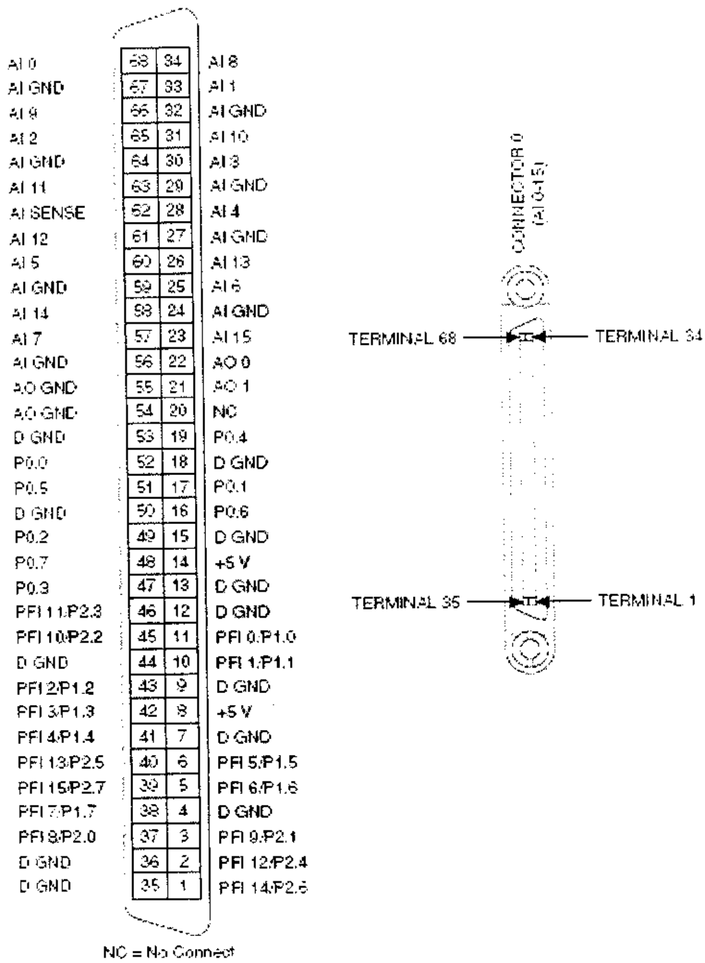


Figure 2. PCI/PXI-6221 (68-Pin) Pinout

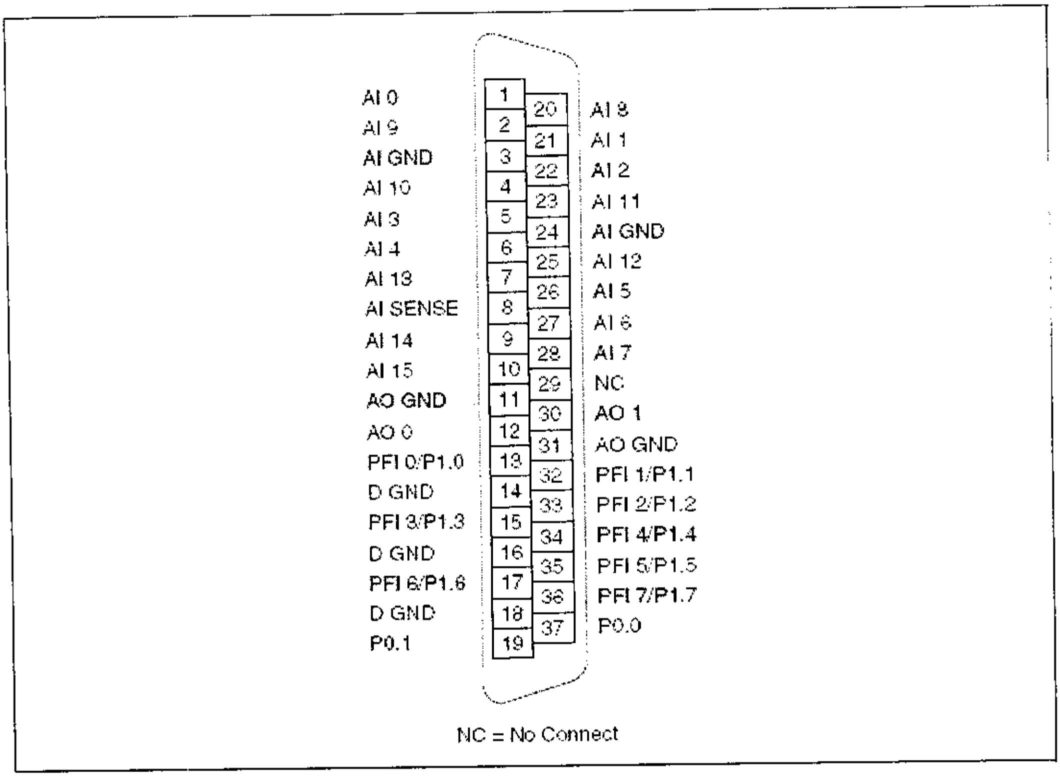


Figure 3. PCI-6221 (37-Pin) Pinout

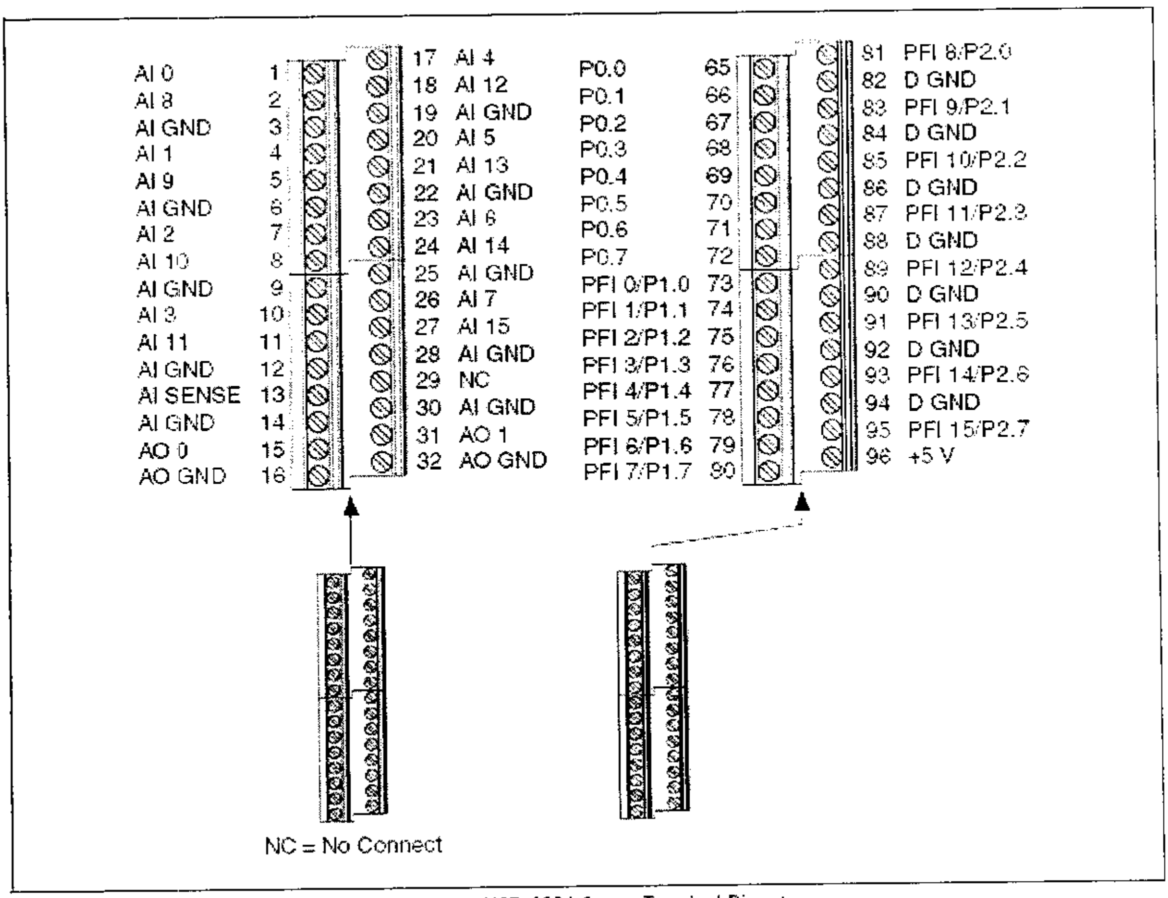


Figure 4. USB-6221 Screw Terminal Pinout

Appendix 2

COMPLEMENTARY SILICON POWER TRANSISTORS

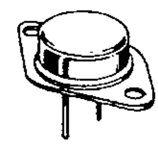
The 2N3773 and 2N6609 are power base power transistors designed for high power audio, disk head positioners,linear amplifiers,switching regulators,solenoid drivers,and dc to dc converters or inverters.

NPN	PNP
2N3773	2N6609

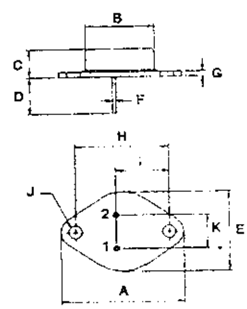
16 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
140 VOLTS
150 WATTS

FEATURES:

* High Power Dissipation
  P_D = 150 W (T_C = 25°C)
* High DC Current Gain and Low Saturation Voltage
  hFE = 15-60 @ I_C = 8 A , V_{CE} = 4 V
  $V_{CE(SAT)}$ = 1.4 V (Max.) @ I_C = 8 A, I_B = 0.8 A



TO-3



PIN 1.BASE
2.EMITTER
COLLECTOR(CASE)

DIM	MILLIMETERS	
	MIN	MAX
A	38.75	39.96
B	19.28	22.23
C	7.96	9.28
D	11.18	12.19
E	25.20	26.67
F	0.92	1.09
G	1.38	1.62
H	29.90	30.40
I	16.64	17.30
J	3.88	4.36
K	10.67	11.18

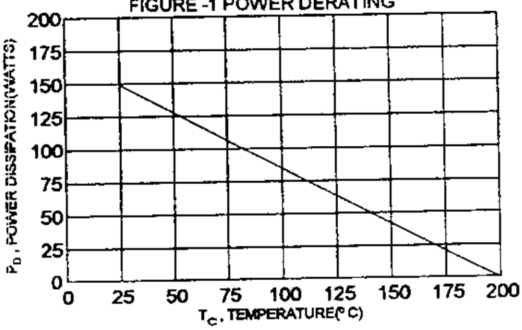
MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Collector-Emitter Voltage	$V_{CEO(SUS)}$	140	V
Collector-Emitter Voltage	V_{CEX}	160	V
Collector-Base Voltage	V_{CBO}	160	V
Emitter-Base Voltage	V_{EBO}	7	V
Collector Current-Continuous Peak (1)	I_C I_{CM}	16 30	A
Base Current-Continuous Peak (1)	I_B I_{BM}	4.0 15	A
Total Power Dissipation @T_C=25°C Derate above 25°C	P_D	150 0.857	W W/°C
Operating and Storage Junction Temperature Range	T_J,T_{STG}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	Rθjc	1.17	°C/W

FIGURE -1 POWER DERATING



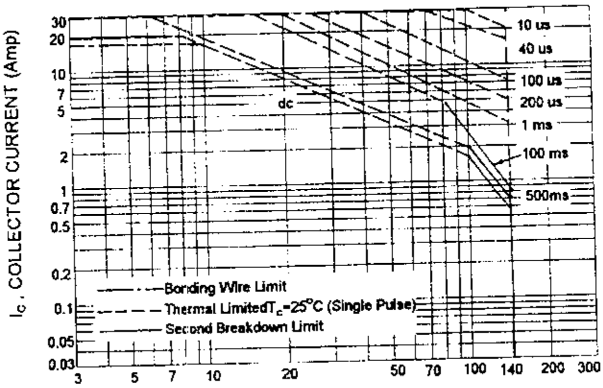
(1) Pulse Test: Pulse width = 5 ms , Duty Cycle < 10%

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector - Emitter Sustaining Voltage (1) (I_C = 200 mA, I_B = 0)	$V_{CEO(SUS)}$	140		V
Collector Cutoff Current (V_{CE} = 120 V, I_B = 0)	I_{CEO}		10	mA
Collector Cutoff Current (V_{CE} = 140 V, $V_{BE(OFF)}$ = 1.5 V)	I_{CEX}		2.0	mA
Collector Cutoff Current (V_{CB} = 140 V, I_E = 0)	I_{CBO}		2.0	mA
Emitter Cutoff Current (V_{EB} = 7.0 V, I_C = 0)	I_{EBO}		5.0	mA
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 8.0 A , V_{CE} = 4.0 V) (I_C = 16 A, V_{CE} = 4.0 V	hFE	15 5.0	60	
Collector - Emitter Saturation Voltage (I_C = 8.0 A , I_B = 800 mA) (I_C = 16 A, I_B = 3.2 A)	$V_{CE(sat)}$		1.4 4.0	V
Base - Emitter On Voltage (I_C = 8.0 A, V_{CE} = 4.0 V)	$V_{BE(ON)}$		2.2	V

* Pulse Test: Pulse width = 300 us , Duty Cycle = 2.0%

ACTIVE-REGION SAFE OPERATING AREA (SOA)

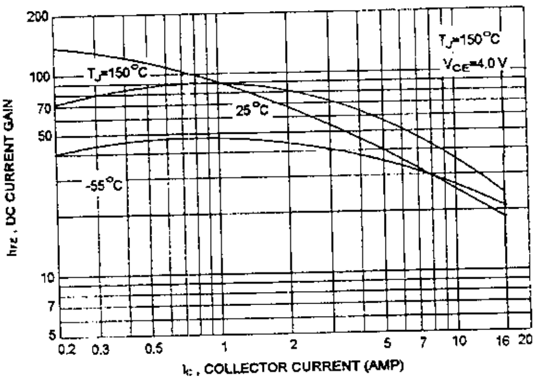


There are two limitation on the power handling ability of a transistor:average junction temperature and second breakdown safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

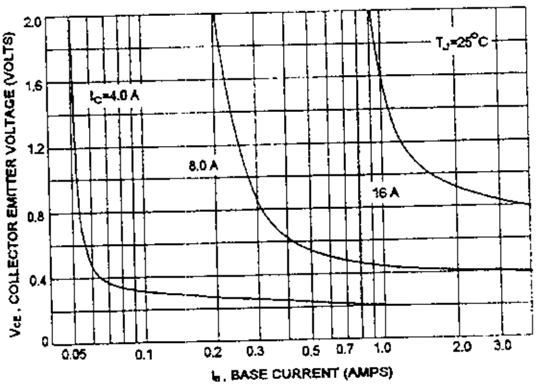
The data of SOA curve is base on $T_{J(PK)}$=200 °C;T_C is variable depending on conditions. second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(PK)} \leq 200$°C.At high case temperatures, thermal limitation will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN 2N3773

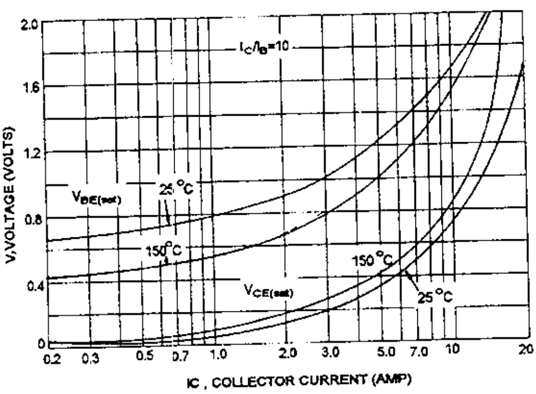
DC CURRENT GAIN



COLLECTOR SATURATION REGION

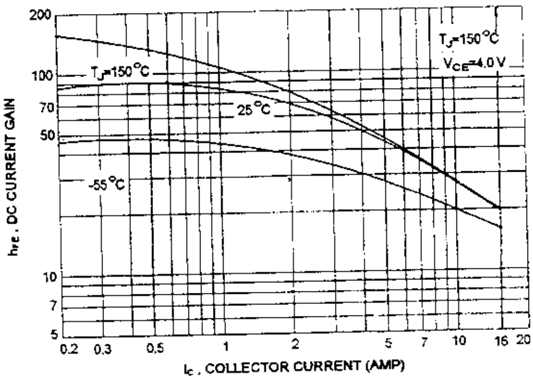


"ON" VOLTAGES

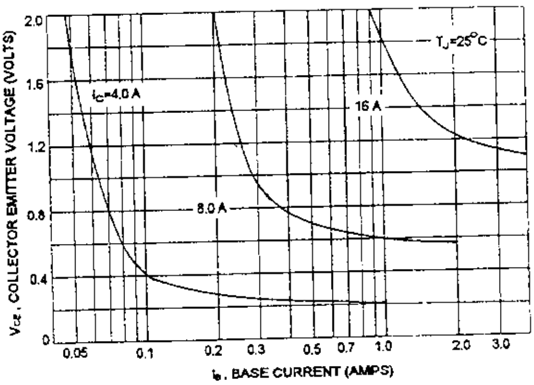


PNP MJ6609

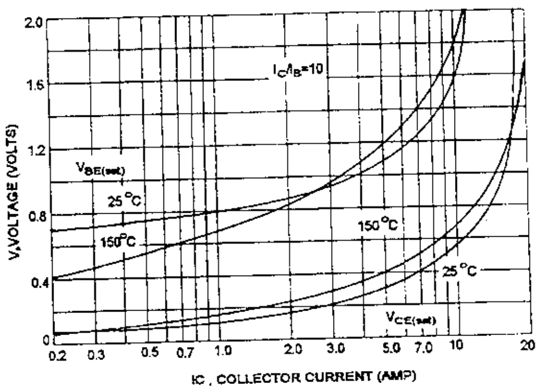
DC CURRENT GAIN



COLLECTOR SATURATION REGION



"ON" VOLTAGES



Appendix 3

RENESAS

HD74LS138

3-Line-to-8-Line Decoders / Demultiplexers

REJ03D0434–0300
Rev.3.00
Jul.13.2005

The HD74LS138 decodes one-of-eight line dependent on the conditions at the three binaly select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

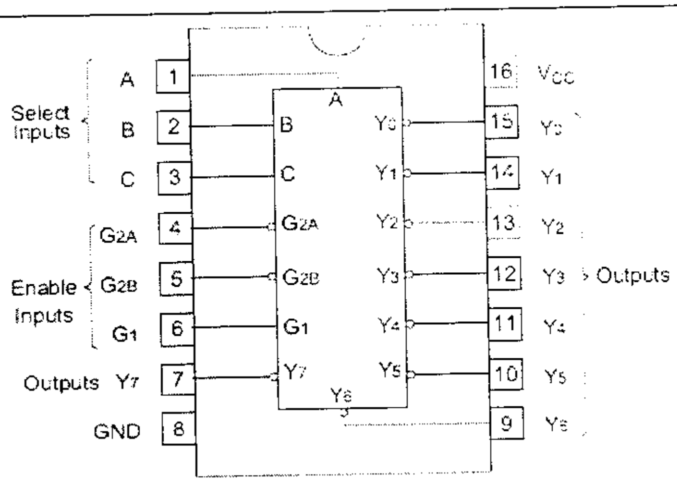
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS138P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	-
HD74LS138FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74LS138RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



(Top view)

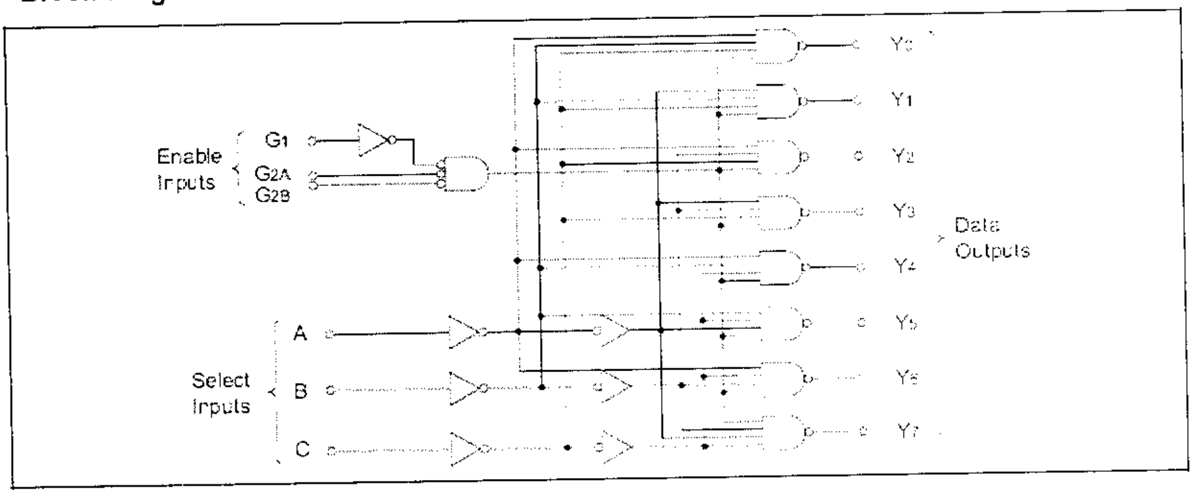
Function Table

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H ; high level, L ; low level, X ; irrelevant

* ; $G_2 = G_{2A} + G_{2B}$

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	–400	µA
	I_{OL}	—	—	8	mA
Operating temperature	Topr	–20	25	75	°C

Electrical Characteristics

(Ta = –20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage	V_{IH}	2.0	—	—	V		
	V_{IL}	—	—	0.8	V		
Output voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA	
	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
		—	—	0.5		I_{OL} = 8 mA	
Input current	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V	
	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V	
	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V	
Short-circuit output current	I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V	
Supply current	I_{CC}	—	6.3	10	mA	V_{CC} = 5.25 V, Outputs enabled and open	
Input clamp voltage	V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA	

Note: * V_{CC} = 5 V, Ta = 25°C

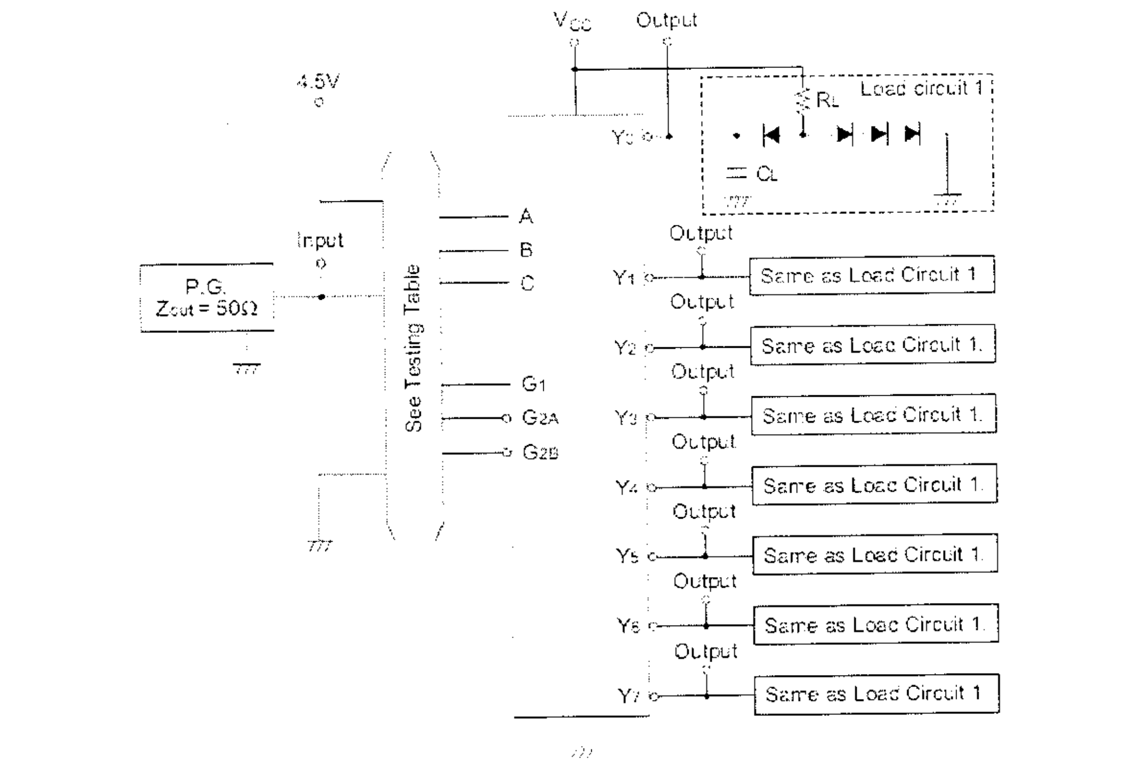
Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Output	Levels of delay	min.	typ.	max.	Unit	Condition
Propagation delay time	t_{PLH}	Binary select A, B, C	Y	2	—	13	20	ns	C_L = 15 pF, R_L = 2 kΩ
	t_{PHL}				—	27	41	ns	
	t_{PLH}			3	—	18	27	ns	
	t_{PLH}				—	26	39	ns	
	t_{PLH}	Enable G_{2A}, G_{2B}	Y	2	—	12	18	ns	
	t_{PHL}				—	21	32	ns	
	t_{PLH}	Enable G_1		3	—	17	26	ns	
	t_{PLH}				—	25	38	ns	

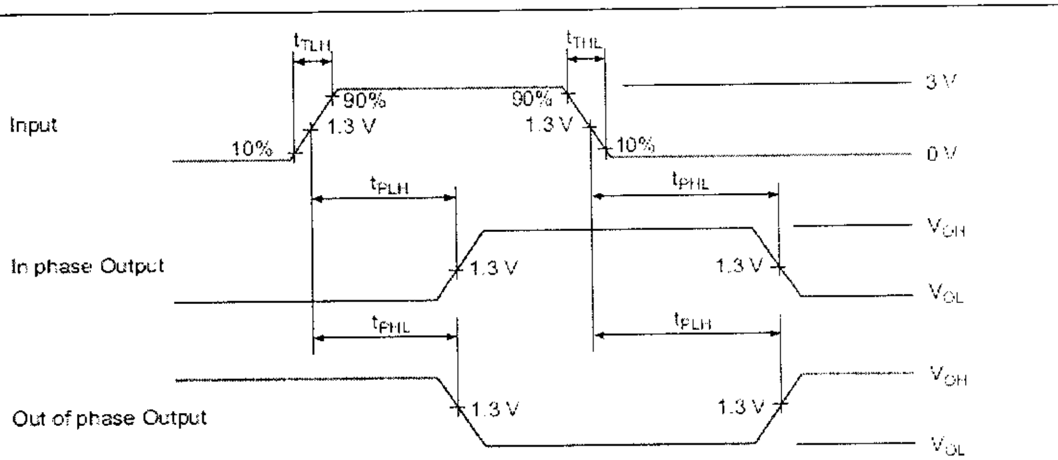
Testing Method

Test Circuit



Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

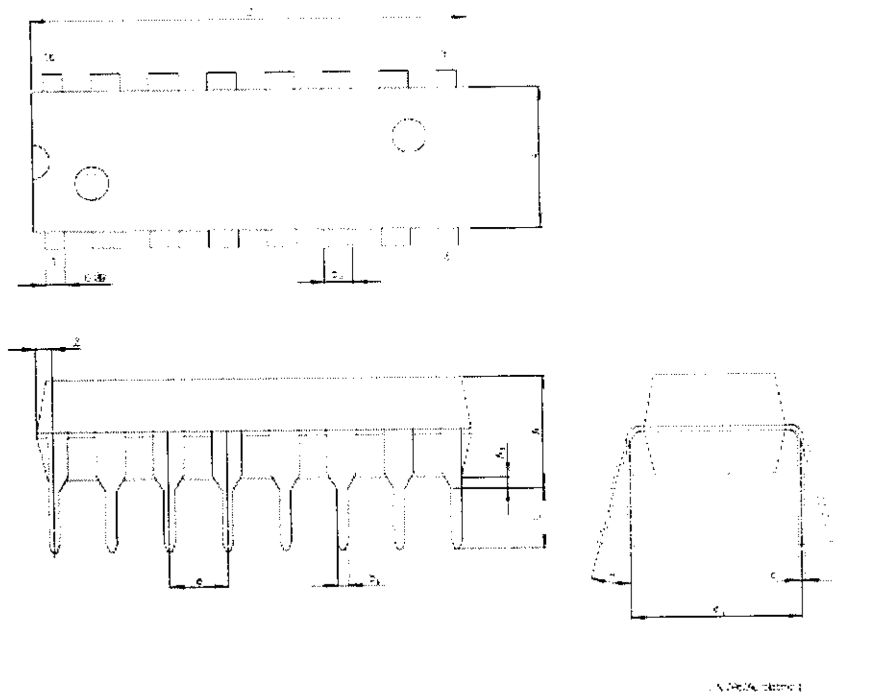
Waveform



Note: Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle 50%

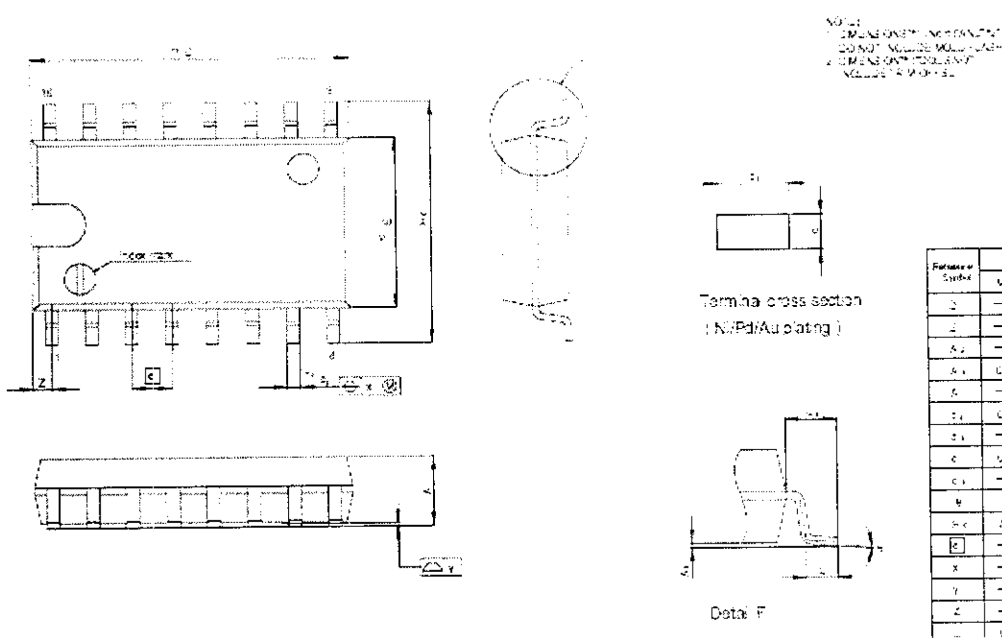
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
[illegible]	[illegible]	[illegible]	[illegible]

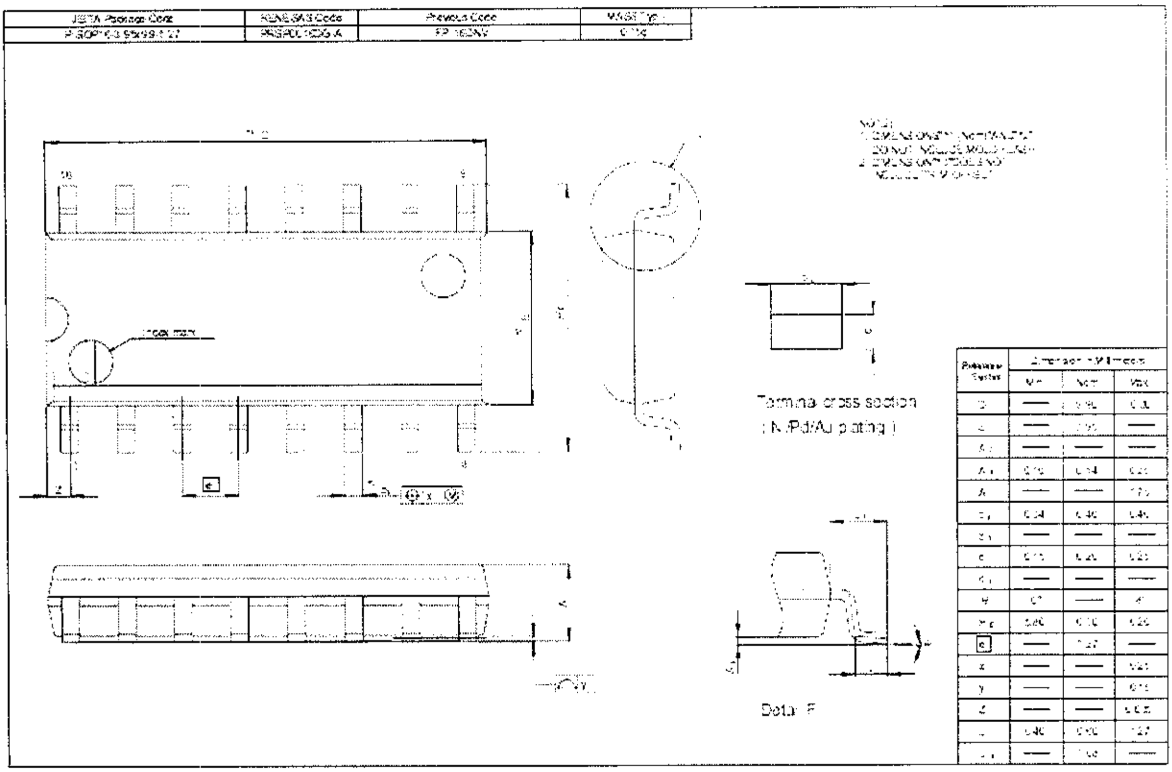


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	—	[illegible]	—
D	—	[illegible]	[illegible]
E	—	[illegible]	[illegible]
A	—	—	[illegible]
A_1	[illegible]	—	—
b_p	0.40	0.48	[illegible]
b_3	—	[illegible]	—
c	[illegible]	[illegible]	[illegible]
θ	[illegible]	—	[illegible]
e	[illegible]	2.54	[illegible]
Z	—	—	[illegible]
L	2.54	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
[illegible]	[illegible]	[illegible]	[illegible]



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	[illegible]	[illegible]
E	—	[illegible]	—
A_2	—	—	—
A_1	[illegible]	[illegible]	0.20
A	—	—	[illegible]
b_p	0.34	0.40	0.46
b_1	—	—	—
c	[illegible]	[illegible]	[illegible]
c_1	—	—	—
θ	[illegible]	—	[illegible]
H_E	[illegible]	[illegible]	[illegible]
e	—	1.27	—
x	—	—	0.12
y	—	—	[illegible]
Z	—	—	[illegible]
L	[illegible]	0.70	[illegible]
L_1	—	[illegible]	—



Relation Between Input and Output to Levels of Delay

Inputs	Outputs							
	2 levels of delay				3 levels of delay			
A	Y_0	Y_2	Y_4	Y_6	Y_1	Y_3	Y_5	Y_7
B	Y_0	Y_1	Y_4	Y_5	Y_2	Y_3	Y_6	Y_7
C	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
G_1					Y_0 to Y_7			
G_{2A}, G_{2B}	Y_0 to Y_7							

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