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Design of Three Phase H-Bridge Multilevel Inverter

A PROJECT REPORT

Submitted by

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BONAFIDE CERTIFICATE

Certified that this project report "**Design of Three phase H-Bridge Multilevel Inverter**" is the bonafide work of "**TAMILARUVI.K,BOOPATHIMUTHU.R,GOWTHAMI.K, MOORTHY.R**" who carried out the project under my supervision.

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ABSTRACT

The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as inverter. Inverters can be broadly classified into single level inverter and multilevel inverter. Multilevel inverter as compared to single level inverters have advantages like minimum harmonic distortion, reduced EMI/RFI generation and can operate on several voltage levels. A multi-stage inverter is being utilized for multipurpose applications, such as active power filters, static var compensators and machine drives for sinusoidal and trapezoidal current applications. Traditionally, each H-bridge needs a dc power supply. The proposed design uses a standard three-leg inverter (one leg for each phase) and an H-bridge in series with each inverter leg which uses a capacitor as the DC power source. A fundamental switching scheme is used to do modulation control and to produce a five-level phase voltage. Experiments show that the proposed DC-AC cascaded H-bridge multilevel inverter can Convert DC-AC voltage with minimum harmonic distortion.

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LIST OF ABBREVIATIONS

AC	Alternating Current
DC	Direct Current
EVs	Electric Vehicles
HEVs	Hybrid Electric Vehicles
Id	Drain Current
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
PIC	Programmable Interrupt Controller
PWM	Pulse Width Modulation
R_{ds}	Drain Source Resistance
SPWM	Sinusoidal Pulse Width Modulation
THD	Total Harmonic Distortion
V_{ds}	Drain Source Voltage

INTRODUCTION

CHAPTER-1

INTRODUCTION

1.1 OVERVIEW

Nowadays, increasing oil prices and environmental concerns, hybrid electric vehicles (HEVs) and electric vehicles (EVs) are gaining increased attention due to their higher efficiencies and lower emissions associated with the development of improved power electronics and motor technologies.

An HEV typically combines a smaller internal combustion engine of a conventional vehicle with a battery pack and an electric motor to drive the vehicle. The combination offers lower emissions but with the power range and convenient fueling of conventional (gasoline and diesel) vehicles. An EV typically uses rechargeable batteries and an electric motor. The batteries need to be charged regularly.

Both HEVs and EVs need a traction motor and a power inverter to drive the traction motor. The requirements for the power inverter include high peak power and low continuous power rating. Currently available power inverter systems for HEVs use a dc–dc boost converter to boost the battery voltage for a traditional three-phase inverter.

If the motor is running at low to medium power, the DC–DC boost converter is not needed, and the battery voltage will be directly applied to the inverter to drive the traction motor. If the motor is running in a high power mode, the DC-DC boost converter will boost the battery voltage to a higher voltage, so that the inverter can provide higher power to the motor.

Present HEV traction drive inverters have low power density, are expensive, and have low efficiency because they need bulky inductors for the DC-DC boost converters. To achieve a boosted output ac voltage from the traditional inverters for HEV and EV applications, the Z-source inverter is proposed, which also requires an inductor.

But this project presents a cascaded H-bridge multilevel boost inverter design which can be used for EV and HEV applications implemented without the use of inductors is proposed. Traditionally, each H-bridge needs a DC power supply. The proposed design uses a standard three-leg inverter (one leg for each phase) and an H-bridge in series with each inverter leg which uses a capacitor as the DC power source.

A fundamental switching scheme is used to do modulation control and to produce a five-level phase voltage. Hence, the proposed dc–ac cascaded H-bridge multilevel boost inverter can output a boosted ac voltage without the use of inductors which has a wider modulation index range than a traditional inverter. The application of this DC-AC boost inverter can result in the elimination of the bulky inductor of present DC-DC boost converters, thereby increasing the power density.

1.2 INVERTER

An inverter is the major electronic component which performs the operation exactly opposite to that of a rectifier i.e. an inverter converts the Direct current into Alternating current.

1.2.1 Types of Inverter

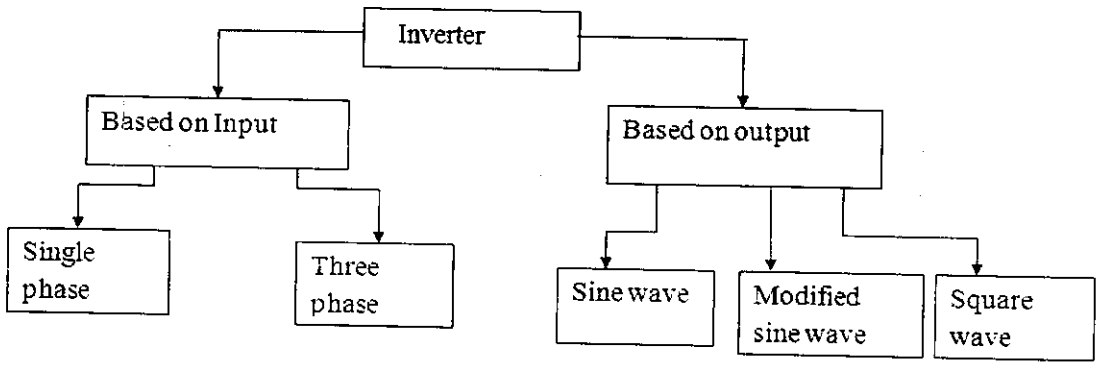


Fig 1.1 Types of Inverter

Inverters can be classified based on input and output. Fig 1.1 shows the classification of inverter based on input and output.

1.2.1.1 Sine Wave Inverter

A sine wave is what you get from your local utility company and (usually) from a generator. This is because it is generated by rotating AC machinery and sine waves are a natural product of rotating AC machinery. The major advantage of a sine wave inverter is that all of the equipment which is sold on the market is designed for a sine wave. This guarantees that the equipment will work to its full specifications. Some appliances, such as motors and microwave ovens will only produce full output with sine wave power. Fig 1.2 shows the output of sine wave inverter.

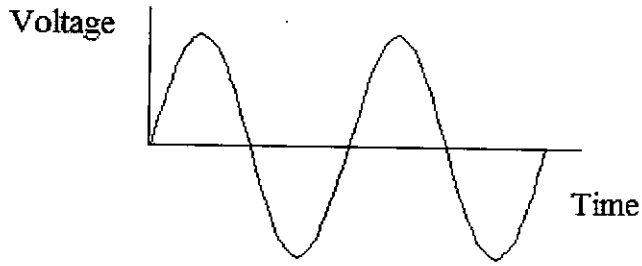


Fig 1.2 Sine wave

1.2.1.2 Modified sinewave(Quasi sine) Inverter

A modified sine wave inverter actually has a waveform more like a square wave, but with an extra step or so. A modified sine wave inverter will work fine with most equipment, although the efficiency or power will be reduced with some. Motors, such as refrigerator motor, pumps, fans etc will use more power from the inverter due to lower efficiency. Most motors will use about 20% more power. This is because a fair percentage of a modified sine wave is higher frequencies that is, not 60 Hz - so the motors cannot use it. Some fluorescent lights will not operate quite as bright, and some may buzz or make annoying humming noises. Fig 1.3 shows the output of modified sine wave inverter.

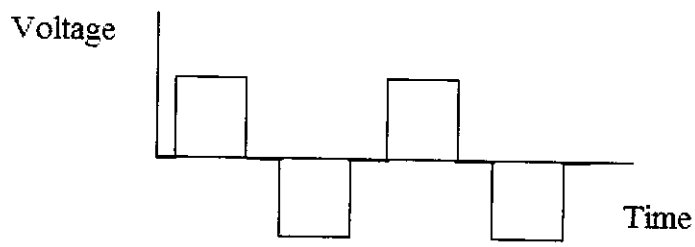


Fig 1.3 Modified sinewave

1.2.1.3 Square wave Inverter

Very few but the very cheapest inverters any more are square wave. A square wave inverter will run simple things like tools with universal motors with no problem - but not

much else. These are seldom seen any more except in the very cheap or very old ones. Fig 1.4 shows the output of the square wave inverter.

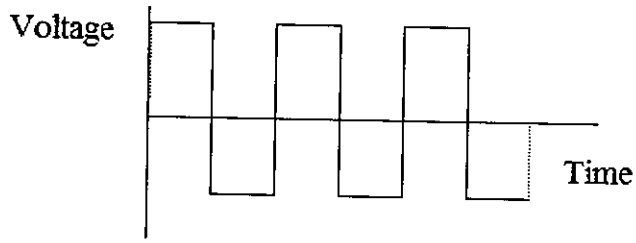


Fig 1.4 Square wave

The emerging trend among Inverters could be titled to Multi-Level Inverters which aim at the Increasing of Inverter Efficiency along with reduced Inverter cost.

1.3 MULTILEVEL INVERTER

Multilevel inverter divide the main dc supply voltage into several smaller dc sources which are used to synthesize an ac voltage into a staircase or stepped approximation of the desired sinusoidal waveform.

1.3.1 Types of Multilevel Inverter

There are three main types of multilevel inverters.

(1) Diode - clamped inverter

(2) Capacitor - clamped inverter

(3) Cascaded inverter.

Applications that have been proposed include static VAR (volt - ampere reactive) compensation, back - to- back high - voltage inverter, and adjustable speed drives. However, using the multilevel inverter as an application for EV and HEV drive systems is a relatively new concept. The multilevel inverter may be implemented at the discrete component level dividing the main dc supply voltage into several smaller voltages.

First two types of the multi-level inverter are discussed in this chapter. The cascaded type multilevel inverter will be discussed briefly in the next chapter.

1.3.1.1 Diode-Clamped Inverter

The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series bank of capacitors. According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors. Descriptions of this topology were limited to three-levels where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology neutral point clamped (NPC) inverter was used .However, with an even number of voltage levels, the neutral point is not accessible, and the term multiple point clamped (MPC) is sometimes applied. Due to capacitor voltage balancing issues, the diode-clamped inverter implementation has been mostly limited to the three levels.

Fig. 1.5 shows the topology of the n-level diode-clamped inverter. The structure is more complicated than the four-level inverter. Each phase node (a, b, or c) can be connected to any node in the capacitor bank (d_0, d_1 or d_2). Connection of the a-phase to junctions' d_0 and d_2 can be accomplished by switching transistors T_{a1} and T_{a2}, both off or both on respectively. These states are the same as the two-level inverter yielding a line-to-ground voltage of zero or the dc voltage.

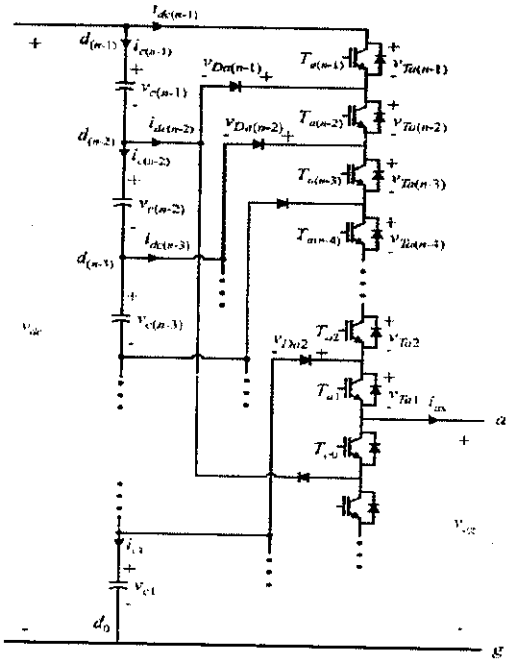


Fig 1.5: n-level diode clamped inverter

Connection to the junction d_1 is accomplished by gating T_{a1} off and T_{a2} on. In this representation, the labels T_{a1} and T_{a2} are used to identify the transistors as well as the transistor logic (1=on and 0=off). Since the transistors are always switched in pairs, the complement transistors are labeled T_{a1} and T_{a2} accordingly. In a practical implementation, some dead time is inserted between the transistor signals and their complements meaning that both transistors in a complementary pair may be switched off for a small amount of time during a transition. However, for the discussion herein, the dead time will be ignored. It can be seen that, with this switching state, the a-phase current as I will flow into the junction through diode D_{a1} if it is negative or out of the junction through diode D_{a2} if the current is positive. If each capacitor is charged to one-half of the dc voltage, then the line-to-ground voltage can be calculated. The general n-level modulator determines the switching state for each phase. For practical implementation, the switching state needs to be converted into MOSFET signals.

1.3.1.2 Flying Capacitor-Clamped Inverter

Another fundamental multilevel topology, the flying capacitor, involves series connection of capacitor clamped switching cells. This topology has several unique and attractive features when compared to the diode-clamped inverter. One feature is that added clamping diodes are not needed. Furthermore, the flying capacitor inverter has switching redundancy within the phase which can be used to balance the flying capacitors so that only one dc source is needed.

The general concept of operation is that each flying capacitor is charged to one-half of the dc voltage and can be connected in series with the phase to add or subtract this voltage.

In comparison to the three-level diode-clamped inverter, an extra switching state is possible. In particular, there are two transistor states which make up the level S_{a1}. Considering the direction of the a-phase flying capacitor current i_{ac1} for the redundant states, a decision can be made to charge or discharge the capacitor and therefore, the capacitor voltage can be regulated to its desired value by switching within the phase. The current i_{adc} is the a-phase component of the dc current. The total dc current can be calculated by summing the components for all phases.

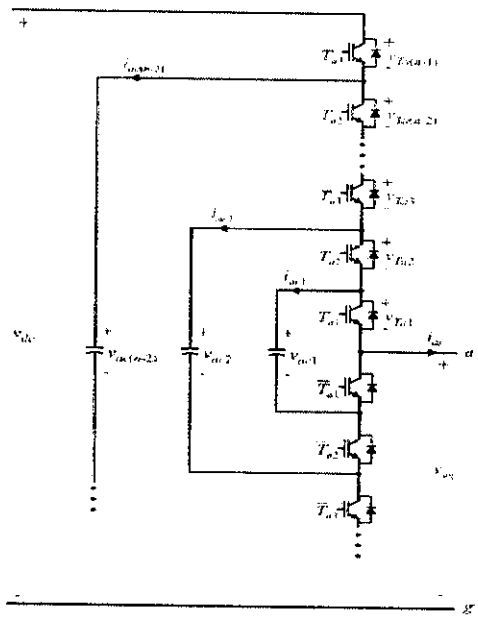


Fig 1.6: n-level capacitor clamped inverter

The structure for the four-level flying capacitor inverter is shown in Fig 1.6. For this inverter, the capacitors V_{ac1} and V_{ac2} are ideally charged to one - third and two-thirds of the dc voltage respectively.

As with the three-level flying capacitor inverter, the highest and lowest switching states do not change the charge of the capacitors. The two intermediate voltage levels contain enough redundant states that both capacitors can be regulated to their ideal voltages.

TOPOLOGY OF PROPOSED 3-PHASE INVERTER

CHAPTER-2

CONVERTER

2.1 INTRODUCTION

As discussed in the previous chapter there are many types of multilevel inverters. In this chapter cascaded H-bridge type inverter is discussed. Cascaded H-bridge multilevel inverter has an advantage as it does not require any inductor for the conversion from DC to AC which results in the higher power density.

2.2 TOPOLOGY OF PROPOSED 3-PHASE INVERTER

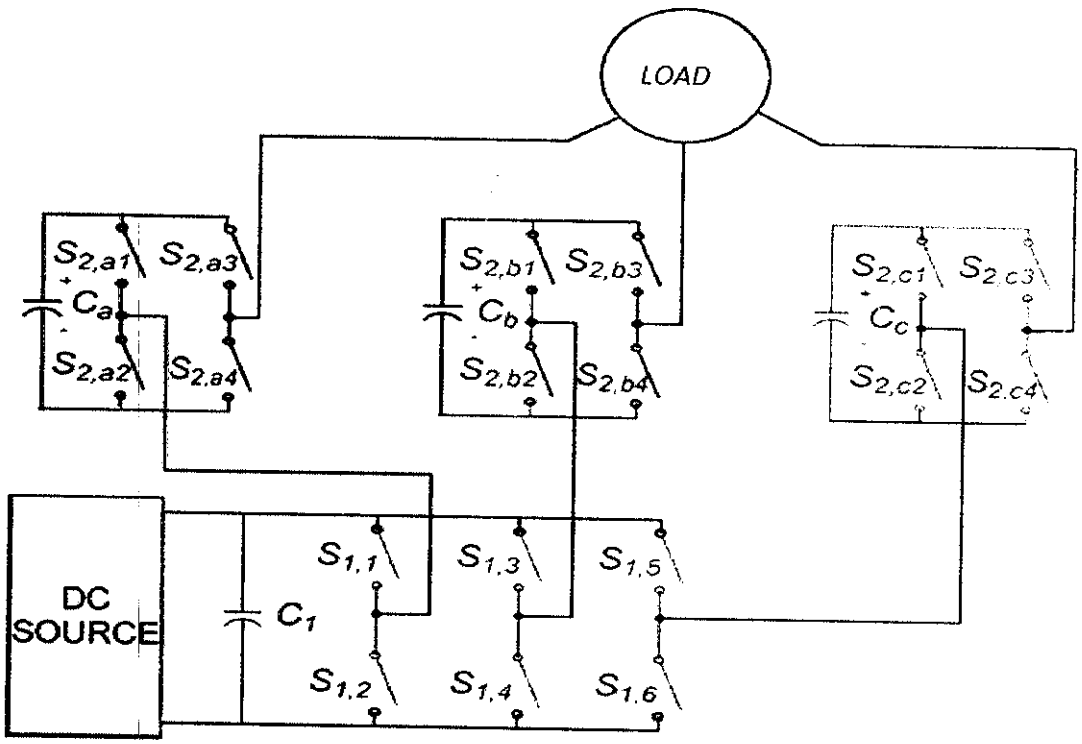


Fig 2.1: Three-Phase H-Bridge multilevel boost inverter

The proposed topology of the three phase cascaded H-Bridge inverter is shown in Fig 2.1. $S_{1,1}$ represents the switch 1 of the first phase in the main inverter bridge where as $S_{2,a1}$ represents the switch of first phase in the capacitor bridge.

The inverter uses a standard three-leg inverter (one leg for each phase) and an H-bridge with a capacitor as its DC source in series with each phase leg.

2.3 TOPOLOGY OF PROPOSED 1-PHASE INVERTER

The proposed topology of the three phase cascaded H-Bridge inverter is shown in Fig 2.2.

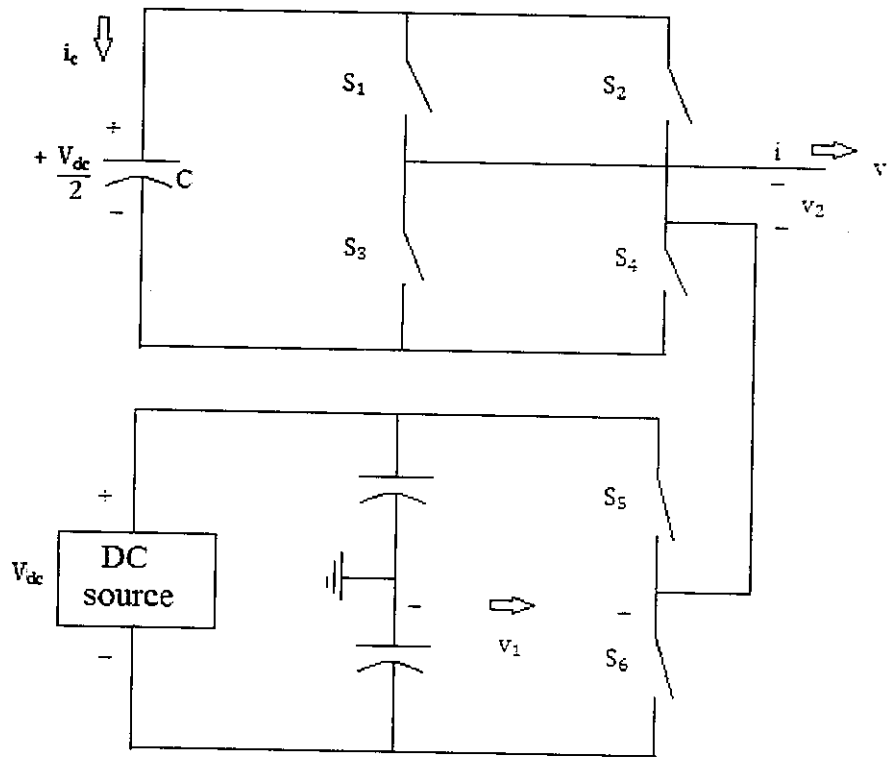


Fig 2.2: Single-Phase H-Bridge multilevel boost inverter

2.4 OPERATION OF THE INVERTER

A simplified single phase topology is shown in Fig 2.2. The output voltage $v1$ of this leg of the bottom inverter (with respect to the ground) is either $+\frac{V_{dc}}{2}$ (S_5 closed) or $-\frac{V_{dc}}{2}$ (S_6 closed). This leg is connected in series with a full H-bridge, which, in turn, is supplied by a capacitor voltage. If the capacitor is kept charged to $\frac{V_{dc}}{2}$, then the output voltage of the H-bridge can take on the values $+\frac{V_{dc}}{2}$ (S_1 and S_4 closed), 0 (S_1 and S_2 closed or S_3 and S_4 closed), or $-\frac{V_{dc}}{2}$ (S_2 and S_3 closed).

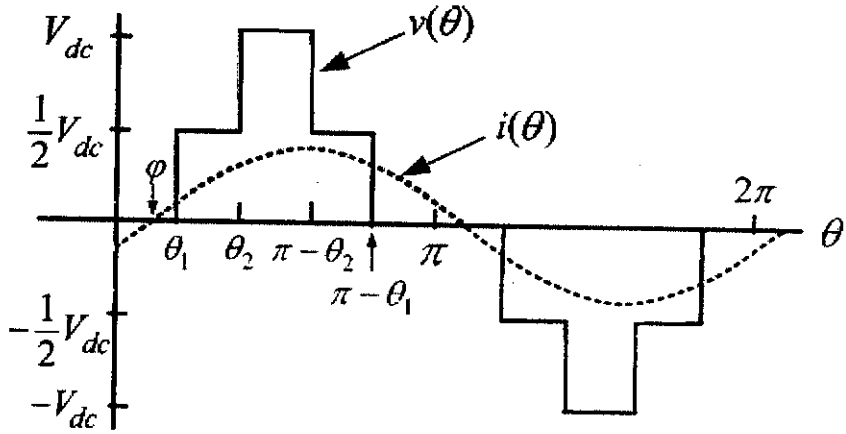


Fig 2.3: Overall output voltage and load current

An example output waveform from this topology is shown in Fig 2.3. When the output voltage $v = v1 + v2$ is required to be zero, one can either set $v1 = +\frac{V_{dc}}{2}$ and $v2 = -\frac{V_{dc}}{2}$ or $v1 = -\frac{V_{dc}}{2}$ and $v2 = +\frac{V_{dc}}{2}$. To explain how the capacitor is kept charged, consider the interval $\theta 1 \quad \theta \quad \pi$, the output voltage in Fig 2.3 is zero, and the current $i > 0$. If S_1 and S_4 are closed (so that $v2 = +\frac{V_{dc}}{2}$) and S_6 is closed (so that $v1 = -\frac{V_{dc}}{2}$), then the capacitor is discharging [$ic = -i < 0$], and $v = v1 + v2 = 0$. On the other hand, if S_2 and S_3 are closed (so that $v2 = \frac{V_{dc}}{2}$) and

S_5 is also closed (so that $v1 = +\frac{V_{dc}}{2}$), then the capacitor is charging [$ic = i > 0$], and $v = v1 + v2 = 0$.

Table 2.1 shows the switching sequence of the proposed single phase inverter.

	S_1	S_2	S_3	S_4	S_5	S_6
0 V	0	1	1	0	1	0
$+\frac{V_{dc}}{2}$	1	1	0	0	1	0
$+V_{dc}$	1	0	0	1	1	0
$+\frac{V_{dc}}{2}$	1	1	0	0	1	0
0V	0	1	1	0	1	0
0 V	0	1	1	0	1	0
$-\frac{V_{dc}}{2}$	1	1	0	0	0	1
$-V_{dc}$	0	1	1	0	0	1
$-\frac{V_{dc}}{2}$	1	1	0	0	0	1
0V	0	1	1	0	1	0

Table 2.1: Operation of H-Bridge multilevel boost inverter

The case $i < 0$ is accomplished by simply reversing the switch positions of the i> 0 case for charging and discharging of the capacitor. Consequently, the method consists of monitoring the output current and the capacitor voltage, so that during periods of zero voltage output, either the switches S_1, S_4, and S_6 are closed or the switches S_2, S_3, and S_5 are closed, depending on whether it is necessary to charge or discharge the capacitor. It is this flexibility in choosing how to make that output voltage zero that is exploited to regulate the capacitor voltage. The goal of using fundamental frequency switching modulation control is to output a five-level voltage waveform, with a sinusoidal load current waveform, as shown in Fig 2.3. If the capacitor's voltage is higher than $V_{dc}/2$, switches S_5 and S_6 are controlled to output

voltage waveform $v1$, and the switches S_1, S_2, S_3, and S_4 are controlled to output voltage waveform $v2$.

2.5 MODES OF OPERATION

The proposed single phase cascaded inverter produces five levels of output voltage. The corresponding five levels are: $-V_{dc}$, $-\frac{V_{dc}}{2}$, 0, $\frac{V_{dc}}{2}$and V_{dc}.

Mode for 0V:

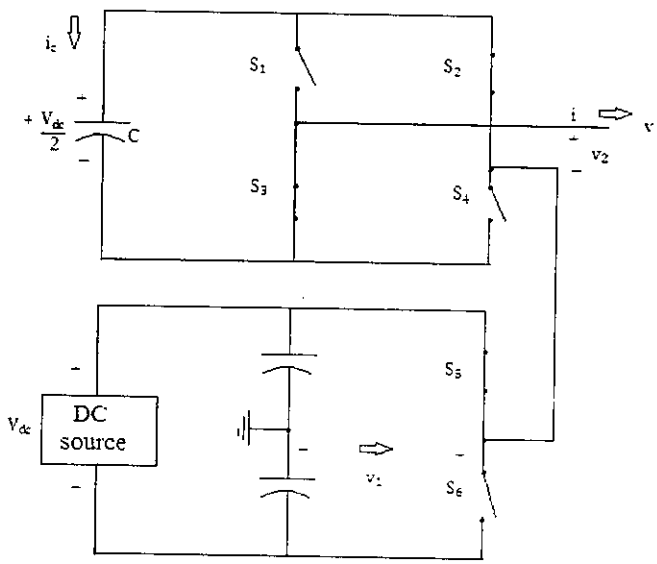


Fig 2.4: Mode for 0V

In this mode, switches S_2,S_3 and S_5 are switched on. Upper bridge i.e., S_2 and S_3 will produce the output voltage of $-\frac{V_{dc}}{2}$ while the lower bridge i.e. switch S_5 will produce output voltage of $\frac{V_{dc}}{2}$. Thus the net output will be v1+v2=0. Fig 2.4 shows the mode for 0V.

Mode for $\frac{V_{dc}}{2}$:

In this mode, switches S_1,S_2 and S_5 are switched on. Upper bridge i.e., S_1 and S_2 will produce the output voltage of 0V as they have zero potential difference while the lower bridge i.e. switch S_5 will produce output voltage of $\frac{V_{dc}}{2}$. Thus the net output will be v1+v2=$\frac{V_{dc}}{2}$. Fig 2.5 shows the mode for $\frac{V_{dc}}{2}$.

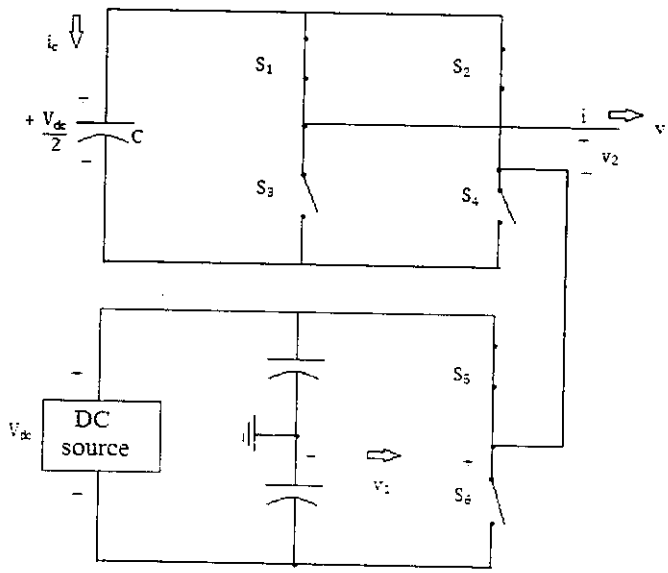


Fig 2.5: Mode for $\frac{V_{dc}}{2}$

Mode for V_{dc}:

In this mode, switches S_1,S_4 and S_5 are switched on. Upper bridge i.e., S_1 and S_4 will produce the output voltage of $\frac{V_{dc}}{2}$while the lower bridge i.e. switch S_5 will produce output voltage of $\frac{V_{dc}}{2}$. Thus the net output will be v1+v2=V_{dc}. Fig 2.6 shows the mode for V_{dc}.

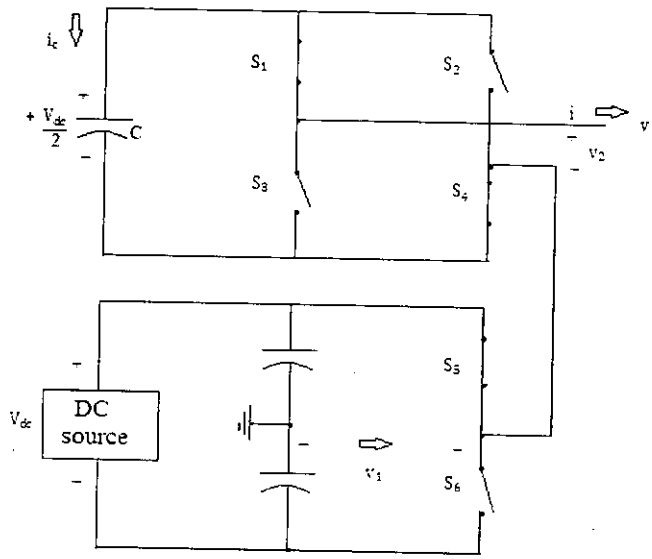


Fig 2.6: Mode for V_{dc}

Mode for $-\frac{V_{dc}}{2}$:

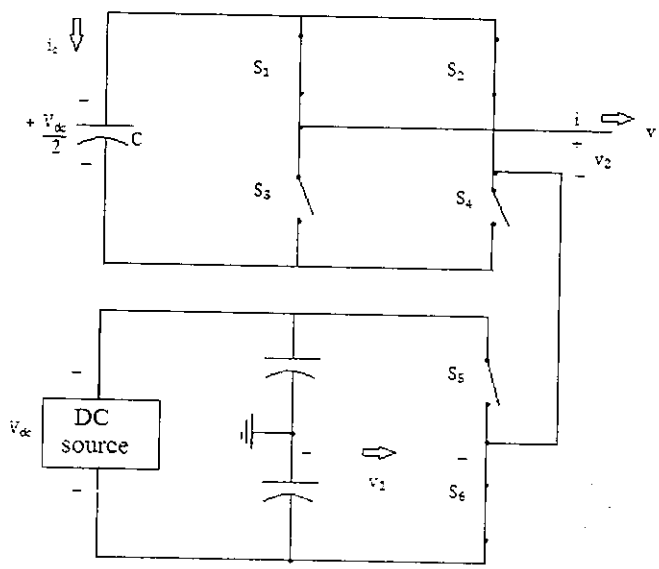


Fig 2.7: Mode for $-\frac{V_{dc}}{2}$

In this mode, switches S_1,S_2 and S_6 are switched on. Upper bridge i.e. S_1 and S_2will produce the output voltage of 0V as they have zero potential difference while the lower bridge i.e. switch S_6 will produce output voltage of $-\frac{V_{dc}}{2}$. Thus the net output will be v1+v2=$-\frac{V_{dc}}{2}$.

Fig 2.7 shows the mode for $-\frac{V_{dc}}{2}$.

Mode for $-V_{dc}$:

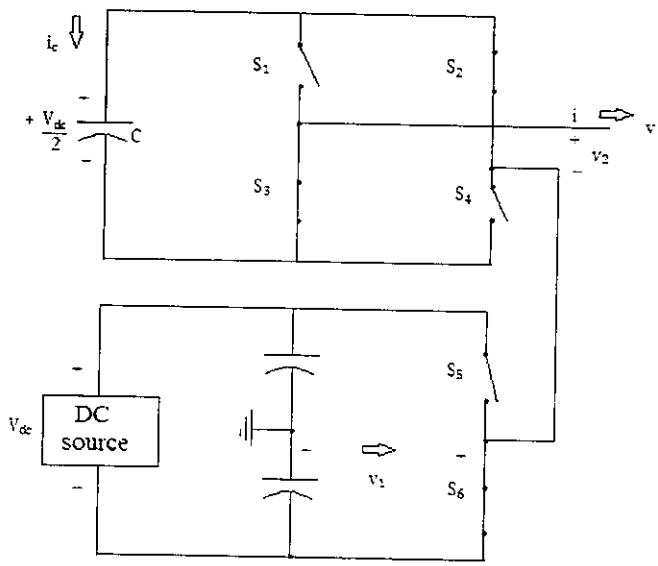


Fig 2.8: Mode for $-V_{dc}$

In this mode, switches S_2,S_3 and S_6 are switched on. Upper bridge i.e. S_2 and S_3 will produce the output voltage of $-\frac{V_{dc}}{2}$while the lower bridge i.e. switch S_6 will produce output voltage of $-\frac{V_{dc}}{2}$. Thus the net output will be v1+v2=$-V_{dc}$. Fig 2.8 shows the mode for - V_{dc}.

BLOCK DESCRIPTION

CHAPTER-3

BLOCK DESCRIPTION

3.1 INTRODUCTION

Block diagram is typically used for a higher level, less detailed description aimed more at understanding the overall concepts and less at understanding the details of implementation. In this chapter the overall block diagram of the project will be discussed.

3.2 BLOCK DIAGRAM

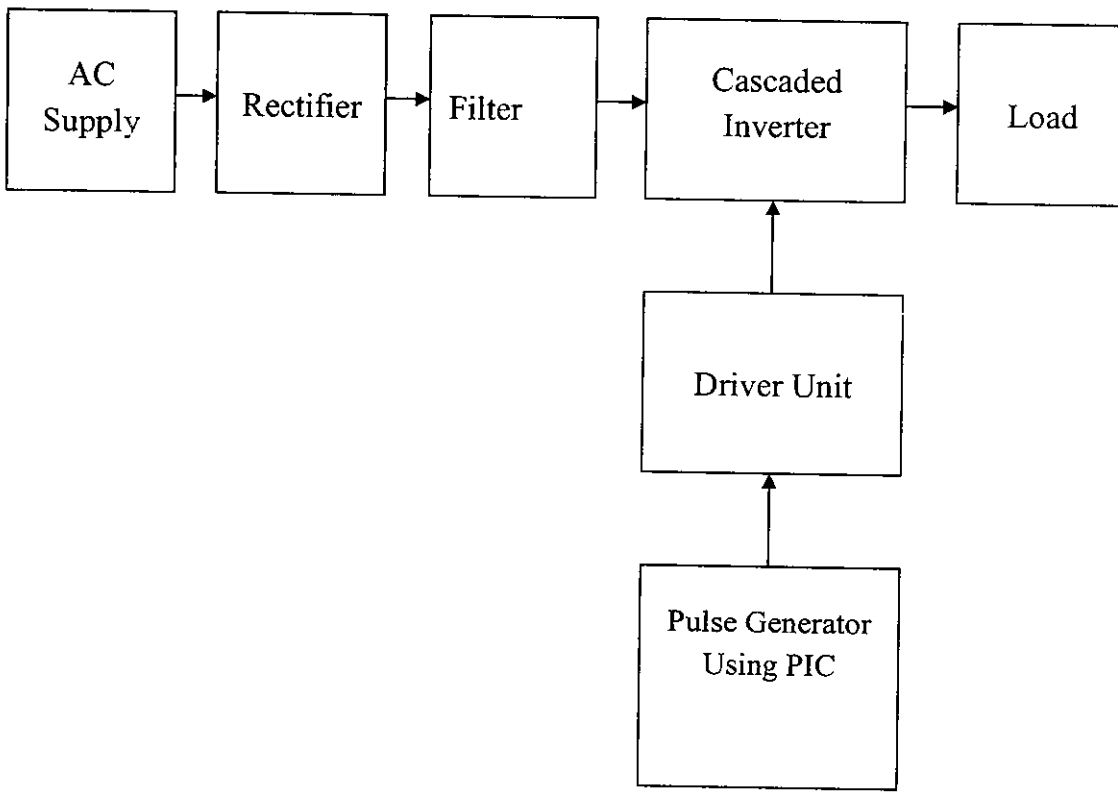


Fig 3.1: Block diagram of H-bridge Multilevel Boost Inverter

3.3 DESCRIPTION

3.3.1 Power Supply Circuit

Power supply circuit comprises of AC supply, rectifier and filter. Initially the 230 V AC supply is stepped down to 24 V AC and the output AC voltage is given to the rectifier bridge. The bridge rectifier rectifies the input ac voltage to the dc voltage of the same magnitude i.e., 24 V AC is converted into 24 V DC. The 24 V DC output obtained from the bridge will be pulsating DC. Then this is given to the capacitor of 1000 μF in order to remove the ripples in the output so as to obtain the pure DC.

3.3.2 Cascaded Inverter Unit

The output dc obtained from capacitor is the input given to the inverter unit. In this cascaded inverter part, two separate bridges are constructed. For inverter switches IRF 840 MOSFET is used. Each bridge is capable of producing an output of 0V or max to a magnitude of $V_{dc}/2$. MOSFET is used as a switch as it does not require separate commutation circuit.

3.3.3 Pulse Generator

For inverter operation the gate pulse has to be generated. A pulse generator can either be an internal circuit or a piece of electronic test equipment used to generate pulses. This pulse is generated using a PIC with certain pulse delays. Separate dc power supply has to be given for this PIC.

3.3.4 Driver Unit

The output obtained from the PIC will not able to drive the gate of the MOSFET due to the lower amplitude of the current. So this has to be amplified. For this driver unit is needed. Separate power supply has to be provided for the driver unit. Driver unit basically consists of buffer and optocoupler circuit. Buffer is used to provide electrical impedance transformation from one circuit to another. The output obtained from PIC is given to Buffer CD4049 and the output obtained from the buffer is given to the optocoupler SFH615. The output of the optocoupler is used to drive the gate of the MOSFET.

3.3.5. Load

Inverter output is given to the resistive load of 10 kilo ohms with a star connected but it has been used for any load based on the output voltage obtained.

HARDWARE DESCRIPTION

CHAPTER-4

HARDWARE DESCRIPTION

4.1 INTRODUCTION

This chapter deals with the actual circuit of each block. All the blocks including power supply circuit, PIC circuit, driver unit and main inverter unit will be explained in detail in this chapter.

4.2 POWER SUPPLY CIRCUIT

The supply voltage is of higher magnitude that it cannot be directly applied to the circuit. Hence, it is necessary to step down the voltage to the required level. Three step-down transformers are used in the overall setup. One is used for the obtaining the main supply for the inverter bridges, one for the PIC controller and another one for optocoupler.

4.2.1 Power circuit for Inverter

The inverter circuit requires a DC input. But the available source is an AC source that, it is required to be converted to DC. This is done with the help of Rectifier Bridge. Rectifier Bridge consists of four diodes that are biased such that the rectification is done. Rectifier Bridges are mainly used to convert Alternating Current to Direct Current. Filters are required to remove the ripples present in the output of the rectifier. 63V, 1000μF electrolytic capacitor is used as Filter.

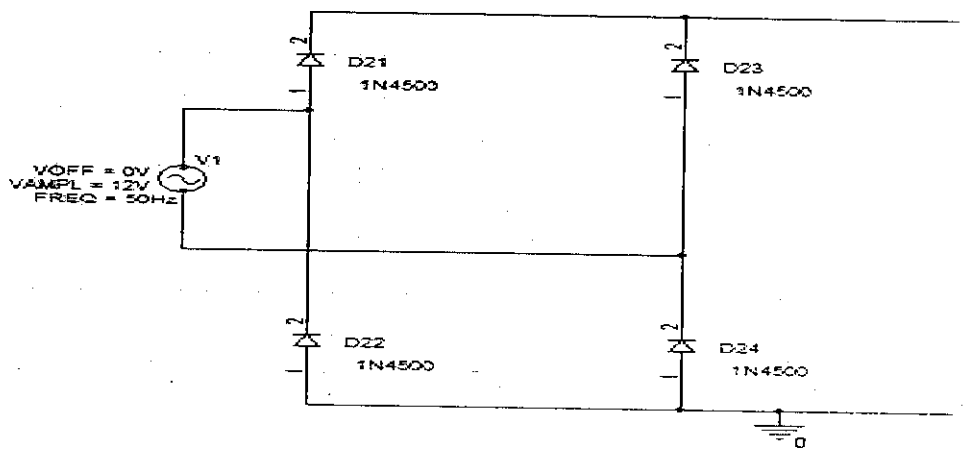


Fig 4.1: Power supply diagram without filter

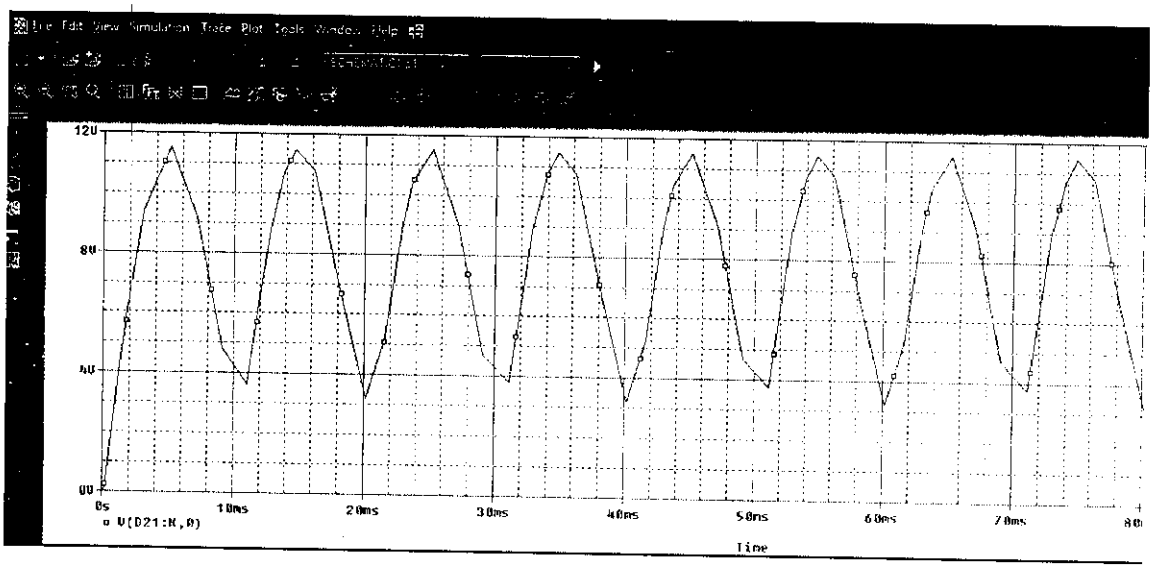


Fig 4.2: Output waveform without filter

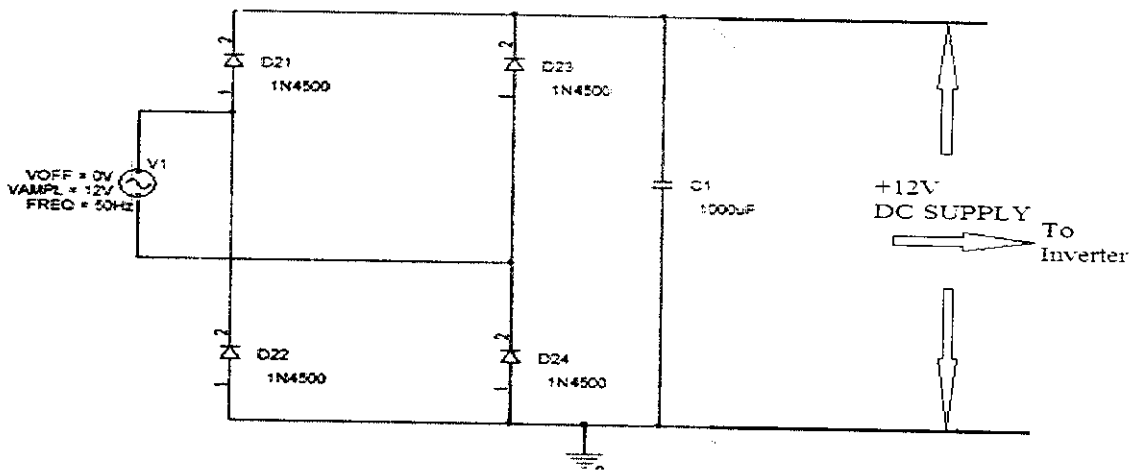


Fig 4.3: Power supply diagram with filter

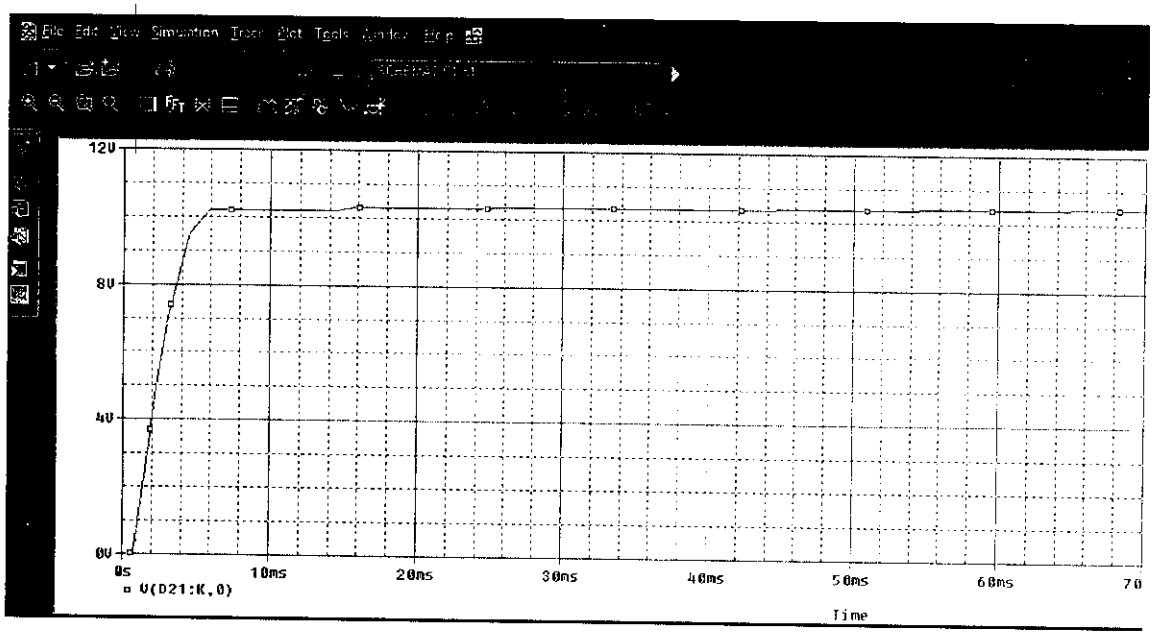


Fig 4.4 Output waveform with filter

4.2.2 Power circuit for PIC

The PIC microcontroller PIC 16F877 requires a 5V DC supply. So it has to be provided separately. This power supply is obtained by stepping down the 230V supply transformer to 12V AC. This is given to a diode bridge to convert it into 12V DC. Then this has to be given to capacitor of 470 μF to remove the ripples so as to obtain the pure DC. This is then given to the 7805 voltage regulator so as to obtain 5V DC constantly. This resulted 5V DC supply is given to the PIC. This same supply is used for buffer IC also.

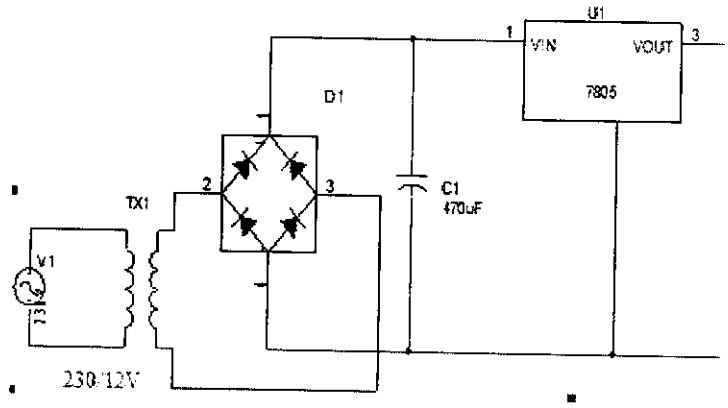


Fig 4.5: Power circuit for Microcontroller PIC16F877

4.2.3 Power circuit for Optocoupler

Optocoupler secondary has to be provided with separate supply in order to avoid confusion with ground of the PIC supply. The power supply circuit is similar to the one which is used for PIC. Instead of using 5V voltage regulator we had used 9V voltage regulator. Using a 5V voltage regulator sometimes provides only 3.5V on secondary output which is sometimes not sufficient for gate to trigger. So in order to obtain boosted voltage we are using a 9V voltage regulator. It gives output of minimum of 6V which is more sufficient for gate to trigger.

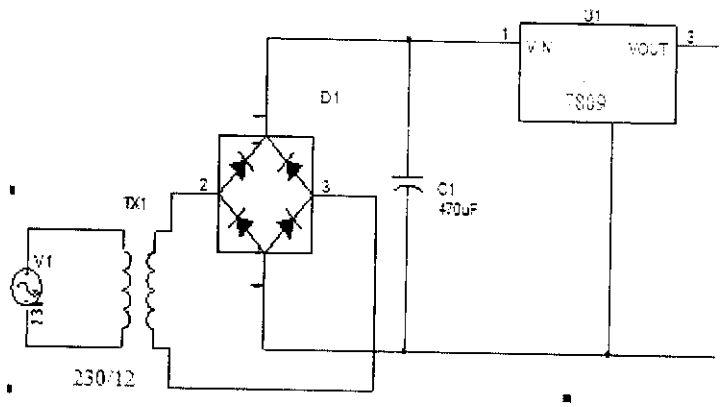


Fig 4.6: Power circuit for optocoupler

4.3 INVERTER CIRCUIT

The switches used in the inverter circuit are MOSFETs. Two inverter bridges are connected in cascade. Hence, the circuit requires eight MOSFETs. But here the number of MOSFETs used is reduced by employing two 63V, 1000μF electrolytic capacitors in the lower bridge. The working of the inverter circuit is already discussed in the chapter 2.The MOSFETs are switched at proper time intervals to produce the required sinusoidal waveform. The MOSFET used is IRF 840.

4.4 BUFFER UNIT

The output obtained from the PIC 16F877 is sent to buffer CD4049 for the purpose of impedance matching. I had generated six pulses from the PIC. So I want to choose a buffer which has at least six input terminals. So I has chosen buffer CD4049 for this purpose. The pin diagram of the buffer IC is shown in Fig 4.7.

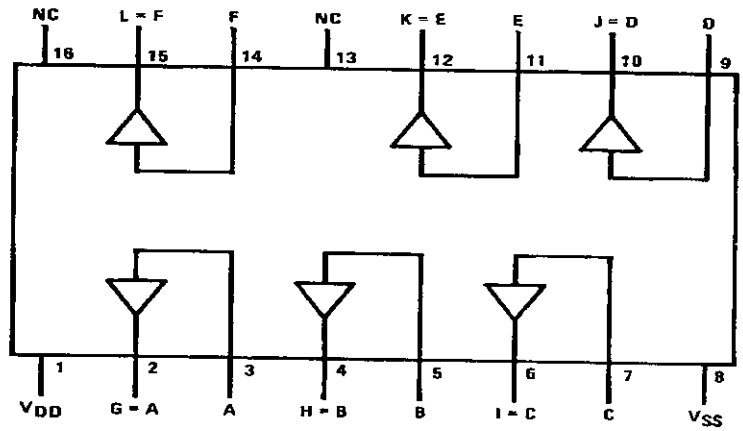


Fig 4.7 Pin diagram of Buffer(CD 4049)

4.5 DRIVER CIRCUIT

The output obtained from the buffer do not has sufficient strength for driving the gate of the MOSFET. So this has to be supplied to driver unit. Driver unit normally consists of optocoupler. Optocoupler used is SFH615.

An optocoupler is used to transfer signal from one subsystem to another within a piece of electronic equipment, or from one piece of equipment to another, without making a direct ohmic electrical connection. This is because the source and destination are (or may be

at times) at very different voltage levels, like a microprocessor, which is operating from 5V DC but being used to control a triac that is switching 240V AC. In such situations the link between the two must be an isolated one, to protect the microprocessor from over voltage damage. So, ultimate choice is choosing an optocoupler. It consists of a LED and a transistor.The primary side consists of LED and secondary side contains a photo transistor. Primary side input is obtained from the buffer output. Secondary side input is fed through a 7809 voltage regulator. Secondary side output is sent to gate of the MOSFET for the trigerring purpose.

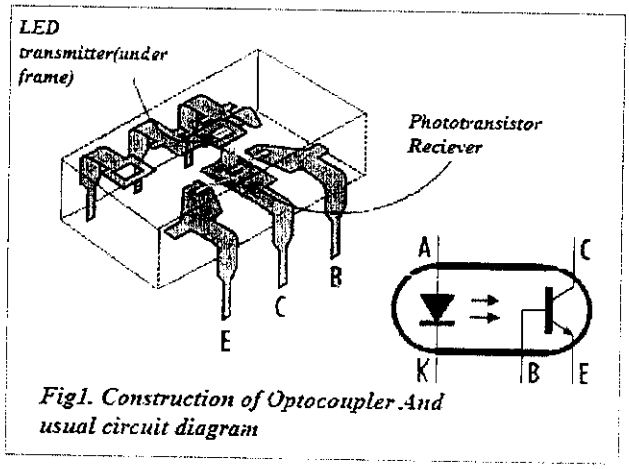


Fig1. Construction of Optocoupler And usual circuit diagram

Fig 4.7: Construction of SFH615

PROGRAMMABLE INTERFACE CONTROLLER (PIC)

CHAPTER-5
PROGRAMMABLE INTERFACE CONTROLLER (PIC)
PIC 16F877

5.1 INTRODUCTION

PICs are popular in industrial developers due to their low cost, wide availability, large user base, extensive application of application notes and serial programming capability. In this chapter the pin diagram of PIC 16F877 along with the coding with the help of algorithm and flowchart will be discussed.

5.2 PIN DIAGRAM

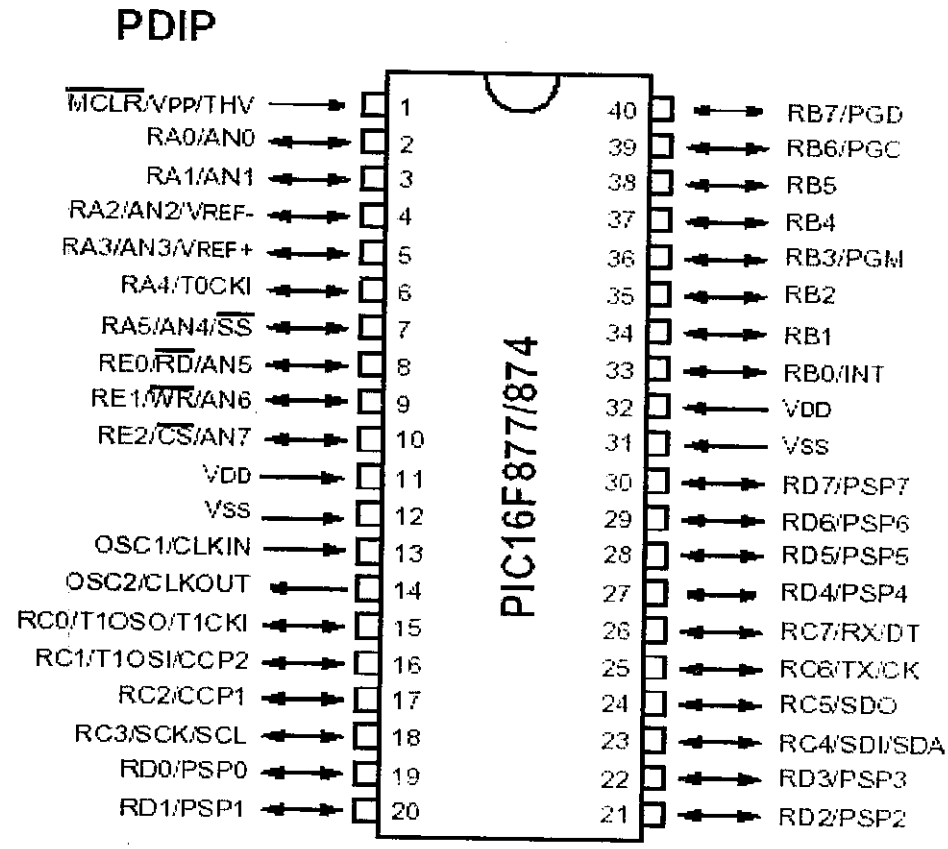


Fig 5.1 PIC 16F877 PIN DETAILS

5.3 FLOWCHART:

Fig 5.2 shows the flowchart of the PIC program.

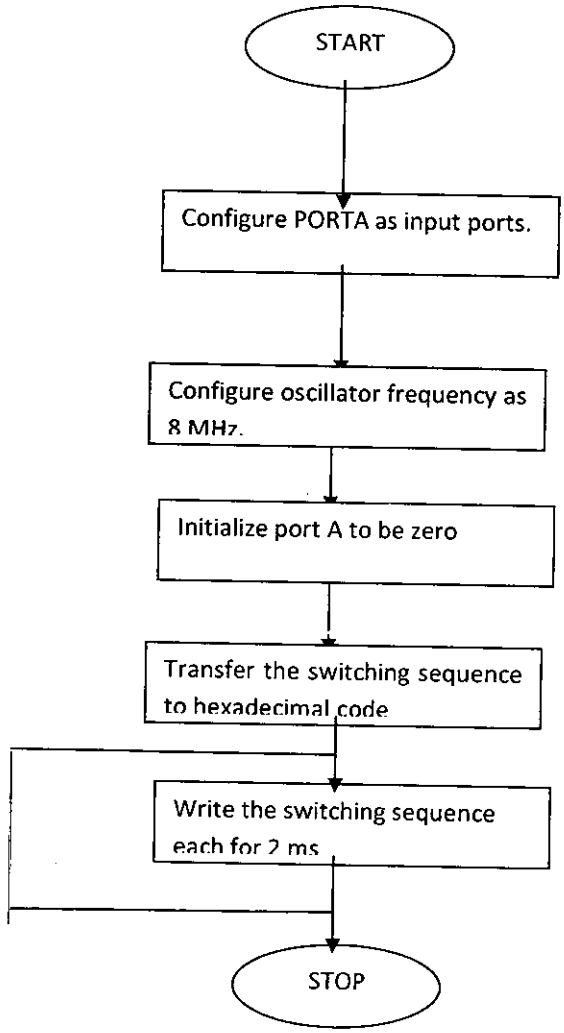


Fig 5.2 Flowchart

5.4 ALGORITHM

1. Start.

2. Configure RA0-RA5 as output ports.

3. Configure oscillator frequency as 8MHz.

4. Configure the A/D port in 18f4550.

5. Initialise Port A to be zero.

6. Start the while loop.

7. Transfer the switching sequence into the corresponding hexadecimal code.

8. Introduce the delay for 2ms for each switching sequence.

9. Stop.

SIMULATION

CHAPTER-6

SIMULATION

6.1 INTRODUCTION

Simulation actually refers to visualizing the output of the circuit without actually implementing them in the hardware. This chapter actually deals with the simulation of our inverter circuit. The simulator which we are going to use is MATLAB.

6.2 SWITCHING SEQUENCE

	S_1	S_2	S_3	S_4	S_5	S_6
0 V	0	1	1	0	1	0
$+\frac{V_{dc}}{2}$	1	1	0	0	1	0
$+V_{dc}$	1	0	0	1	1	0
$+\frac{V_{dc}}{2}$	1	1	0	0	1	0
0V	0	1	1	0	1	0
0 V	0	1	1	0	1	0
$-\frac{V_{dc}}{2}$	1	1	0	0	0	1
$-V_{dc}$	0	1	1	0	0	1
$-\frac{V_{dc}}{2}$	1	1	0	0	0	1
0V	0	1	1	0	1	0

Table 6.1 Switching sequence

The switching sequence of the switches are generated in such a way the inversion or the not function of the one pulse is another input pulse. It is shown clearly that input of S_3 is not input of S_1, input of S_4 is not input of S_2 and input of S_5 is not input of S_6.

6.3 DIAGRAM OF THE INVERTER

The simulation diagram of the inverter circuit is drawn in Fig 6.1. Voltage V_{in} is given as 24V and capacitor C_3 is initially assumed to be 12V.

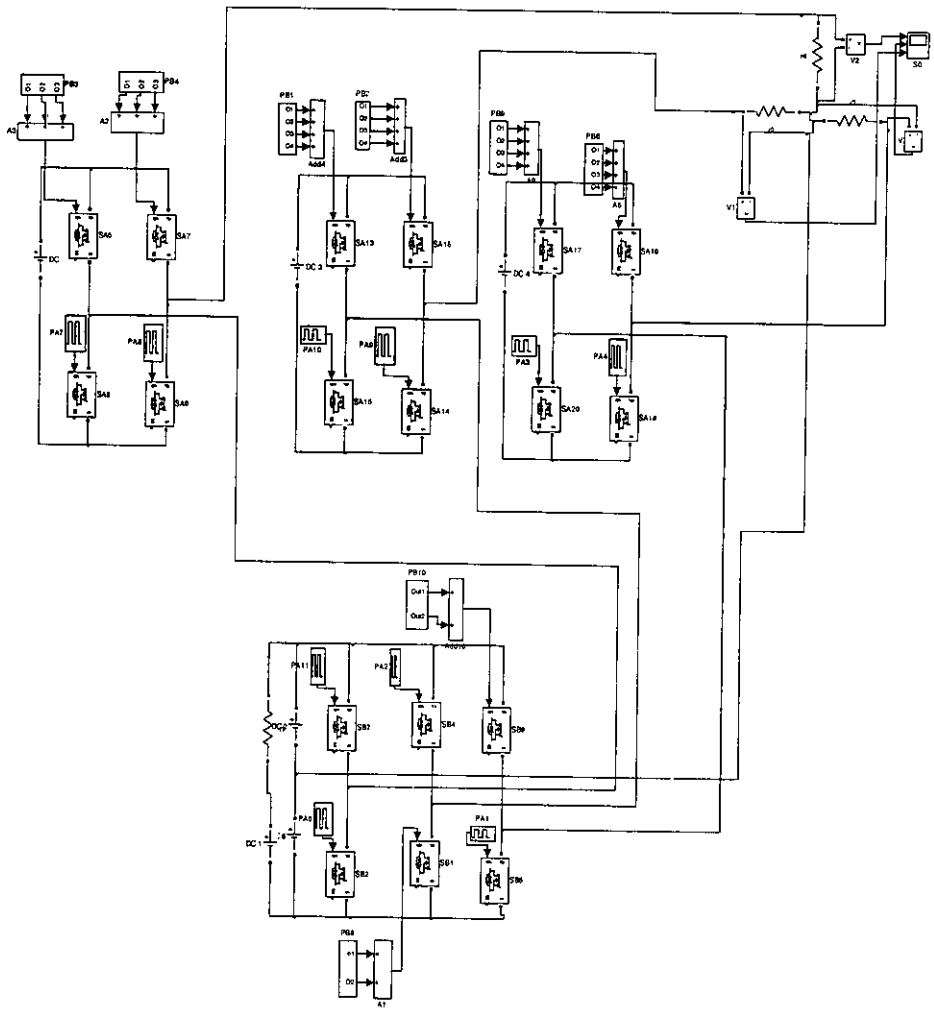


Fig 6.1: Simulation Diagram of Inverter

6.4 INPUT PULSES TO THE MOSFET

Input pulses are generated using pulse generator block. Input parameters needed are phase delay, pulse width and time. For the continuous pulse a single pulse generator is sufficient while for discontinuous pulse many number of single pulse is generated and the pulses are OR ed in order to obtain the necessary pulse.

Total time of 360 degree radian is splitted into ten parts. Therefore each part consists of 36 degree radian.

Time is calculated as inversion of frequency.

$$\text{Time}=1/(\text{Frequency})$$

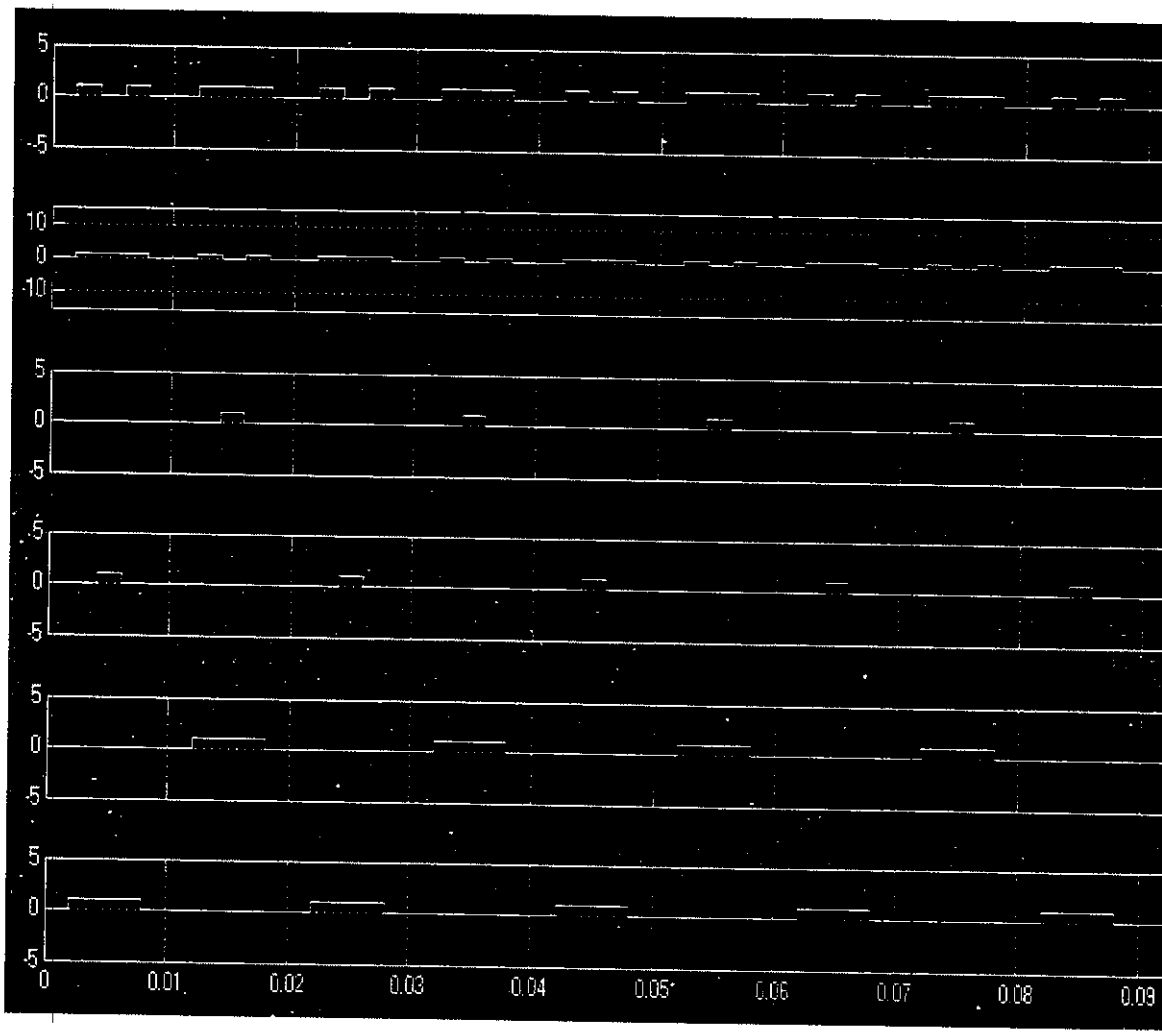
Pulse width is calculated as

$$\text{Pulse width}= [\text{Ton}/T]*100$$

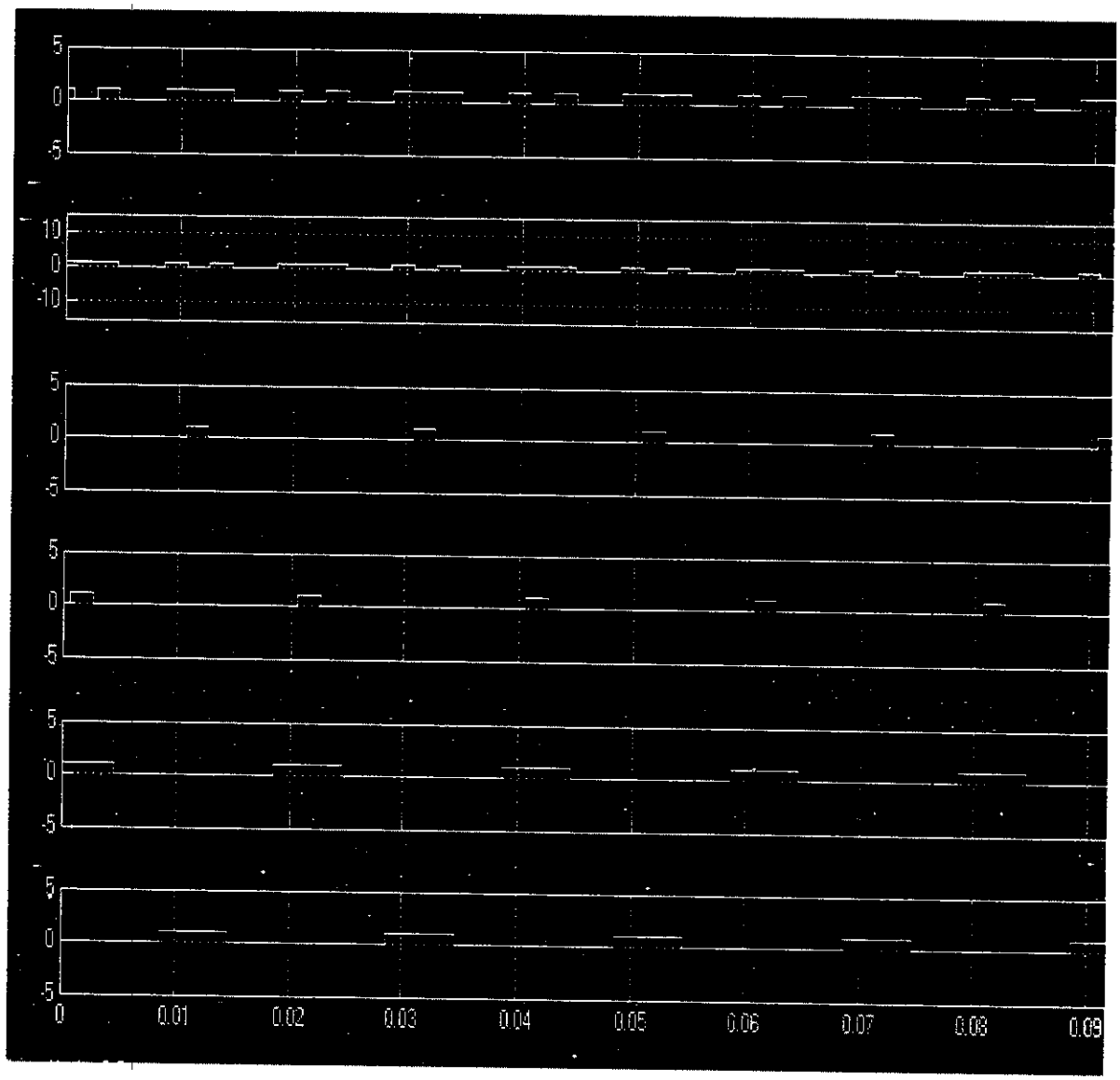
The input pulses for the inverter are calculated using the above formula and pulses are generated as shown below as in Fig 5.2. and the corresponding inverter output is shown in Fig 5.3. which is five level output and the five levels of the output are 0, $\frac{V_{dc}}{2}$, V_{dc}, $-\frac{V_{dc}}{2}$ and $-V_{dc}$.

Fig 6.2 Input pulses to the MOSFET

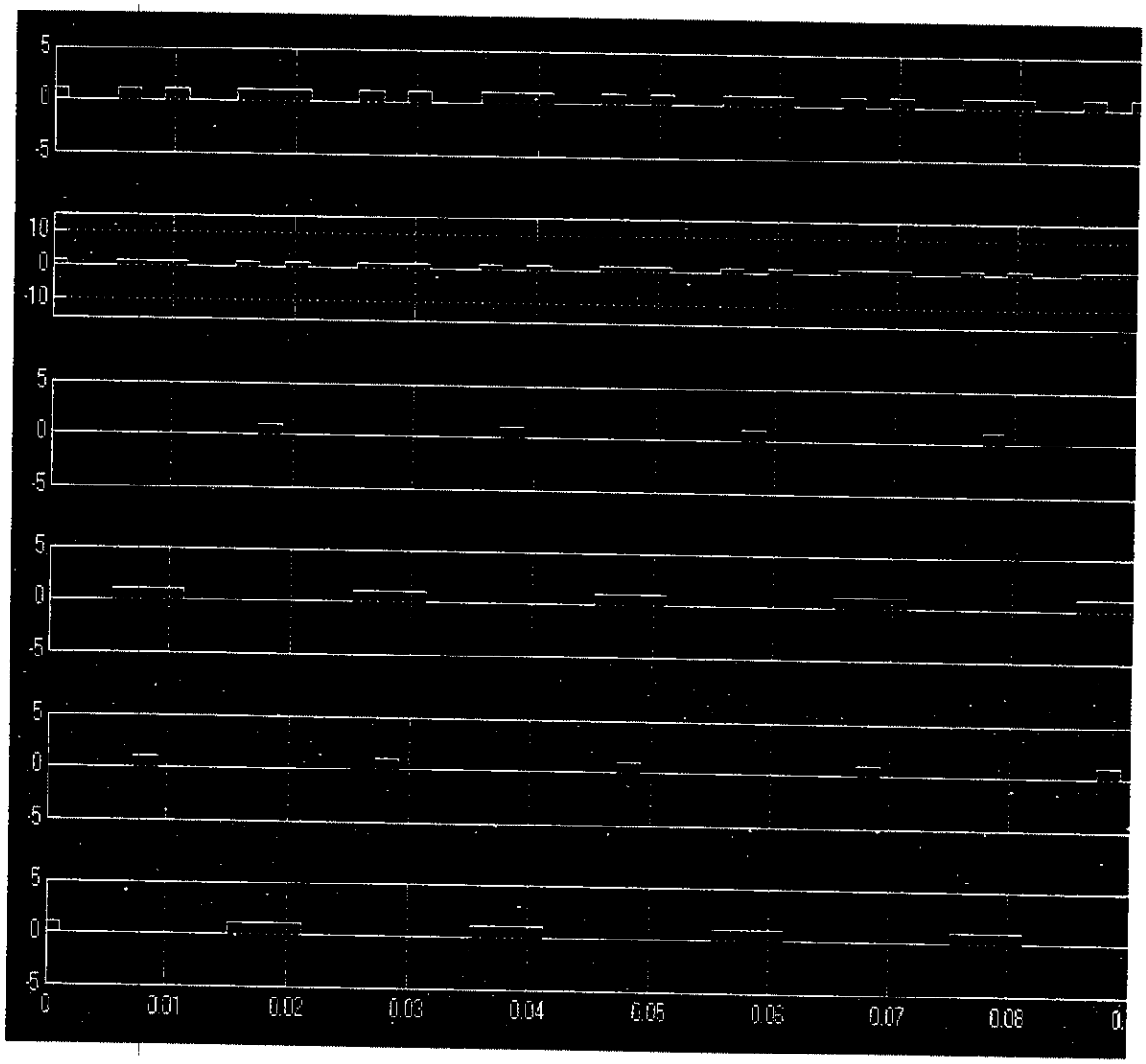
MODE 0



MODE 120



MODE 240



6.5 OUTPUT OF THE INVERTER

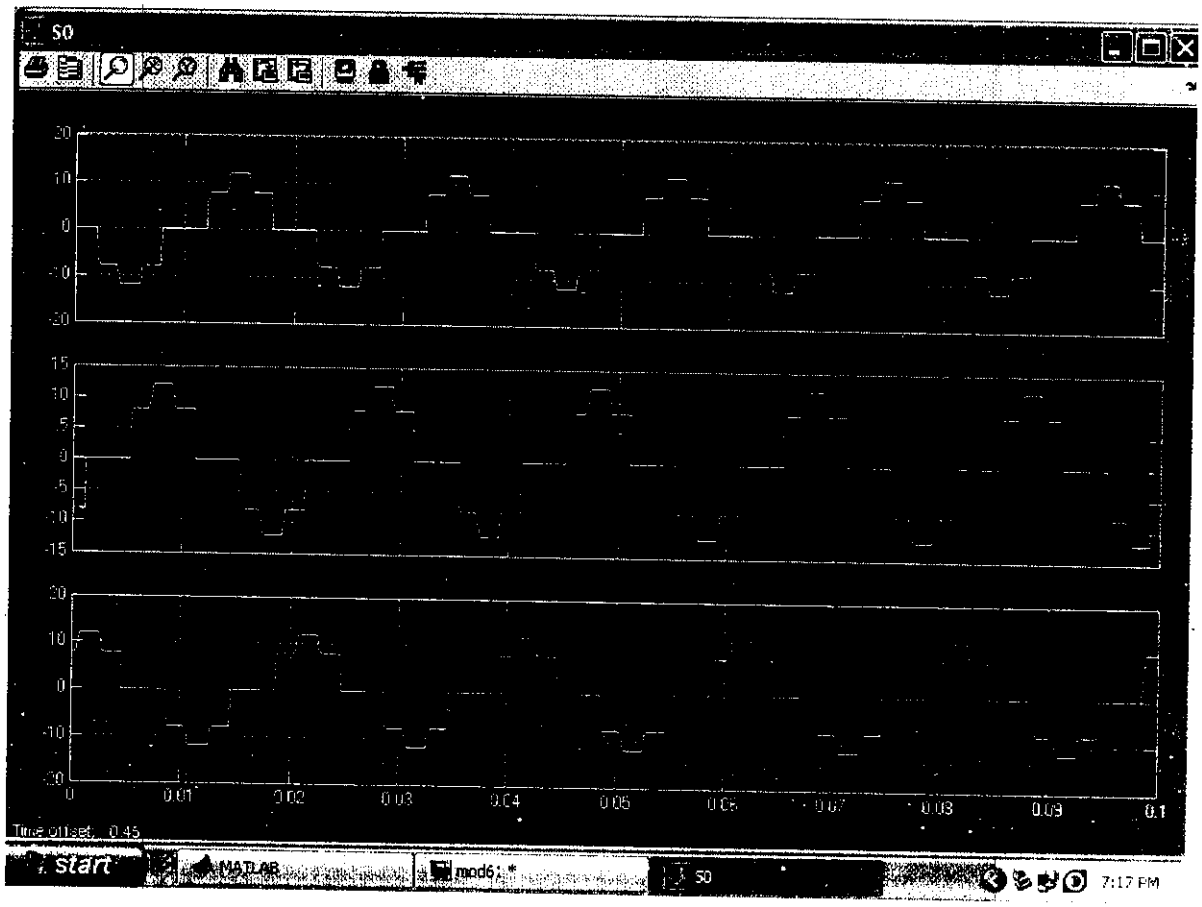


Fig 6.3 Simulation output

RESULTS

CHAPTER-7

RESULT

7.1 SIMULATION RESULT

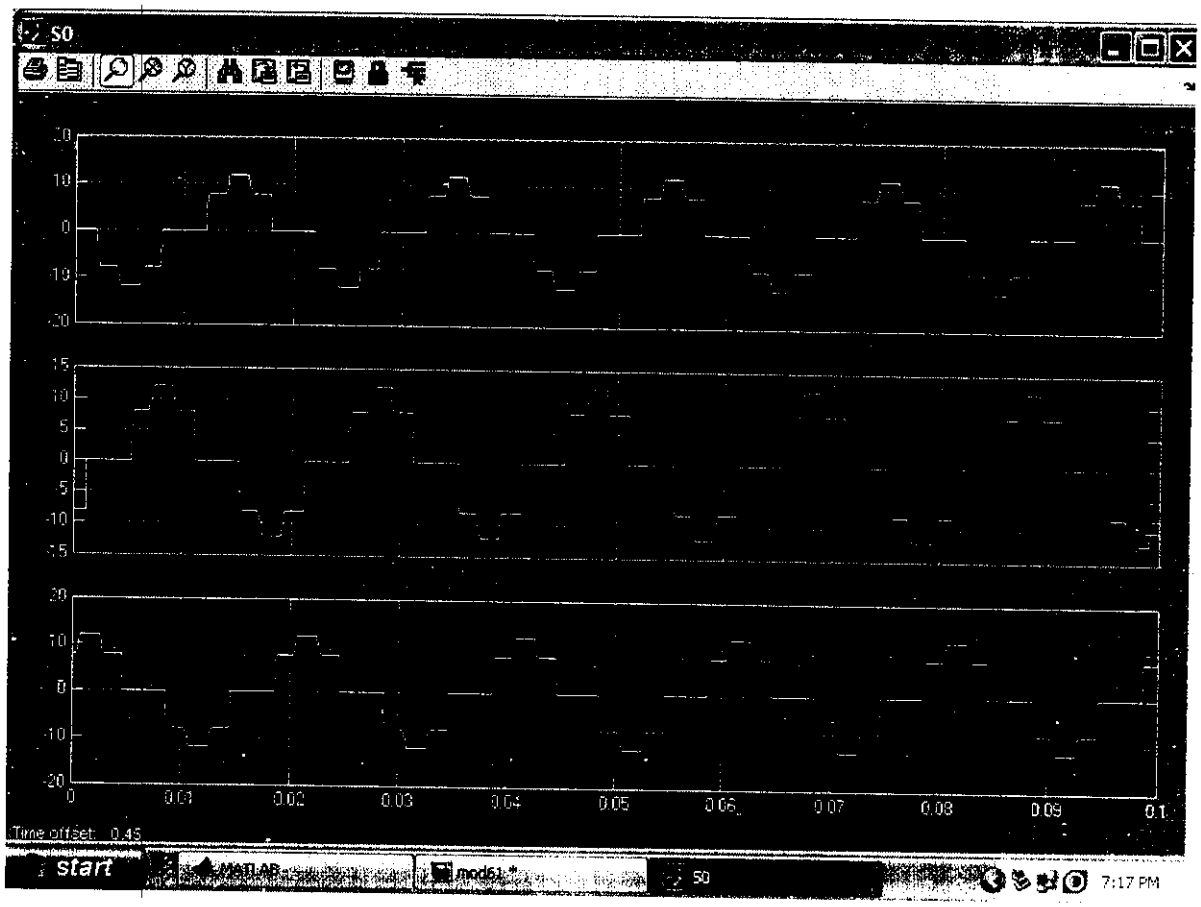


Fig 7.1 Simulation Result

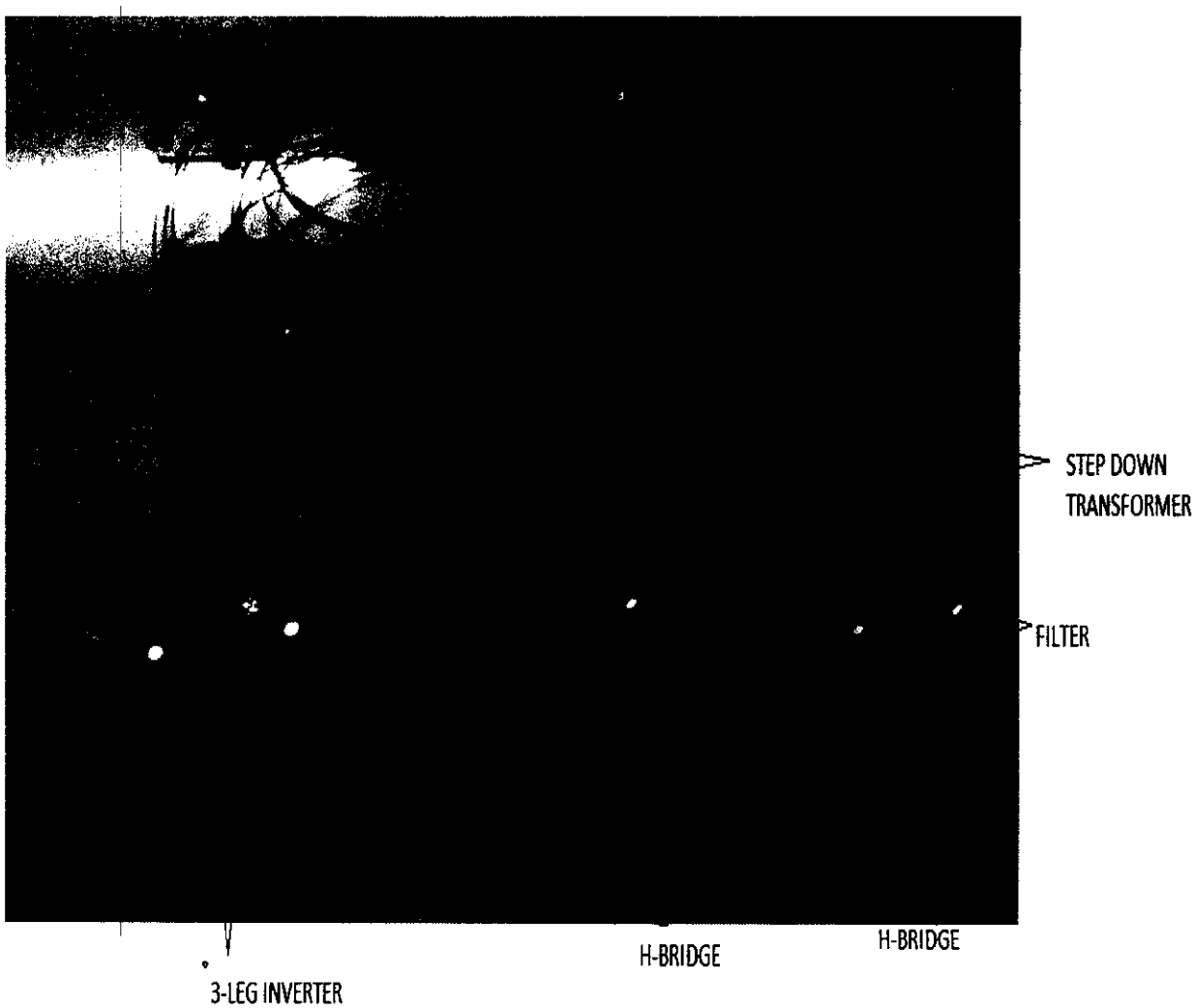
X-axis 1cm=0.01ms

Y-axis 1cm=5V

Simulation output of the cascaded H-bridge multilevel boost inverter is shown in the Fig 7.1. The magnitude of the output voltage is 24V AC and the time period of one cycle is 20ms. As said in the switching table the output is a five level output.

7.2 HARDWARE RESULT

Output of the hardware implementation is same as that of the simulation output. The magnitude of the output voltage is 24V AC and the time period of one cycle is 20ms.



CONCLUSION

CHAPTER-8

CONCLUSION

8.1 Contribution

The proposed cascaded H-bridge multilevel boost inverter without inductors uses a standard three-leg inverter (one leg for each phase) and an H-bridge in series with each inverter leg. A fundamental switching scheme is used for modulation control, to output five-level phase voltages. Experiments show that the proposed DC-AC cascaded H-bridge multilevel boost inverter can output a boosted ac voltage with the same dc power supply, which has a wider modulation index range than a traditional inverter.

8.2 Scope for Future work

The future cannot rely on the batteries which we are using now in cars and other vehicles as it still works on the old techniques which are of less use nowadays as energy conservation plays a vital role in the world which we are living. The hybrid vehicles, the automatic SUVs and hydrogen powered vehicles will form the future in this energy conscious world. Thus this technique can be used in the future as it has high power density due to the absence of bulky inductor.

APPENDIX

APPENDIX-1

CODINGS FOR PIC 18F4550 MICROCONTROLLER

```
#include<p18f4550.h>
#include<stdio.h>
#include<delays.h>
#include<math.h>


#define out1 PORTAbits.RA0
#define out2 PORTAbits.RA1
#define out3 PORTAbits.RA2
#define out4 PORTAbits.RA3
#define out5 PORTAbits.RA4
#define out6 PORTAbits.RA5


void main()
{
 ADCON1=0x0F;
 CMCON=0x07;

 TRISA=0x00;
 PORTA=0x00;

 OSCCONbits.IRCF2=1;
 OSCCONbits.IRCF1=1;
```

```
 OSCCONbits.IRCF0=1;
 OSCCONbits.IOFS=1;


while(1)
{

 PORTA=0x16;
 Delay100TCYx(40);

 PORTA=0x13;
 Delay100TCYx(40);

 PORTA=0x19;
 Delay100TCYx(40);

 PORTA=0x13;
 Delay100TCYx(40);

 PORTA=0x16;
 Delay100TCYx(40);

 PORTA=0x16;
 Delay100TCYx(40);

 PORTA=0x23;
 Delay100TCYx(40);

PORTA=0x26;
```

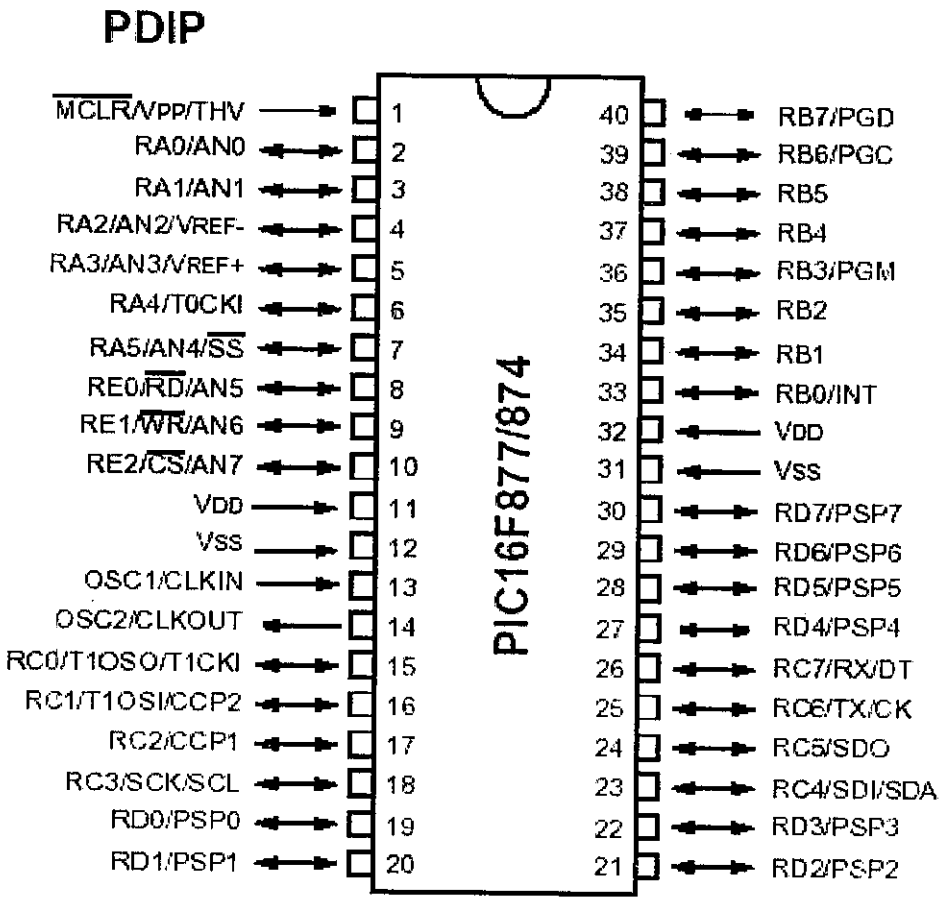
```
  Delay100TCYx(40);

  PORTA=0x23;
  Delay100TCYx(40);

  PORTA=0x16;
  Delay100TCYx(40);
}
}
```

APPENDIX-2

PIC DATASHEET(PIC 18F4550)



PIC MICROCONTROLLER

4.1 CORE FEATURES:

- High-performance RISC CPU
- Only 35 single word instructions to learn
- Operating speed: DC - 20 MHz clock input

  DC - 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory,

  Up to 368 x 8 bytes of Data Memory (RAM)

  Up to 256 x 8 bytes of EEPROM data memory
- Interrupt capability (up to 14 internal/external
- Eight level deep hardware stack
- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC Oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- In-Circuit Serial Programming (ICSP) via two pins
- Only single 5V source needed for programming capability
- In-Circuit Debugging via two pins
- Wide operating voltage range: 2.5V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial and Industrial temperature ranges

• Low-power consumption:

< 2 mA typical @ 5V, 4 MHz

20mA typical @ 3V, 32 kHz

< 1mA typical standby current

4.2 Peripheral Features:

• Timer0: 8-bit timer/counter with 8-bit prescaler

• Timer1: 16-bit timer/counter with prescaler

• Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler

• Two Capture, Compare, PWM modules

Capture is 16-bit, max resolution is 12.5 ns,

Compare is 16-bit, max resolution is 200 ns,

PWM max. Resolution is 10-bit

• 10-bit multi-channel Analog-to-Digital converter

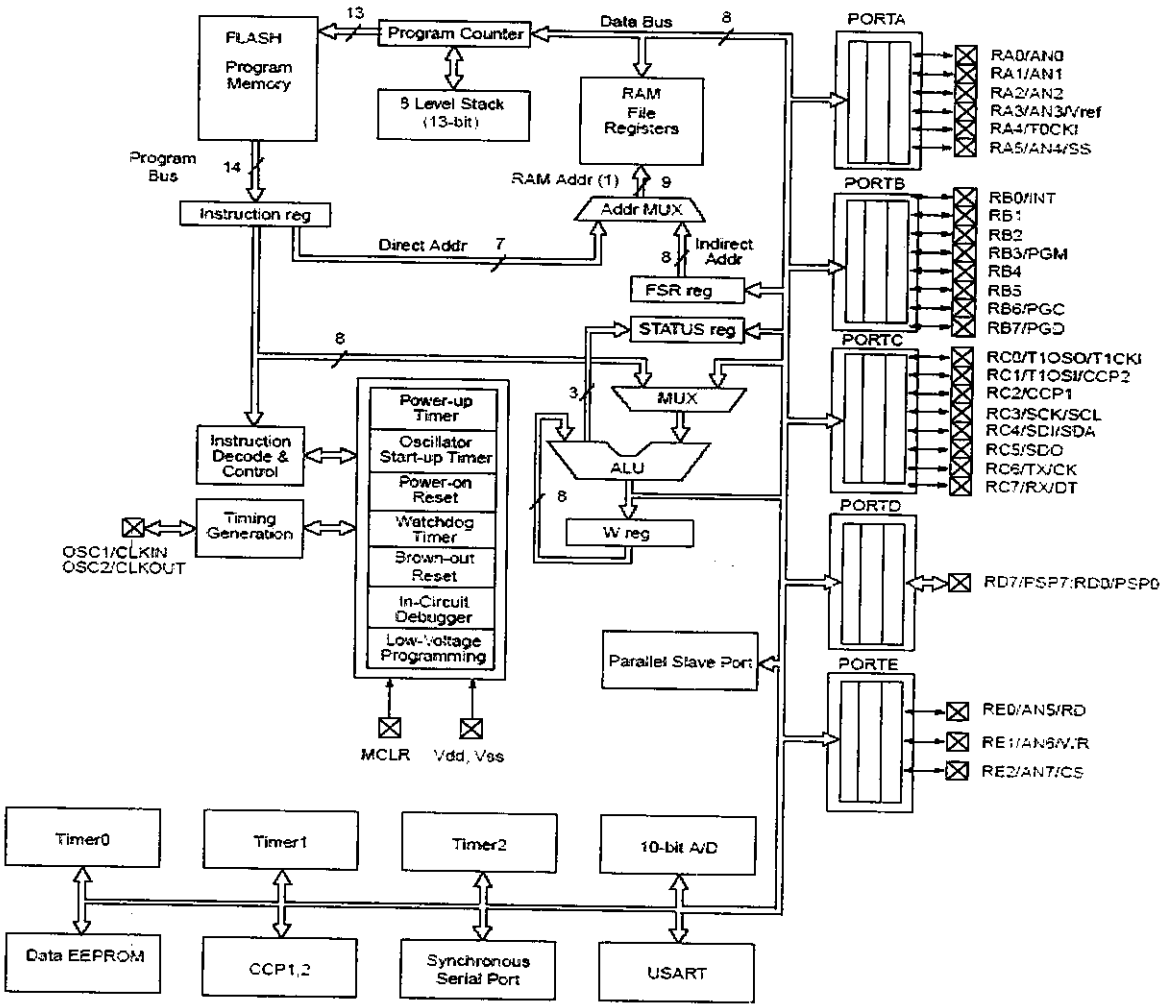
• Synchronous Serial Port (SSP) with SPI. (Master Mode) and I2C. (Master/Slave)

• USART/SCI with 9-bit address detection.

• Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls.

PIC BLOCK DIAGRAM

Device	Program Flash	Data Memory	Data EEPROM
PIC16F874	4K	192 Bytes	128 Bytes
PIC16F877	8K	368 Bytes	256 Bytes



Note 1: Higher order bits are from the STATUS register.

4.4 PIN OUT DESCRIBTION

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	I	ST/CMOS[4]	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/V_{PP}/THV	1	2	18	I/P	ST	Master clear (reset) input or programming voltage input or high voltage test mode control. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0/AN0	2	3	19	I/O	TTL	RA0 can also be analog input0
RA1/AN1	3	4	20	I/O	TTL	RA1 can also be analog input1
RA2/AN2/V_{REF-}	4	5	21	I/O	TTL	RA2 can also be analog input2 or negative analog reference voltage
RA3/AN3/V_{REF+}	5	6	22	I/O	TTL	RA3 can also be analog input3 or positive analog reference voltage
RA4/T0CKI	6	7	23	I/O	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/$\overline{SS}$/AN4	7	8	24	I/O	TTL	RA5 can also be analog input4 or the slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST[1]	RB0 can also be the external interrupt pin.
RB1	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3/PGM	36	39	11	I/O	TTL	RB3 can also be the low voltage programming input
RB4	37	41	14	I/O	TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6/PGC	39	43	16	I/O	TTL/ST[2]	Interrupt on change pin or In-Circuit Debugger pin Serial programming clock.
RB7/PGD	40	44	17	I/O	TTL/ST[2]	Interrupt on change pin or In-Circuit Debugger pin. Serial programming data.

APPENDIX 3

MOSFET DATASHEET

14A, 500V, 0.400 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17435.

Ordering Information

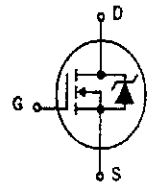
PART NUMBER	PACKAGE	BRAND
IRFP450	TO-247	IRFP450

NOTE: When ordering, use the entire part number.

Features

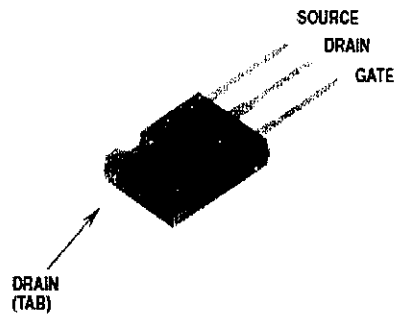
- 14A, 500V
- $r_{DS(ON)} = 0.400\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

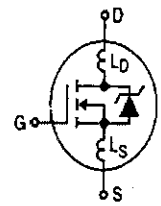
JEDEC STYLE TO-247



Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V (Figure 10)	500	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	25	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 125^oC$	-	-	250	µA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V	14	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 7.9A, V_{GS} = 10V (Figures 8, 9)	-	0.3	0.4	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50V$, I_D = 7.9A (Figure 12)	9.3	13.8	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, $I_D \approx$ 14A, V_{GS} = 10V, R_{GS} = 6.1Ω, R_L = 17.4Ω MOSFET Switching Times are Essentially Independent of Operating Temperature	-	16	27	ns
Rise Time	t_r		-	45	66	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	68	100	ns
Fall Time	t_f		-	41	60	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 10V, $I_D \approx$ 14A, V_{DS} = 0.8 x Rated BV_{DSS} $I_{G(REF)}$ = 1.5mA (Figure 14) Gate Charge is Essentially Independent of OperatingTemperature	-	82	130	nC
Gate to Source Charge	Q_{gs}		-	12	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	42	-	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 11)	-	2000	-	pF
Output Capacitance	C_{OSS}		-	400	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Internal Drain Inductance	L_D	Measured from the Contact Screw on Header Closer to Source and Gate Pins to Center of Die	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the Source Lead, 6.0mm (0.25in) from Header to Source Bonding Pad	-	12.5	-	nH
Thermal Resistance, Junction to Case	$R_{\theta JC}$		-	-	0.70	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	$^oC/W$

Modified MOSFET Symbol Showing the Internal Device Inductances



Typical Performance Curves Unless Otherwise Specified

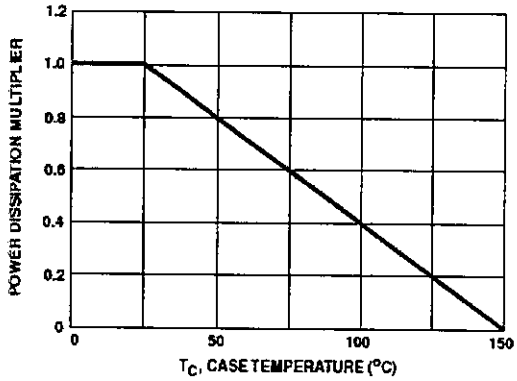


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

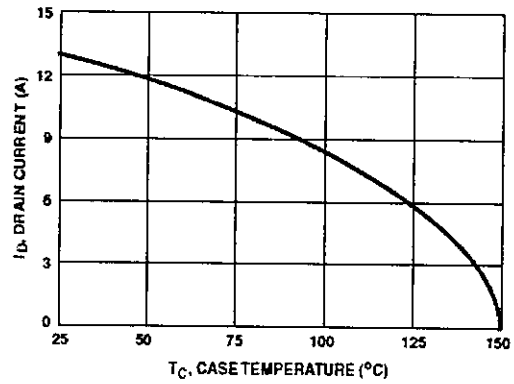


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

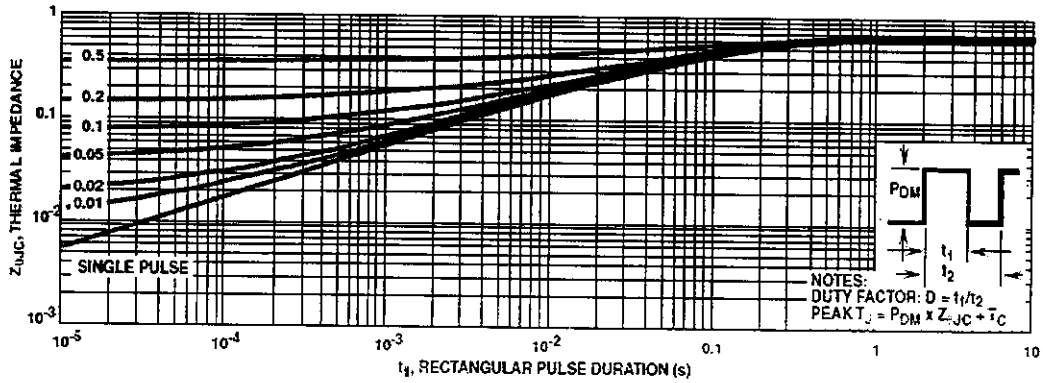


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

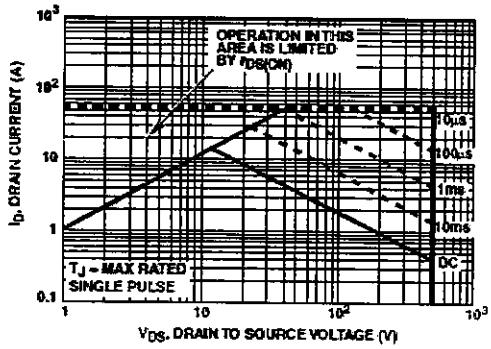


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

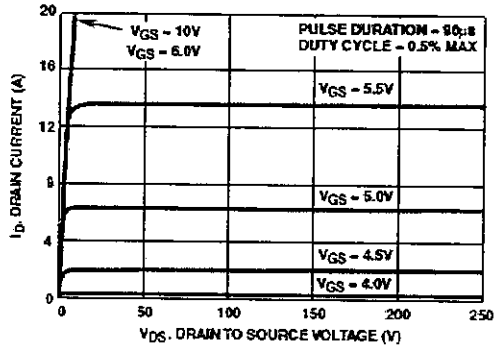


FIGURE 5. OUTPUT CHARACTERISTICS

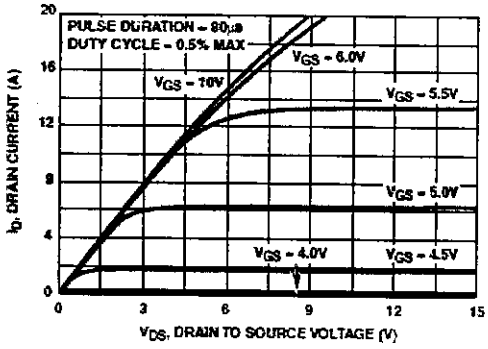


FIGURE 6. SATURATION CHARACTERISTICS

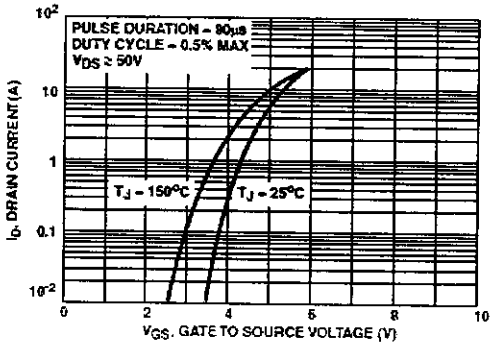
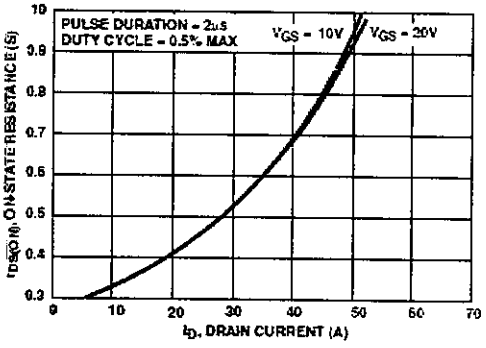
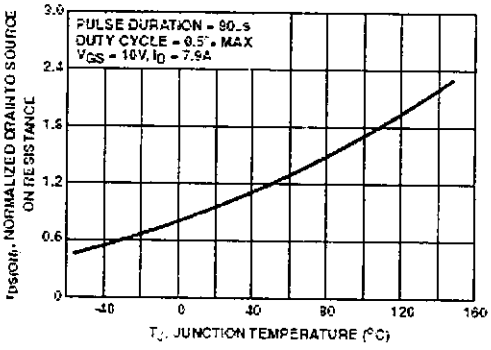


FIGURE 7. TRANSFER CHARACTERISTICS





APPENDIX 4

BUFFER DATASHEET

General Description

The CD4049UBC and CD4050BC hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. These devices feature logic level conversion using only one supply voltage (V_{DD}). The input signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers, and at V_{DD} = 5.0V, they can drive directly two DTL/TTL loads over the full operating temperature range.

Features

- Wide supply voltage range: 3.0V to 15V
- Direct drive to 2 TTL loads at 5.0V over full temperature range
- High source and sink current capability
- Special input protection permits input voltages greater than V_{DD}

Applications

- CMOS hex inverter/buffer
- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS HIGH-to-LOW logic level converter

Ordering Code:

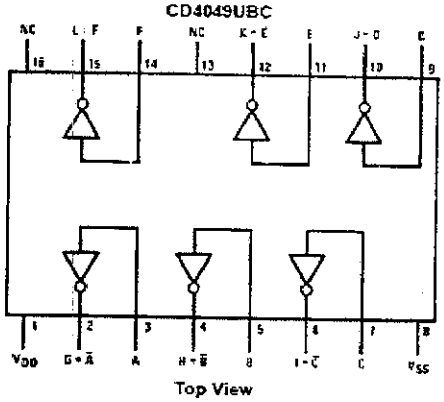
Order Number	Package Number	Package Description
CD4049UBCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4049UBCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4050BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4050BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

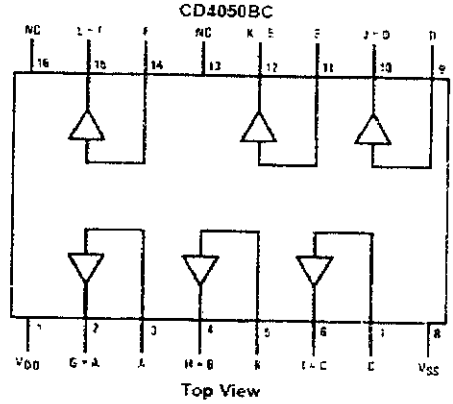
Pin Assignments for DIP

CD4049UBC



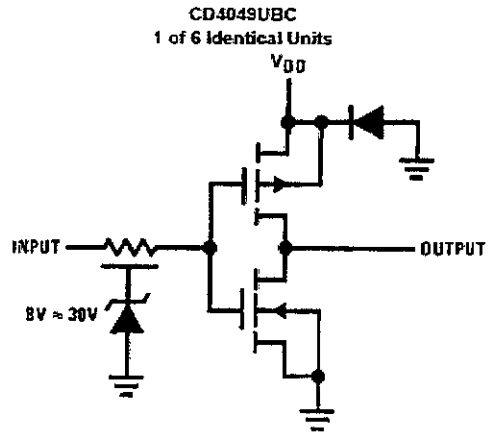
Top View

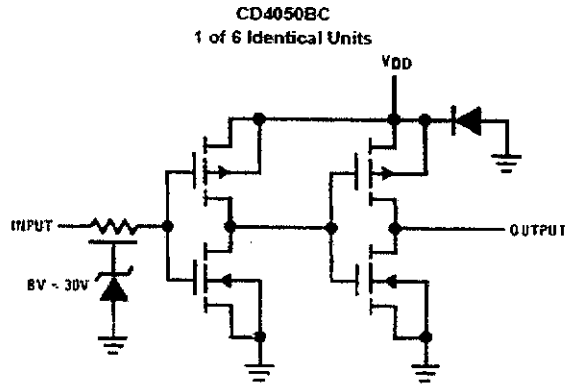
CD4050BC



Top View

Schematic Diagrams





Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{DD})	-0.5V to +18V
Input Voltage (V_{IN})	-0.5V to +18V
Voltage at Any Output Pin (V_{OUT})	-0.5V to V_{DD} + 0.5V
Storage Temperature Range (T_S)	-65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to 15V
Voltage at Any Output Pin (V_{OUT})	0 to V_{DD}
Operating Temperature Range (T_A)	
CD4049UBC, CD4050BC	-40°C to +85°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

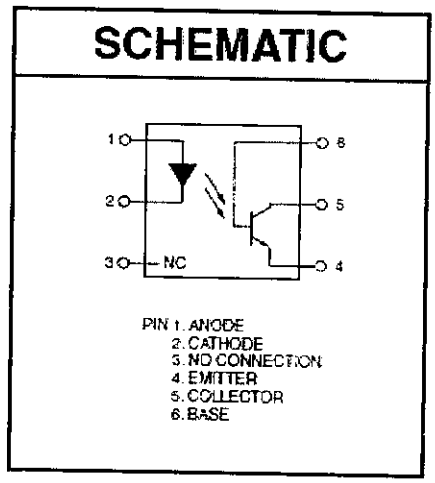
Note 2: V_{SS} = 0V unless otherwise specified.

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4		0.03	4.0		30	µA
		V_{DD} = 10V		8		0.05	8.0		60	µA
		V_{DD} = 15V		16		0.07	16.0		120	µA
V_{OL}	LOW Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V,								
		$\|I_O\|$ < 1 µA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V,								
		$\|I_O\|$ < 1 µA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	LOW Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4050BC Only)	V_{DD} = 5V, V_O = 0.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6.75	4.0		4.0	V
V_{IL}	LOW Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4049UBC Only)	V_{DD} = 5V, V_O = 4.5V		1.0		1.5	1.0		1.0	V
		V_{DD} = 10V, V_O = 9V		2.0		2.5	2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0		3.5	3.0		3.0	V
V_{IH}	HIGH Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4050BC Only)	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	8.25		11.0		V
V_{IH}	HIGH Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4049UBC Only)	V_{DD} = 5V, V_O = 0.5V	4.0		4.0	3.5		4.0		V
		V_{DD} = 10V, V_O = 1V	8.0		8.0	7.5		8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0	11.5		12.0		V
I_{OL}	LOW Level Output Current	V_{IH} = V_{DD}, V_{IL} = 0V								
	(Note 4)	V_{DD} = 5V, V_O = 0.4V	4.6		4.0	5		3.2		mA
		V_{DD} = 10V, V_O = 0.5V	9.6		8.5	12		6.9		mA
		V_{DD} = 15V, V_O = 1.5V	29		25	40		20		mA
I_{OH}	HIGH Level Output Current	V_{IH} = V_{DD}, V_{IL} = 0V								
	(Note 4)	V_{DD} = 5V, V_O = 4.6V	-1.0		-0.9	-1.6		-0.72		mA
		V_{DD} = 10V, V_O = 9.5V	-2.1		-1.9	-3.6		-1.5		mA
		V_{DD} = 15V, V_O = 13.5V	-7.1		-6.2	-12		-5		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V	-0.3		-0.3	-10^{-5}			-1.0	µA
		V_{DD} = 15V, V_{IN} = 15V	0.3		0.3	10^{-5}			1.0	µA

Note 3: V_{SS} = 0V unless otherwise specified.

APPENDIX 5

OPTOCOUPLER DATASHEET



DESCRIPTION

The general purpose optocouplers consist of a gallium arsenide infrared emitting diode driving a silicon phototransistor in a 6-pin dual in-line package.

FEATURES

- Also available in white package by specifying -M suffix, eg. 4N25-M
- UL recognized (File # E90700)
- VDE recognized (File # 94766)
  - Add option V for white package (e.g., 4N25V-M)
  - Add option 300 for black package (e.g., 4N25.300)

APPLICATIONS

- Power supply regulators
- Digital logic inputs
- Microprocessor inputs

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Value	Units
TOTAL DEVICE			
Storage Temperature	T_{STG}	-55 to +150	°C
Operating Temperature	T_{OPR}	-55 to +100	°C
Lead Solder Temperature	T_{SOL}	260 for 10 sec	°C
Total Device Power Dissipation @ T_A = 25°C	P_D	250	mW
Derate above 25°C		3.3 (non-M), 2.94 (-M)	
EMITTER			
DC/Average Forward Input Current	I_F	100 (non-M), 60 (-M)	mA
Reverse Input Voltage	V_R	6	V
Forward Current - Peak (300µs, 2% Duty Cycle)	I_F(pk)	3	A
LED Power Dissipation @ T_A = 25°C	P_D	150 (non-M), 120 (-M)	mW
Derate above 25°C		2.0 (non-M), 1.41 (-M)	mW/°C
DETECTOR			
Collector-Emitter Voltage	V_{CEO}	30	V
Collector-Base Voltage	V_{CBO}	70	V
Emitter-Collector Voltage	V_{ECO}	7	V
Detector Power Dissipation @ T_A = 25°C	P_D	150	mW
Derate above 25°C		2.0 (non-M), 1.76 (-M)	mW/°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Min	Typ*	Max	Unit
EMITTER						
Input Forward Voltage	(I_F = 10 mA)	V_F		1.18	1.50	V
Reverse Leakage Current	(V_R = 6.0 V)	I_R		0.001	10	µA
DETECTOR						
Collector-Emitter Breakdown Voltage	(I_C = 1.0 mA, I_F = 0)	BV_{CEO}	30	100		V
Collector-Base Breakdown Voltage	(I_C = 100 µA, I_F = 0)	BV_{CBO}	70	120		V
Emitter-Collector Breakdown Voltage	(I_E = 100 µA, I_F = 0)	BV_{ECO}	7	10		V
Collector-Emitter Dark Current	(V_{CE} = 10 V, I_F = 0)	I_{CEO}		1	50	nA
Collector-Base Dark Current	(V_{CB} = 10 V)	I_{CBO}			20	nA
Capacitance	(V_{CE} = 0 V, f = 1 MHz)	C_{CE}		8		pF

TRANSFER CHARACTERISTICS (T_A = 25°C Unless otherwise specified.) (Continued)

AC Characteristic	Test Conditions	Symbol	Device	Min	Typ*	Max	Unit
Turn-off Time	(I_F = 10 mA, V_{CC} = 10 V, R_L = 100Ω) (Fig.20)	T_{OFF}	4N25, 4N26, 4N27, 4N28, H11A1, H11A2, H11A3, H11A4, H11A5		2		µs
	(I_C = 2 mA, V_{CC} = 10 V, R_L = 100Ω) (Fig.20)		4N35, 4N36, 4N37		2	10	

TYPICAL PERFORMANCE CURVES

Fig. 1 LED Forward Voltage vs. Forward Current
(Black Package)

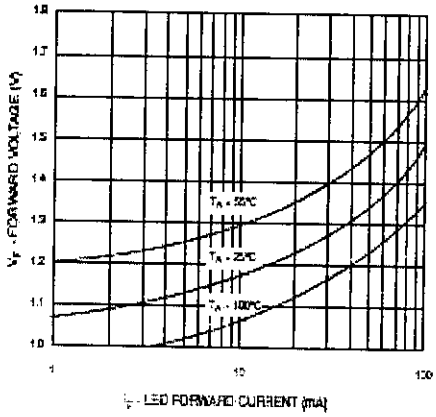


Fig. 2 LED Forward Voltage vs. Forward Current
(White Package)

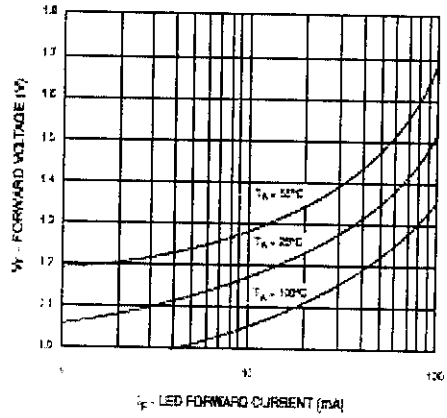


Fig.3 Normalized CTR vs. Forward Current
(Black Package)

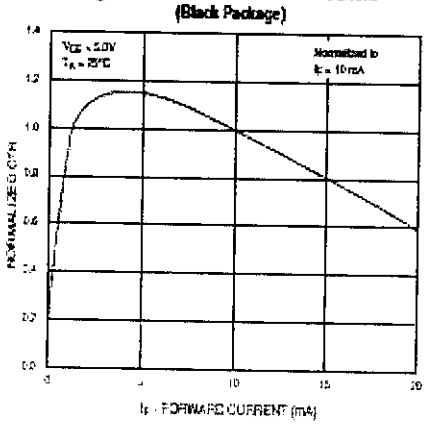


Fig.4 Normalized CTR vs. Forward Current
(White Package)

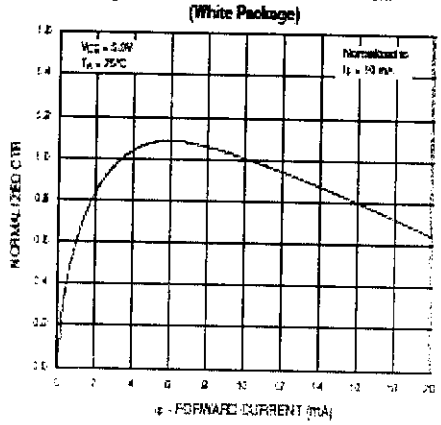


Fig. 5 Normalized CTR vs. Ambient Temperature
(Black Package)

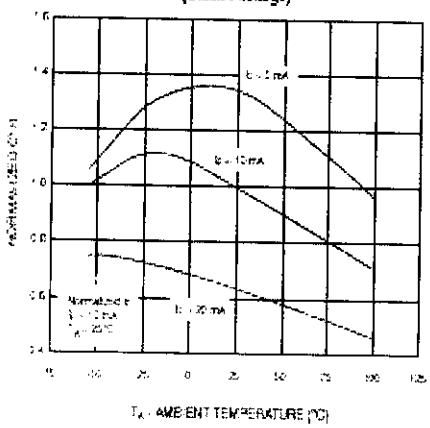
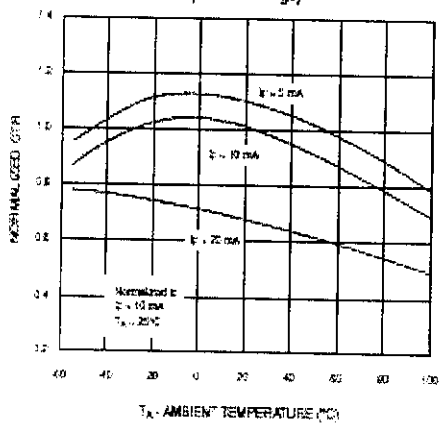


Fig. 6 Normalized CTR vs. Ambient Temperature
(White Package)



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