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**DESIGN AND IMPLEMENTATION  
OF TEMPERATURE CONTROLLER  
FOR  
FURNACE USING  
INDIRECT MATRIX CONVERTER**

P-3428  
**A Project Report**

*Submitted by*

Bindhiya B	-	0710105011
DeviBaala T.N	-	0710105016
Karthick M	-	0710105026
Vishnu Sivaram	-	0710105060

*in partial fulfillment for the award of the degree  
of*

**Bachelor of Engineering  
in  
Electrical & Electronics Engineering**

**DEPARTMENT OF ELECTRICAL AND ELECTRONICS  
ENGINEERING**

**KUMARAGURU COLLEGE OF TECHNOLOGY**

(An Autonomous Institution Affiliated to Anna University, Coimbatore.)

**COIMBATORE – 641 049**

**ANNA UNIVERSITY: COIMBATORE 641013**

**APRIL 2011**

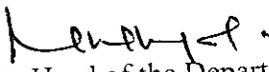
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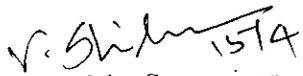
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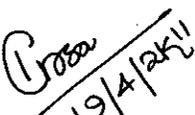
Bindhiya B - Register No. 0710105011  
DeviBaala T.N - Register No. 0710105016  
Karthick M - Register No. 0710105026  
Vishnu Sivaram - Register No. 0710105060

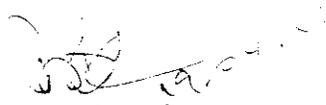
who carried out the project work under my supervision.

  
Signature of the Head of the Department  
DR. RANI THOTTUNGIAL  
HOD

  
Signature of the Supervisor  
MRS. SHARMILA DEVE, ASST PROF.

Certified that the candidate with university Register No. \_\_\_\_\_ was examined in  
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External Examiner

## **ABSTRACT**

The project aims at helping the industries where the necessity of maintaining constant temperature is required. Temperature control is very important in many industries which uses furnace. In this project, the temperature of a heating element of an iron box is maintained constant by using a matrix converter. Here the required temperature is set and a microcontroller is used to produce suitable pulses whose frequency variation varies the temperature. The microcontroller is used to compare the temperature of the heating element with the set temperature and maintain it at set temperature.

## ACKNOWLEDGEMENT

I humbly submit all the glory and thanks to the almighty for showering the blessings and giving the necessary wisdom for accomplishing this project.

I would like to express my deep sense of gratitude and profound thanks to our guide **Mrs. Sharmila Deve**, Assistant Professor (SRG), Electrical and Electronics Engineering Department, for her valuable guidance, support, constant encouragement and co-operation rendered throughout the project.

I take immense pleasure in thanking **Dr.Rani Thottungal, HOD** Department of Electrical and Electronics Engineering, Kumaraguru College of Technology, for her constant encouragement and support.

I would like to express my heartfelt thanks to our beloved Principal **Dr.S.Ramachandran**, for his support.

I am also thankful to all my **teaching and technical supporting staff** of Electrical and Electronics Engineering department, for their kind help and encouragement.

Finally, I thank my parents for giving me the moral support and abundant blessings in all of my activities and to my dear friends who made me endure my difficult times with their unfailing humor and warm wishes.

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## LIST OF ABBREVIATIONS

01	AC	Alternating Current
02	DC	Direct Current
03	PWM	Pulse Width Modulation
04	PIC	Programmable Interface Control
05	MOSFET	Metal Oxide Semiconductor Field Effect Transistor
06	MC	Micro Controller
07	IC	Integrated Circuit
08	PCB	Printed Circuit Board
09	CMOS	Complementary Metal Oxide Semiconductor

**CHAPTER-1**  
**INTRODUCTION**

## **1.1 INTRODUCTION:**

Temperature control is an inevitable process in many industries. This project aims at maintaining the temperature constant. Conventionally the temperature is controlled using separate rectifier and inverter circuit which is subjected to many disadvantages. To overcome these disadvantages, indirect matrix converter is used which provides better efficient output.

The AC/AC converters are commonly classified as direct converters and indirect converters. An Indirect converter consists of two converter stages and an energy storage element, which converts input ac to dc and then reconverts dc back to ac output with variable amplitude and frequency. The energy storage element can be either a capacitor or an inductor. However, the energy storage element is not needed in a direct converter. In general, direct converters can be classified into three topologies namely ac voltage controller, cyclo-converter and matrix converter.

Matrix converter is the most versatile converter without any limit on the output frequency and amplitude. It replaces the multiple conversion stages and the intermediate energy storage element by a single power conversion stage. The usage of indirect matrix converter also reduces the switching losses and protects the system from experiencing over voltages under reverse power conditions. The output obtained thus has a better power factor. The size is reduced considerably because of the absence of the dc link capacitor.

## **1.2 NEED FOR THE PROJECT:**

Matrix converter based drive topology has some interesting characteristics of its own. It has intrinsic power regeneration capabilities. It can have a smaller mounting place than conventional AC-AC converters because neither braking resistor nor large electrolytic capacitor is required. It has low total harmonics of input current with high efficiency and power factor. Since the matrix converter drive has no large DC-bus capacitor (usually electrolytic) it has a longer lifetime and is more reliable. Moreover provides direct ac-ac conversion thus eliminating the need for reactive energy storage elements. This system provides independent control of the output voltage, magnitude, frequency and phase angle and operation at lagging, unity or leading power factor. As a result much higher efficiency and performance can be achieved by these drives with reduced harmonics.

Pulse Width Modulated (PWM) signals applied to the gates of the power transistors. PWM signals are pulse trains with fixed frequency and magnitude and variable pulse width. When a PWM signal is applied to the gate of a power transistor, it causes the output voltage of the inverter to vary according to its turn on time. The inverter converts DC power to AC power at the required frequency and amplitude. The inverter consists of six power MOSFETs that turn on and off in a desired pattern to produce three phase AC output voltage. The control IC is programmed and implemented in MicroController to generate PWM gating pulses for the MOSFETs.

In this project, an embedded controller for inverter using microcontroller is developed. The output voltage of the inverter is varied by varying the PWM switching frequency of the gating pulses given to the power transistors (MOSFETs) of the inverter. The PWM switching frequency can be varied to a maximum of 10kHz. High switching frequency is achieved which improves the performance by reducing total harmonics distortion and switching loss.

### **1.3 OBJECTIVE:**

The main objective of this project is to design and implement a matrix converter in order to maintain the furnace temperature constant by maintaining the frequency of the supply constant.

### **1.4 ADVANTAGES OVER THE EXISTING SYSTEM:**

The rapid development in high-performance, low-cost microcontrollers has encouraged research on digital PWM control. This control scheme has the advantages of simple circuitry, software control, and flexibility in adaptation to various applications.

- ▶ Reduced switching losses.
- ▶ Protect the system from experiencing over voltages under reverse power conditions.
- ▶ The matrix converter shows better efficiencies due to lower switching losses.
- ▶ Power factor improvement.
- ▶ No use of dc link capacitor

**CHAPTER 2**  
**INDIRECT MATRIX CONVERTER**  
**AN OVERVIEW**

## 2.1 INDIRECT MATRIX CONVERTER:

### 2.1.1 BASICS:

An **AC/AC converter** converts an AC waveform such as the mains supply, to another AC waveform, where the output voltage and frequency can be set arbitrarily.

AC/AC converters can be categorized into

- Converters with a DC-link.
- Cycloconverters
- Hybrid Matrix Converters.
- Matrix Converters.

For such AC-AC conversion today typically converter systems with a voltage or current DC-link are employed. For the voltage DC-link, the main coupling could be implemented by a diode bridge. The disadvantages of this solution are the relatively high main distortion and high reactive power requirements (especially during inverter operation).

An AC/AC converter with approximately sinusoidal input currents and bidirectional power flow can be realized by coupling a PWM rectifier and a PWM inverter to the DC-link. The DC-link quantity is then impressed by an energy storage element that is common to both stages, which is a capacitor  $C$  for the voltage DC-link or an inductor  $L$  for the current DC-link. The PWM rectifier is controlled in a way that a sinusoidal main current is drawn, which is in phase or anti-phase (for energy feedback) with the corresponding mains phase voltage.

Due to the DC-link storage element, there is the advantage that both converter stages are to a large extent decoupled for control purposes. Furthermore, a constant, mains independent input quantity exists for the PWM inverter stage, which results in high utilization of the converter's power capability. On the other hand, the DC-link energy storage element has a relatively large physical volume, and when electrolytic capacitors are used, in the case of a voltage DC-link, there is potentially a reduced system lifetime.

In order to achieve higher power density and reliability, it makes sense to consider Matrix Converters that achieve three-phase AC/AC conversion without any intermediate energy storage

element. Conventional Direct Matrix Converters perform voltage and current conversion in single stage.

The matrix converter has several advantages over traditional rectifier-inverter type power frequency converters. It provides sinusoidal input and output waveforms, with minimal higher order harmonics and no sub harmonics; it has inherent bi-directional energy flow capability; the input power factor can be fully controlled. Last but not the least, it has minimal energy storage requirements, which allows to get rid of bulky and lifetime- limited energy-storing capacitors. But the matrix converter has also some disadvantages. First of all, it has a maximum input/output voltage transfer ratio limited to 87 % for sinusoidal input and output waveforms. It requires more semiconductor devices than a conventional AC-AC indirect power frequency converter, since no monolithic bi-directional switches exist and consequently discrete unidirectional devices, variously arranged, have to be used for each bi-directional switch. Finally, it is particularly sensitive to the disturbances of the input voltage system.

### **2.1.2 NEED FOR MATRIX CONVERTER**

Recently, matrix converter has received considerable interest as a viable alternative to the conventional back-to-back PWM converter in the ac/ac conversion. This direct ac/ac converter provides some attractive characteristics such as: inherent four-quadrant operation; absence of bulky dc-link electrolytic capacitors; clean input power characteristics and increased power density. However, industrial application of the converter is still limited because of some practical issues such as common mode voltage effects, high susceptibility to input power disturbances and low voltage transfer ratio.

The matrix converter is the most general converter-type in the family of AC-AC direct converters. On one hand, the matrix converter fulfills the requirements to provide a sinusoidal voltage at the load side and, on the other hand, it is possible to adjust the unity power factor on the mains side under certain conditions. Since there is no DC link as in common converters, the matrix converter can be built as a full-silicon structure. Using a sufficiently high pulse frequency, the output voltage and the input current both are shaped sinusoidally. The converter consists of four bi-directional switches, arranged as two sets of two so that any of the input phases can be connected to any of the output line. The switches are then controlled in such a way that the average output voltages are sinusoids at the required frequency and magnitude.

**2.1.3 ADVANTAGES OF MATRIX CONVERTER**

- Multilevel conversion is possible, even in the basic version. This enables improvement of the low-wind efficiency of the converter, without sacrificing performance at rated power.
- The converter can both step up and step down the voltage magnitude.
- Switch commutation is simple.
- Simple bus bar structures.
- High quality waveforms.

**2.1.4 COMPARISON OF CONVENTIONAL CONVERTERS WITH PROPOSED NEW MATRIX CONVERTER**

Property/Parameters	Conventional Converter	Proposed Matrix Converter
Voltage conversion Ratio $V_{out}/V_{in}$	$V_{out} \leq 0.866 V_{in}$	$0 \leq V_{out} \leq \infty$
Switching commutation	Coordination of 4-quadrant switches	Simple transistor and freewheeling of diodes
Bus bar Structure	Complex	Modular and Simple
Multilevel operation	Not possible	Possible
Utility side Filter Elements	AC Capacitors	Inductive

Table 2.1.4 Comparison of conventional converters with proposed matrix converters

# 2.2 PULSE WIDTH MODULATION

## 2.2.1 INTRODUCTION

Pulse Width Modulation, is a modulation technique that generates variable-width pulses to materialize the amplitude of an analog input signal. It is a method of transmitting information on a series of pulses. The data that is being transmitted is encoded on the width of these pulses to control the amount of power being sent to a load.

Using digital pulses we can create some analog value other than just 'high' and 'low' signal levels. Many digital systems are powered by a 5-Volt power supply, so by filtering a signal that has a 50% duty cycle we get an average voltage of 2.5 Volts. Other duty cycles produce any voltage in the range of 0 to 100% of the raised voltage, depending upon the PWM resolution. The duty cycle is defined as the percentage of digital 'high' to digital 'low' signals present during a PWM period. The PWM resolution is defined as the maximum number of pulses that can pack into a PWM period. The PWM period is an arbitrarily time period in which PWM takes place. It is chosen to give best results for our particular use. The figure 3.8 shows the PWM pulse generated by comparing the saw tooth carrier and a reference signal.

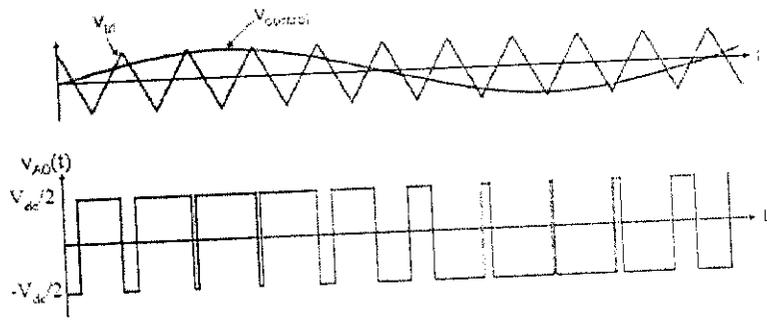


Fig 2.1 Pulse Width Modulation

## 2.2.2 TYPES OF PULSE WIDTH MODULATION:

There are many ways of generating a PWM output such as

- Single pulse width modulation
- Multiple pulse width modulation
- Sinusoidal pulse width modulation
- Space vector pulse width modulation
- Modified pulse width modulation

### Multiple PWM

The harmonic content can be reduced by using several pulses in each half-cycle of the output voltage. It is generated by comparing a linear reference signal with a triangular carrier wave. The frequency of reference signal sets the output frequency and the frequency of the carrier determines the number of pulses per half cycle. By varying the 'on time' of the pulses the output voltage can be controlled. This is also known as UNIFORM pulse width modulation.

### Sinusoidal PWM

The simplest analog form of generating fixed frequency PWM is by comparison with a linear slope waveform such as a sawtooth. The output signal goes high when the sine wave is higher than the sawtooth. This is implemented using a comparator whose output voltage goes to logic HIGH when the input is greater than the other.

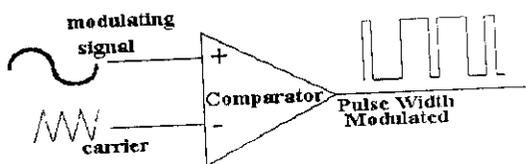


Fig. 2.2 Sine Saw tooth PWM

### Space vector PWM

This PWM technique approximates the reference voltage  $V_{ref}$  by a combination of the eight switching patterns ( $V_0$  to  $V_7$ ). The sinusoidal voltage is treated as a constant amplitude vector rotating at constant frequency. The vectors ( $V_1$  to  $V_6$ ) divide the plane into six sectors (each sector: 60 degrees).  $V_{ref}$  is generated by two adjacent non-zero vectors and two zero vectors.  $S_1$ - $S_6$  are the six power transistors of the inverter. The transistors are switched on and off in the specific pattern to produce the required output.

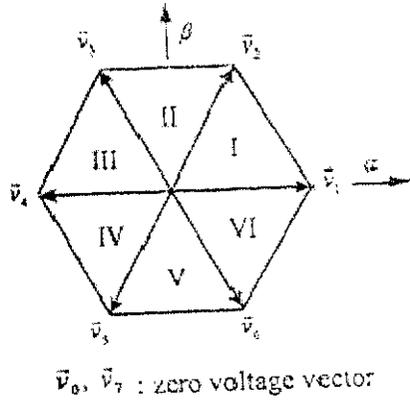


Fig 2.3 Basic switching vector

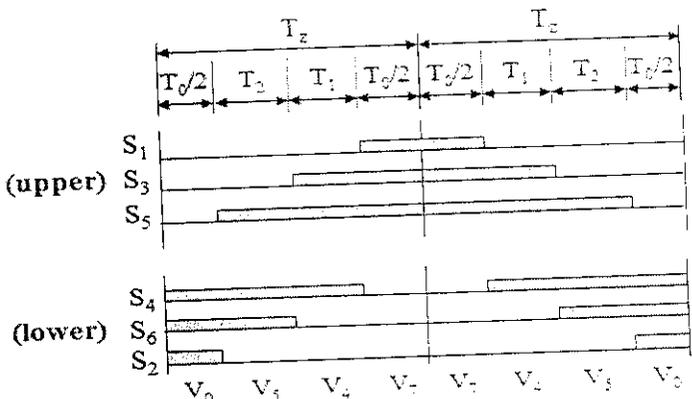


Fig 2.4 Switching pattern for sector-1



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### 2.2.3 ADVANTAGES OF PWM

PWM technique has the following advantages

- Suppresses lower order voltage and current harmonics
- Improved power factor.
- Include a simple drive circuit
- Good start-up characteristics and minimal heat dissipation in the pass transistor
- The signal remains digital all the way from the processor to the controlled system hence no digital-to-analog conversion is needed

### 2.2.4 PWM CONTROLLER VS. RESISTIVE CONTROLLER

At a 50 percent level, the PWM will use about 50 percent of full power, almost all of which is transferred to the load. A resistive controller at 50 percent load power would consume about 71 percent of full power; 50 percent of the power goes to the load, and the other 21 percent is wasted heating the resistors. It takes a constant trickle of power to operate, so the efficiency improves with higher power loads.

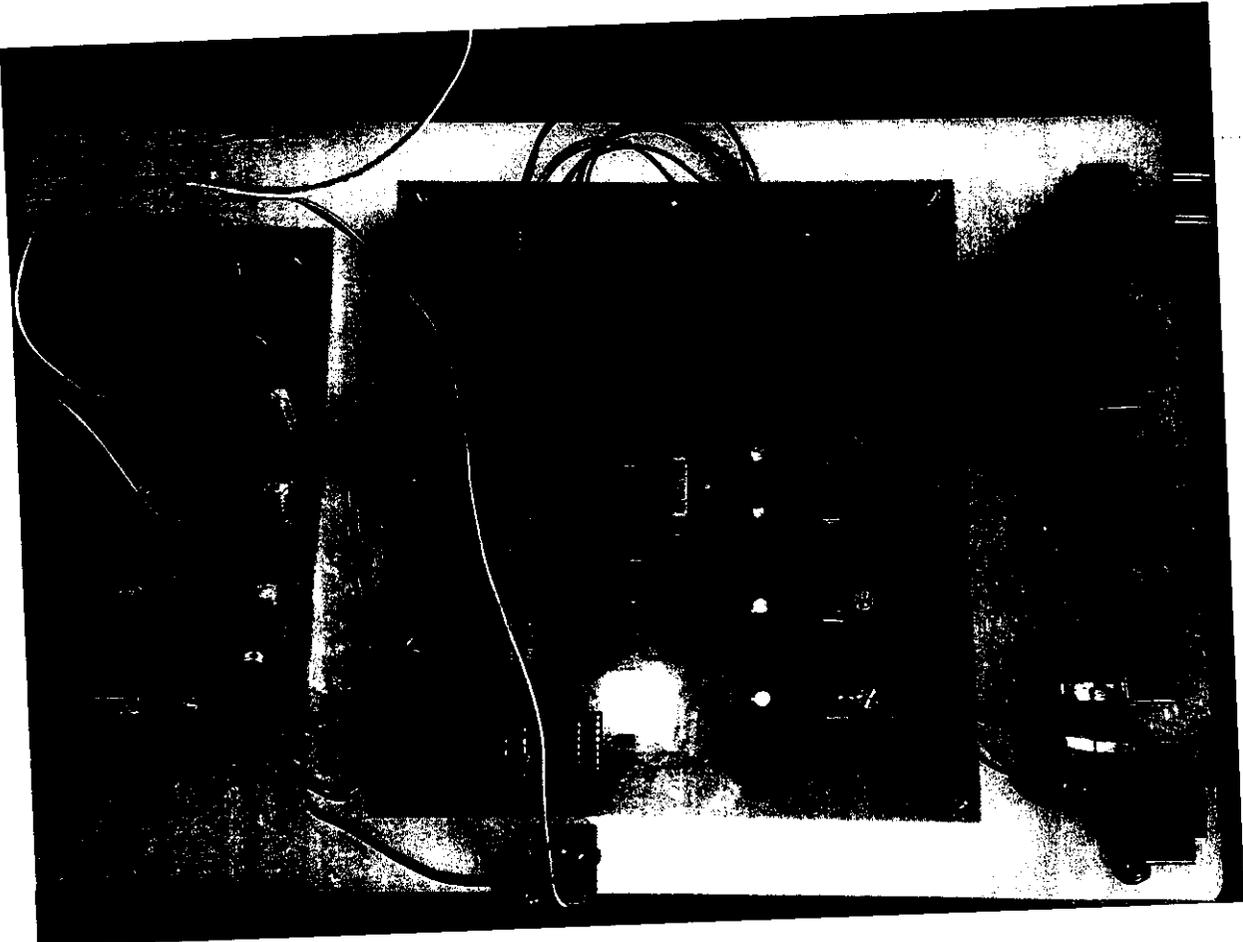
The pulses are at the full supply voltage and will produce more torque in a motor by being able to overcome the internal motor resistances more easily. A resistive speed control will present a reduced voltage to the load, which can cause stalling in motor applications. Finally, in a PWM circuit, common small potentiometers may be used to control a wide variety of loads, whereas large and expensive high power variable resistors are needed for resistive controllers.

Analog control scheme possesses the advantage of fast dynamic response, but suffers the disadvantages of complex circuitry, limited functions, and difficulty in circuit modification. The rapid development in high-performance low-cost microcontroller processors has encouraged research on digital PWM control. This control scheme has the advantages of simple circuitry, software control, and flexibility in adaptation to various applications.

CHAPTER 3  
**HARDWARE DESCRIPTION**

### 3.1 HARDWARE DESCRIPTION:

This chapter describes the hardware model of the furnace temperature controller. Based on the previous methods and considering their disadvantages the following model is proposed. The figure below shows the complete hardware of the prototype developed.



**Fig 3.1 (a) Hardware implementation of the circuit (module 1)**



**Fig 3.1 (b) Hardware implementation of the circuit (module 2)**

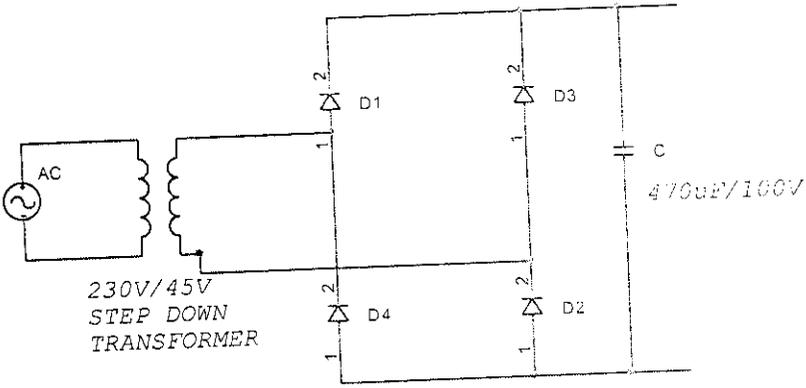


### 3.3 DESCRIPTION OF THE BLOCK DIAGRAM:

The above figure represents the block diagram of the proposed model. The diagram shows that the circuit is closed type. The single phase, 230V, AC supply is given to the diode rectifier which provides the required DC supply to the voltage source inverter (VSI). The VSI is driven by the PWM pulse produced by the microcontroller. The PWM pulses are varied based on the difference between the actual and the set temperature. The thermistor provides the actual temperature to the controller and the keypad is used to set the required temperature. So the VSI is driven so as to bring the actual temperature equal to the set temperature.

#### 3.3.1 Input Source

The electronic circuits work under proper supply voltages. The input source given to the circuit should be DC. The figure given below represents the input source given to the circuit.



**Fig3.3 Representation of Input Source**

The transformer is used to step down the voltage. The transformer used is of 230V/45V step down transformer. The bridge circuit which consists of four diodes is available as a module. The module number used here is 68424 International Rectifier (IR). This module is used for rectification purpose. The capacitor is used to filtering the unwanted signals. Thus a dc output is obtained. The output obtained is given to the inverter circuit.

### 3.3.2 Power Supply circuit for triggering circuit

All electronic circuits works only in low DC voltage, so an appropriate voltage supply is provided for their proper functioning. Therefore, the power supply circuit for triggering circuit unit consists of transformer, rectifier, filter and regulator. AC voltage of typically 230V is connected to a transformer which steps down to the level to desired ac voltage. A diode rectifier that provides the full wave rectified voltage that is initially filtered by a simple capacitor filter to produce dc voltage is provided. The resulting dc voltage usually has some ripple or ac voltage variation . A regulator circuit can use this dc input to provide dc voltage that not only has much less ripple voltage but also remains the same dc value even when the dc voltage varies somewhat, or the load connected to the output dc voltages changes. In our project there are two power supply circuits. Now for microcontroller, a regulator of IC LM 7805 is used .Here the output voltage is regulated to be 5V and is given as supply to the PIC microcontroller.

In addition to this four other supplies are used. Here 12V is given as supply by using IC LM 7812 regulator which will be discussed later in this report. The general block diagram and the circuit designed for 12V power supply is shown below.

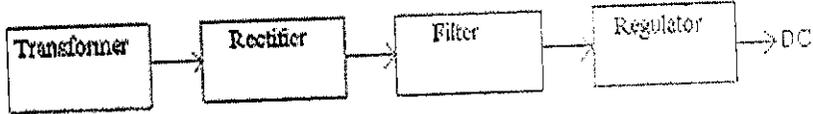


Fig3.4 (a) Block diagram of Power Supply circuit.

# POWER SUPPLY CIRCUIT:

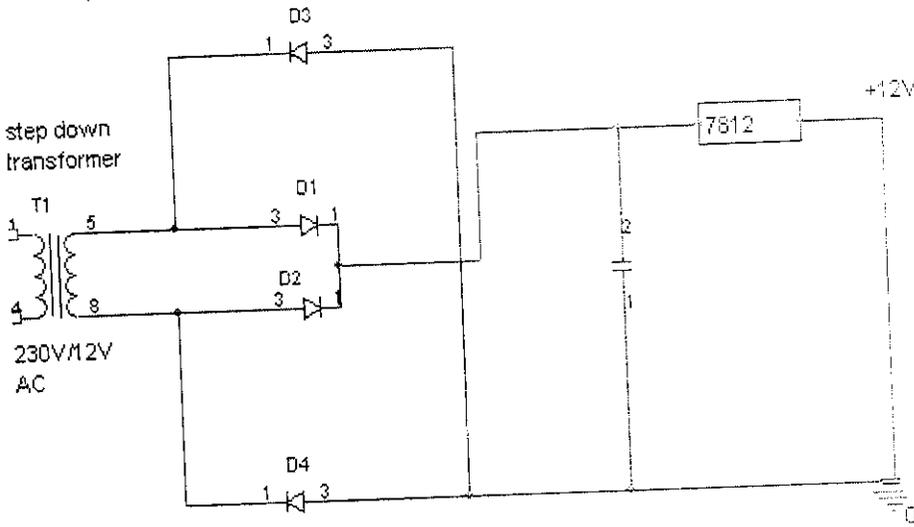


Fig3.4 (b) Power Supply Circuit.

## Transformer

A transformer is a static apparatus in which electric power in one circuit is transformed into electric power of same frequency into another circuit. It can raise or lower the voltage in the circuit, but with a corresponding decrease or increase in current. It works on the principle of mutual induction. Hence a step down transformer is used to provide the necessary supply for the electronic circuits. Here a step down transformer of 230V/12V is used to step down the voltage.

## Rectifier

A dc voltage level obtained from a sinusoidal input can be improved fully using a process called full wave rectification. Therefore the full wave rectification is obtained using Full-wave bridge rectifier. From the basic bridge configuration, it can be observed that during the positive half-cycle of the input voltage, the power is supplied to the load through diodes D1

and D2. During the negative cycle, diodes D3 and D4 conducts. In the bridge rectifier the diodes may be of variable types like 1N4001, 1N4003, 1N4004, 1N4005, 1N4007 etc... can be used. Here the diode used is 1N4007, because it can withstand voltages upto 1000V.

### **Filters**

In order to obtain a dc voltage of 0 Hz, a low pass filter is used. So that a capacitive filter circuit is used where a capacitor is connected at the rectifier output and a dc voltage is obtained across it. The filtered waveform is essentially a dc voltage with negligible ripples and it is ultimately fed to the load.

### **Regulators**

The output voltage from the capacitor is more filtered and finally regulated. The voltage regulator is a device, which maintains the output voltage constant irrespective of the change in supply variations, load variations and temperature changes. In our project we make use of two voltage regulators. Here fixed voltage regulators namely LM7805 and LM7812 are used. The IC LM7805 is a +5V regulator which is used for microcontroller and IC LM7812 is used for the MOSFETs at the driver side.

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point these regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators devices can be used with external components to obtain adjustable voltages and currents. The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided.

Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sink provided, the thermal shutdown circuit takes over preventing the IC from overheating. Considerable effort was expended to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input by-

passing is needed only if the regulator is located far from the filter capacitor of the power supply. For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

Output current in excess of 1A is obtained and it also provides internal thermal overload protection. No external components are required. Available in the aluminum TO-3 package.

**Circuit diagram of LM78XX:**

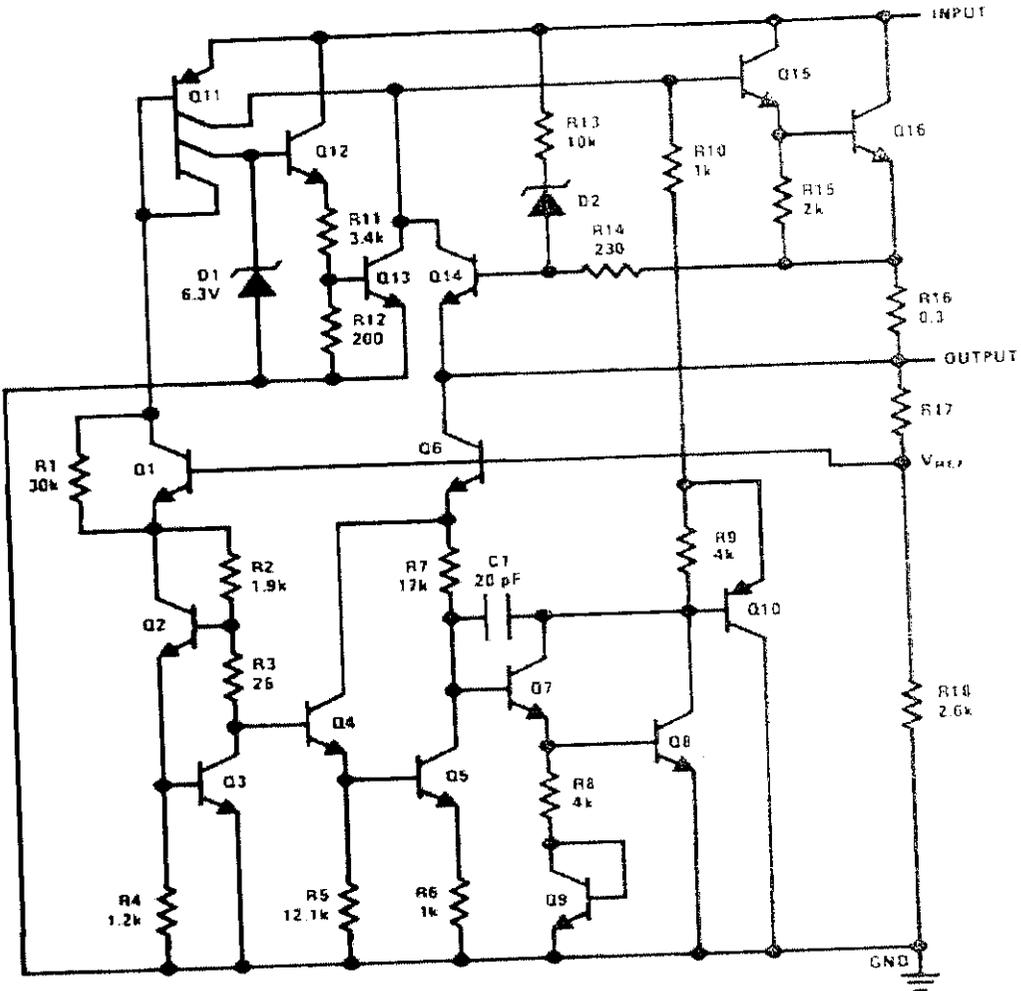
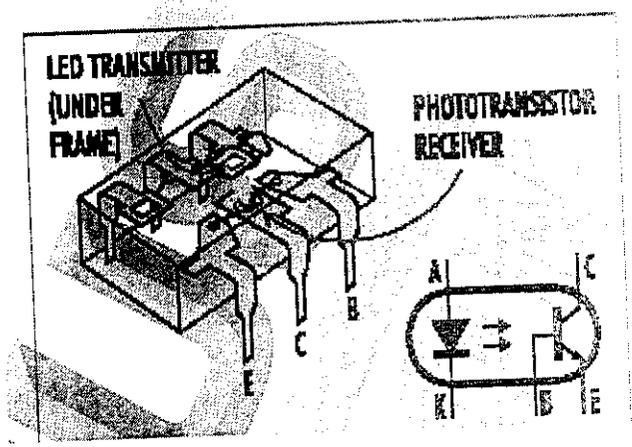


Fig 3.5 Circuit diagram of LM78XX

### 3.3.3 Optocoupler

Optocoupler is also termed as optoisolator. They are essentially a combination of two distinct devices: an optical transmitter, typically a gallium arsenide LED (Light-Emitting Diode) and an optical receiver such as a phototransistor or light-triggered diac or a resistor that changes resistance with variations in light intensity or other device that conducts differently in the presence of light. These devices are used to isolate the control voltage from the controlled circuit. Optocouplers typically come in a small 6-pin or 8-pin IC package. The two are separated by a transparent barrier which blocks any electrical current flow between the two, but does allow the passage of light.



**Fig 3.6 Construction of a typical optocoupler and the circuit symbol**

Usually the electrical connections to the LED section are brought out to the pins on one side of the package and those for the phototransistor or diac to the other side, to physically separate them as much as possible. This usually allows optocouplers to withstand voltages of anywhere between 500V and 7500V between input and output. Optocouplers are essentially digital or switching devices, so they are best for transferring either on-off control signals or digital data. Analog signals can be transferred by means of frequency or pulse-width modulation. Thus the triggering pulses are given to the inverter circuit.

The optocoupler used in our circuit is SFH615. This features a high current transfer ratio, low coupling capacitance and high isolation test voltage. They employ a Gallium Arsenide LED

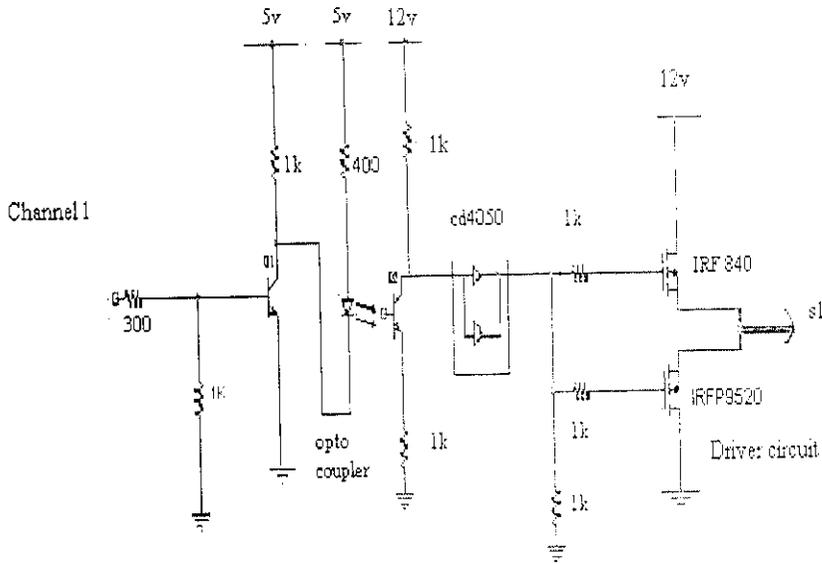
as emitter which is optically coupled with a silicon planar photo transistor as detector. The components are incorporated in a plastic plug-in DIP-4 package. The coupling devices are designed for signal transmission between two electrically isolated circuits. The potential difference between the circuits to be coupled is not allowed to exceed the maximum permissible reference voltages. The couplers are end stackable in a 2.54 mm and are considered as successor types for the couplers in metal case. Multi couplers can thus easily be implemented and conventional multicouplers can be easily replaced.

#### **FEATURES:**

- Isolation test voltage is 2800 Volts.
- High current transfer ratio
  - At 10 mA : 40-320 %
  - At 1 mA : 60 %.
- Fast switching times
- Stable temperature
- Low saturation voltage
- High collector emitter voltage of 70V

#### **3.3.4 Driver Circuit:**

The driver circuit forms the most important part of the hardware unit because it acts as the backbone of the inverter. It gives the triggering pulses to the switches in the proper sequence. The signal after being electrically isolated is given to the driver circuit. The diagram given below (fig 3.7) represents the driver unit.



**Fig 3.7 Driver circuit for a single channel**

The above figure shows a single channel of the driver circuit. Similarly there are five other channels and each channel is used to drive the inverter circuit. The digital signal from the PIC 16F877A comes to this driver circuit. It forms the main part of the hardware developed. The driver unit contains the following important units.

- A. Capacitor
- B. Supply
- C. Resistor
- D. Buffer
- E. MOSFETs

The signal from the mc reaches the optocoupler where it is electrically isolated from the rest of the circuit to prevent damage to the microcontroller in case of improper or back firing. The 330 ohm resistor is used for current limiting(biasing).

When the signal is electrically isolated, it is passed through the buffer cd 4050. This buffer is used to increase the signal strength and then it is sent to the darlington pair. The resistor and capacitor are used for pull down.

### Buffer

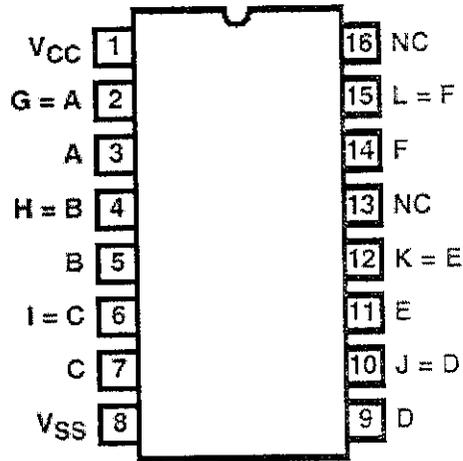


Fig 3.8 Pin diagram of CD4050

### Schematic Diagram of CD4050B:

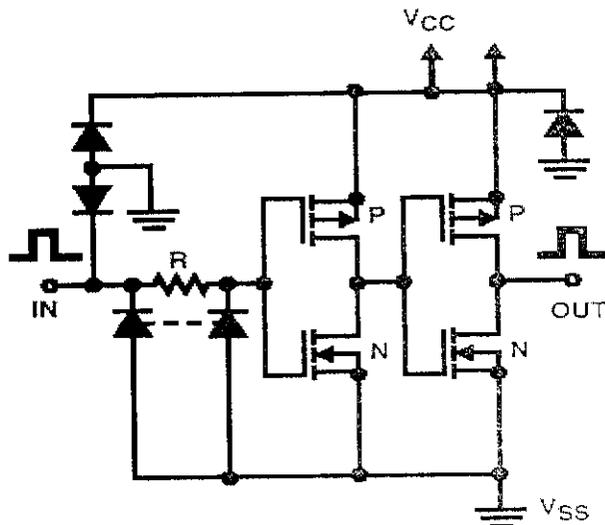


Fig 3.9 Schematic Diagram of CD4050B

CD4050B device is an inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage ( $V_{cc}$ ). The input-signal high level ( $V_{IH}$ ) can exceed the  $V_{cc}$  supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL / TTL converters and can drive directly two DTL/TTL loads. ( $V_{cc} = 5V$ ,  $V_{ol} = 0.4V$ , and  $I_{ol} = 3.3mA$ ). The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because CD4050B requires only one power supply, they are preferred over the CD4010B and should be used in place of CD4010B in all inverters, current drivers, or logic-level conversion applications. In these applications the CD4049UB and CD4050B is pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation.

## MOSFETs

The signal from the buffer amplifier is given to the MOSFET circuit. On top is the N channel IRF 840 and P channel IRFP 9520. When the input is 0V, P channel MOSFET conducts which is connected to ground. So there is no output. When the input is 1V, then the N channel mosfet conducts and gives an output voltage of 12V, which in turn is used to drive the inverter. The output obtained by this manner is sharp.

### IRF 840

Symbol of IRF 840.

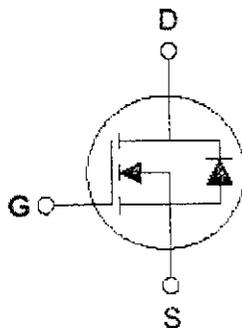


Fig 3.10 Symbol of IRF 840

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, CMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies, power factor correction and electronic lamp ballasts based on half bridge.

**Features:**

- 8.0A, 500V,  $R_{ds(on)} = 0.8$ ;  $V_{GS} = 10$  V.
- Fast switching.
- 100% avalanche tested.
- Improved  $dV/dt$  capability.

**IRF9520**

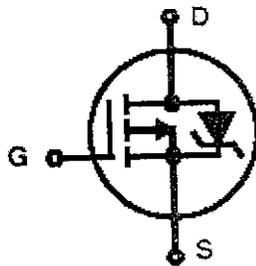


Fig 3.11 Symbol of IRF9520

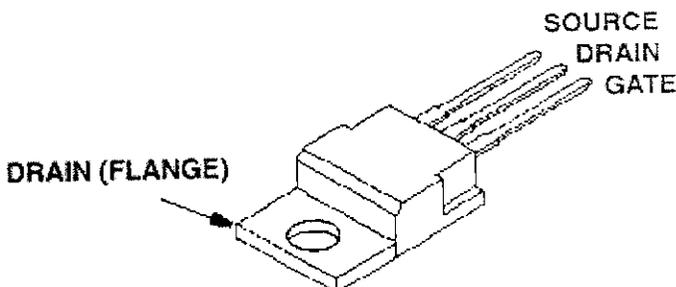


Fig 3.12 IRF9520 packaging.

This advanced power MOSFET is designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are P-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

**Features:**

- $R_{ds(ON)} = 0.600$  ohm.
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

**3.3.5 Inverter Unit:**

The inverter circuit involves six switches. It consists of a single DC source. The figure given below represents the inverter circuit. The switches used for the inverter circuit is MOSFET. The number involves IRF P460. There are totally six switches namely s1,s3,s5 on top and s4, s2, s6 at the bottom. A snubber circuit is being provided along with the MOSFET. The snubber circuit consists of a resistor and a capacitor. The resistor is rated 100 ohms and the capacitor is rated 0.1 micro farad. The values of capacitor and resistor are same for all the snubber circuits in the inverter circuit.

## REFERENCES

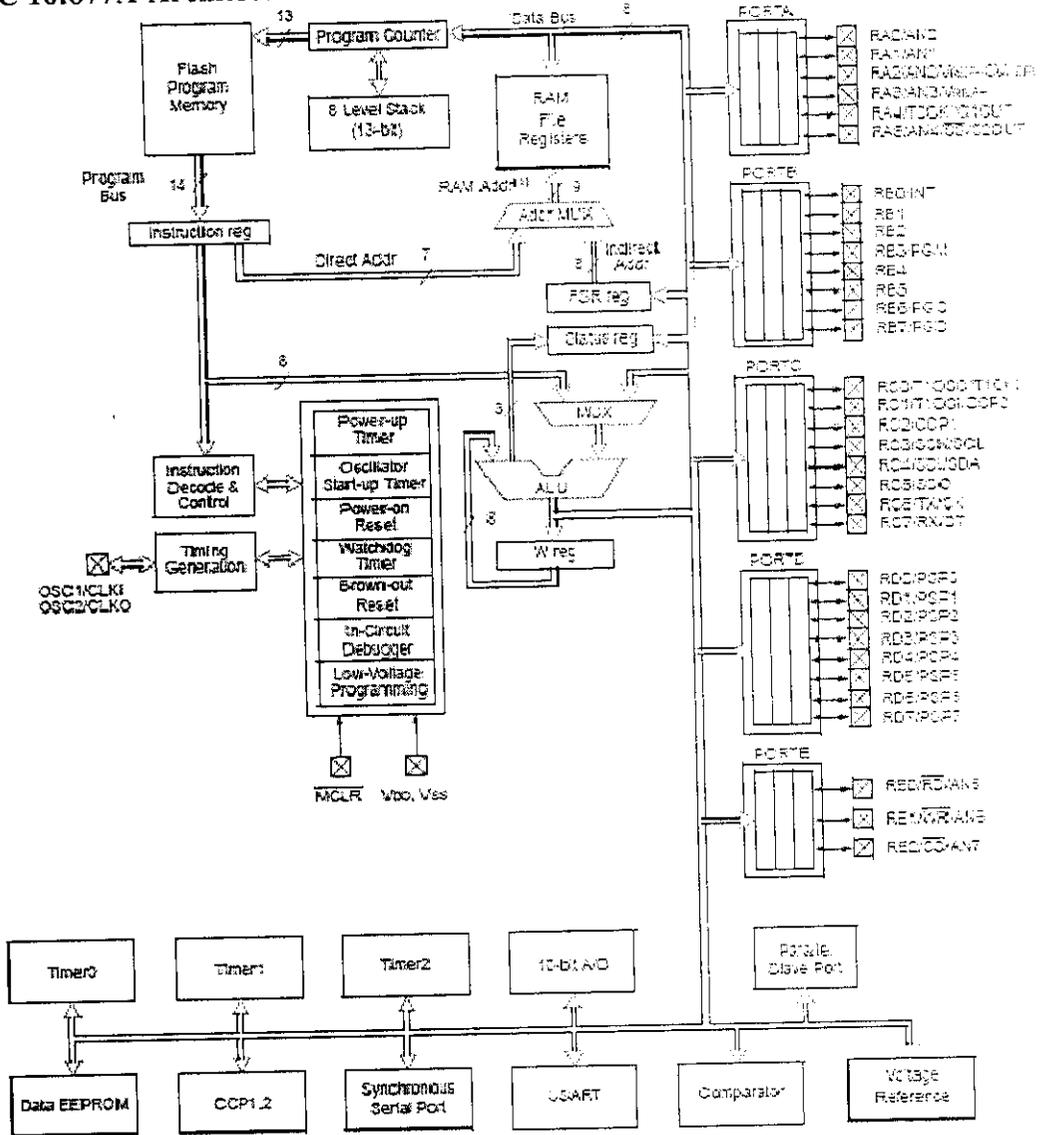
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- [9] B. Mwinyiwiwa, Z. Wolanski, and B. Ooi, "Microprocessor-Implemented SPWM for Multiconverters with Phase-Shifted Triangle Carriers", *IEEE Trans.on Industry applications*, Vol. 34, NO.3, pp-487-494, 1998.

## APPENDIX A

# APPENDIX A

## PIC 16F877A-Architecture



Device	Program Flash	Data Memory	Data EEPROM
PIC16F874A	4K words	192 Bytes	128 Bytes
PIC16F877A	8K words	384 Bytes	256 Bytes

Note 1: Higher order bits are from the Status register.

Fig A.1 PIC 16F877A-Architecture

## PIC16F87XA DEVICE FEATURES

Table A.1 PIC16F87XA device features

Key Features	PIC16F873A	PIC16F874A	PIC16F875A	PIC16F877A
Operating Frequency	DC – 20 MHz			
Resets (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
Flash Program Memory (14-bit words)	4K	4K	5K	5K
Data Memory (bytes)	192	192	385	385
EEPROM Data Memory (bytes)	128	128	256	256
Interrupts	14	15	14	15
I/O Ports	Ports A, B, C	Ports A, B, C, D, E	Ports A, B, C	Ports A, B, C, D, E
Timers	3	3	3	3
Capture/Compare/PWM modules	2	2	2	2
Serial Communications	MSCR, USART	MSCR, USART	MSCR, USART	MSCR, USART
Parallel Communications	—	PSP	—	PSP
10-bit Analog-to-Digital Module	5 Input channels	6 Input channels	5 Input channels	6 Input channels
Analog Comparators	2	2	2	2
Instruction Set	35 Instructions	35 Instructions	35 Instructions	35 Instructions
Packages	28-pin PDIP 20-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin PLCC 44-pin TQFP 44-pin QFN	28-pin PDIP 20-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin PLCC 44-pin TQFP 44-pin QFN

# PIC16F874A/877A PINOUT DESCRIPTION

## Table A.2 PIC16F874A/877A pinout description

Pin Name	PDIP Pin#	PLCC Pin#	TQFP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKI OSC1  CLKI	13	14	30	32	I  I	ST/CMOS(4)	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; otherwise CMOS. External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO OSC2  CLKO	14	15	31	33	O  O	—	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
MCLR/VPP MCLR  VPP	1	2	18	15	I  P	ST	Master Clear (input) or programming voltage (output). Master Clear (Reset) input. This pin is an active low Reset to the device. Programming voltage input.
RA0/AN0 RA0 AN0	2	3	19	19	I/O I	TTL	PORTA is a bidirectional I/O port.  Digital I/O. Analog input 0.
RA1/AN1 RA1 AN1	3	4	20	20	I/O I	TTL	Digital I/O. Analog input 1.
RA2/AN2/VREF-/CVREF RA2 AN2 VREF- CVREF	4	5	21	21	I/O I I O	TTL	Digital I/O. Analog input 2. A/D reference voltage (Low) input. Comparator VREF output.
RA3/AN3/VREF+ RA3 AN3 VREF+	5	6	22	22	I/O I I	TTL	Digital I/O. Analog input 3. A/D reference voltage (High) input.
RA4/T0CKI/C1OUT RA4  T0CKI C1OUT	8	7	23	23	I/O  I Q	ST	Digital I/O – Open-drain when configured as output. Timer0 external clock input. Comparator 1 output.
RA5/AN4/SS/C2OUT RA5 AN4 SS C2OUT	7	8	24	24	I/O I I O	TTL	Digital I/O. Analog input 4. SPI slave select input. Comparator 2 output.

Legend: I = input      O = output      I/O = input/output      P = power  
 — = Not used      TTL = TTL input      ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.  
 2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.  
 3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

# PIC16F874A/877A PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDIP Pin#	PLCC Pin#	TQFP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
PORT0 is a bidirectional I/O port.							
RC0/T1OSO/T1CKI RC0 T1OSO T1CKI	15	18	32	34	I/O O I	ST	Digital I/O. Timer1 oscillator output. Timer1 external clock input.
RC1/T1OSI/CCP2 RC1 T1OSI CCP2	16	18	35	35	I/O I I/O	ST	Digital I/O. Timer1 oscillator input. Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1 RC2 CCP1	17	19	36	36	I/O I/O	ST	Digital I/O. Capture1 input, Compare1 output, PWM1 output.
RC3/SCK/SCL RC3 SCK SCL	18	20	37	37	I/O I/O I/O	ST	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I2C mode.
RC4/SDI/SDA RC4 SDI SDA	23	26	42	42	I/O I I/O	ST	Digital I/O. SPI data in. I2C data I/O.
RC5/SDO RC5 SDO	24	26	43	43	I/O O	ST	Digital I/O. SPI data out.
RC6/TX/CK RC6 TX CK	25	27	44	44	I/O O I/O	ST	Digital I/O. USART asynchronous transmit. USART1 synchronous clock.
RC7/RX/DT RC7 RX DT	26	29	1	1	I/O I I/O	ST	Digital I/O. USART asynchronous receive. USART synchronous data.

Legend: I = input    O = output    I/O = input/output    P = power  
 — = Not used    TTL = TTL input    ST = Schmitt Trigger input

- Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.  
 2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.  
 3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

## TIMER0 MODULE

The Timer0 module timer/counter has the following

Features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

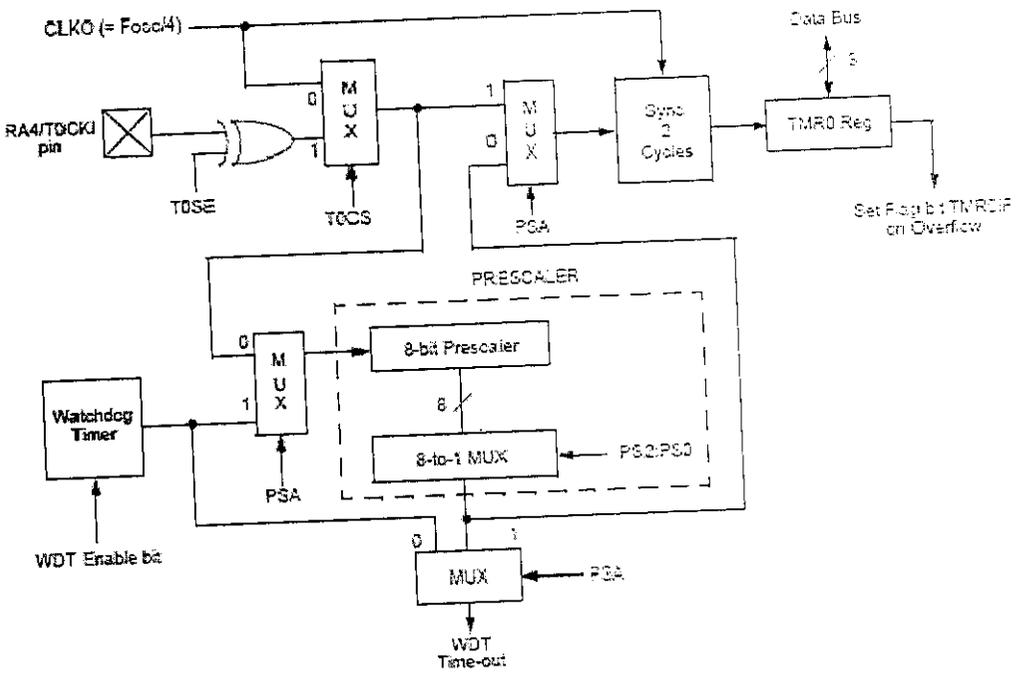
Figure 9.2 is a block diagram of the Timer0 module and the prescaler shared with the WDT. Additional information on the Timer0 module is available in the PICmicro® Mid-Range MCU Family Reference Manual (DS33023). Timer mode is selected by clearing bit T0CS (OPTION\_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register. Counter mode is selected by setting bit T0CS

(OPTION\_REG<5>). In Counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit, T0SE (OPTION\_REG<4>). Clearing bit T0SE selects the rising edge. The prescaler is mutually exclusively shared between the Timer0 module and the Watchdog Timer. The prescaler is not readable or writable.

**Timer0 Interrupt**

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit TMR0IF (INTCON<2>). The interrupt can be masked by clearing bit TMR0IE (INTCON<5>). Bit TMR0IF must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from Sleep since the timer is shut-off during Sleep.

**BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER**



Note: T0CS, T0SE, PSA, PS2:PS0 are (OPTION\_REG<5:0>).

Fig A.2 block diagram of the timer0/wdt prescaler

**I/O PORTS**

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin. Additional information on I/O ports may be found in the PICmicro™ Mid-Range Reference Manual (DS33023).

### PORTA and the TRISA Register

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin). Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, the value is modified and then written to the port data latch. Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The A4/T0CKI pin is a Schmitt Trigger input and an open-drain output. All other PORTA pins have TTL input levels and full CMOS output drivers. The operation of each pin is selected by clearing/setting the appropriate control bits in the ADCON1 and/or CMCON registers. The TRISA register controls the direction of the port pins even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

### BLOCK DIAGRAM OF RA3:RA0 PINS

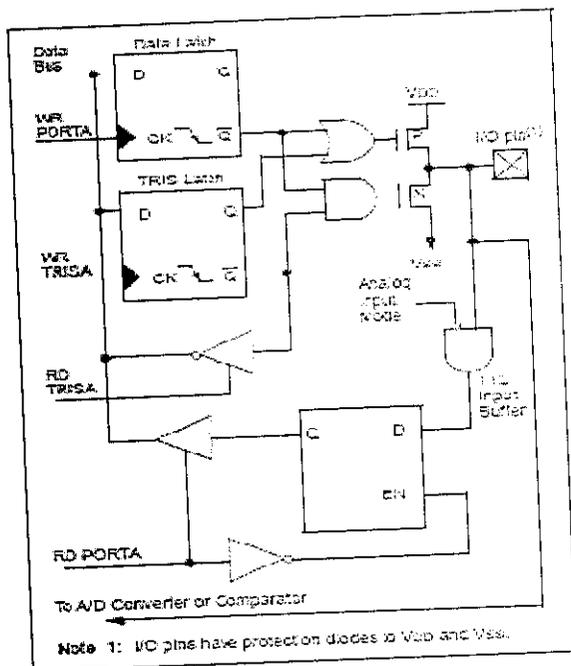


Fig A.3 block diagram of ra3:ra0 pins

## BLOCK DIAGRAM OF RA4/T0CKI PIN

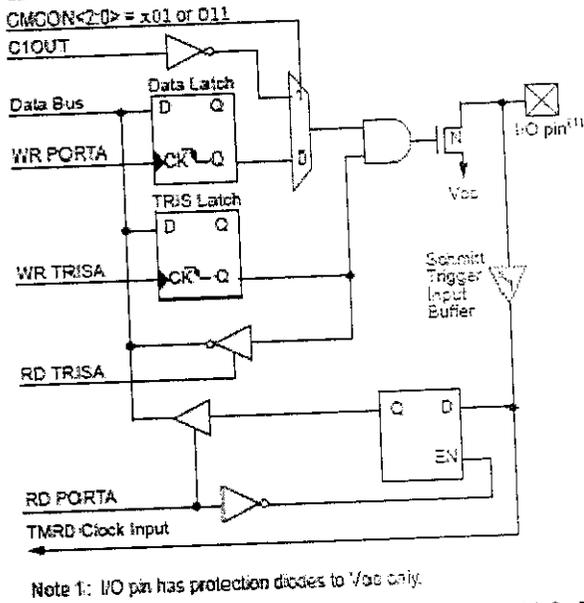


Fig A.4 block diagram of ra4/t0cki pin

## BLOCK DIAGRAM OF RA5 PIN

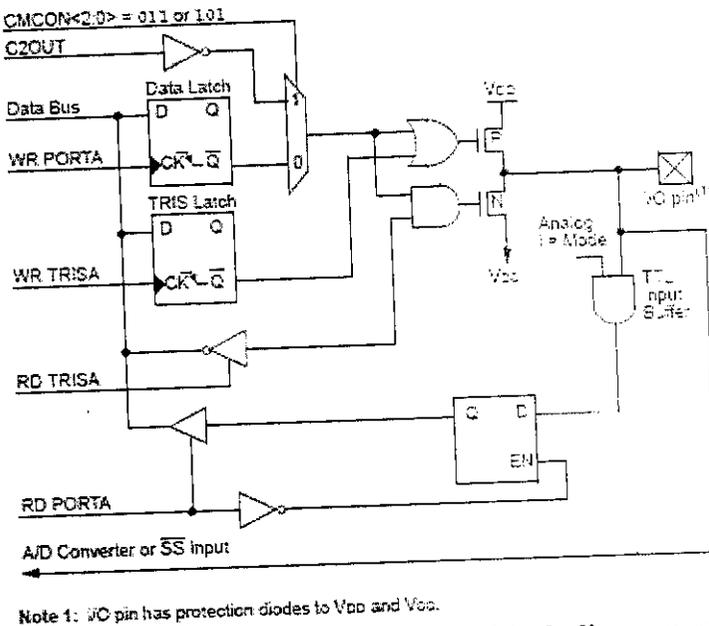


Fig A.5 block diagram of ra5 pin

# PORTA FUNCTIONS

Table A.3 PORTA functions

Name	Bit#	Buffer	Function
RA0/AN0	bit 0	TTL	Input/output or analog input.
RA1/AN1	bit 1	TTL	Input/output or analog input.
RA2/AN2/REF-/CVREF-	bit 2	TTL	Input/output or analog input or VREF- or CVREF-
RA3/AN3/REF+	bit 3	TTL	Input/output or analog input or VREF+.
RA4/T0CK/C1OUT	bit 4	ST	Input/output or external clock input for Timer0 or comparator output. Output is open-drain type.
RA5/AN4/SS/C2OUT	bit 5	TTL	Input/output or analog input or slave select input for synchronous serial port or comparator output.

Legend: TTL = TTL input, ST = Schmitt Trigger input

# SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Table A.4 summary of registers associated with PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--0x 0000	--0x 0000
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
9Ch	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	0000 0111
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVRC	000- 0000	000- 0000
9Fh	ADCON1	ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0	00-- 0000	00-- 0000

Legend: x = unknown, u = unchanged, - = unimplemented (locations read as '0'). Shaded cells are not used by PORTA.

Note: When using the SSP module in SPI Slave mode and SS enabled, the A/D converter must be set to one of the following modes, where PCFG3:PCFG0 = 0100, 0101, 011x, 1101, 1110, 1111.

## PORTB and the TRISB Register

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin). Three pins of PORTB are multiplexed with the In-Circuit Debugger and Low-Voltage Programming function: RB3/PGM, RB6/PGC and RB7/PGD. Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION\_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

# BLOCK DIAGRAM OF RB3:RB0 PINS

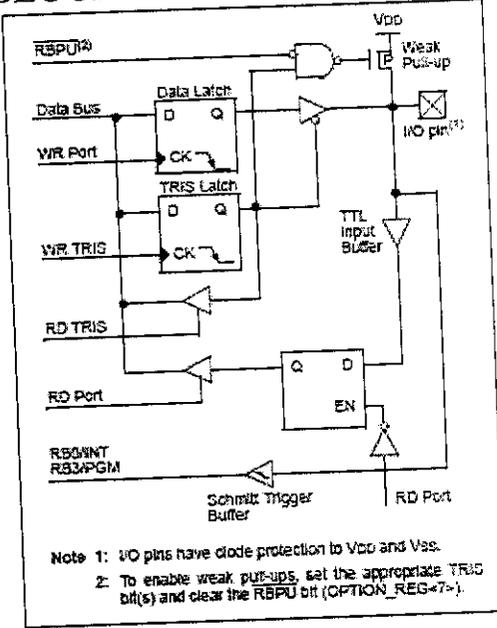


Fig A.6 block diagram of rb3:rb0 pins

# BLOCK DIAGRAM OF RB7:RB4 PINS

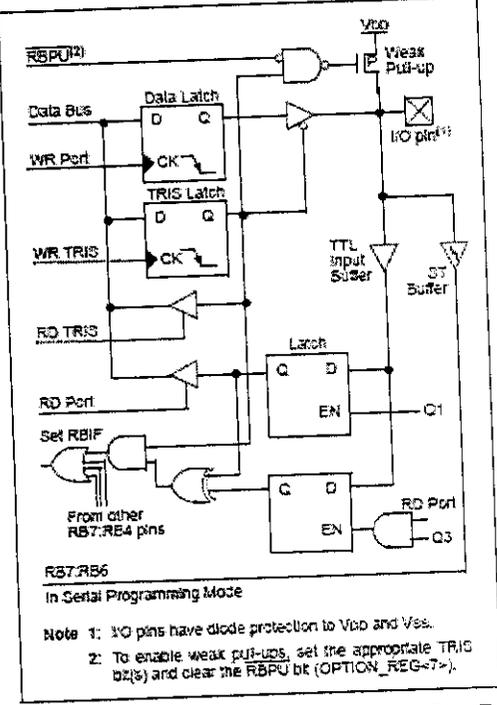


Fig A.7 block diagram of rb7:rb4 pins

## PORTB FUNCTIONS

Table A.5 PORTB functions

Name	Bit#	Buffer	Function
RB0/INT	bit 0	TTL/ST <sup>(1)</sup>	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit 1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit 2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3/PGM <sup>(3)</sup>	bit 3	TTL	Input/output pin or programming pin in LVP mode. Internal software programmable weak pull-up.
RB4	bit 4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit 5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6/PGC	bit 6	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt-on-change) or in-circuit debugger pin. Internal software programmable weak pull-up. Serial programming clock.
RB7/PGD	bit 7	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt-on-change) or in-circuit debugger pin. Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode or in-circuit debugger.

3: Low-Voltage ICSP Programming (LVP) is enabled by default which disables the RB3 I/O function. LVP must be disabled to enable RB3 as an I/O pin and allow maximum compatibility to the other 28-pin and 40-pin mid-range devices.

## SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Table A.6 summary of registers associated with PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h, 186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
81h, 181h	OPTION_REG	RSPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

# BUFFER-CD4050B

## Table A.7 Electrical specifications of buffer-CD4050B

DC Electrical Specifications				LIMITS AT INDICATED TEMPERATURE (°C)									
PARAMETER	TEST CONDITIONS									25			UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	0	25	125	MIN	TYP	MAX		
Quiescent Device Current I <sub>DD</sub> (Max)	-	0.5	5	1	1	20	30	-	0.02	1	0.5		
	-	0.10	10	2	2	60	60	-	0.02	2	0.5		
	-	0.15	15	4	4	120	120	-	0.02	4	0.5		
	-	0.20	20	20	20	600	200	-	0.04	20	0.5		
Output Low (Sink) Current I <sub>OL</sub> (Max)	0.4	0.5	4.5	3.3	3.1	2.1	1.8	2.8	3.0	-	0.5		
	0.4	0.5	5	4	3.8	2.3	2.4	3.2	3.4	-	0.5		
	0.6	0.10	10	10	8.6	6.8	6.8	6	16	-	0.5		
	1.5	0.15	15	25	25	20	18	24	40	-	0.5		
Output High (Source) Current I <sub>OH</sub> (Max)	4.0	0.5	5	-0.71	-0.70	-0.55	-0.45	-0.05	-0.7	-	0.5		
	2.5	0.5	5	-2.6	-2.4	-1.0	-1.55	-0.1	-0.9	-	0.5		
	0.5	0.10	10	-2.0	-1.2	-1.35	-1.15	-1.05	-3.0	-	0.5		
	13.5	0.15	15	-5.2	-4.6	-3.5	-3.1	-4.0	-8.0	-	0.5		
Output Voltage Low Level V <sub>OL</sub> (Max)	-	0.5	5	0.06	0.06	0.07	0.06	-	0	0.05	V		
	-	0.10	10	0.25	0.15	0.15	0.05	-	0	0.05	V		
	-	0.15	15	0.05	0.05	0.02	0.05	-	0	0.05	V		
Output Voltage High Level V <sub>OH</sub> (Min)	-	0.5	5	4.96	4.95	4.93	4.93	4.90	5	-	V		
	-	0.10	10	0.96	0.95	0.95	0.95	0.92	10	-	V		
	-	0.15	15	14.95	14.90	14.90	14.95	14.90	10	-	V		
Input Low Voltage, V <sub>IL</sub> (Max) CD4050B	4.5	-	5	1	1	1	1	-	-	1	V		
	0	-	10	2	2	2	2	-	-	2	V		
	13.5	-	15	2.5	2.3	2.5	2.5	-	-	2.5	V		
Input Low Voltage, V <sub>IL</sub> (Max) CD4050B	0.5	-	5	1.5	1.5	1.5	1.5	-	-	1.5	V		
	1	-	10	3	3	3	3	-	-	3	V		
	1.5	-	15	4	4	4	4	-	-	4	V		

# Continued

## DC Electrical Specifications (Continued)

PARAMETER	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURE (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>CC</sub> (V)	25							
				-55	-40	25	125	MIN	TYP	MAX	
Input High Voltage, V <sub>IH</sub> Min CD4040UB	0.5	-	5	4	4	4	4	4	-	-	V
	1	-	10	5	5	5	5	5	-	-	V
	1.5	-	15	12.5	12.5	12.5	12.5	12.5	-	-	V
Input High Voltage, V <sub>IH</sub> Min CD4060B	4.5	-	5	3.5	3.5	3.5	3.5	3.5	-	-	V
	5	-	10	7	7	7	7	7	-	-	V
	13.5	-	15	11	11	11	11	11	-	-	V
Input Current, I <sub>IN</sub> Max	-	0.18	18	+0.1	+0.1	-0.1	-0.1	-	-	+10 <sup>-5</sup>	mA

## AC Electrical Specifications T<sub>A</sub> = 25°C, Input I<sub>I</sub> = 20mA, C<sub>L</sub> = 50pF, R<sub>L</sub> = 200kΩ

PARAMETER	TEST CONDITIONS		LIMITS (ALL PACKAGES)		UNITS
	V <sub>IN</sub>	V <sub>CC</sub>	TYP	MAX	
Propagation Delay Time Low to High, t <sub>PLH</sub> CD4049UB	5	5	60	120	ns
	10	10	50	100	ns
	10	5	60	120	ns
	15	15	125	250	ns
	15	5	40	80	ns
Propagation Delay Time Low to High, t <sub>PLH</sub> CD4060B	5	5	70	140	ns
	10	10	60	120	ns
	10	5	45	90	ns
	15	15	90	180	ns
	15	5	40	80	ns
Propagation Delay Time High to Low, t <sub>PHL</sub> CD4049UB	5	5	50	100	ns
	10	10	50	100	ns
	10	5	15	30	ns
	15	15	15	30	ns
	15	5	10	20	ns
Propagation Delay Time High to Low, t <sub>PHL</sub> CD4060B	5	5	50	100	ns
	10	10	50	100	ns
	10	5	50	100	ns
	15	15	15	30	ns
	15	5	50	100	ns
Transition Time, Low to High, t <sub>TLH</sub>	5	5	50	100	ns
	10	10	40	80	ns
	15	15	50	100	ns
Transition Time, High to Low, t <sub>THL</sub>	5	5	50	100	ns
	10	10	50	100	ns
	15	15	15	30	ns



P-3428

# MOSFET-IRF840

Table A.8 Electrical characteristics of mosfet-IRF840

**Electrical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.55	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 4.0\text{ A}$	--	0.65	0.8	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 4.0\text{ A}$ (Note 4)	--	7.3	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	--	1400	1800	pF
$C_{oss}$	Output Capacitance		--	145	190	pF
$C_{rss}$	Reverse Transfer Capacitance		--	35	45	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 8.0\text{ A}, R_G = 25\ \Omega$	--	22	55	ns	
$t_r$	Turn-On Rise Time		--	65	140	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4, 5)	--	125	260	ns
$t_f$	Turn-Off Fall Time	$V_{DS} = 400\text{ V}, I_D = 8.0\text{ A}, V_{GS} = 10\text{ V}$	--	75	160	ns	
$Q_g$	Total Gate Charge		(Note 4, 5)	--	41	53	nC
$Q_{gs}$	Gate-Source Charge		--	--	6.5	--	nC
$Q_{gd}$	Gate-Drain Charge		--	17	--	nC	

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current		--	--	8.0	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current		--	--	32	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 8.0\text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 8.0\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	390	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	4.2	--	$\mu\text{C}$

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $L = 9.0\text{ mH}, I_{AS} = 8.0\text{ A}, V_{DD} = 60\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} = 8.0\text{ A}, dI/dt = 200\text{ A}/\mu\text{s}, V_{DD} = BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

### Peak Diode Recovery dv/dt Test Circuit & Waveforms

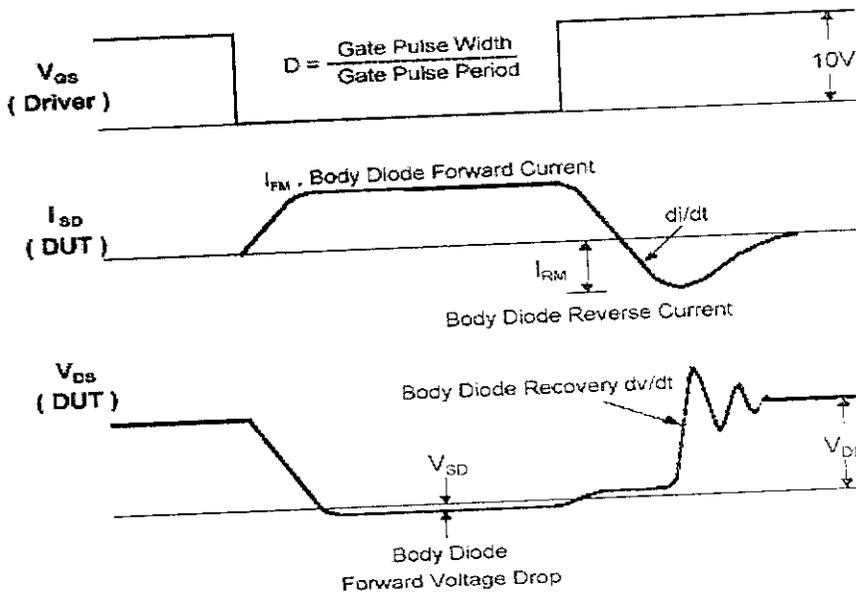
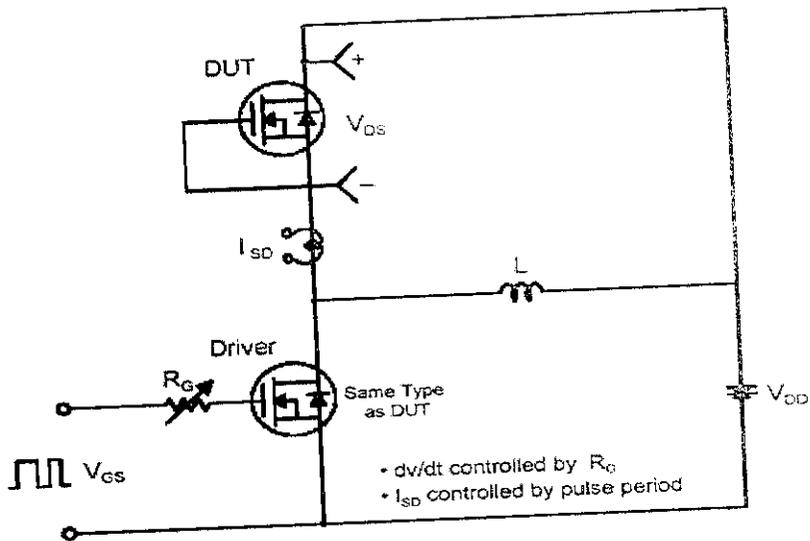


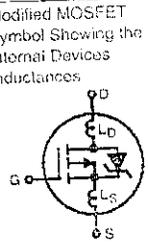
Fig A.8 peak diode recovery dv/dt test circuits and waveforms

# MOSFET- IRF9520

**Table A.9 Electrical specifications of mosfet- IRF9520**

Electrical Specifications  $T_C = 25^\circ\text{C}$ . Unless Otherwise Specified

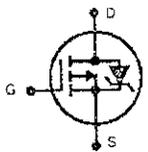
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = -250\mu\text{A}$ , $V_{GS} = 0\text{V}$ (Figure 10)	-100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = -250\mu\text{A}$	-2	-	-4	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{Rated } BV_{DSS}$ , $V_{GS} = 0\text{V}$ $V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ , $V_{GS} = 0\text{V}$ $T_C = 125^\circ\text{C}$	-	-	-250	$\mu\text{A}$
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ MAX. $V_{GS} = -10\text{V}$	-6	-	-	A
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	0.500	0.600	$\mu\text{A}$
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = -3.5\text{A}$ , $V_{GS} = -10\text{V}$ (Figures 8, 9)	0.0	2	-	$\Omega$
Forward Transconductance (Note 2)	$g_{fs}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ MAX. $I_D = -3.5\text{A}$ (Figure 12)	-	-	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 0.5 \times \text{Rated } BV_{DSS}$ , $I_D = -6.0\text{A}$ , $R_G = 50\Omega$ , $R_{th} = 7.7\Omega$ for $V_{DSS} = 50\Omega$	-	25	50	ns
Rise Time	$t_r$	MOSFET Switching Times are Essentially Independent of Operating Temperature	-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	$t_f$		-	16	22	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_g(TOT)$	$V_{GS} = -10\text{V}$ , $I_D = -6\text{A}$ , $V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ (Figure 14) Gate Charge is Essentially Independent of Operating Temperature	-	9	-	nC
Gate to Source Charge	$Q_{gs}$		-	7	-	nC
Gate to Drain "Miller" Charge	$Q_{gd}$		-	-	-	nC
Input Capacitance	$C_{iss}$	$V_{DS} = -25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$ (Figure 11)	-	300	-	pF
Output Capacitance	$C_{oss}$		-	200	-	pF
Reverse Transfer Capacitance	$C_{rss}$		-	50	-	pF
Internal Drain Inductance	$L_D$	Measured From the Contact Screw on Tab To Center of Die	Modified MOSFET Symbol Showing the Internal Device Inductances			
		Measured From the Drain Lead, 6mm (0.25in) from Package to Center of Die	-	4.5	-	nH
Internal Source Inductance	$L_S$	Measured From the Source Lead, 6mm (0.25in) From Header to Source Bonding Pad	-	7.5	-	nH
Thermal Resistance Junction-to-Case	$R_{thJC}$		-	-	3.12	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Ambient	$R_{thJA}$	Typical Socket Mount	-	-	62.5	$^\circ\text{C/W}$



**Table A.10 Source to drain diode specifications**

### Source to Drain Diode Specifications

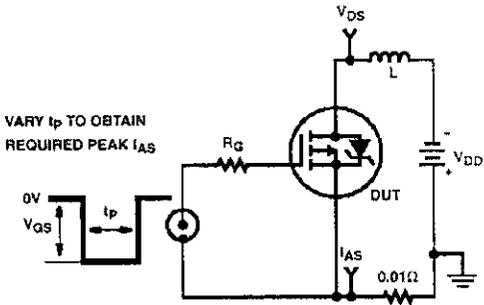
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	$I_{SD}$	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode	-	-	-0.5	A
Pulse Source to Drain Current (Note 3)	$I_{SDM}$		-	-	24	A
Source to Drain Diode Voltage (Note 2)	$V_{SD}$	$T_C = 25^\circ\text{C}$ , $I_{SD} = -6.0\text{A}$ , $V_{GS} = 0\text{V}$	-	-	-1.5	V
Reverse Recovery Time	$t_{rr}$	$T_J = 150^\circ\text{C}$ , $I_{SD} = -6.0\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	230	-	ns
Reverse Recovery Charge	$Q_{RR}$	$T_J = 150^\circ\text{C}$ , $I_{SD} = -6.0\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	1.3	-	nC



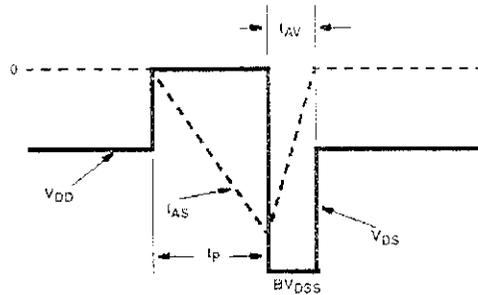
**NOTES:**

2. Pulse test: pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 9)
4.  $V_{DD} = 25\text{V}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 15.4\text{mH}$ ,  $R_G = 25\Omega$ , peak  $i_{GS} = 6.0\text{A}$ .

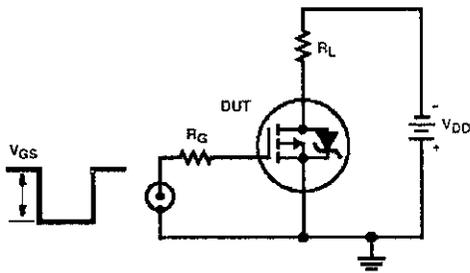
**Test Circuits and Waveforms**



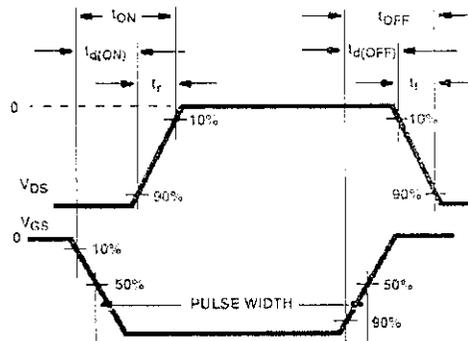
**UNCLAMPED ENERGY TEST CIRCUIT**



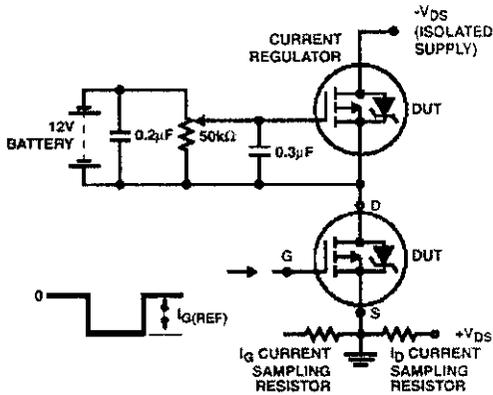
**UNCLAMPED ENERGY WAVEFORMS**



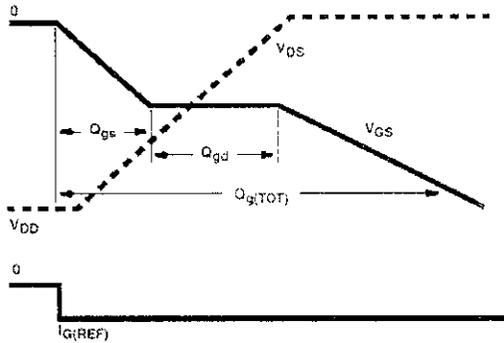
**SWITCHING TIME TEST CIRCUIT**



**RESISTIVE SWITCHING WAVEFORMS**



**GATE CHARGE TEST CIRCUIT**



**GATE CHARGE WAVEFORMS**

**Fig A.9 Test circuits and waveforms of MOSFET- IRF9520**

# OPTOISOLATOR-SFH615

## Maximum Ratings

Emitter (GaAs LED)	6 V
Reverse Voltage	60 mA
DC Forward Current	2.6 A
Surge Forward Current (t ≤ 10 μs)	100 mW
Total Power Dissipation	

## Detector (Silicon Phototransistor)

Collector-Emitter Voltage	70 V
Collector Current	50 mA
Collector Current (t ≤ 1 ms)	100 mA
Total Power Dissipation	150 mW

## Optocoupler

Storage Temperature Range	-55°C to +150°C
Ambient Temperature Range	-55°C to +100°C
Junction Temperature	100°C
Soldering Temperature (max. 10 s) <sup>1)</sup>	260°C
Isolation Test Voltage <sup>2)</sup>	

(between emitter and detector referred to standard climate 23/50 DIN 50014) . . . . . 2800 VDC  
Isolation Resistance (V<sub>iso</sub>=500 V) . . . . . 10<sup>11</sup> Ω

- Notes:**  
1 Dip soldering: minimum clearance from bottom edge of package 1.5 mm. Special soldering conditions apply when through-contacted circuit boards are used. Please request appropriate specification.  
2 DC test voltage in accordance with DIN 57853, draft 4/78

## Characteristics (T<sub>A</sub>=25°C)

### Emitter (GaAs LED)

Forward Voltage (I <sub>F</sub> =60 mA)	V <sub>F</sub>	1.25 (±1.65)	V
Breakdown Voltage (I <sub>R</sub> =10 μA)	V <sub>BR</sub>	30 (±6)	V
Reverse Current (V <sub>R</sub> =6 V)	I <sub>R</sub>	0.01 (±10)	μA
Capacitance (V <sub>R</sub> =0 V, f=1 MHz)	C <sub>0</sub>	25	pF
Thermal Resistance	R <sub>thJA</sub>	750	K/W

### Detector (Silicon Phototransistor)

Capacitance (V <sub>CE</sub> =5 V, f=1 MHz)	C <sub>CE</sub>	6.8	pF
Thermal Resistance	R <sub>thJA</sub>	500	K/W

### Optocoupler

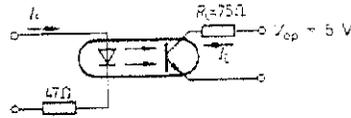
Collector-Emitter Saturation Voltage (I <sub>F</sub> =10 mA, I <sub>C</sub> =2.5 mA)	V <sub>CE(sat)</sub>	0.25 (±0.4)	V
Coupling Capacitance	C <sub>k</sub>	0.25	pF

The optocouplers are grouped according to their current transfer ratio I<sub>C</sub>/I<sub>F</sub> at V<sub>CE</sub>=5 V, marked by dash numbers

	-1	-2	-3	-4	
I <sub>C</sub> /I <sub>F</sub> (I <sub>F</sub> =10 mA)	40-80	63-125	100-200	160-320	%
I <sub>C</sub> /I <sub>F</sub> (I <sub>F</sub> =1 mA)	30 (>13)	46 (>22)	70 (>34)	90 (>56)	%
Collector-Emitter Leakage Current (V <sub>CE</sub> =10 V) (I <sub>CE</sub> )	2 (≤50)	2 (≤50)	5 (≤100)	5 (≤100)	nA

## SWITCHING TIMES

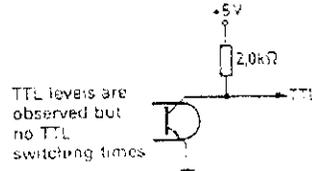
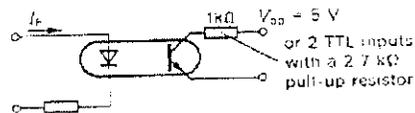
### Linear Operation (without saturation)



I<sub>F</sub>=10 mA, V<sub>CE</sub>=5 V, T<sub>A</sub>=25°C

Load Resistance	R <sub>L</sub>	75	Ω
Turn-On Time	t <sub>on</sub>	3.0 (±5.6)	μs
Rise Time	t <sub>r</sub>	2.0 (±4.0)	μs
Turn-Off Time	t <sub>off</sub>	2.3 (±4.1)	μs
Fall Time	t <sub>f</sub>	2.0 (±3.5)	μs
Cut-Off Frequency	F <sub>3dB</sub>	260	kHz

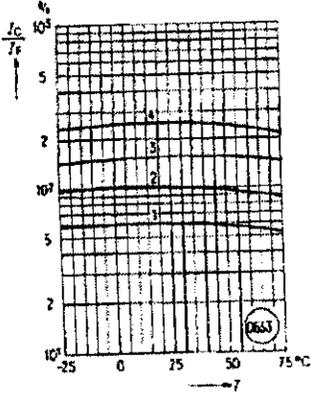
### Switching Operation (with saturation)



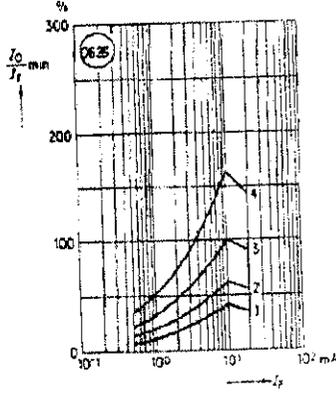
Group	-1 (I <sub>F</sub> =20 mA)	-2 and -3 (I <sub>F</sub> =10 mA)	-4 (I <sub>F</sub> =5 mA)		
Turn-On Time	t <sub>on</sub>	3.0 (±5.5)	4.2 (±6.0)	6.0 (±10.5)	μs
Rise Time	t <sub>r</sub>	2.0 (±4.0)	3.0 (±6.0)	4.6 (±6.0)	μs
Turn-Off Time	t <sub>off</sub>	18 (±34)	23 (±39)	25 (±43)	μs
Fall Time	t <sub>f</sub>	11 (±20)	14 (±24)	15 (±26)	μs
V <sub>CE(sat)</sub>		0.25 (±0.4)			V

# CHARACTERISTICS:

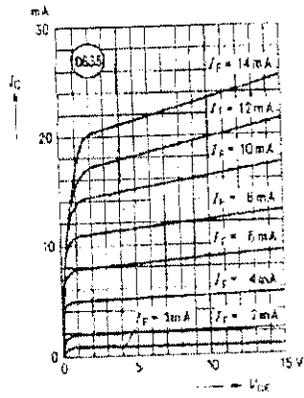
**Current transfer ratio (typ.) versus temperature**  
( $I_F = 10 \text{ mA}$ ,  $V_{CE} = 5 \text{ V}$ )



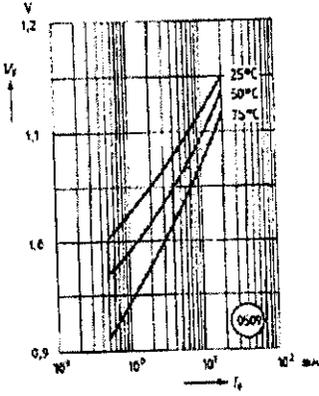
**Minimum current transfer ratio versus diode forward current**  
( $T_A = 25^{\circ}\text{C}$ ,  $V_{CE} = 5 \text{ V}$ )



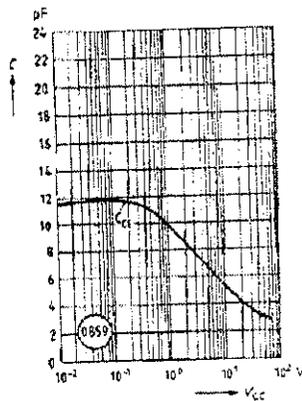
**Output characteristics (typ.)**  
Collector current versus collector-emitter voltage  
( $T_A = 25^{\circ}\text{C}$ )



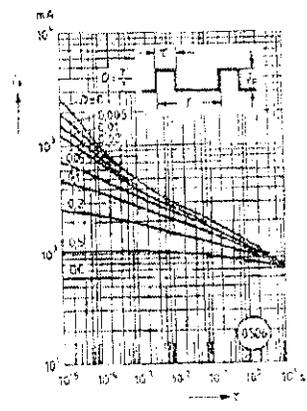
**Diode forward voltage (typ.) versus forward current**



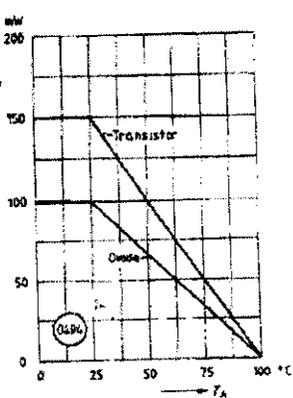
**Transistor capacitance (typ.) versus collector-emitter voltage**  
( $T_A = 25^{\circ}\text{C}$ ,  $f = 1 \text{ MHz}$ )



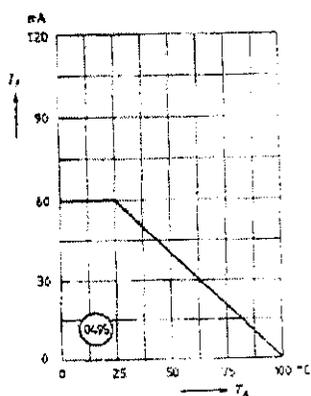
**Permissible pulse handling capability**  
Forward current versus pulse width  
( $D = \text{parameter}$ ,  $T_A = 25^{\circ}\text{C}$ )



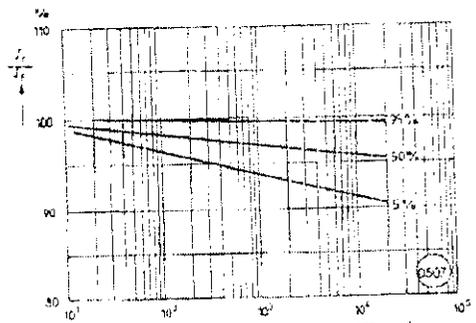
**Permissible power dissipation versus ambient temperature**



**Permissible forward current of the diode versus ambient temperature**



**Current transfer ratio versus load time**  
( $V_{CE} = 5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$ ,  $T_A = 60^{\circ}\text{C}$ ,  $I_B = 60 \text{ mA}$ , Measuring current = 10 mA, Confidence coefficient  $S = 60\%$ )



**Fig A.10 characteristics of optoisolator-SFH615**

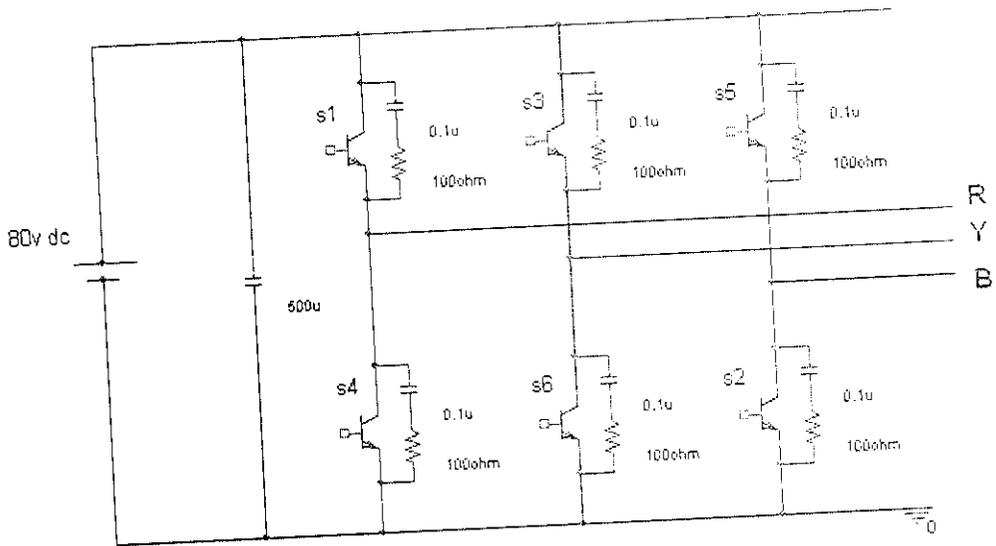


Fig. 3.13 Inverter Circuit

## MOSFET

The component that is used as the switch in the inverter unit is the MOSFET which is a voltage controlled device. They are the power semi conductor devices that have a fast switching property with a simple drive requirement.

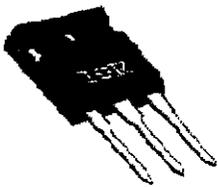


Fig 3.14 (a) MOSFET Switch

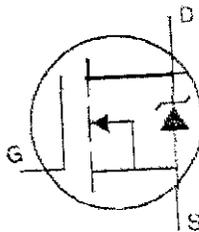


Fig 3.14 (b) MOSFET Symbol

$$V_{ds} = 500 \text{ V}$$

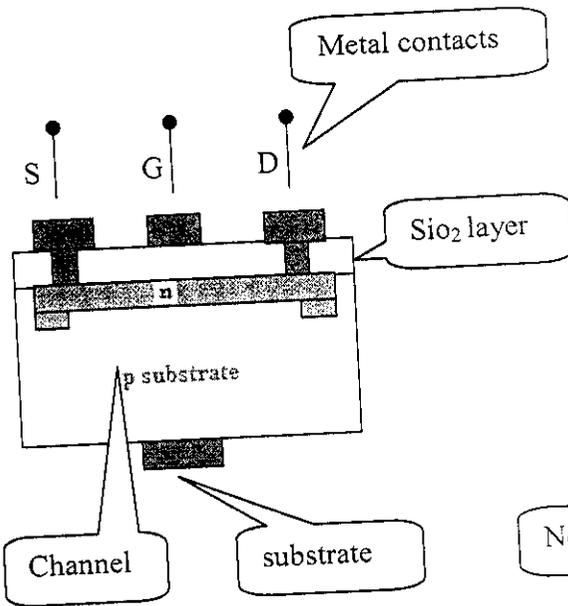
$$R_{ds}(\text{on}) = 0.27 \text{ ohm}$$

$$I_d = 20 \text{ A}$$

## Construction and Operation principle of MOSFET

There are two basic types of MOSFETs. They are N Channel depletion type and N Channel enhancement type.

### A. N Channel depletion type



### B. N Channel enhancement type

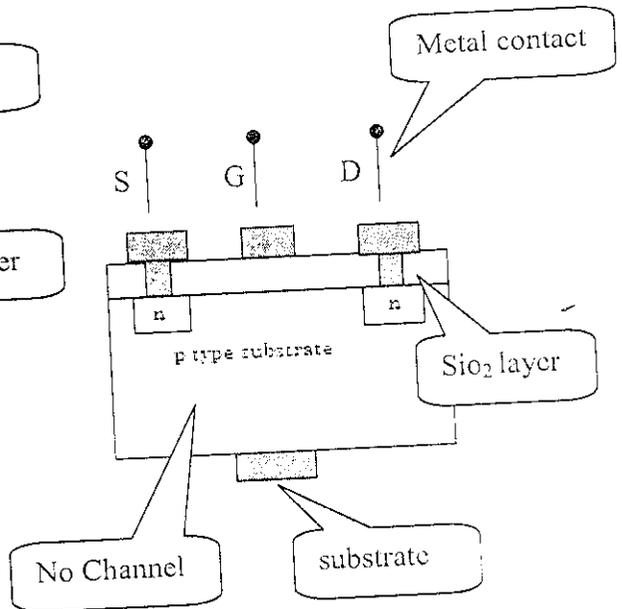


Fig 3.15 A, B MOSFET Types

### A.N Channel depletion

The N channel depletion type of MOSFET is constructed with p-Substrate. It has two n-doped regions, which forms the drain and source. It has SiO<sub>2</sub> insulating layer between the channel and the metal layer. Thus it has three terminals namely drain source and gate.

With a negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, leaving positive ions in their place. Thereby, the N-channel is depleted of some of its electrons, thus by decreasing the channel conductivity.

When a positive voltage is applied between the gate and source, more electrons are induced in the channel by capacitor action. So there is a flow of current from drain to source. As the gate source voltage increases, the channel gets wider by accumulation of more negative charges and resistance to the channel decreases. Thus more current flows from drain to source. As there is a current flow through device for zero gate source voltage, it is normally called as ON MOSFET.

### **B.N Channel Enhancement:**

The N channel enhancement MOSFET is similar to the depletion type in the construction except that there is no physical existence of the channel when it is unbiased.

When the positive voltage is applied between the gate and the source, the electrons get accumulated in the channel by capacitive induction in the channel formed out of electrons allowing the flow of current. This channel gets widened as more positive voltage is applied between gate and source. There will not be any condition through the device if the gate source voltage is negative.

As the enhancement type MOSFET conduct only after applying positive gate voltage, it is also called as normally OFF MOSFET. For this reason it becomes easily controllable and is used in power electronics as a switch.

## **PIC16F877 MICROCONTROLLER**

### **3.4.1 MICROCONTROLLER CORE FEATURES:**

#### **High-Performance RISC CPU:**

- Only 35 single-word instructions to learn
- All single-cycle instructions except for program branches, which are two-cycle
- Operating speed: DC – 20 MHz clock input DC – 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory,
  - Up to 368 x 8 bytes of Data Memory (RAM),
  - Up to 256 x 8 bytes of EEPROM Data Memory
- Pin out compatible to other 28-pin or 40/44-pin
  - PIC16CXXX and PIC16FXXX microcontrollers

### **Analog Features:**

- 10-bit, up to 8-channel Analog-to-Digital Converter (A/D)
- Brown-out Reset (BOR)
- Analog Comparator module with:
  - Two analog comparators
  - Programmable on-chip voltage reference (VREF) module
  - Programmable input multiplexing from device inputs and internal voltage references
  - Comparator outputs are externally accessible

### **Special Microcontroller Features:**

- 100,000 erase/write cycle Enhanced Flash Program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory typical
- Data EEPROM Retention > 40 years
- Self-reprogrammable under software control
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Single-supply 5V In-Circuit Serial Programming
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving Sleep mode
- Selectable oscillator options
- In-Circuit Debug (ICD) via two pin
- Low-power, high-speed Flash/EEPROM technology
- Fully static design
- Wide operating voltage range (2.0V to 5.5V)
- Commercial and Industrial temperature ranges
- Low-power consumption
- Programmable code protection
- Power saving Sleep mode

### 3.4.2 PIN DIAGRAM:

#### 40-Pin PDIP

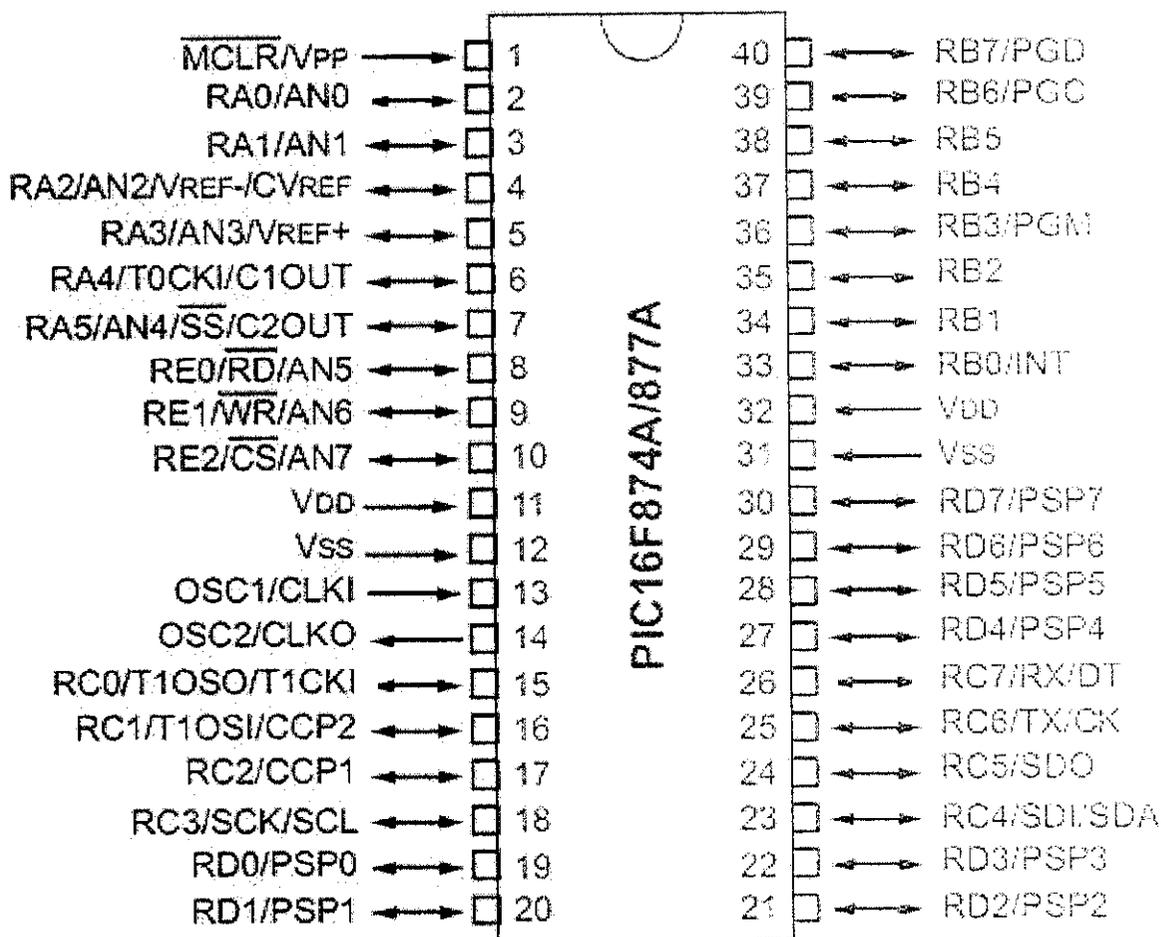


Fig 3.16 Pin diagram of PIC 16F877A

## Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during Sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
  - Capture is 16-bit, max. resolution is 12.5 ns
  - Compare is 16-bit, max. resolution is 200 ns
  - PWM max. resolution is 10-bit
- Synchronous Serial Port (SSP) with SPI™
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) – 8 bits wide with external RD, WR and CS controls
- Brown-out detection circuitry for Brown-out Reset (BOR)
- The PIC16F873A and PIC16F874A have one-half of the total on-chip memory of the PIC16F876A and PIC16F877A
- The 28-pin devices have three I/O ports, while the 40/44-pin devices have five
- The 28-pin devices have fourteen interrupts, while the 40/44-pin devices have fifteen
- The 28-pin devices have five A/D input channels, while the 40/44-pin devices have eight
- The Parallel Slave Port is implemented only on 40/44 pin devices.

**CHAPTER 4**  
**CONCLUSION**

## **CONCLUSION:**

In this project **TEMPERATURE CONTROLLER FOR FURNACE USING INDIRECT MATRIX CONVERTER** has been designed and implemented. By doing so, the disadvantages present in analog based design are overcome. The advantages of the new system are a simple circuitry, reduced system size, power factor improvement and minimum cost.

A buffer circuit is used to enhance the signal strength so that the inverter designed can be used for industrial purposes. The PIC 16F877A has the required features for programming in C language. By this method accurate and precise temperature control can be obtained.