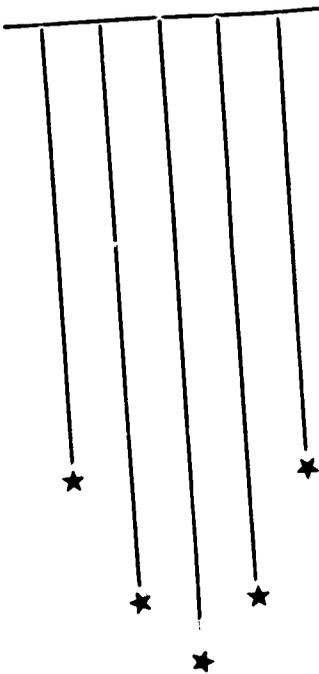


REACTIVE POWER REGULATOR

PROJECT REPORT

P-347



1998 - 99

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TAMIL NADU STATE COUNCIL F
SCIENCE & TECHNOLO

in partial fulfilment of the requirem

for the award of the degr

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BRANCH OF THE BHARATHIAR UNIVER

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CERTIFICATE

This is to certify that the project entitled

REACTIVE POWER REGULATOR

has been submitted by

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In partial fulfillment of the requirements for the award of degree of Bachelor of Engineering in the Electrical & Electronics Engineering branch of the Bharathiar University, Coimbatore - 641 006 during the academic year 1998-1999.

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CERTIFICATE

This is to certify that the following final year B.E. (E.E.E) students of
Kumaraguru College of Technology, Coimbatore have carried out a project work
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The title of the project was " REACTIVE POWER REGULATOR "

During this period, their attendance and conduct were found to be good.

We wish them the very best for a bright future.

Place : Samichettipalayam

Date : 12-03-1999


(R.DEVARAJ)
(FOR MICRO INSTRUMENTS LIMITED)

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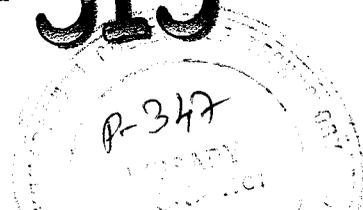
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SYNOPSIS



SYNOPSIS

The subject of management of reactive power in power system has not received due importance. This is a vital action which needs to be taken urgently to set right many maladies of transmission and distribution systems and provide quality in supply voltage.

In the present context of energy crisis in the country, the role of reducing transmission system losses is significant. This can be achieved by proper allocation of reactive power. The optimal scheduling of reactive power not only leads to reduction of system active power loss but also improves the system voltage profile. Further, it also reduces line and equipment loading and thus results in increased power capability.

Demand for reactive power arises out of electromagnetic circuits of motors, transformers, inductance of transmission lines, electric furnaces, florescent and gas discharge lamps, etc.,. Voltage control, essentially means reactive power control in a network. The reactive power generated by synchronous generators, lines and capacitor units are required to balance the reactive power requirements.

There are three types of compensation for HV and EHV transmission lines,

- (a) Series compensation
- (b) shunt capacitor compensation
- (c) static VAR compensation (SVC)

In our project the reactive power control is done by connecting / disconnecting the capacitor banks according to the reactive power requirement.

The connection and disconnection of capacitor banks is done by using contactors connected with Electromagnetic relays. The relays are in turn switched on or off by the logical decision of a micro computer.

The micro computer here decides the number of steps to be Connected, by making complex calculations. The steps here are controlled under the ratio 1 : 1 : 1. i.e., equal rating of Capacitor Banks.

Here in our project we have made an attempt to positively control the reactive power thus improving the power factor of the system. This system can be extended to 1 : 2 : 2 or 1 : 2 : 4 steps ratio as explained in figure (i).

In the process of maintaining good voltage profile in a power system it is essential to keep in view the Q transport, its generation and absorption. Thus losses in transmission system can be minimized by judicious choice of reactive power injection and power transformer tap settings.

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PIN DETAILS OF IC LM339

IC 74LS86

IC 74LS47

RELAYS

CHAPTER I

INTRODUCTION

Present day rural distribution networks are predominant connected with reactive loads having very low lagging power factor contributing for increased currents and poor voltage regulation. If the receiving end voltage of the distribution is to be maintained within reasonable limits, the network should have adequate reactive power support.

The method adopted consist of automatic switched capacitor scheme comprising of a bank of L.T. capacitors of rating suitable for maximum KVAR requirement of concerned L.T. distribution with necessary provision of switching a suitable value of capacitor bank, such that, the remaining capacitor bank suits to reactive KVA demand of the system at a particular period of time.

Capacitor across individual consumers gives the benefit of loss Reduction and voltage improvement to the maximum extent possible and also acts as automatic switched capacitor without using semi-automatic switch gear.

In our project, the reactive power control is achieved by three units,

- (i) Power factor measurement unit
- (ii) Control unit
- (iii) Power factor improvement unit

In practice most of distribution circuits catering inductive loads selected for the study, power factor was found to be in the range of 0.6 to 0.75 from this it is inferred that large number of distribution circuits supplying power to inductive consumer have low power factor which can be improved around unity by application of shunt capacitors.

The percent reduction in losses after application of capacitors in terms of losses of a distribution systems before application of capacitors can be calculated by:

The saving in line losses expressed as a

$$\text{percentage of former value losses} = [1 - \{\cos\theta_1/\cos\theta_2\}]$$

The general block diagram of the project is shown in Fig 1.1

In general, capacitor, by reducing peak load feeder voltage drops, allow greater feeder loads to be carried. Also capacitors by reducing KVA loads, release substation and generation capacity. The application of shunt capacitors to a distribution feeder catering inductive consumers produces a uniform voltage boost per unit length of line, out to its point of application.

The fundamental KVAR and KW relations in a circuit when the power factor is improved are readily portrayed in the Fig 1.2

The following relations define some of the properties of the figure, regarding released capacity in inductive equipment which has a current magnitude as the limiting factor.

Capacitor KVAR to go from θ_1 to θ_2

$$CKVA = KVA_1 (\sin\theta_1 - (\cos\theta_1 * \sin\theta_2) / \cos\theta_2)$$

Resultant KVA at θ_2

$$KVA_2 = KVA_1 \cos\theta_1 / \cos\theta_2$$

The KVA released $(KVA) - KVA_1$

$$((KVA / KVA_1 (\sin \theta_1 - 1) + 1 - [(KVA_2 / KVA_1^2] \cos^2 \theta_1$$

Released KW = released KVA cos θ_1

1.1: POWER FACTOR MEASURING UNIT:

The power factor measuring unit consists of

- 1) A voltage transformer to measure the voltage
- 2) A Current Transformer to measure the current
- 3) A comparator for both voltage and current for converting the analog signal to the corresponding pulses (positive).
- 4) An EX-OR gate to compare the voltage and current and measure the phase angle between them.

1.2: CONTROL UNIT:

The control unit consists of

- 1) A microcomputer unit, in which the microprocessor reads the phase angle pulse and finds out the corresponding power factor and displays it and takes decision to either connect or disconnect relays.

2) Relay unit to send the control signal to the contractor to either connect or disconnect the capacitor bank connected to it corresponding from the microcomputer.

1.3: POWER FACTOR IMPROVEMENT UNIT:

Power factor improvement unit consists of capacitor banks which adds leading KVAR to the supply voltage and improves the corresponding power factor.

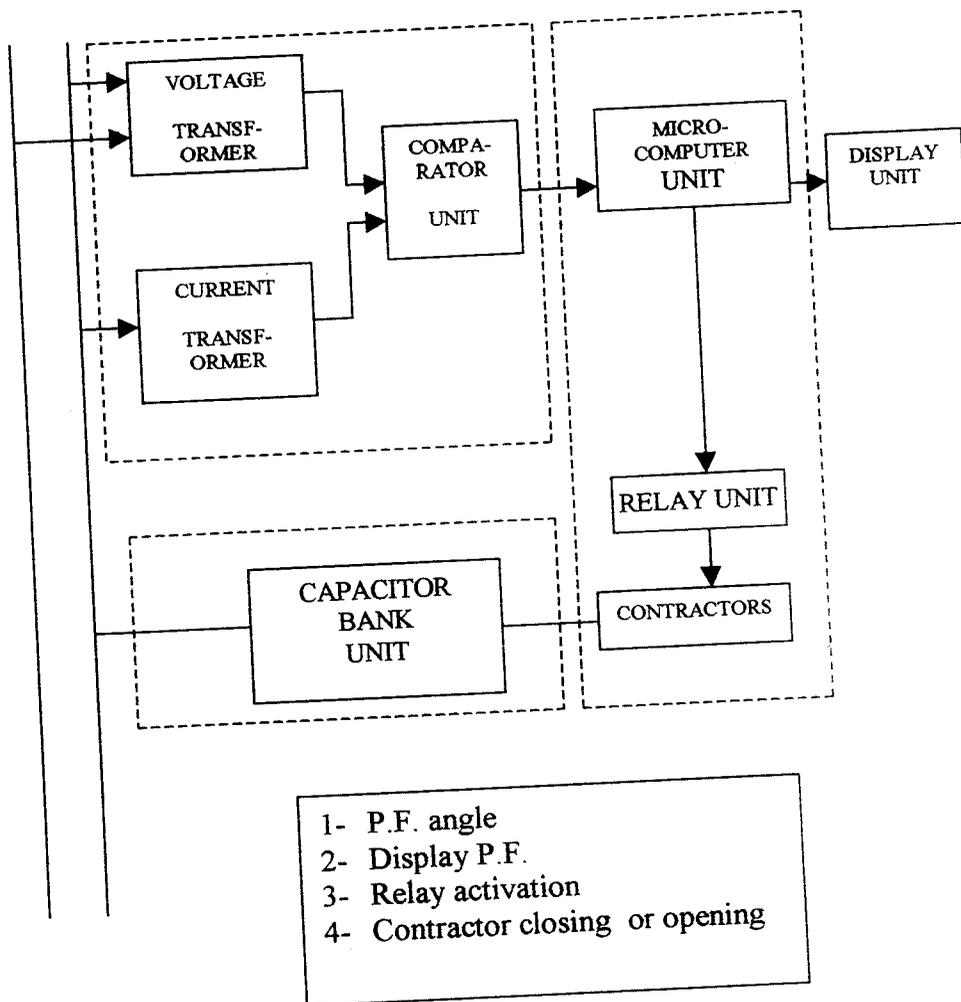


Fig 1.1 General Block Diagram

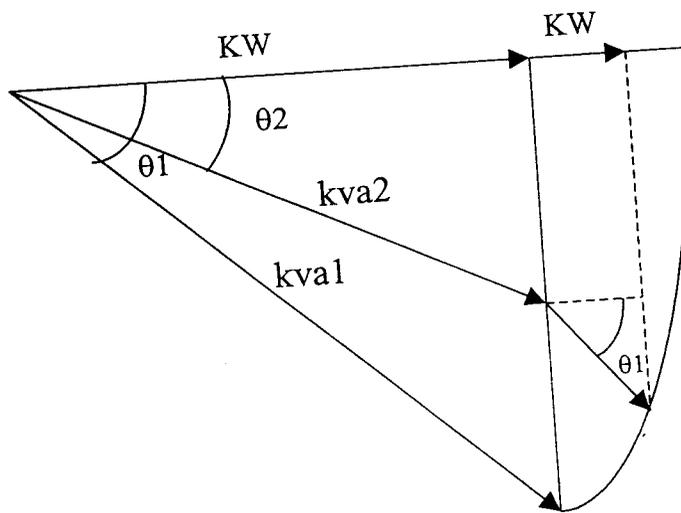


Fig 1.2 Phasor Diagram

CHAPTER II

HARDWARE

2.1 POWER FACTOR MEASUREMENT UNIT:

Fig 2.1 shows the circuit used for measurement of P.F.

The power factor measurement unit consists of

2.1.1) Potential Transformer :-

Specifications:

Primary →	415 V AC	230V
	2 V	
Secondary →	0 – 1.5 V AC, 050mA	
	12.5V	10A
	0 – 15 V AC, 500 mA	

It measures the circuit voltage and 1.5 V input is used for the input to the comparator circuit.

2.1.2) Current Transformer :-

Specifications:

Primary →	10 A	✓
Secondary →	1 A	✓

It measures the current on the mains and the reactive current is fed to the comparator circuit. For heavy loads the C.T. can be replaced by suitable ratio.

2.1.3) Comparator :-

Specifications:

IC LM339 (16 pin)

Supply - + 5V and gnd

It has four comparators of which two are utilized each one for the Voltage input and reactive current input. The C / k settings for the comparator is set. The C / K settings is set manually by the formula,

Transformer ratio : $I_t / 5 = K$

Reactive current adjustments, $C/K = I_c / K$

Where I_t = rated transformer current

I_c = current of the first capacitor

Example :

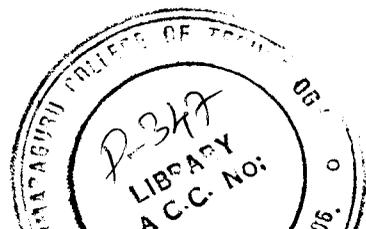
Transformer ratio : $K = 500 / 5A = 100$

First capacitor = 60 KVAR, 400V

= 86.7A

C/K setting control = $I_c/K = 86.7/100 = 0.867$

Thus the voltage and current inputs are transformed into positive pulses as shown in the Fig 2.2 .



2.1.4) EX-OR gate :-

This gate compare the voltage and current unit input, such that phase difference between them or the phase angle width is given out as a positive pulse. The positive pulse corresponds to the power factor.

Specification :

IC – 74LS86 (14 pin)

Supply - + 5V and gnd

Input - 2 input quad gates

The phase angle measured is fed as an input to the microcomputer using a connector IDC 26 pin to pin 1 and the voltage input is given as input to pin 3. Fig 2.3 shows the measurement of power factor angle.

So this input forms a relation between the phase angle and power Factor

$$\text{Phase angle width } \propto \frac{1}{\text{Power factor}}$$

So if the phase angle width increases, then power factor decreases if the phase angle width decreases, the power factor increases.

When the phase angle width becomes 5 ms, then power factor, $\cos \theta = 0$ where $\theta = \pi / 2$.

2.2) CONTROL UNIT:

The control unit is based on the microelectronic technology, a well Proven single board microcomputer unit which uses a microprocessor control circuit to get the

input, process the data and make complex decisions to either connect or disconnect the capacitor bank and to provide signals to display the power factor value.

The control unit consists of a

- MC - 8051
- 1) Microprocessor unit -8085AH
 - 2) 8255A peripheral interface (programmable)
 - 3) 8279 programmable keyboard / display interface
 - 4) Relay unit

2.2.1 MICROPROCESSOR UNIT [8085]

The microprocessor is a semiconductor device consisting of electronic logic circuits manufactured by using either a large scale [LSI] or very-large-scale integration [VLSI] Technique.

It is a multipurpose, programmable logic device that reads binary instructions from a storage device called memory, accepts binary data as input and processes data according to those instructions and provides results as output.

40 pin integrated, Intel 8085 microprocessor is used for 8 bit data manipulation and it has 16 address lines that can locate 64 KB (2^{16}) of memory. It requires a +5V single power supply, and can operate with a 3MHz single-phase clock.

The 8085 is an enhanced version of its predecessor, the 8080A; its instruction set is upward – compatible with that of the 8080A, means that 8085 instruction set includes all the 8080 A instructions plus some additional ones. Programs written for 8080A will be executed by the 8085, but the 8085 and 8080A are not compatible. Figure shows the logic pinout of 8085 microprocessor.

* All the signals can be classified into six groups.

- Address bus
- Data bus
- Control and status signal
- Power supply and frequency signals
- Externally initiated signals and
- Serial I/O ports.

2.2.2) Address bus:

The 8085 has eight signal lines, A15 – A8, which are unidirectional And used as the high order address bus. Multiplexed address / data bus (AD0- AD7) will act as a low order address lines (A0 – A7) when address latch enable (ALE) is high signal.

2.2.3) Data bus:

Multiplexed address / data bus AD0 – AD7 will act as a data bus (D0 – D7) when address latch enable (ALE) is low signal.

2.2.4) Control and status signal:

This group of signals includes two control signals RD and WR , three status signals IO/M, S1, S0 to identify the nature of the operation, and one special signal ALE to indicate the beginning of the operation.

2.2.5) Power supply and clock frequency:

These signals are

V _{cc}	:	+ 5 volt power supply
V _{ss}	:	Ground reference
X ₁ , X ₂	:	Crystal Oscillator for 3.6 MHz

2.2.6) Externally initiated signals including interrupts:

The 8085 has five input interrupt signals and one input signal namely

1. INTR (input) – interrupt request
2. INTA (output) – interrupt acknowledge
3. RST 7.5 (input) – restart interrupt
4. RST 6.5 (input) – restart interrupt
5. RST 5.5 (input) – restart interrupt
6. TRAP (input) – Non- Maskable-Interrupt

In addition to the interrupts, three pins – RESTART, HOLD and READY – accept the externally initiated signals as inputs.

2.2.7) Serial I/O ports:

The 8085 has two signals to implement the serial transmission:

SID (serial input data) and

SOD (serial output data)

The microprocessor can be separated as follows

- 1) Arithmetic / logic unit
- 2) Timing and control unit
- 3) Instruction register and decoder
- 4) Register array
- 5) Other registers including pointer and counters.

Microprocessor will provide signals to other elements. These signals are conveyed

on cables known as highways or bus. Figure shows the functional block diagram of 8085 microprocessor.

1) The Alu:

The arithmetic logic unit performs the computing functions; it includes

- a) The Accumulator
- b) The temporary register
- c) The arithmetic and logic circuits and
- d) Five Flags.

The temporary register is used to hold data during an arithmetic operation. The result is stored in the accumulator and the flags are set or reset according to the result of the operation. There are five flags namely Sign flag (S), Zero flag (Z), Auxiliary carry flag (AC), Parity flag (P) and Carry flag (CY)

2) Timing and Control Unit:

This unit synchronizes all the microprocessor operations with the clock and generates the control signals are similar to a synchronous pulse in an oscilloscope. The RD and WR signals are synchronous pulses indicating the availability of data on the data bus.

3) Instruction register and decodes:

The instruction register and decoder are part of the ALU. When an instruction is fetched from memory, it is loaded in the instruction register. The decoder decodes the instruction and establishes the sequence of events to follow. The instruction register is not programmable and cannot be accessed through any instruction.

4) Register Array:

The 8085 has six general purpose registers to store 8-bit data during a program execution. These registers are named as B, C, D, E, H, and L and they can be combined as register pairs – BC, DE and HL to perform some 16 bit operations. Two additional registers W and Z are included in register array.

2.2.8) Other Registers including pointers and counters:

(i) Accumulator (A):

The accumulator is an 8 bit register that is part of the arithmetic unit (ALU). This register is used to store 8 bit data and perform arithmetic and logical operations. The result of an operation is stored in the accumulator. The accumulator is also identified and as register A.

(ii) Program counter (PC).

This 16 bit register is used to sequence the execution of instruction. This register is a memory pointer. Memory locations have 16 bit address, and that is why this is a 16-bit register. The function of the program counter is to point to the memory address from which the next byte is to be fetched. When a byte is being fetched, the program counter is incremented by one to point to the next memory location.

(iii) Stack pointer (SP):

The stack pointer is a 16 bit register used as a memory pointer to point the starting address of the stack. The stack can be described as a set of memory locations in R/W memory, specified by a programmer in a main program. These memory locations are used to store binary information temporarily during the execution of the program.

2.3) Program Memory:

Read only memory (ROM) is used to store programs that do not want alterations. That is once all the faults have been removed from a program. The instruction will probably not need any change. It is unnecessary to hold it in read / write memory (RAM), because it is a volatile memory. So it needs supply to hold the data but ROM is a non-volatile memory. It is simple and also safer than RAM.

The programmable ROM (PROM) on the other hand allow user to do their own field programming of their control memory and a part of the main memory which keeps the monitor program of a single board microcomputer.

A type of ROM known as erasable PROM (EPROM) allows the user change its contents which can be held for years of routine operation. EPROMS are loaded by PROM programmer and erased by ultraviolet light in a safety case. As from above, we refer EPROM as program memory.

2.3.1) Data memory:

The read/write memory $\overline{(R/W)} \overline{M}$ (or) Random Access Memory (RAM) is also known as user memory or data memory. It is used to store user programs and data. In single board microcomputers, the monitor program monitors the hex keys and stores those instructions and data in RAM only.

Before, store in to the EPROM we enter all the programs in RAM only because error in the program can be easily rectified in this memory. After, the all correction only program will be stored in the EPROM.

All the data including user inputs and results after the manipulation is to be stored in the RAM memory.

User program is also a data for the single ship microcomputer because it varies according to the user. RAM holds all the user data temporarily to read randomly at any time before switch offing the supply. As from above RAM is known a data memory.

2.4. Programmable key board / display interfacing

[8279]:

The 8279 is a hardware approach to interfacing a matrix keyboard and a multiplexed display. The software approach to interfacing a matrix keyboard and a multiplexed display of seven segment LEDs is obtained by writing program to access the input key and also the display a data which includes debounce by delay program. Software approach occupies considerable amount of time in checking the keyboard and refreshing the display.

The trade – offs between the hardware approach and the software approach are producing cost vs . the processor time and the software development cost. Logic symbol of 8279 is shown in figure.

Four major sections of the 8279 are:

1. Keyboard section
2. Scan section
3. Display section
4. MPU interface section.

The functions of this sections are described below:

2.4.1. Keyboard section:

This section has eight lines (RL0 – RL7) that can be connected to eight columns of a keyboard. The keys are automatically debounced, and the keyboard can operate in two modes: two - key lock out or N – key rollover.

In the two-key lock out mode, if two keys are pressed almost simultaneously, only the first key is recognized. In the N – key roller mode, simultaneous keys

are recognized and their codes are stored in the internal buffer; it can also be set up show that no key is recognized until only one key remains pressed.

The keyboard section also includes 8 x 8 FIFO (first-in-first-out) RAM. The FIFO RAM consist of eight registers that can store 8 keyboard entries; each is then read in the order of entries. The status logic keeps tack of the number of entries and provides an IRQ (interrupt request) signal when the FIFO is not empty.

2.4.2. Scan section:

The scan section has a scan counter and four scan lines (SL0-SL3). These four scan lines can be decoded using a 4 to 16 decoder to generate 16 lines for scanning. These lines can be connected to the row of a matrix keyboard and the digit drivers of a multiplexed display.

2.4.3. Display section:

The display section has eight output lines divided into two groups A0 – A3 and B0 – B3. These lines can be used, either as a group of eight lines or as two groups of four, in conjunction with the scan lines for a multiplexed display. The display can be blanked by using the BD line. This section includes 16 x 8 display RAM. The MPU can read from or write in to any of these registers.

2.4.4. MPU Interface Section:

This section includes eight bi-directional data lines (DB0 – DB7), one interrupt request line (IRQ), and six lines for interfacing, including the buffer address line (A0). When A0 is high, signals are interpreted as control words or status; when A0 is low signals are interpreted as data. The IRQ line goes high whenever data entries are stored in FIFO. This signal is used to interrupt the MPU to indicate the availability of data.

2.4.5. Input / Output Unit:

Input section transfers data and instructions in binary from the outside world to the microprocessor. Hex-keyboard is to be given input to the microprocessor. PRI 85 AD kit keyboard consist 16 keys for hexadecimal input, six command keys including EXAM REG, delimiter group key (NEXT, PREV, EXEC) and system operation keys RESET and KBINT keys.

Output section transfer data from microprocessor to the out side world using six seven segment LEDs (light emitting diodes)

Four LED's starting from left is used to display the location of memory (address) and other two LED's is used to display the content of that address.

2.4.6. Interfacing devices:

Several types of interfacing devices are necessary to interconnect the component of a bus – oriented system. The devices used in today's microcomputer systems are designed using medium – scale integration (MSI) technology. In addition, tri-state devices are essential to proper functioning of bus – oriented system, in which the same bus lines are shared by several components.

2.4.7. BUFFER:

The buffer is a logic circuit that amplifier the current or power. It has one input line and ne output line. The logic level of the output is the same as that of input. The buffer is used primarily to increase the driving capacity of a logic circuit. It is also known as a driver. We used [74LS244] tri-state buffer to amplifier the high order bus lines (A7 – A15).

The data bus of a micro computer system is bi-directional, therefore, it requires a buffer that allows data to flow in both direction. Bi-direction buffer 74LS245 is used for data lines (D0-D7). It Is also called as octal bus transreceiver.

The 74LS245 includes 16 bus drivers (A1-A8 and B1-B8), eight for each direction, with tri-state output. The direction of date flow is controlled by the pin DIR (direction). When DIR is high, data flow from the A bus to the B bus, when it is low, data flow from B to A.

2.4.8. Decoder:

The decoder is a logic circuit that identifies each combination of the signals present at its input. For example, if the input to a decoder has two binary lines, the decoder will have four output lines. The two lines can assume four combinations of input signals – 00 , 01 , 10, 11 with each combination identified by the output lines 0 to 3.

If the input is 11_2 , the output line 3 will be a logic 1, and the others will remain at logic 0. This is called decoding.

The 74LS138 is called 1 - out of - 8 binary decoders or demultiplexers. It has three input lines and 8 active output lines. It requires three enable inputs; two are active low and one is active high; all three enable lines should be activated so that the device can function as a decoder. If the 74138 is enabled ($G_2 = G_1 = 0$ and $G_0 = 1$) and if the input is 101_2 the output Y_5 will go low, others will remain high.

2.4.9. LATCH:

A latch is a D flip-flop and used commonly to interface output devices. When the MPU sends an output, data are available on the data bus for only a few micro seconds: therefore, a latch is used to hold data for display.

This octal latch is used to latch 8 bit data. The device (74LS373) Includes eight D latches with tri-state buffers, and it requires two input signals, enable (G) and output control (OC).

The enable is an active high signal connected to the clock input of the flip-flop. When the signal goes low, data are latched from the data bus. The output control signal is active low, and it enables the tri-state buffers to output data to display devices.

Latch (74LS373) is mainly used to demultiplex the multiplexed address / data lines AD_0-AD_7 .

2.5. 8255A Programmable Peripheral Interface.

The 8255A is a widely used, programmable, parallel I/O device. It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O. It is flexible, versatile, and economical (when multiple I/O ports are required), but somewhat complex. It is an important general-purpose I/O device that can be used almost any microprocessor.

The 8255A has 24 I/O pins that can be grouped primarily in two 8-bit parallel ports: A and B, with the remaining eight bit of port C can be used as individual bits or be grouped in to 4-bit ports: C_{UPPER} (C_U) And C_{LOWER} (C_L), as in figure 2.5.1(a) . The functions of these ports are defined by writing a control word in the control register.

Figure 2.5.1(b) shows all the functions of the 8255A, classified according to two modes: the Bit Set / Reset (BSR)

mode and the I/O mode. The BSR mode is used to set or reset the bits in port C. The I/O mode is further divided into three modes: mode 0, mode 1, and mode 2. In mode 0, all ports function as simple I/O ports. Mode 1 is a handshake mode whereby ports A and / or B use bits from port C as handshake signals. In the handshake mode, two types of I/O data transfer can be implemented: status check and interrupt. In mode 2, port A can be set up for bi-directional data transfer using handshake signals from port C, and port B can be set up in either in mode 0 or mode 1.

2.5.1 BLOCK DIAGRAM OF THE 8255A

The block diagram in Figure 2.5.2(a) shows two 8-bit ports (A and B), two 4-bit ports (C_U and C_L), the data bus buffer, and control logic. Figure 2.5.2(b) shows a simplified but expanded version of the internal structure, including a control register. This block diagram includes all the elements of a programmable device; port C performs functions similar to that of the status register in addition to providing handshake signals.

2.5.2 CONTROL LOGIC

The control section has six lines. Their functions and connections are as follows:

□ $\overline{\text{RD}}$ (Read) :

This control signal enables the Read operation. When the signal is low, the MPU reads data from a selected I/O port of the 8255A.

□ $\overline{\text{WR}}$ (Write):

This control signal enables the Write operation. When the signal goes low, the MPU writes into a selected I/O port or the control register.

□ RESET (Reset):

This is an active high signal; it clears the control register and sets all ports in the input mode.

□ \overline{CS} , A_0 , and A_1 :

These are device select signals. \overline{CS} is connected to a decoded address, and A_0 and A_1 are generally connected to MPU address lines A_0 and A_1 , respectively.

The \overline{CS} signal is the master chip select, and A_0 and A_1 specify one of the I/O ports or the control register as given below:

\overline{CS}	A_1	A_0	Selected
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	X	X	8255A is not selected

2.6. RELAY UNIT:-

Specification:

Type : Single contact (Normally open)

Operating Voltage : 12 V DC (unregulated)

Current : 500 mA

The relay unit is actuated from the signals at the port. It is closed and the contactor coil connects the capacitor bank. When it is open, the contactor coil disconnects the capacitor bank.

The relay used here is an Electro Magnetic Induction type over current relay.

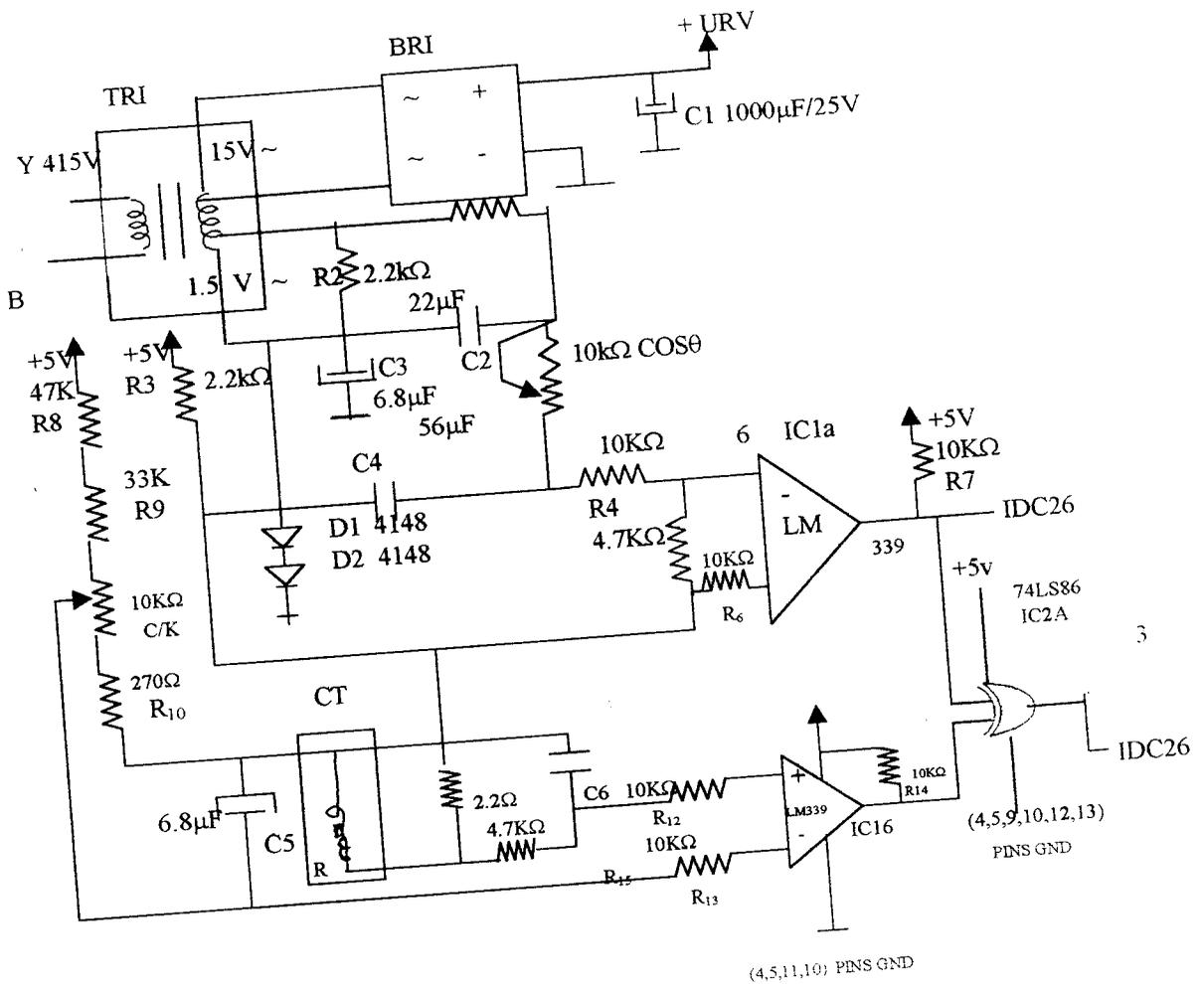
2.6.1. DISPLAY UNIT:-

The microcomputer counts the pulse width and displays the corresponding power factor by using a 74LS247 or 74LS47 BCD to 7 segment decoder / driver. The port outputs a BCD value which is the power factor.

There are 2 LED 7 segment display units to show the power factor as shown in Fig 2.

2.7. POWER FACTOR IMPROVEMENT UNIT:-

The capacitor banks are connected in equal ratios 1:1:1 so that the relay when it operates, the connector coil includes the bank and when it disconnects, it allows a delay of 150 sec to make the capacitor discharge.



CT-Current transformer
 TR- Potential transformer
 UR-Unregulated voltage
 BR-Bridge rectifier
 R -Resistor
 C -Capacitor
 IC1-LM339 Comparator
 IC2-74LS86 EX-OR gate

IDC 26-Input / Output connector(26 pin)
 Pot - Potentiometer
 C / K -Current setting
 Cos θ - Power factor setting
 P - Primary side

Fig 2.1 Power factor measuring circuit

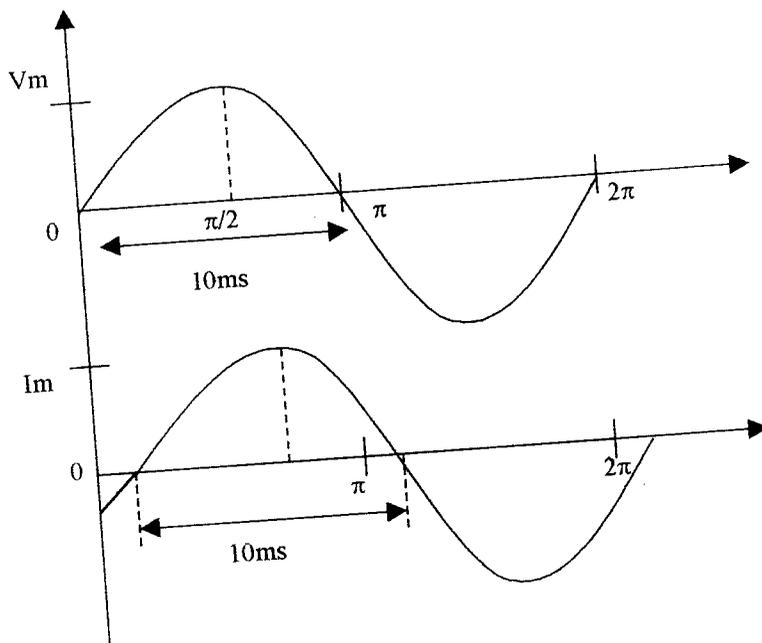


Fig 2.2(a) Voltage and Current Waveforms

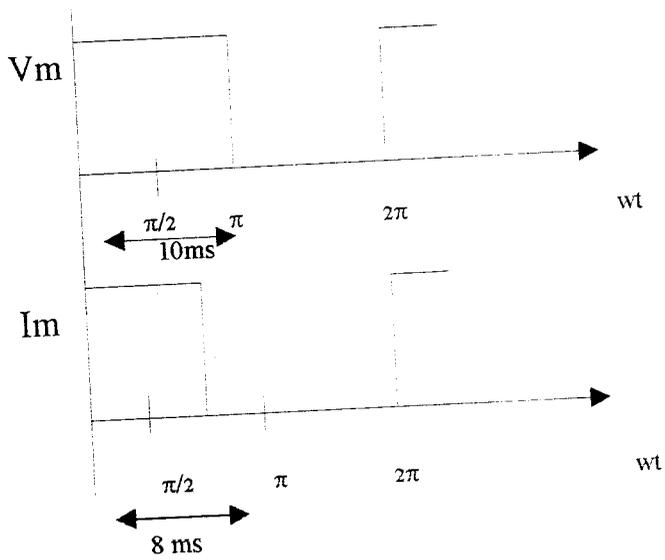


Fig 2.2(b) comparator output wave form

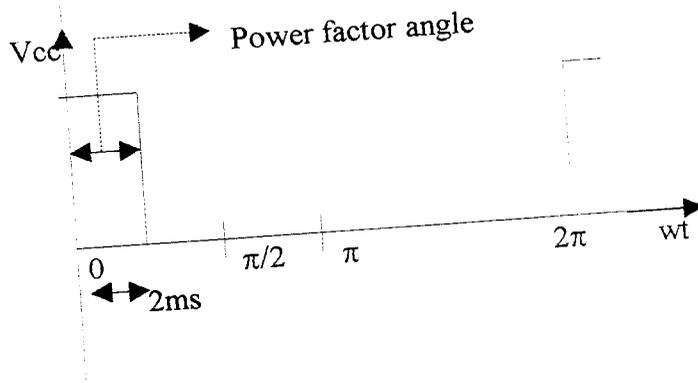
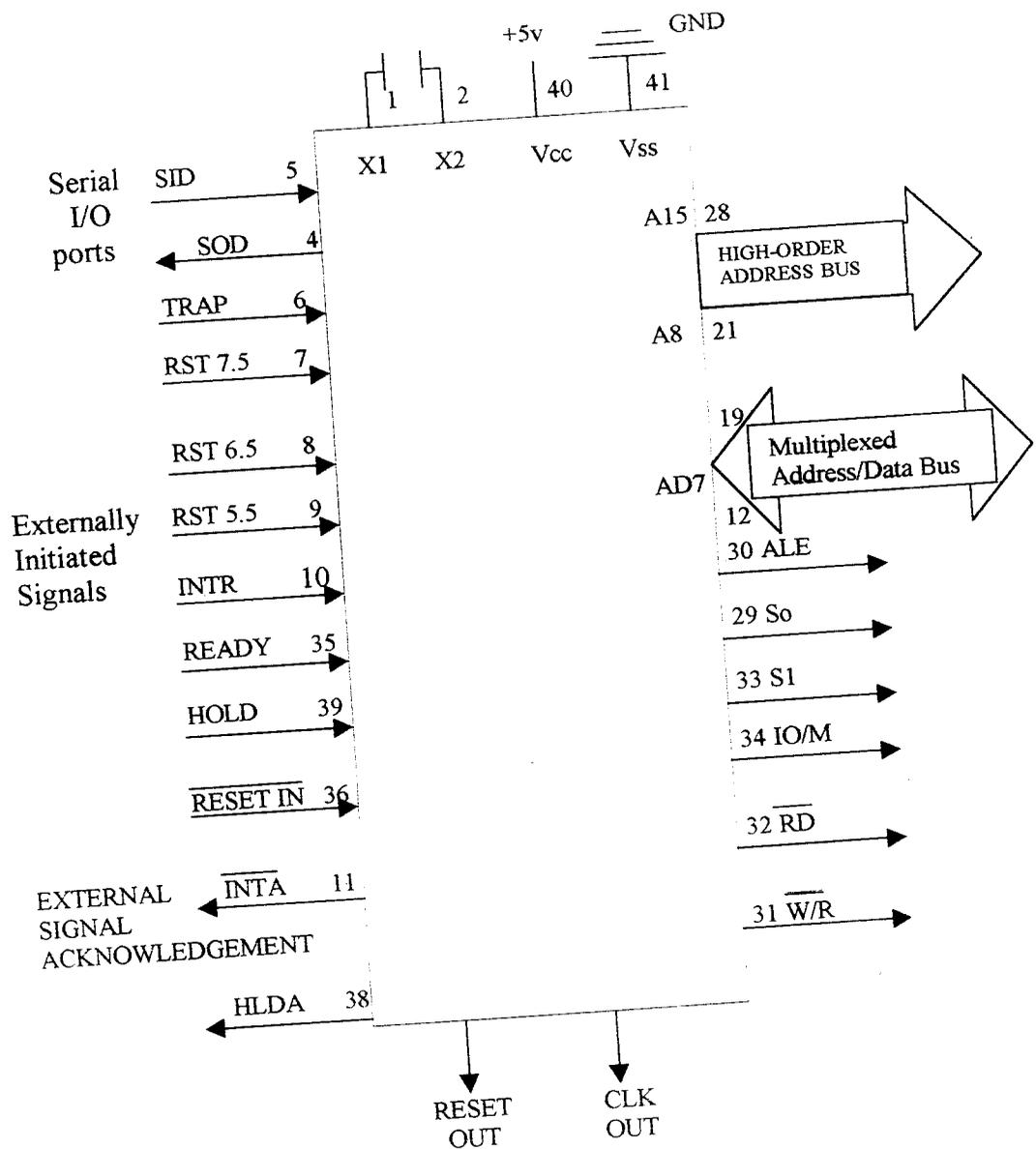


Fig 2.3 Measurement of Power Factor Angle



LOGIC PINOUT OF 8085

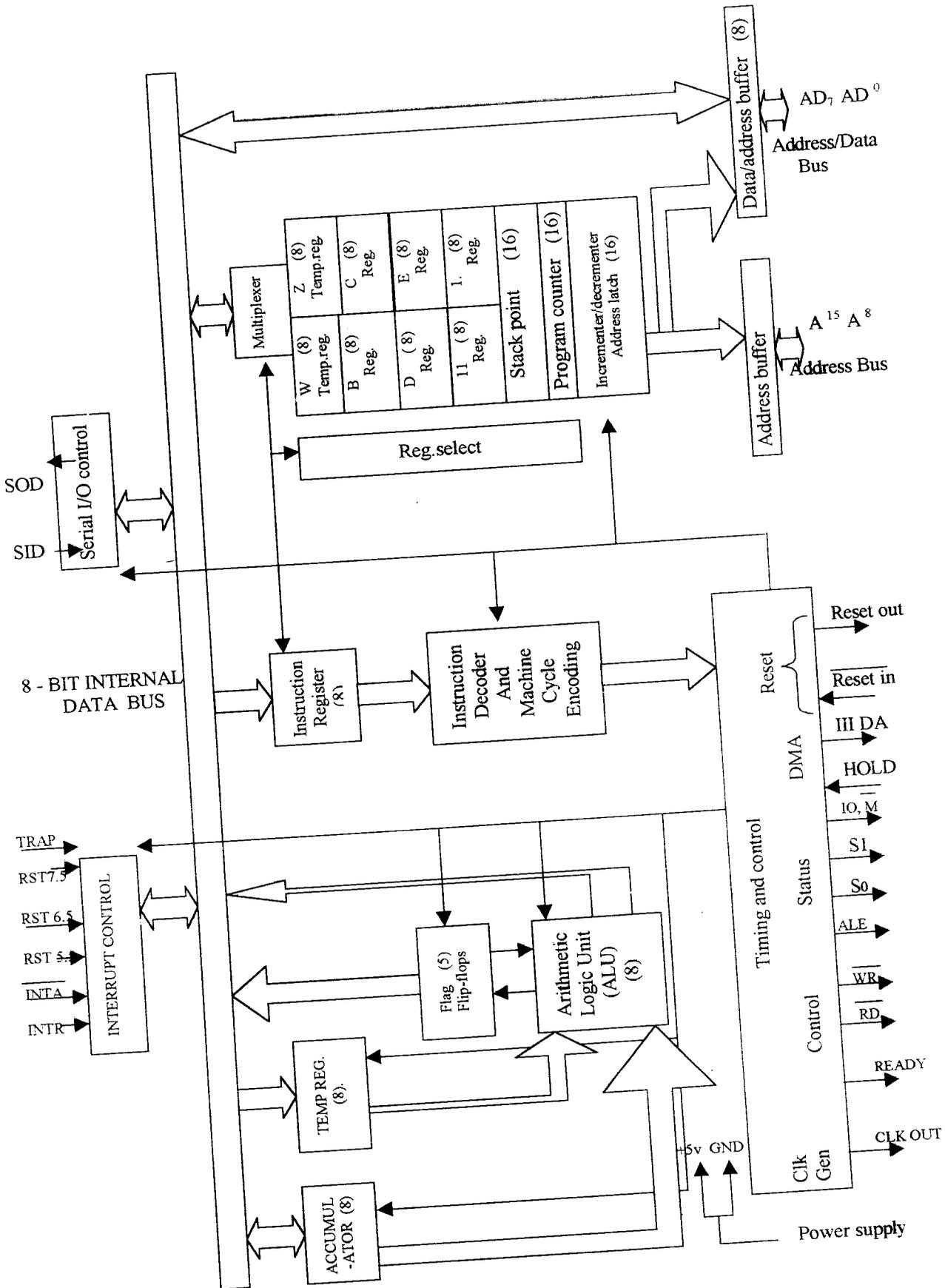


Fig 2.5 Functional block diagram of 8085

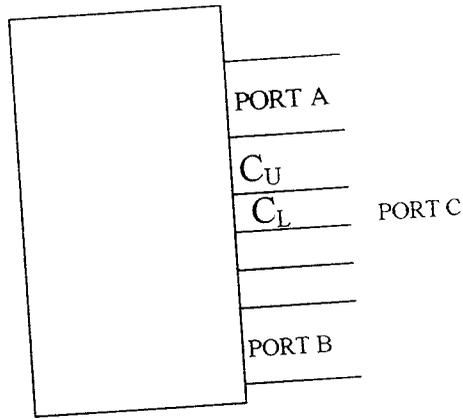
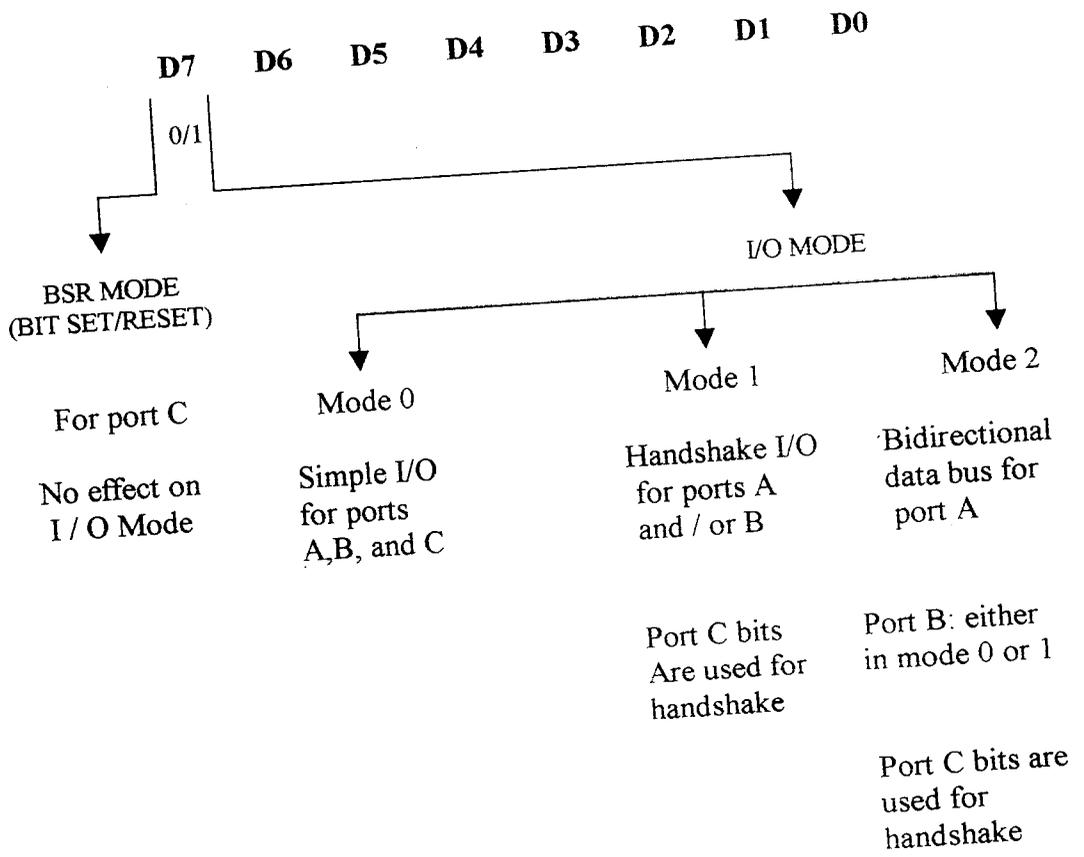
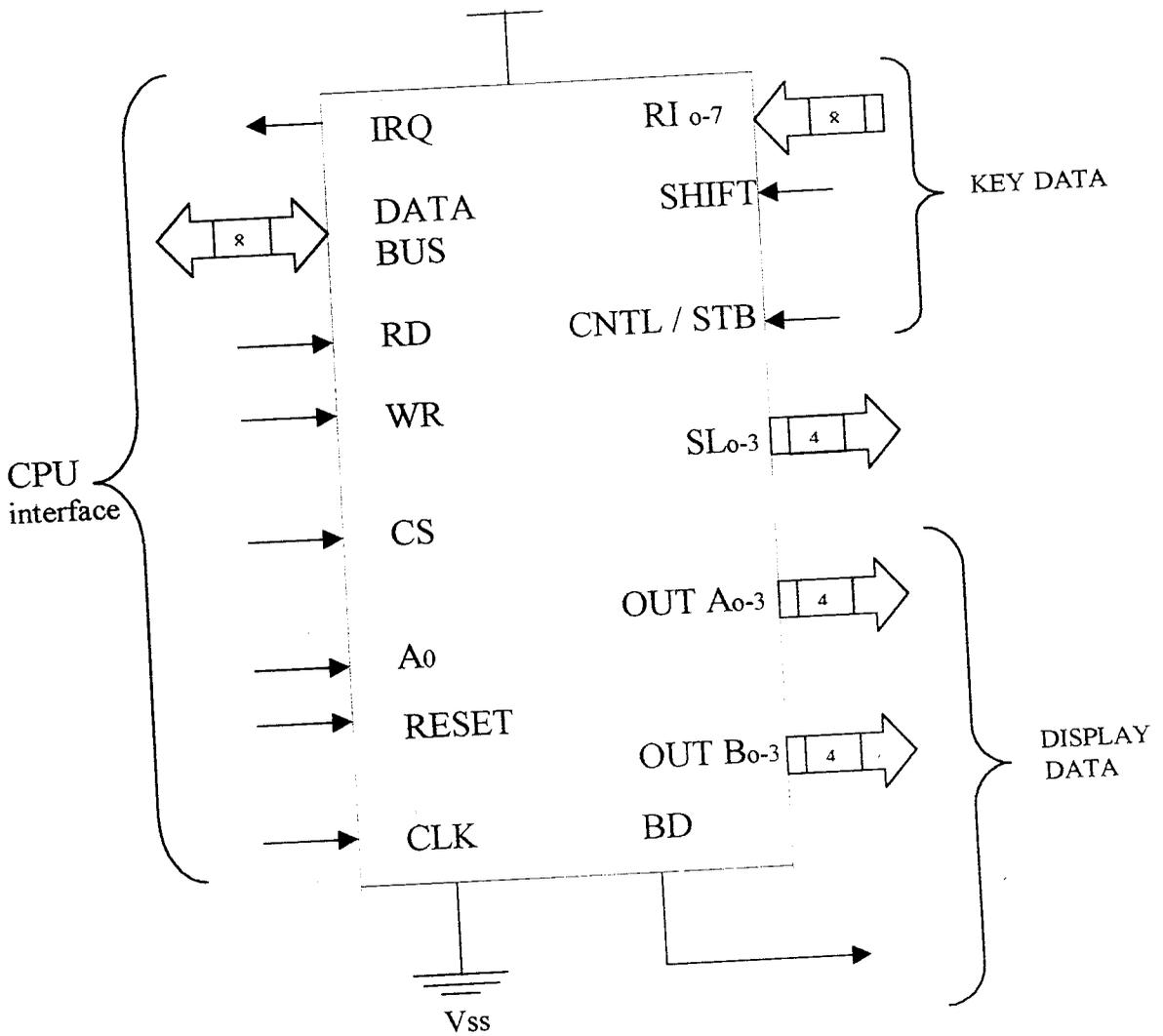


Fig 2.7 (a) ports



2.7(b) MODES



2.6 LOGIC SYMBOL OF 8279

in Configuration

1	CS	6	PA ₄	10	8255A	16	PC ₂	22	PB ₄	28	D ₆	34	D ₀	40	PA ₄
2	GND	7	PA ₅	11	PC ₇	17	PC ₃	23	PB ₅	29	D ₅	35	D ₁	39	PA ₅
3	A ₁	8	PA ₆	12	PC ₆	18	PC ₄	24	PB ₆	30	D ₄	36	D ₂	38	PA ₆
4	A ₀	9	PA ₇	13	PC ₅	19	PB ₀	25	PB ₇	31	D ₃	37	D ₃	37	PA ₇
5	WR	10	WR	14	PC ₄	20	PB ₁	26	V _{CC}	32	D ₂	38	D ₄	38	PA ₇
6	RESET	11	RESET	15	PC ₀	21	PB ₂	27	PB ₇	33	D ₁	39	D ₅	39	PA ₇
7	D _{7-D₀}	12	D _{7-D₀}	16	PC ₁	22	PB ₃	28	PB ₆	34	D ₀	40	D ₆	40	PA ₇
8	A ₁	13	A ₁	17	PC ₂	23	PB ₄	29	PB ₅	35	D ₁	35	D ₇	35	RESET
9	A ₀	14	A ₀	18	PC ₃	24	PB ₅	30	PB ₆	36	D ₂	36	D ₇	36	WR
10	PC ₇	15	PC ₇	19	PB ₀	25	PB ₇	31	PB ₇	37	D ₃	37	D ₇	37	WR
11	PC ₆	16	PC ₆	20	PB ₁	26	V _{CC}	32	V _{CC}	38	D ₄	38	D ₇	38	WR
12	PC ₅	17	PC ₅	21	PB ₂	27	PB ₇	33	V _{CC}	39	D ₅	39	D ₇	39	WR
13	PC ₄	18	PC ₄	22	PB ₃	28	PB ₆	34	V _{CC}	40	D ₆	40	D ₇	40	WR
14	PC ₀	19	PC ₀	23	PB ₄	29	PB ₅	35	V _{CC}	1	CS	1	RESET	1	RESET
15	PC ₁	20	PC ₁	24	PB ₅	30	PB ₆	36	V _{CC}	2	D _{7-D₀}	2	D ₀	2	D _{7-D₀}
16	PC ₂	21	PC ₂	25	PB ₇	31	PB ₇	37	V _{CC}	3	PA _{7-PA₀}	3	D ₁	3	PA _{7-PA₀}
17	PC ₃	22	PC ₃	26	V _{CC}	32	V _{CC}	38	V _{CC}	4	PC _{7-PC₀}	4	D ₂	4	PC _{7-PC₀}
18	PB ₀	23	PB ₀	27	PB ₇	33	V _{CC}	39	V _{CC}	5	WR	5	D ₃	5	WR
19	PB ₁	24	PB ₁	28	PB ₆	34	V _{CC}	40	V _{CC}	6	RESET	6	D ₄	6	RESET
20	PB ₂	25	PB ₂	29	PB ₅	35	V _{CC}	1	V _{CC}	7	D ₀	7	D ₅	7	D ₀
		26	V _{CC}	30	PB ₆	36	V _{CC}	2	V _{CC}	8	D ₁	8	D ₆	8	D ₁
		27	PB ₇	31	PB ₇	37	V _{CC}	3	V _{CC}	9	D ₂	9	D ₇	9	D ₂
		28	PB ₆	32	V _{CC}	38	V _{CC}	4	V _{CC}	10	D ₃	10	D ₇	10	D ₃
		29	PB ₅	33	V _{CC}	39	V _{CC}	5	V _{CC}	11	PC ₇	11	D ₇	11	PC ₇
		30	PB ₄	34	V _{CC}	40	V _{CC}	6	V _{CC}	12	PC ₆	12	D ₇	12	PC ₆
		31	PB ₃	35	V _{CC}	1	V _{CC}	7	V _{CC}	13	PC ₅	13	D ₇	13	PC ₅
		32	V _{CC}	36	V _{CC}	2	V _{CC}	8	V _{CC}	14	PC ₄	14	D ₇	14	PC ₄
		33	V _{CC}	37	V _{CC}	3	V _{CC}	9	V _{CC}	15	PC ₀	15	D ₇	15	PC ₀
		34	V _{CC}	38	V _{CC}	4	V _{CC}	10	V _{CC}	16	PC ₁	16	D ₇	16	PC ₁
		35	V _{CC}	39	V _{CC}	5	V _{CC}	11	V _{CC}	17	PC ₂	17	D ₇	17	PC ₂
		36	V _{CC}	40	V _{CC}	6	V _{CC}	12	V _{CC}	18	PC ₃	18	D ₇	18	PC ₃
		37	V _{CC}	1	V _{CC}	7	V _{CC}	13	V _{CC}	19	PB ₀	19	D ₇	19	PB ₀
		38	V _{CC}	2	V _{CC}	8	V _{CC}	14	V _{CC}	20	PB ₁	20	D ₇	20	PB ₁
		39	V _{CC}	3	V _{CC}	9	V _{CC}	15	V _{CC}						
		40	V _{CC}	4	V _{CC}	10	V _{CC}	16	V _{CC}						
				11	V _{CC}	11	V _{CC}	17	V _{CC}						
				12	V _{CC}	12	V _{CC}	18	V _{CC}						
				13	V _{CC}	13	V _{CC}	19	V _{CC}						
				14	V _{CC}	14	V _{CC}	20	V _{CC}						
				15	V _{CC}	15	V _{CC}								
				16	V _{CC}	16	V _{CC}								
				17	V _{CC}	17	V _{CC}								
				18	V _{CC}	18	V _{CC}								
				19	V _{CC}	19	V _{CC}								
				20	V _{CC}	20	V _{CC}								

Power Supplies
+5 V
GND

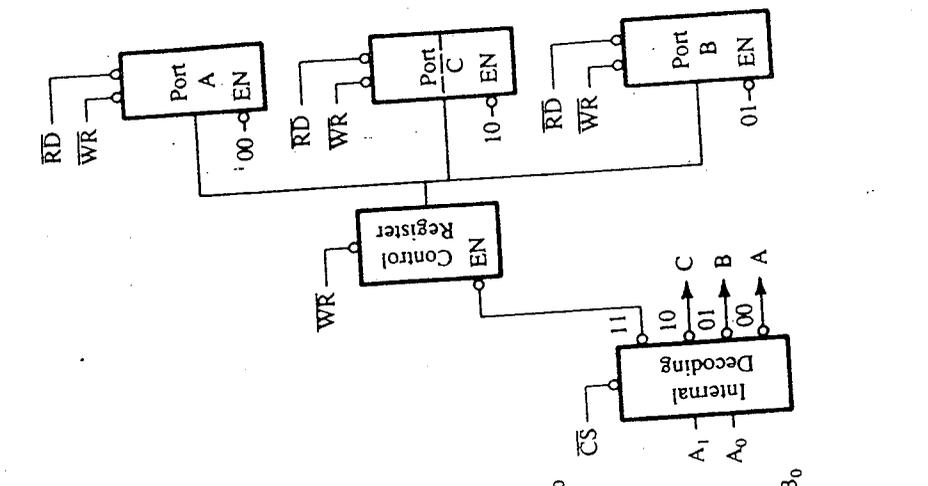
Bidirectional Data Bus
D_{7-D₀}

8-Bit Internal Data Bus

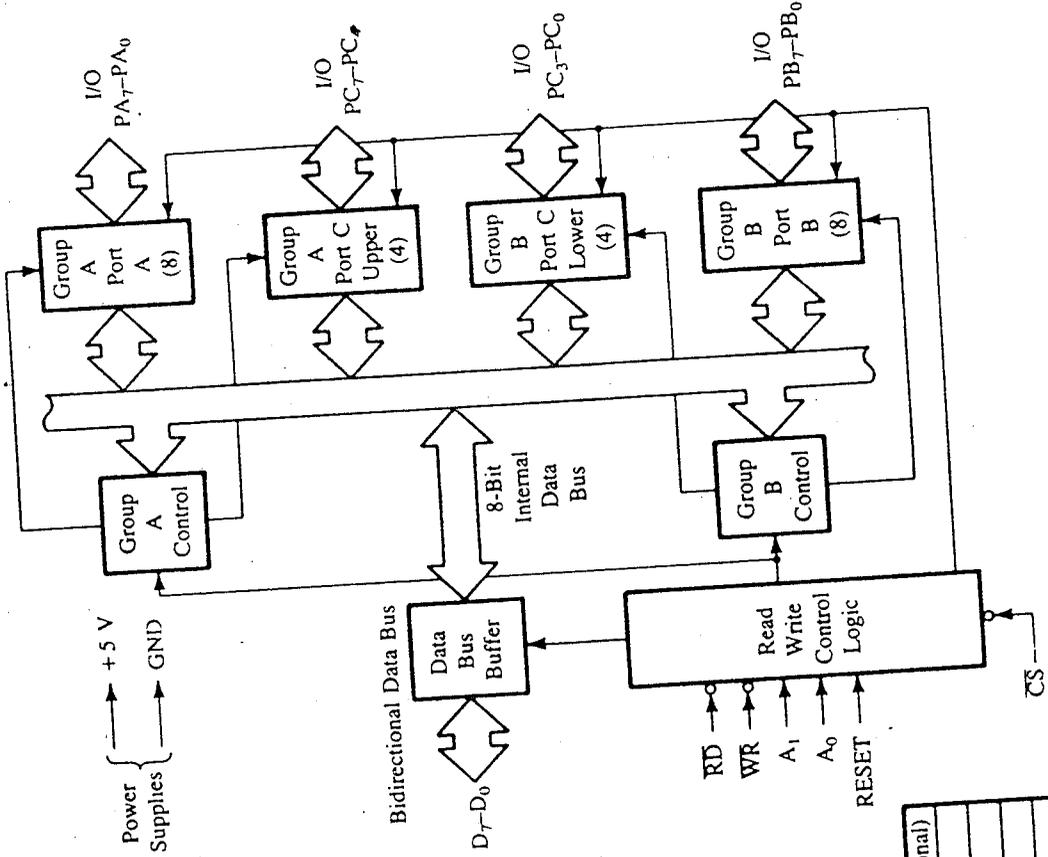
Read Write Control Logic
RD
WR
A₁
A₀
RESET

Pin Names

Pin Name	Function
D _{7-D₀}	Data Bus (Bidirectional)
RESET	Reset Input
CS	Chip Select
RD	Read Input
WR	Write Input
A ₀ , A ₁	Port Address
PA _{7-PA₀}	Port A (Bit)
PB _{7-PB₀}	Port B (Bit)
PC _{7-PC₀}	Port C (Bit)
V _{CC}	+5 Volts
GND	0 Volts

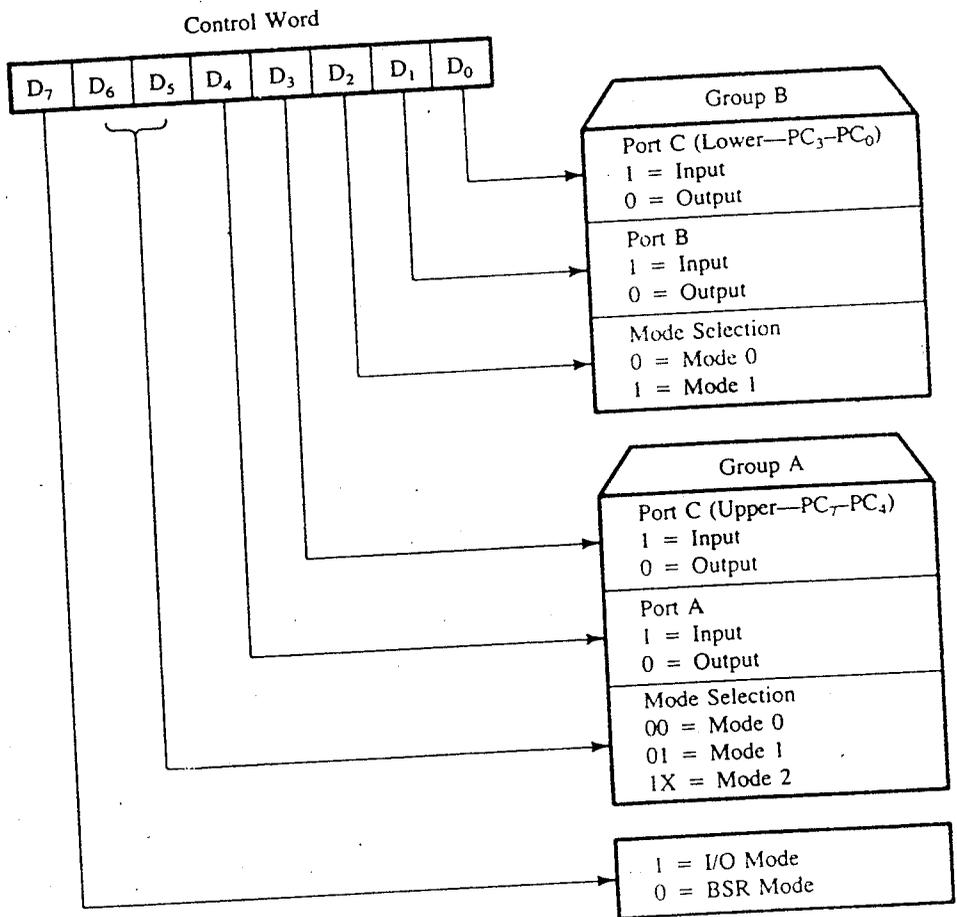


(b)



(a)



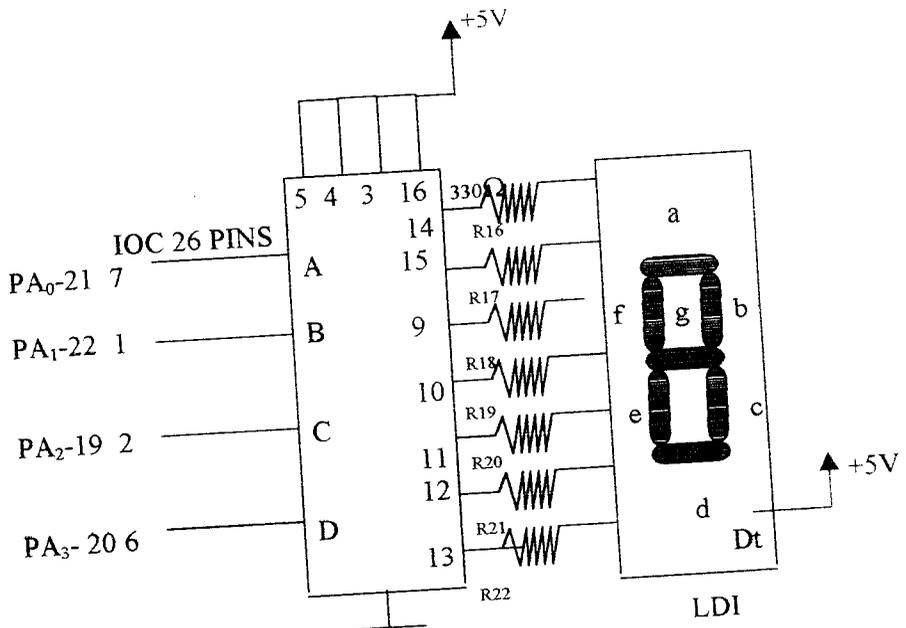


8255A Control Word Format for I/O Mode

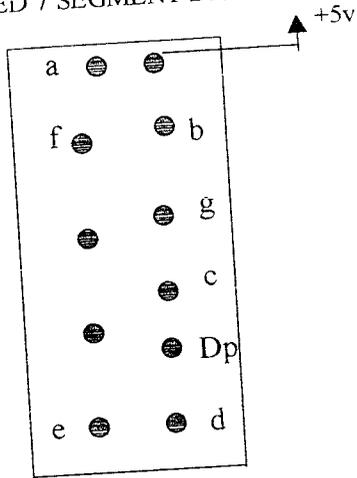
SOURCE: Adapted from Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), p. 3-104.

CON1
PIN PORT PIN

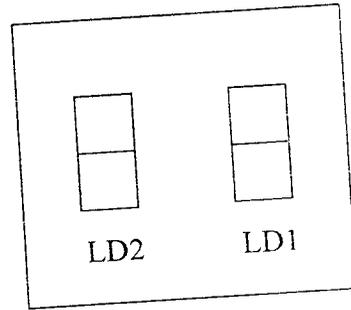
1	PC ₄	PC ₅	2
3	PC ₂	PC ₃	4
5	PC ₀	PC ₁	6
7	PB ₆	PB ₇	8
9	PB ₄	PB ₅	10
11	PB ₂	PB ₃	12
13	PB ₀	PB ₁	14
15	PA ₆	PB ₇	16
17	PA ₄	PA ₅	18
19	PA ₂	PA ₃	20
21	PA ₀	PA ₁	22
23	PC ₆	PC ₇	24
25	+5V	GND	26



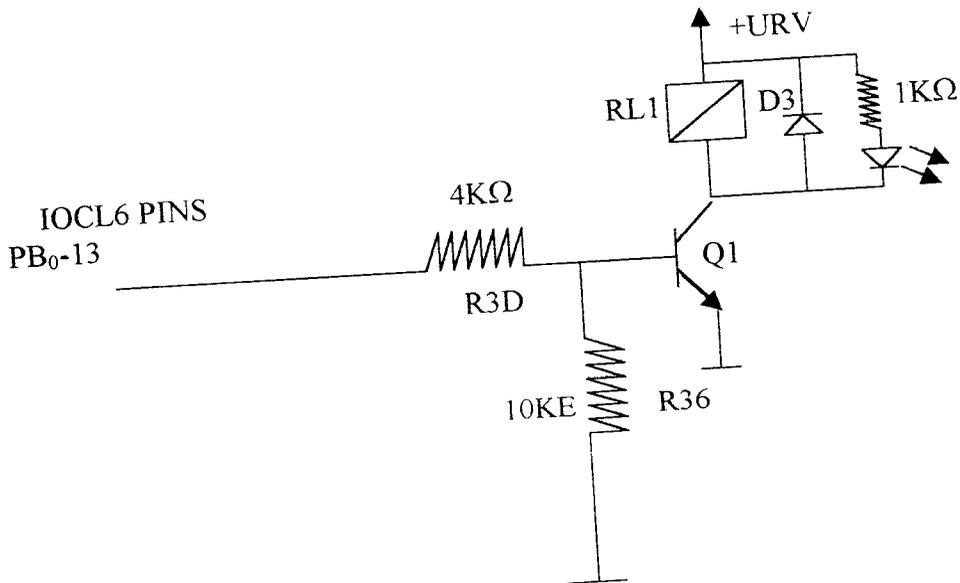
LED 7 SEGMENT DISPLAY



TOP VIEW



LED ARRANGEMENT



CHAPTER III

SOFTWARE

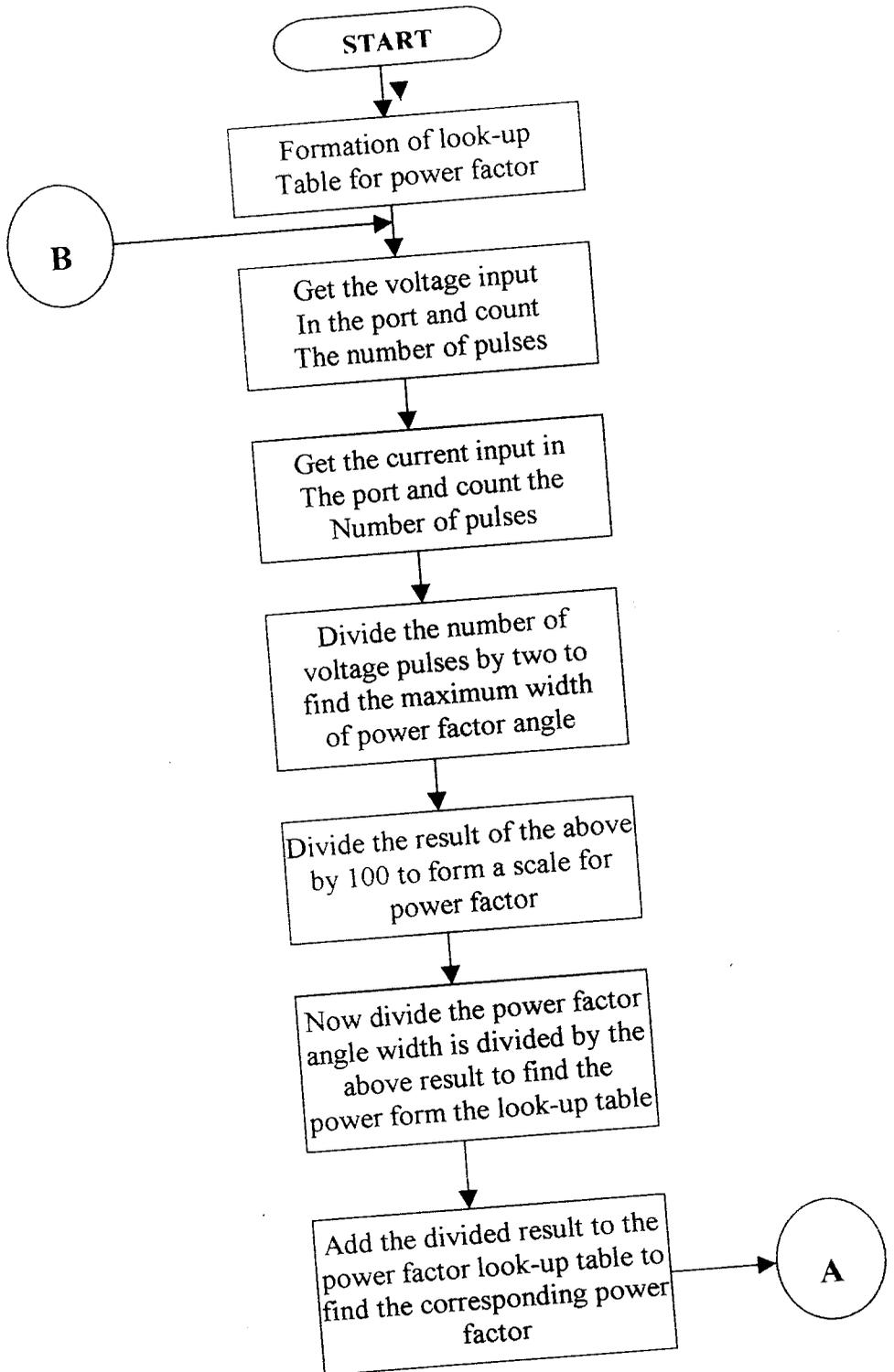
The software here is written in 8085 Assembly language and coded in the hexadecimal format into the microcomputer using the keyboard and monitor program.

The detailed steps involved are depicted in the flowchart as shown in Fig 3.1

3.1 Program:

The assembly language program developed for reactive power control is enclosed

FLOW CHART



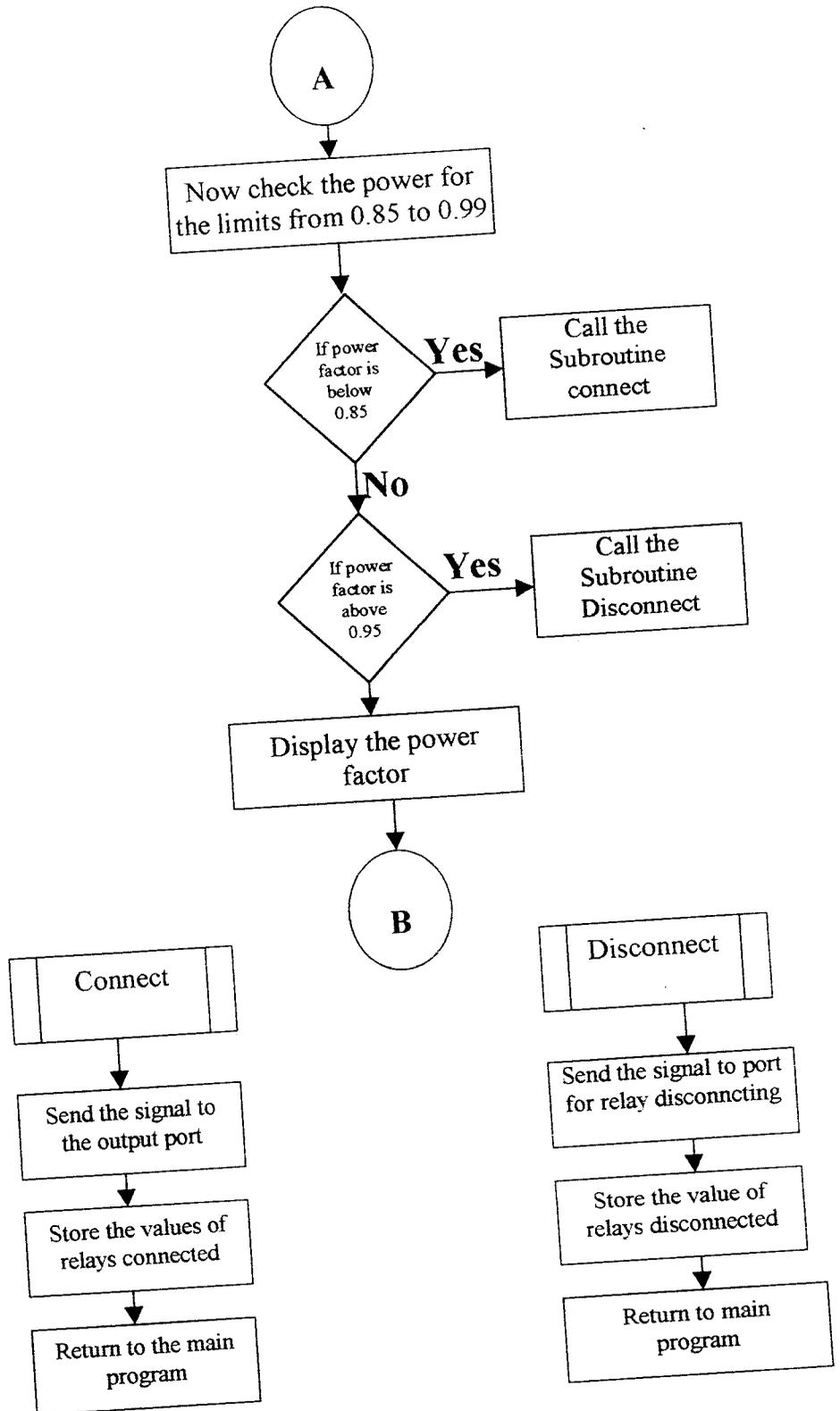


Fig 3.1 Flow Chart

ADDRESS	OPCODE	LABEL	MNEMONIC	OPERAND
8000	3E		MV1	A,89H
8001	89		OUT	03H
8002	D3			
8003	03		MVI	A,00H
8004	3E			
8005	00		STA	8700H
8006	32			
8007	00			
8008	87		STA	8702H
8009	32			
800A	02			
800B	87		LXI	H,9200H
800C	21			
800D	00			
800E	92		MVI	M,64H
800F	36			
8010	64		MOV	B,M
8011	46		INX	H,9200H
8012	23	LKTBL	DCR	B,M
8013	05		MOV	M,B
8014	70		JNZ	LKTBL
8015	C2			
8016	12			
8017	80	INPUTS	CALL	CLEAR
8018	CD			
8019	DD			
801A	80		LXI	H,9000H
801B	21			
801C	00			
801D	90		IN	02H
801E	DB	VINP		
801F	02			

ADDRESS	OPCODE	LABEL	MNEMONIC	OPERAND
8020	E6		ANI	04H
8021	04		JNZ	VINP
8022	C2			
8023	1E			
8024	80	VINP0	IN	02H
8025	DB			
8026	02		ANI	04H
8027	E6			
8028	04		JZ	VINP0
8031	CA			
802A	25			
802B	80	VINP1	INR	B
802C	04		MOV	A,B
802D	78		ADI	01H
802E	C6			
802F	01		JNC	NEXT
8030	D2			
8031	34			
8032	80		INR	C
8033	0C	NEXT	IN	02H
8034	DB			
8035	02		ANI	04H
8036	E6			
8037	04		JNZ	VINP1
8038	C2			
8039	2C			
803A	80		MOV	M,B
803B	70		INX	H
803C	23		MOV	M,C
803D	71		CALL	CLEAR
803E	CD			
803F	DD			

ADDRESS	OPCODE	LABEL	MNEMONIC	OPERAND
8040	80		LXI	H,9050H
8041	21			
8042	50			
8043	90		IN	02H
8044	DB	PFINP		
8045	02		ANI	10H
8046	E6			
8047	10		JNZ	PFINP
8048	C2			
8049	44			
804A	80		IN	02H
804B	DB	PFINP0		
804C	02		ANI	10H
804D	E6			
804E	10		JZ	PFINP0
804F	CA			
8050	4B			
8051	80		INR	B
8052	04	PFINP1	MOV	A,B
8053	78		ADI	01H
8054	C6			
8055	01		JNC	NXT
8056	D2			
8057	5A			
8058	80		INR	C
8059	0C		IN	02H
805A	DB	NXT		
805B	02		ANI	10H
805C	E6			
805D	10		JNZ	PFINP1
805E	C2			
805F	52			

ADDRESS	OPCODE	LABEL	MNEMONIC	OPERAND
8060	80		MOV	M,B
8061	70		INX	H
8062	23		MOV	M,C
8063	71		CALL	CLEAR
8064	CD			
8065	DD			
8066	80		MVI	C,02H
8067	0E			
8068	02		LHLD	9000H
8069	2A			
806A	00			
806B	90		CALL	DIV
806C	CD			
806D	E6			
806E	80		SHLD	9003H
806F	22			
8070	03			
8071	90		XCHG	
8072	EB		SHLD	9005H
8073	22			
8074	05			
8075	90		CALL	CLEAR
8076	CD			
8077	DD			
8078	80		MVI	C,64H
8079	0E			
807A	64		LHLD	9005H
807B	2A			
807C	05			
807D	90		CALL	DIV
807E	CD			
807F	E6			

ADDRESS	OPCODE	LABEL	MNEMONIC	OPERAND
8080	80		SHLD	9007H
8081	22			
8082	07			
8083	90		XCHG	
8084	EB		SHLD	9009H
8085	22			
8086	09			
8087	90		CALL	CLEAR
8088	CD			
8089	DD			
808A	80		LHLD	9009H
808B	2A			
808C	09			
808D	90		MOV	C,L
808E	4D		MOV	B,H
808F	44		LHLD	9050H
8090	2A			
8091	50			
8092	90		CALL	DIV
8093	CD			
8094	E6			
8095	80		SHLD	9010H
8096	22			
8097	10			
8098	90		XCHG	
8099	EB		SHLD	9012H
809A	22			
809B	12			
809C	90		CALL	CLEAR
809D	CD			
809E	DD			
809F	80			

ADDRESS	OPCODE	LABEL	MNEMONIC	OPERAND
			LHLD	9012H
80A0	2A			
80A1	12			
80A2	90		MOV	C,L
80A3	4D		MOV	B,H
80A4	44		LXI	H,9200H
80A5	21			
80A6	02			
80A7	92		MOV	A,L
80A8	7D		ADD	C
80A9	81		MOV	L,A
80AA	6F		MOV	A,H
80AB	7C		ADC	B
80AC	88		MOV	H,A
80AD	67		MOV	A,M
80AE	7E		STA	8500H
80AF	32			
80B0	00			
80B1	85		CALL	CLEAR
80B2	CD			
80B3	DD			
80B4	80		CALL	BCDWNV
80B5	CD			
80B6	FE			
80B7	80		LDA	8500H
80B8	3A			
80B9	00			
80BA	85		MVI	B,5AH
80BB	06			
80BC	5A		CMP	B
80BD	B8		JC	CONNECT
80BE	DA			
80BF	2F			

ADDRESS	OPCODE	LABEL	MNEMONIC	OPERAND
80C0	81		JNC	OPER
80C1	D2			
80C2	CA			
80C3	80		CZ	BCCONV
80C4	CC			
80C5	FE			
80C6	80		JMP	END
80C7	C3			
80C8	DA			
80C9	80			
80CA	CD	OPER	CALL	BCDCONV
80CB	FE			
80CC	80		NOP	
80CD	00		MVI	C,63H
80CE	0E			
80CF	63		LDA	8500H
80D0	3A			
80D1	00			
80D2	85		CMP	C
80D3	B9		CNC	DISCONNECT
80D4	D4			
80D5	5E			
80D6	81		CALL	BCDCONV
80D7	CD			
80D8	FE			
80D9	80		JMP	INPUTS
80DA	C3	END		
80DB	18			
80DC	80		MVI	A,00H
80DD	3E	CLEAR		
80DE	00		MVI	B,00H
80DF	06			

ADDRESS	OPCODE	LABEL	MNEMONIC	OPERAND
80E0	00		MVI	C,OOH
80E1	0E			
80E2	00		MVI	D,OOH
80E3	16			
80E4	00		RET	
80E5	C9		MVI	D,OOH
80E6	16	DIV		
80E7	00		MVI	E,OOH
80E8	1E			
80E9	00		MOV	A,L
80EA	7D	LOCO	SUB	C
80EB	91		MOV	L,A
80EC	6F		MOV	A,H
80ED	7C		SBB	B
80EE	98		MOV	H,A
80EF	67		JC	LOCI
80F0	DA			
80F1	F7			
80F2	80		INX	D
80F3	13		JMP	LOCO
80F4	C3			
80F5	EA			
80F6	80		MOV	A,L
80F7	7D	LOCI	ADD	C
80F8	81		MOV	L,A
80F9	6F		MOV	A,H
80FA	7C		ADC	B
80FB	88		MOV	H,A
80FC	67		RET	
80FD	C9		LDA	8500H
80FE	3A	BCDCONV		
80FF	00			

ADDRESS	OPCODE	LABEL	MNEMONIC	OPERAND
8100	85			
8101	CD		CALL	PWRTEN
8102	08			
8103	81			
8104	CD		CALL	DISPLAY
8105	21			
8106	81			
8107	C9		RET	
8108	21	PWRTEN	LXI	H,8600H
8109	00			
810A	86			
810B	06		MVI	B,64H
810C	64			
810D	CD		CALL	BINBCD
810E	17			
810F	81			
8110	06		MVI	B,0AH
8111	0A			
8112	CD		CALL	BINBCD
8113	17			
8114	81			
8115	77		MOV	M,A
8116	C9		RET	
8117	36	BINBCD	MVI	M,FFH
8118	FF			
8119	34	NXTBUF	INR	M
811A	90		SUB	B
811B	D2		JNC	NXTBUF
811C	19			
811D	81			
811E	80		ADD	B
811F	23		INX	H

ADDRESS	OPCODE	LABEL	MNEMONIC	OPERAND
8120	C9		RET	
8121	21	DISPLAY	LXI	H,8602H
8122	02			
8123	86			
8124	3A		LDA	8601H
8125	01			
8126	86			
8127	07		RLC	
8128	07		RLC	
8129	07		RLC	
812A	07		RLC	
812A	07		ADD	M
812B	86		OUT	OOH
812C	D3			
812D	00			
812E	C9		RET	
812E	C9		CALL	BCDCONV
812F	CD	CONNECT		
8130	FE			
8131	80			
8131	80		LDA	8700H
8132	3A			
8133	00			
8134	87			
8134	87		MOV	D,A
8135	57			
8135	57		CALL	MUL
8136	CD			
8137	47			
8138	81			
8138	81		ADD	D
8139	82			
8139	82		STA	8700H
813A	32			
813B	00			
813C	87			
813C	87		OUT	01H
813D	D3			
813E	01			
813E	01		MVI	D,IEH
813F	16			

ADDRESS	OPCODE	LABEL	MNEMONIC	OPERAND
8140	IE		CALL	DELAY
8141	CD			
8142	8C			
8143	81		JMP	END
8144	C3			
8145	DA			
8146	80		LDA	8702H
8147	3A	MUL		
8148	02			
8149	87		MOV	B,A
814A	47		MVI	A,00H
814B	3E			
814C	00		MVI	C,02H
814D	0E			
814E	02			
814F	80	REPEAT	ADD	B
8150	0D		DCR	C
8151	C2		JNZ	REPEAT
8152	4F			
8153	81		CPI	00H
8154	FE			
8155	00		JNZ	STORE
8156	C2			
8157	5A			
8158	81		INR	A
8159	3C		STA	8702
815A	32	STORE		
815B	02			
815C	87		RET	
815D	C9		CALL	BCDCONV
815E	CD	DISCONNECT		
815F	FE			

ADDRESS	OPCODE	LABEL	MNEMONIC	OPERAND
8160	80		LDA	8702H
8161	3A			
8162	02			
8163	87		MOV	B,A
8164	47		LDA	8700H
8165	3A			
8166	00			
8167	87		SUB	B
8168	90		STA	8700H
8169	32			
816A	00			
816B	87		OUT	01H
816C	D3			
816D	01		MVI	D,96H
816E	16			
816F	96		CALL	DELAY
8170	CD			
8171	8C			
8172	81		CALL	DIVD
8173	CD			
8174	77			
8175	81		RET	
8176	C9		LDA	8702H
8177	3A	DIVD		
8178	02			
8179	87		MVI	B,00H
817A	06			
817B	00		MVI	C,02H
817C	0E			
817D	02		SUB	C,02H
817E	91	LOOP1	JC	LOC3
817F	DA			

ADDRESS	OPCODE	LABEL	MNEMONIC	OPERAND
8180	86			
8181	81		INR	B
8182	04		JMP	LOOP1
8183	C3			
8184	7E			
8185	81			
8186	89	LOC3	ADC	C
8187	78		MOV	A,B
8188	32		STA	8702H
8189	02			
818A	87			
818B	C9		RET	
818C	CD	DELAY	CALL	COUNT
818D	97			
818E	81			
818F	CD		CALL	COUNT
8190	97			
8191	81			
8192	15		DCR	D
8193	C2		JNZ	DELAY
8194	8C			
8195	81			
8196	C9		RET	
8197	21	COUNT	LXI	H,FFFFH
8198	FF			
8199	FF			
819A	2B	NXTC	DCX	H
819B	7D		MOV	A,L
819C	B4		ORA	H
819D	C2		JNZ	NXTC
819E	9A			
819F	81			
81A0	C9		RET	

CHAPTER IV

TEST RESULTS :-

- 1) The input waveforms to the EXOR gate is shown in fig 4.1
- 2) The voltage waveform and current waveform are fed to the EX-OR gate
- 3) The voltage & current waveform used for phase angle measurement shown in fig.2
- 4) The microcomputer unit gets the input and displays the power factor as 0.63
- 5) Then relay is turned on and the display waits for 30 sec and the next instant power factor is measured
- 6) The 5 KVAR capacitor bank connected to the 1st relay is turned on
- 7) The power factor is raised to 0.71, then again the next relay is turned on
- 8) Another 5KVAR added increases p.f. to 0.83, then the next relay is turned on
- 9) Again 5KVAR added, increases p.f to 0.91 and then the display shows 0.91
- 10) Now the relay remains as it is and no more further addition of capacitor banks is done

CHAPTER V

CONCLUSION

The reactive power regulator has been designed, fabricated and tested on the induction motors load and its operation is found to be satisfactory. In practice, the L.T consumers use manual switching and may lead to loss in energy.

With the adaption of microprocessors to the control of the reactive power, a new generation of regulators are developed with high performance.

The advantage of regulator over manual switching systems is that,

1. Automatic switching using complex logical decisioning.
2. Time delay for the disconnecting of capacitors banks is inbuilt.
3. Errors in human readings can be avoided.
4. The display of power factor is instantaneous, and the corresponding value is displayed.

FURTHER DEVELOPMENTS:-

Further developments can be made on this product,

1. Necessary changes can be made in the program to display the No of capacitor banks connected.
2. The ratio of capacitors bank to be made 1:2:4 or 1:2:2 can also be developed.
3. Over voltage and under voltage indication.

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REFERENCES

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3. "PRI-85AD users manual", precitron , Coimbatore-28
4. "Intel Handbook of Microcontrollers", Intel cooperation,1985.
5. W.H.Gothmann, "Digital Electronics An introduction to theory and practice". Second edition, Prentice , U.S.A.
6. J.L.Hilburn and P.M.Julich, "Microcomputers / Microprocessors: Hardware, Software and Applications," Prentice-Hall, New Jersey.

7. Proceedings of FICCI seminar on "Energy savers 88", New Delhi, 1988.
8. Energy 2001, a report from advisory Board of Board of Energy, govt. of. India, S.P.Marg, New Delhi, 1987.
9. Mathur B.L. and Sangha C.S., "Electrical Power", New Asian Publisher, Nai Saruk, Delhi, 1970.
10. Mitch cotton , " The Transmission & Distribution of Electrical Energy", ELBS, London, 1962.

APPENDIX

PRI_85 AD SYSTEM HARDWARE

SPECIFICATIONS:

CPU : Intel 8085 with 246 instructions and 3.072 MHz maximum clock rate.

MEMORY:

PRI 85 AD has three sockets (U7,U8,U9) for accepting memory devices.

U7 and U9 are populated and U8 is not populated one. Populated devices in U7 and U9 and option for unpopulated socket are as follows.

Display :

6 – digit, 0.5 seven segment LED display

Keyboard :

32 Keys including hexadecimal digits 0 to F.

Device with socket no.	Address range	Type with capacity
27128 at U7	0000 – 3FFF	16 K EPROM
62256 at U9	8000 – FFFF	32 K RAM
2764 at U8	4000 – 5FFF (or) (6000 -7FFF)	8 K EPROM
6264 at U8	4000 – 5FFF (or) 6000 – 7 FFF	8 K EPROM
27128 AT V8	4000 – 7FFR	16K EPROM
62256 at V8	4000 – 7FFF	16 K RAM

54/7446A • 54/7447A 54LS/74LS47

BCD TO 7-SEGMENT DECODER/DRIVER

DESCRIPTION — The '46A, '47A and 'LS47 accept four lines of BCD (8421) input data, generate their complements internally and decode the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 40 mA (24 mA for the 'LS47) in the ON (LOW) state and withstand 15 V (30 V for the '46A) in the OFF (HIGH) state with a maximum leakage current of 250 μ A. Auxiliary inputs provide blanking, lamp test and cascadable zero-suppression functions. Also see the 'LS247 data sheet.

- OPEN-COLLECTOR OUTPUTS
- DRIVE INDICATOR SEGMENTS DIRECTLY
- CASCADABLE ZERO-SUPPRESSION CAPABILITY
- LAMP TEST INPUT

ORDERING CODE: See Section 9

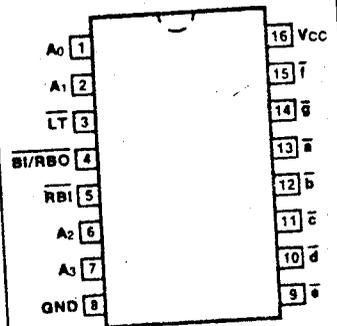
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = +5.0 V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP (P)	A	7446APC, 7447APC 74LS47PC		9B
Ceramic DIP (D)	A	7446ADC, 7447ADC 74LS47DC	5446ADM, 5447ADM 54LS47DM	7B
Flatpak (F)	A	7446AFC, 7447AFC 74LS47FC	5446AFM, 5447AFM 54LS47FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

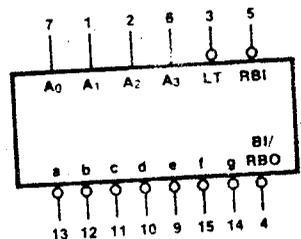
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	BCD Inputs	1.0/1.0	0.5/0.25
\overline{RBI}	Ripple Blanking Input (Active LOW)	1.0/1.0	0.5/0.25
LT	Lamp Test Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{BI/RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)	-/2.5	-/0.75
$\overline{a} - \overline{g}$	Segment Outputs (Active LOW)	5.0/5.0	1.25/2.0
		OC*/25	(1.0) OC*/15 (7.5)

*OC — Open Collector

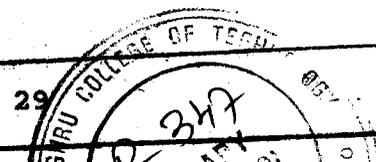
**CONNECTION DIAGRAM
PINOUT A**



LOGIC SYMBOL

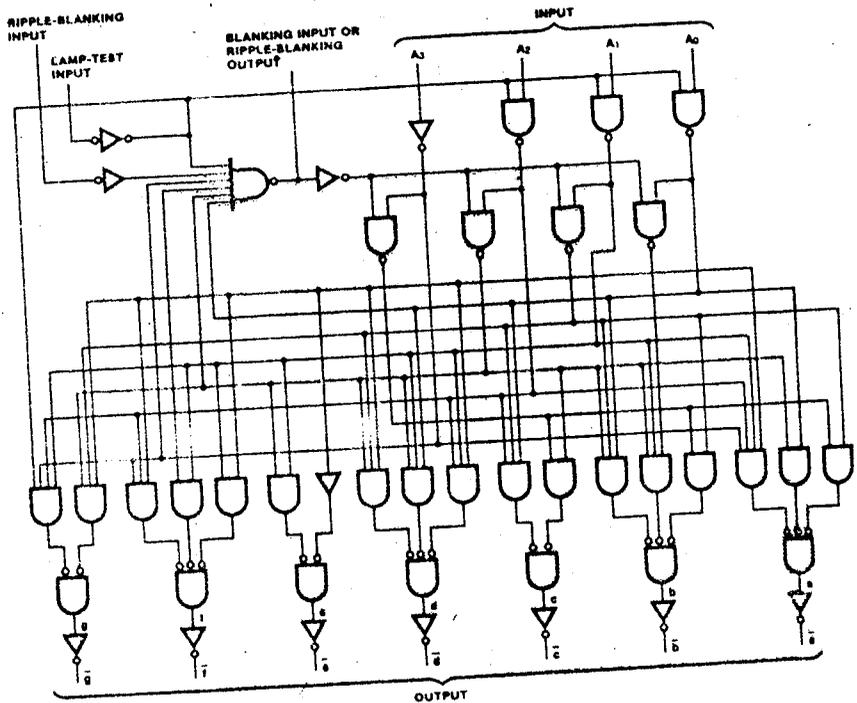


$V_{CC} = \text{Pin } 16$
 $GND = \text{Pin } 8$

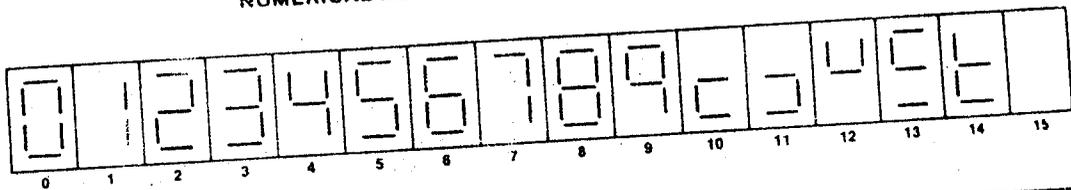


FUNCTIONAL DESCRIPTION — The '46A, '47A and 'LS47 decode the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the RBI blanks the display and causes a multidigit display. For example, by grounding the RBI of the highest order decoder and connecting its BI/RBO to RBI of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding RBI of the lowest order decoder and connecting its BI/RBO to RBI of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, i.e. by driving RBI of an intermediate decoder from an OR gate whose inputs are BI/RBO of the next highest and lowest order decoders. BI/RBO also serves as an unconditional blanking input. The internal NAND gate that generates the RBO signal has a resistive pull-up, as opposed to a totem pole, and thus BI/RBO can be forced LOW by external means, using wired-collector logic. A LOW signal thus applied to BI/RBO turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to LT turns on all segment outputs, provided that BI/RBO is not forced LOW.

LOGIC DIAGRAM



NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS



TRUTH TABLE

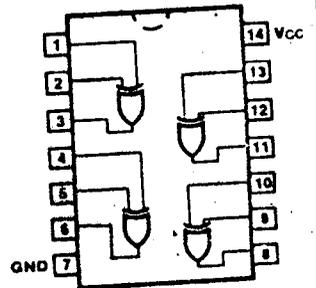
DECIMAL OR FUNCTION	INPUTS						OUTPUTS							NOTE
	$\overline{\text{LT}}$	$\overline{\text{RBI}}$	A ₃	A ₂	A ₁	A ₀	$\overline{\text{BI/RBO}}$	$\overline{\text{a}}$	$\overline{\text{b}}$	$\overline{\text{c}}$	$\overline{\text{d}}$	$\overline{\text{e}}$	$\overline{\text{f}}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H
1	H	X	L	L	L	L	H	L	L	L	L	L	L	L
2	H	X	L	L	L	H	L	L	L	L	L	L	L	L
3	H	X	L	L	L	H	H	L	L	L	L	L	L	L
4	H	X	L	L	H	L	L	L	L	L	L	L	L	L
5	H	X	L	L	H	L	H	L	L	L	L	L	L	L
6	H	X	L	L	H	H	L	L	L	L	L	L	L	L
7	H	X	L	L	H	H	H	L	L	L	L	L	L	L
8	H	X	L	L	H	L	L	L	L	L	L	L	L	L
9	H	X	L	L	H	L	H	L	L	L	L	L	L	L
10	H	X	L	L	H	H	L	L	L	L	L	L	L	L
11	H	X	L	L	H	H	H	L	L	L	L	L	L	L
12	H	X	L	L	H	L	L	L	L	L	L	L	L	L
13	H	X	L	L	H	H	L	L	L	L	L	L	L	L
14	H	X	L	L	H	H	L	L	L	L	L	L	L	L
15	H	X	L	L	H	H	H	L	L	L	L	L	L	L
$\overline{\text{BI}}$	X	X	L	L	X	X	L	L	L	L	L	L	L	L
$\overline{\text{RBI}}$	L	L	L	L	L	L	L	L	L	L	L	L	L	L
$\overline{\text{LT}}$	L	X	X	X	X	X	L	L	L	L	L	L	L	L

NOTES:

- (1) $\overline{\text{BI/RBO}}$ is wire-AND logic serving as blanking input ($\overline{\text{BI}}$) and/or ripple-blanking output ($\overline{\text{RBO}}$). The blanking out ($\overline{\text{BI}}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{\text{RBI}}$) must be open or at a HIGH level if blanking or a decimal 0 is not desired. X = input may be HIGH or LOW.
- (2) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.
- (3) When ripple-blanking input ($\overline{\text{RBI}}$) and inputs A₀, A₁, A₂ and A₃ are (L)W level, with the lamp test input at (HIGH) level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{\text{RBO}}$) goes to a LOW level (response condition).
- (4) When the blanking input/ripple-blanking output ($\overline{\text{BI/RBO}}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

54/7486
54S/74S86
54LS/74LS86
 QUAD 2-INPUT EXCLUSIVE-OR GATE

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	7486PC, 74S86PC 74LS86PC		9A
Ceramic DIP (D)	A	7486DC, 74S86DC 74LS86DC	5486DM, 54S86DM 54LS86DM	6A
Flatpak (F)	A	7486FC, 74S86FC 74LS86FC	5486FM, 54S86FM 54LS86FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.0/0.375
Outputs	20/10	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I _{CC}	Power Supply Current	XM	43		75		10	mA	V _{CC} = Max, V _{IN} = Gnd
		XC	50		75		10		
t _{PLH} t _{PHL}	Propagation Delay		23 17	3.5 3.0	10.5 10		12 17	ns	Other Input LOW Figs. 3-1, 3-5
t _{PLH} t _{PHL}			30 22	3.5 3.0	10.5 10		13 12		

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54/7489 54LS/74LS89

64-BIT RANDOM ACCESS MEMORY (With Open-Collector Outputs)

DESCRIPTION — The '89 is a high speed, low power 64-bit Random Access Memory organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the off (HIGH) state when both the Chip Select (\overline{CS}) and Write Enable (\overline{WE}) are HIGH. For all other combinations of \overline{CS} and \overline{WE} the outputs are active, presenting the complement of the stored data (READ mode) or the information present on the D inputs.

- OPEN-COLLECTOR OUTPUTS FOR WIRED-AND APPLICATIONS
- BUFFERED INPUTS MINIMIZE LOADING
- ADDRESS DECODING ON-CHIP
- DIODE CLAMPED INPUTS MINIMIZE RINGING

ORDERING CODE: See Section 9

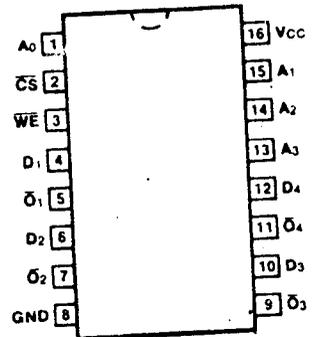
PKG'S	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0 \text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	7489PC, 74LS89PC		9B
Ceramic DIP (D)	A	7489DC, 74LS89DC	5489DM, 54LS89DM	7B
Flatpak (F)	A	7489FC, 74LS89FC	5489FM, 54LS89FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

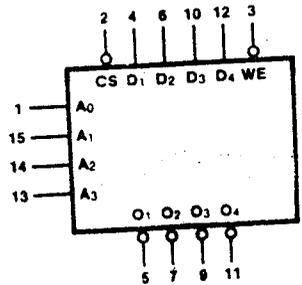
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	1.0/1.0	0.5/0.013
\overline{CS}	Chip Select Input (Active LOW)	1.0/1.0	0.5/0.013
\overline{WE}	Write Enable Input (Active LOW)	1.0/1.0	0.5/0.013
$D_1 - D_4$	Data Inputs	1.0/1.0	0.5/0.013
$\overline{O}_1 - \overline{O}_4$	Inverted Data Outputs	OC*/7.5	OC*/10 (5.0)

*OC — Open Collector

**CONNECTION DIAGRAM
PINOUT A**



LOGIC SYMBOL



$V_{CC} = \text{Pin 16}$
 $GND = \text{Pin 8}$

LM139/LM239/LM339/LM139A/LM239A/LM339A/LM2901/LM3302



LM139/LM239/LM339/LM139A/LM239A/LM339A/LM2901/LM3302 Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic—where the low power drain of the LM339 is a distinct advantage over standard comparators.

Advantages

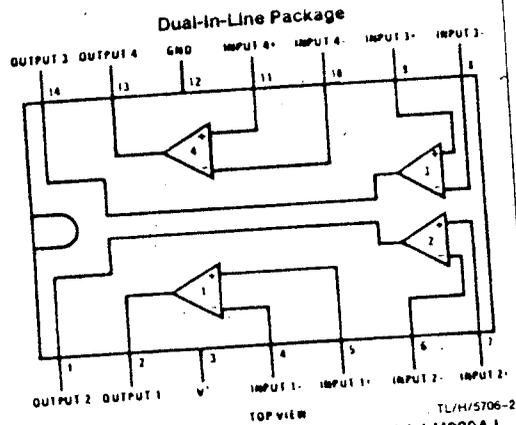
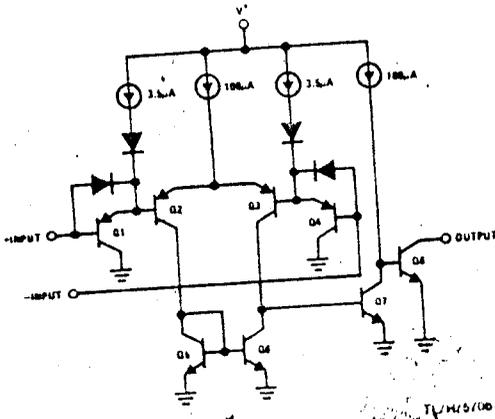
- High precision comparators
- Reduced V_{OS} drift over temperature

- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Wide single supply voltage range of dual supplies
 - LM139 series, 2 V_{DC} to 36 V_{DC} or ±1 V_{DC} to ±18 V_{DC}
 - LM139A series, LM2901 2 V_{DC} to 28 V_{DC}
 - LM3302 or ±1 V_{DC} to ±14 V_{DC}
- Very low supply current drain (0.8 mA) — independent of supply voltage
- Low input biasing current 25 nA
- Low input offset current ±5 nA
- Low input offset voltage and offset voltage ±3 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams



Order Number LM139J, LM139AJ, LM239J, LM239AJ, LM339J, LM339AJ, LM2901J or LM3302J
 See NS Package Number J14A
 Order Number LM339AM, LM339M or LM2901M
 See NS Package Number M14A
 Order Number LM339N, LM339AN, LM2901N or LM3302N
 See NS Package Number N14A

Absolute Maximum Ratings if Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 10)

LM139/LM239/LM339 LM3302 LM139A/LM239A/LM339A LM2901
 LM139/LM239/LM339 LM3302 LM139A/LM239A/LM339A LM2901
 -40°C to +85°C

Supply Voltage, V^+ 28 VDC or ± 14 VDC Operating Temperature Range
 LM339/LM339A 0°C to +70°C
 LM239/LM239A -25°C to +85°C
 LM2901 -40°C to +85°C
 LM139/LM139A -55°C to +125°C

Differential Input Voltage (Note 8) 36 VDC or ± 18 VDC
 28 VDC
 0.3 VDC to ± 28 VDC
 0.3 VDC to ± 36 VDC
 50 mA
 1050 mW
 1190 mW
 760 mW

Input Voltage Input Current ($V_{IN} < \pm 0.3$ VDC) 50 mA
 (Note 3)
 Power Dissipation (Note 1) 1050 mW
 Molded DIP 1190 mW
 Cavity DIP 760 mW
 Small Outline Package
 Output Short-Circuit to GND, Continuous
 (Note 2) -65°C to +150°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature 260°C
 (Soldering, 10 seconds)

Output Current (Note 4) 50 mA
 1050 mW
 1190 mW
 760 mW
 Continuous
 -65°C to +150°C
 260°C

Input Offset Voltage (Note 9) $I_{IN(+)} - I_{IN(-)}$ with Output in Linear Range, (Note 5), $V_{CM} = 0V$
 Input Bias Current $I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$
 Input Offset Current $I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$
 Input Common-Mode Voltage Range $V^+ = 30$ VDC (LM3302, $V^+ = 28$ VDC) (Note 6)
 Supply Current $R_L = \infty$, $V^+ = 36V$, (LM3302, $V^+ = 28$ VDC)
 Voltage Gain $R_L \geq 15$ k Ω , $V^+ = 15$ VDC
 $V_O = 1$ VDC to 11 VDC

Large Signal Response Time V_{IN} = TTL Logic Swing, $V_{REF} = 1.4$ VDC, $V_{RL} = 5$ VDC, $R_L = 5.1$ k Ω ,
 Response Time $V_{RL} = 5$ VDC, $R_L = 5.1$ k Ω , (Note 7)
 Output Sink Current $V_{IN(-)} = 1$ VDC, $V_{IN(+)} = 0$,
 $V_O \leq 1.5$ VDC

Parameter	Conditions	LM139A		LM239A, LM339A		LM139		LM239, LM339		LM2901		LM3302		Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 9)	$I_{IN(+)} - I_{IN(-)}$ with Output in Linear Range, (Note 5), $V_{CM} = 0V$	0	± 3.0	± 2.5	± 5.0	± 5.0	± 3.0	± 2.5	± 5.0	± 5.0	± 2.0	± 3	± 20	mVDC
Input Bias Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$	± 1.0	± 2.0	± 1.0	± 2.0	± 2.0	± 2.0	± 5.0	± 2.0	± 2.0	± 2.0	± 3	± 20	mVDC
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$	25	100	25	250	25	100	25	250	25	250	25	500	nADC
Input Common-Mode Voltage Range	$V^+ = 30$ VDC (LM3302, $V^+ = 28$ VDC) (Note 6)	± 3.0	± 2.5	± 5.0	± 5.0	± 3.0	± 2.5	± 5.0	± 5.0	± 5.0	± 5.0	± 3	± 100	μ ADC
Supply Current	$R_L = \infty$, $V^+ = 36V$, (LM3302, $V^+ = 28$ VDC)	50	200	50	200	50	200	50	200	25	100	2	30	V/mV
Voltage Gain	$R_L \geq 15$ k Ω , $V^+ = 15$ VDC $V_O = 1$ VDC to 11 VDC	300	300	300	300	300	300	300	300	300	300	300	300	ns
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4$ VDC, $V_{RL} = 5$ VDC, $R_L = 5.1$ k Ω ,	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	μ s
Response Time	$V_{RL} = 5$ VDC, $R_L = 5.1$ k Ω , (Note 7)	6.0	16	8.0	16	6.0	16	6.0	16	6.0	16	6.0	16	mADC
Output Sink Current	$V_{IN(-)} = 1$ VDC, $V_{IN(+)} = 0$, $V_O \leq 1.5$ VDC	6.0	16	8.0	16	6.0	16	6.0	16	6.0	16	6.0	16	mADC

LM139/LM239/LM339/LM139A/LM239A/LM339A/LM2901/LM3302

LM139/LM239/LM339/LM139A/LM239A/LM339A/LM2901/LM3302

Electrical Characteristics (V⁺ = 5 VDC, I_A = 25°C, unless otherwise stated) (Continued)

Parameter	Conditions	LM139A		LM239A, LM339A		LM139		LM239, LM339		LM2901		LM3302		Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Saturation Voltage	V _{IN(+)} = 1 VDC, V _{IN(+)} = 0, I _{SINK} ≤ 4 mA	250	400	250	400	250	400	250	400	250	400	250	500	mVDC
Output Leakage Current	V _{IN(+)} = 1 VDC, V _{IN(-)} = 0, V _O = 5 VDC	0.1		0.1		0.1		0.1		0.1		0.1		nADC

Electrical Characteristics (V⁺ = 5.0 VDC, Note 4)

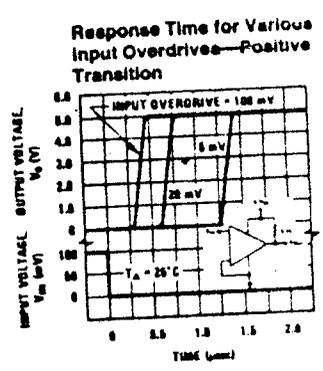
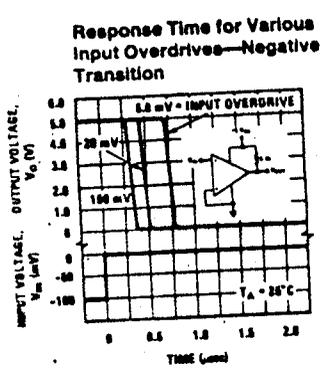
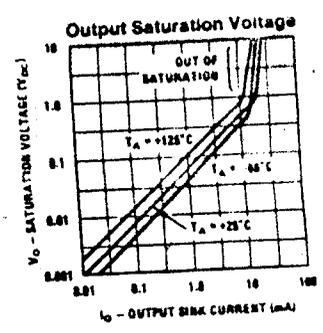
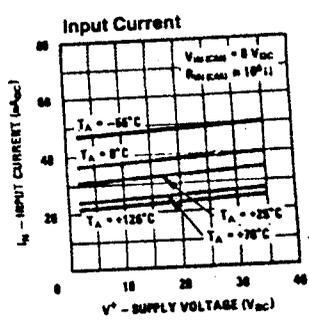
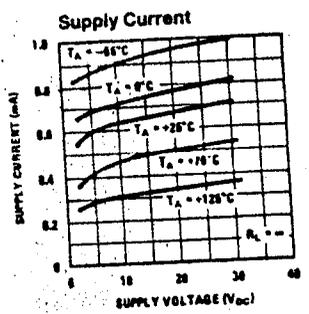
Parameter	Conditions	LM139A		LM239A, LM339A		LM139		LM239, LM339		LM2901		LM3302		Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)		± 4.0		± 4.0		± 9.0		± 9.0		± 9		± 15	mVDC
Input Offset Current	I _{IN(+)} - I _{IN(-)} , V _{CM} = 0V		± 100		± 150		± 100		± 150		± 50		± 200	nADC
Input Bias Current	I _{IN(+)} + I _{IN(-)} with Output in Linear Range, V _{CM} = 0V (Note 5)		300		400		300		400		200		500	nADC
Input Common-Mode Voltage Range	V ⁺ = 30 VDC (LM3302, V ⁺ = 28 VDC) (Note 6)	0	V ⁺ - 2.0	0	V ⁺ - 2.0	0	V ⁺ - 2.0	0	V ⁺ - 2.0	0	V ⁺ - 2.0	0	V ⁺ - 2.0	VDC
Saturation Voltage	V _{IN(+)} = 1 VDC, V _{IN(-)} = 0, I _{SINK} ≤ 4 mA		700		700		700		700		400		700	mVDC
Output Leakage Current	V _{IN(+)} = 1 VDC, V _{IN(-)} = 0, V _O = 30 VDC (LM3302, V _O = 28 VDC)		1.0		1.0		1.0		1.0		1.0		1.0	μADC
Differential Input Voltage	Keep all V _{IN} 's > 0 VDC (or V ₋ if used), (Note 8)		36		36		36		36		36		28	VDC

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 95°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small (P_D ≤ 100 mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V⁺ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V⁺. Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V⁺ voltage level for a large duration for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3 VDC (at 25°C overdrive) for the time duration that an input is driven negative. Note 4: The LM239/LM239A, all temperature specifications are limited to -25°C ≤ T_A ≤ +85°C, the LM339/LM339A temperature specifications are limited to -50°C ≤ T_A ≤ +125°C, for the LM139/LM139A, V_{IN(+)} = 0, I_{SINK} ≤ 4 mA, the LM2901, LM3302 temperature range is -40°C ≤ T_A ≤ +85°C. Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, no loading change exists on the reference or input lines. Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V⁺ - 1.5V at 25°C, but either or both inputs can go to +30 VDC without damage (25V for LM3302), independent of the magnitude of V⁺. Note 7: The response time specified is a 100 mV input step with 5 mV overdrive. For larger overdrive signals, 300 ns can be obtained, see typical performance characteristics section. Note 8: Positive excursions of input voltage may exceed the power supply level as long as the output voltage remains within the common-mode range; the comparator will provide a proper output state. The low input voltage state must not be less than -0.3 VDC (or 0.3 VDC below the magnitude of the negative power supply), if used, (at 25°C). Note 9: At output switch point, V_O = 1.4 VDC, R_{EQ} = 0Ω with V⁺ from 5 VDC to 30 VDC, and over the full input common-mode range (0 VDC to V⁺ - 1.5 VDC) at 25°C. For LM3302, V⁺ from 5 VDC to 28 VDC.

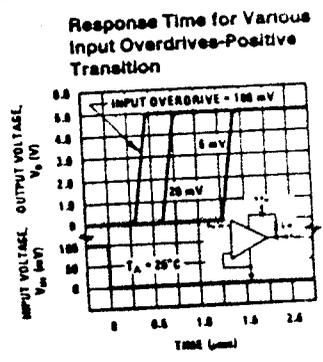
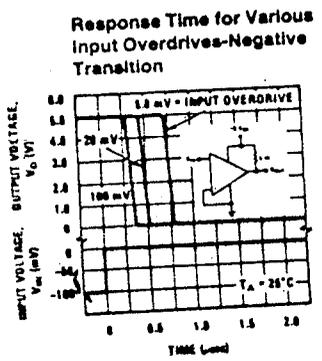
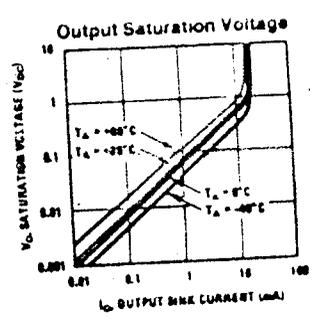
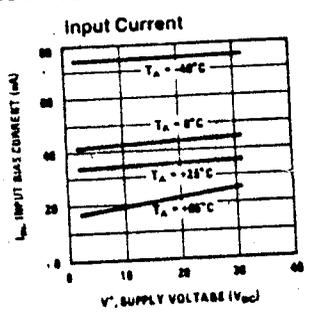
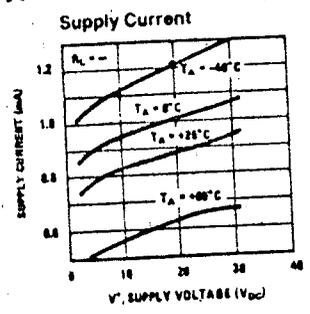
LM139/LM239/LM339/LM139A/LM239A/LM339A/LM2901/LM3302

Typical Performance Characteristics LM139/LM239/LM339, LM139A/LM239A/LM339A, LM3302



TL/H/5706-6

Typical Performance Characteristics LM2901



TL/H/5706-7

Application Hints

The LM139 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing this input resistors to $< 10\text{ k}\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

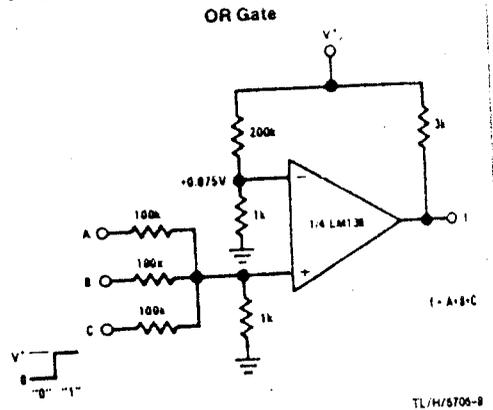
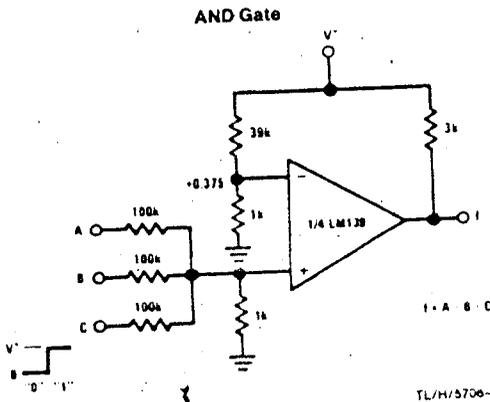
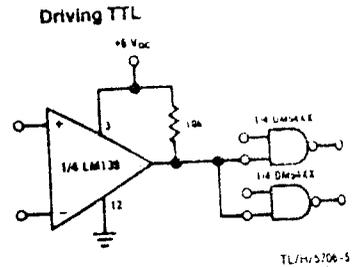
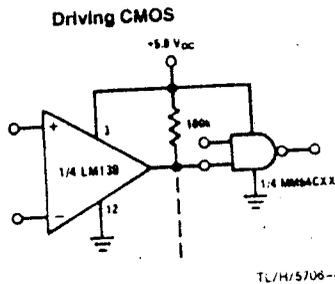
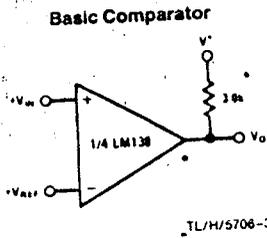
The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC} .

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

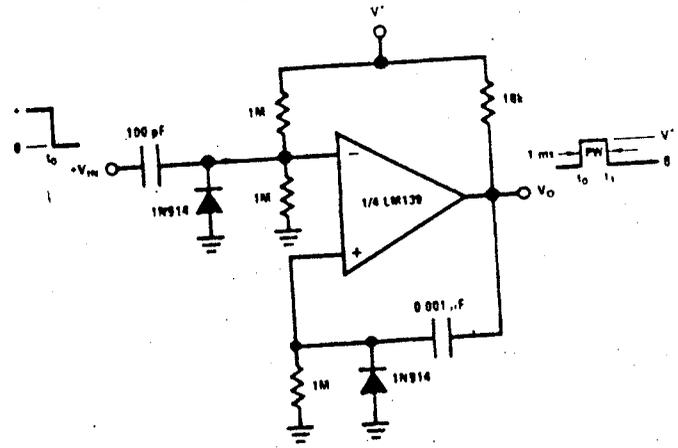
The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 15 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 600 R_{SAT} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications ($V^+ = 5.0\text{ V}_{DC}$)



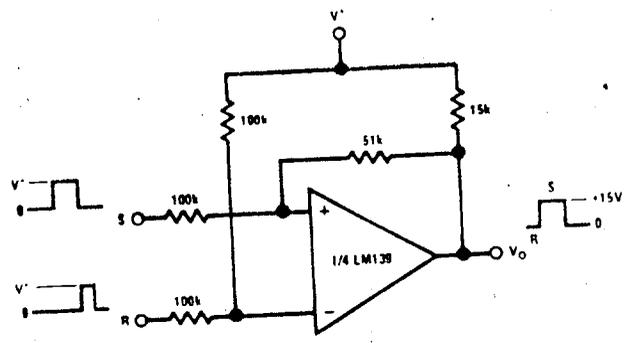
Typical Applications ($V^+ = 15\text{ V}_{DC}$) (Continued)

One-Shot Multivibrator



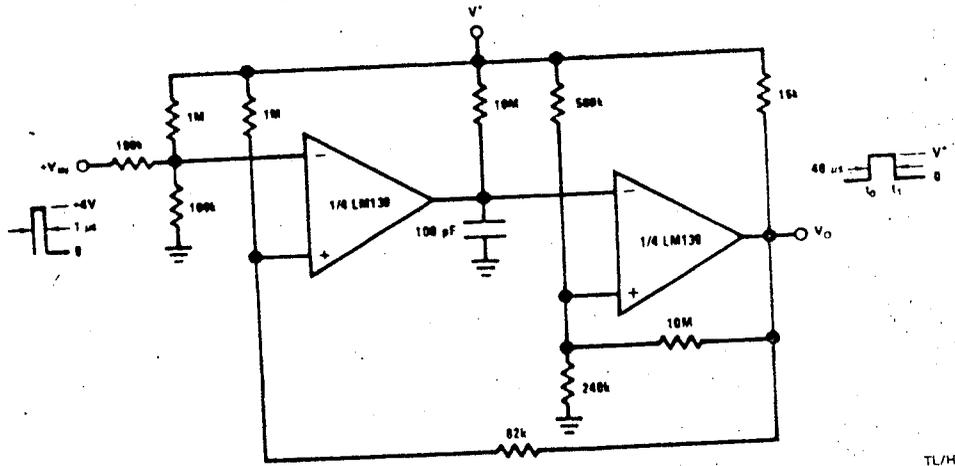
TL/H/5708-10

Bi-Stable Multivibrator



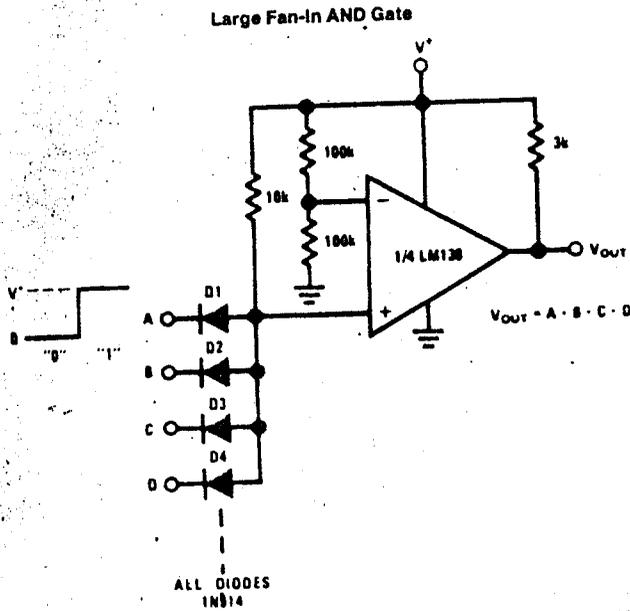
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One-Shot Multivibrator with Input Lock Out

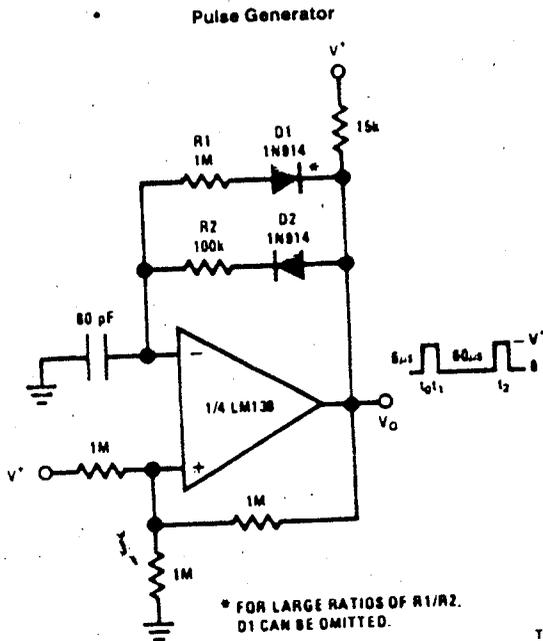


TL/H/5708-12

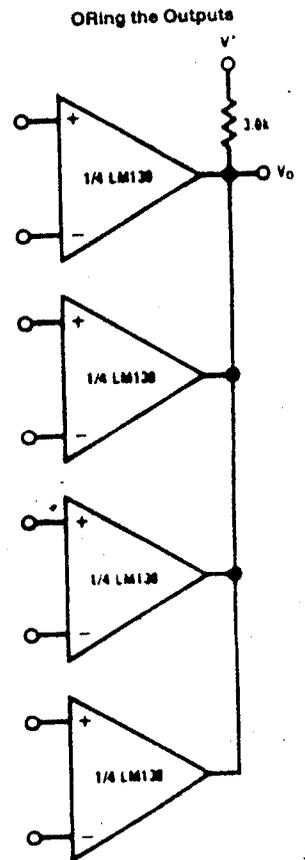
Typical Applications ($V+ = 15 V_{DC}$) (Continued)



TL/H/5708-13



TL/H/5706-17

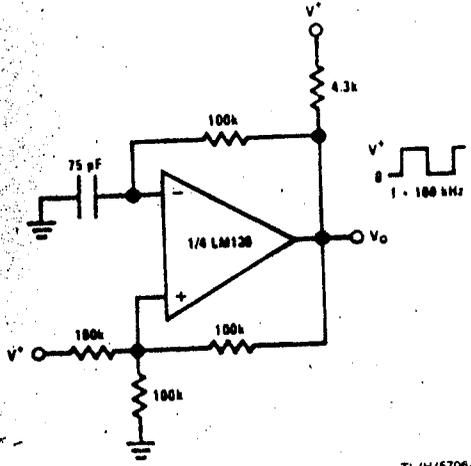


TL/H/5706-15

LM139/LM239/LM339/LM139A/LM239A/LM339A/LM2901/LM3302

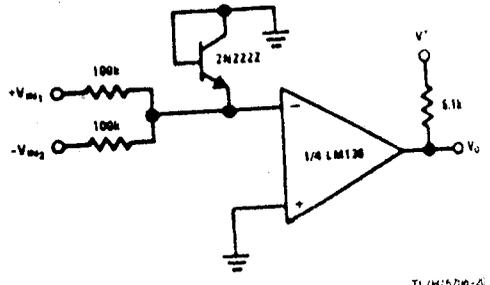
Typical Applications ($V^+ = 15\text{ V}_{DC}$) (Continued)

Squarewave Oscillator



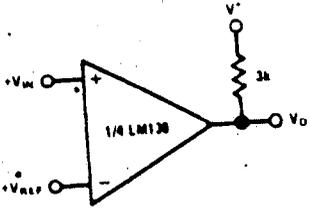
TL/H/5706-16

Comparing Input Voltages of Opposite Polarity



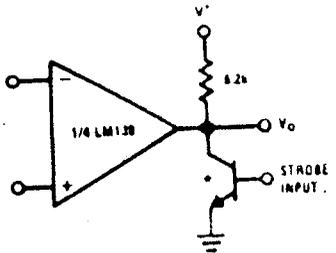
TL/H/5706-20

Basic Comparator



TL/H/5706-21

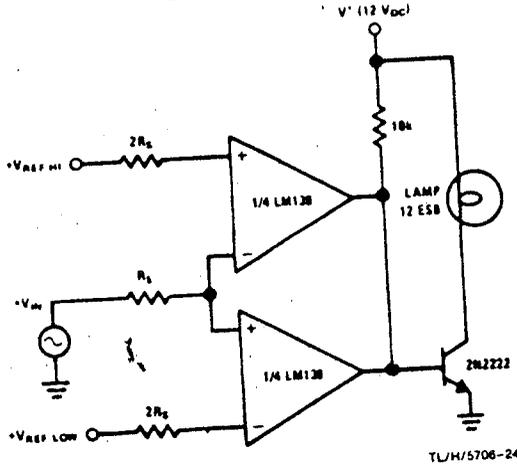
Output Strobing



TL/H/5706-24

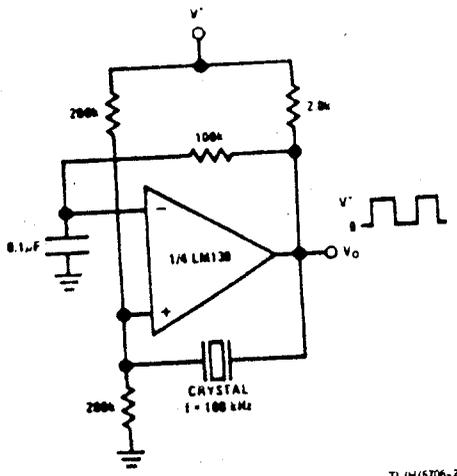
*Or open-collector logic gate without pull-up resistor

Limit Comparator



TL/H/5706-24

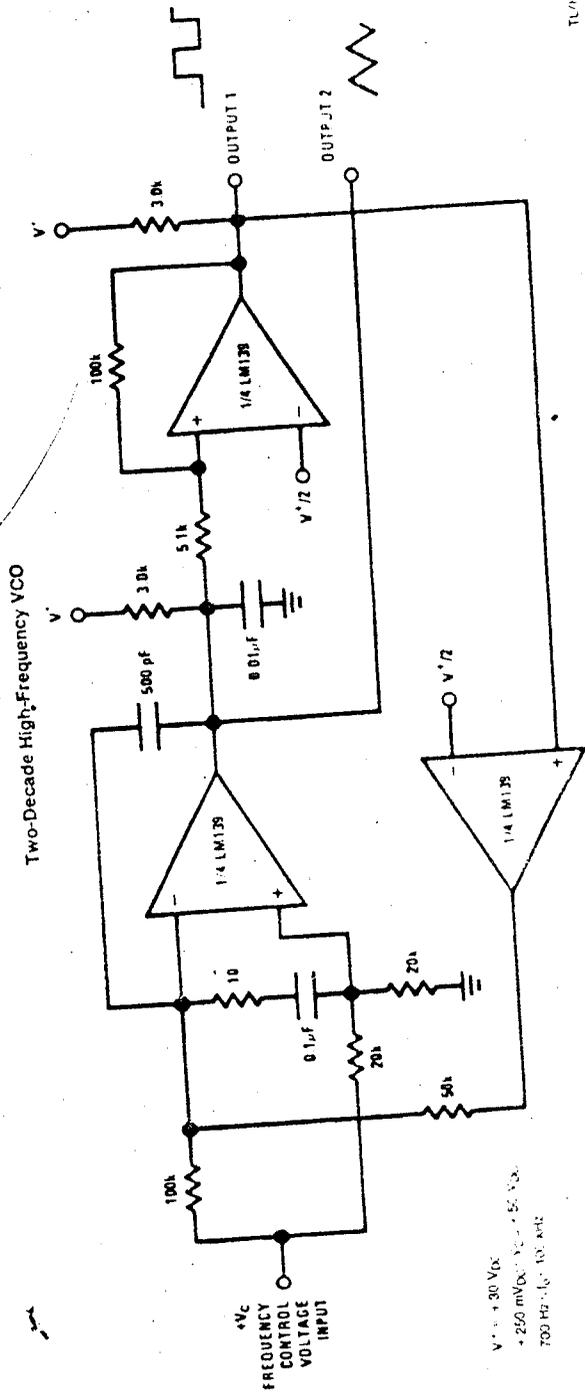
Crystal Controlled Oscillator



TL/H/5706-25

Typical Applications ($V^+ = 15\text{ VDC}$) (Continued)

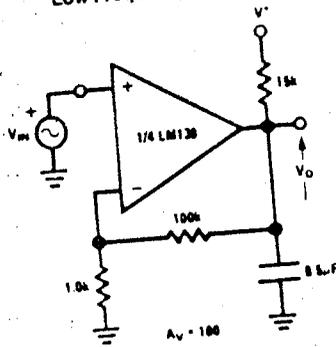
LM139/LM239/LM339/LM139A/LM239A/LM339A/LM2901/LM3302



$V^+ = +30\text{ VDC}$
 $V^- = 250\text{ mVDC}$
 $V_{in} = 10\text{ mV}$
 $f = 10\text{ kHz}$

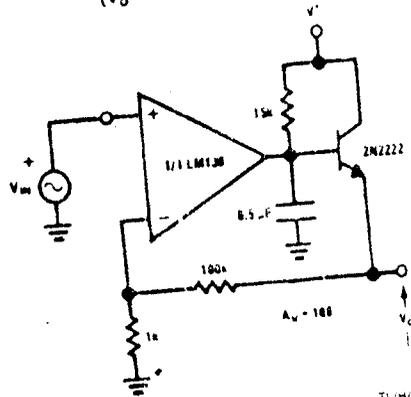
Typical Applications ($V^+ = 5V_{DC}$) (Continued)

Low Frequency Op Amp



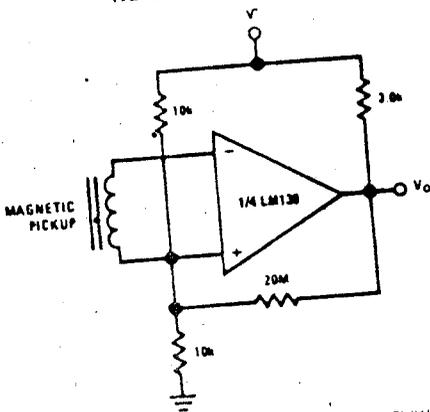
TL/H/5706-26

Low Frequency Op Amp
($V_O = 0V$ for $V_{IN} = 0V$)



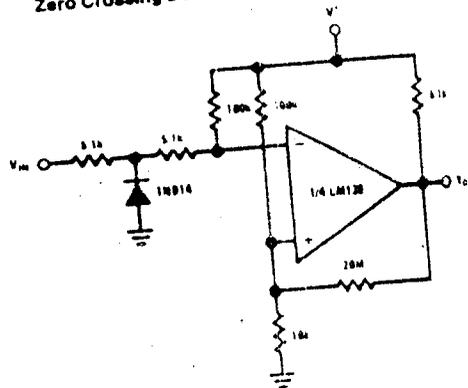
TL/H/5706-27

Transducer Amplifier



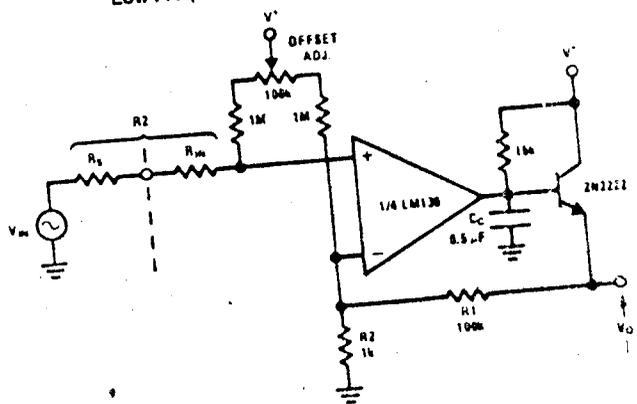
TL/H/5706-28

Zero Crossing Detector (Single Power Supply)



TL/H/5706-29

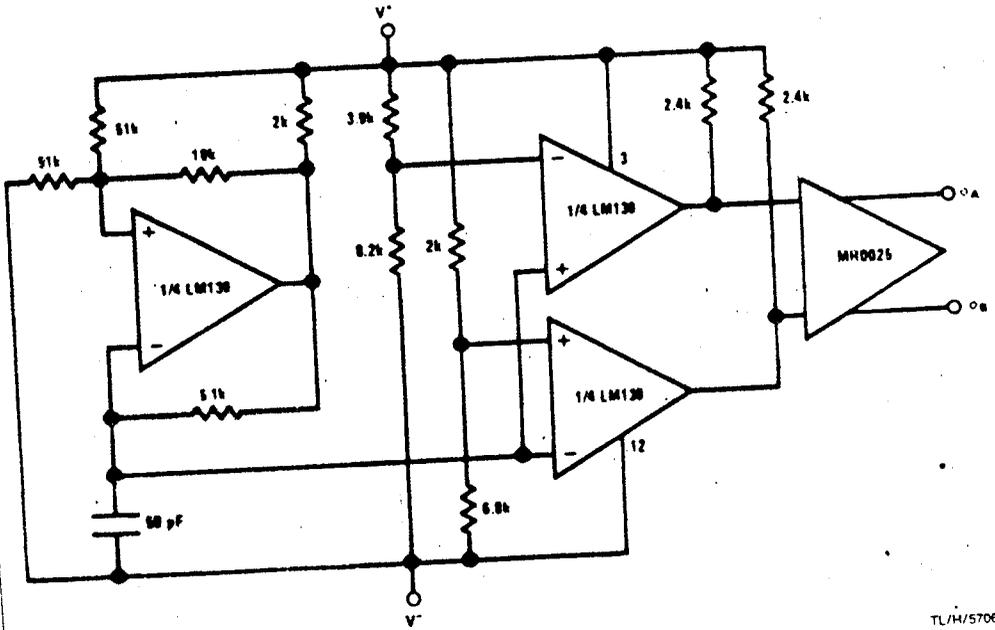
Low Frequency Op Amp with Offset Adjust



TL/H/5706-29

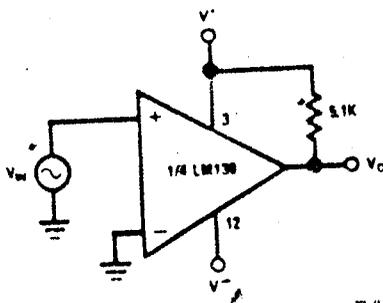
Split-Supply Applications ($V^+ = +15\text{ V}_{DC}$ and $V^- = -15\text{ V}_{DC}$)

MOS Clock Driver



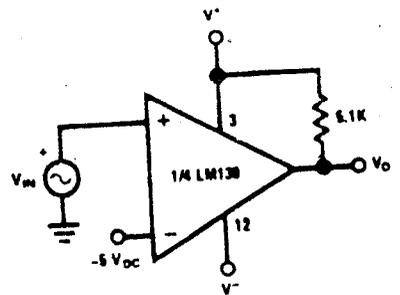
TL/H/5706-31

Zero Crossing Detector



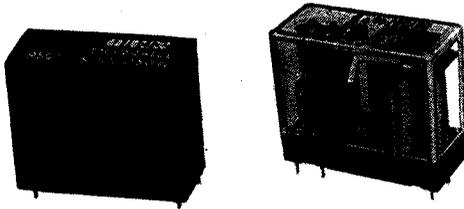
TL/H/5706-32

Comparator With a Negative Reference



TL/H/5706-33

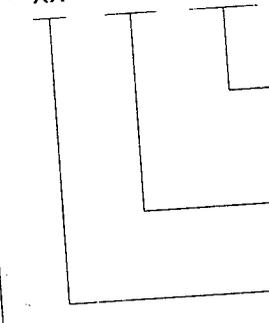




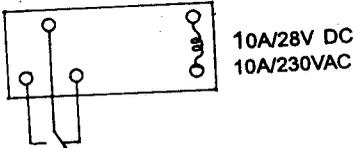
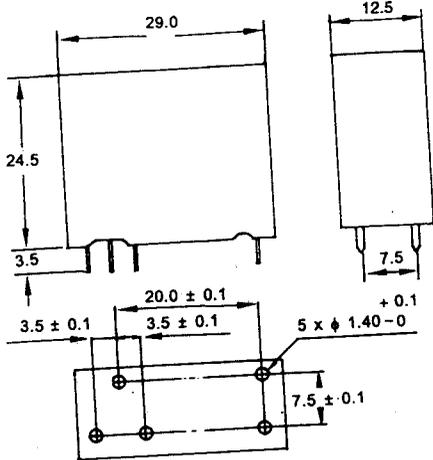
MINIATURE INDUSTRIAL RELAY

The series 58 miniature relays are specially designed for industrial control applications where space and cost are critical. These miniature relays are ideally suited for high density p.c. board applications with pin arrangement for 2.5mm/3.5mm grid.

SPECIFICATIONS		COIL DATA			
		(at 25°C ambient temperature)			
		Coil No.	Coil Resistance ohms ± 10%	Nominal Voltage V DC	Must Operate Voltage V DC
Enclosure	: Polycarbonate	05	50	5	4.0
Contact Arrangement	: 1 change over and 2 change over 1 form C, 1 form A (K type), 1 form C (K type), 2 form C	06	72	6	4.8
Contact Resistance	: 100 m ohms Max (initial)	09	160	9	7.2
Life Expectancy	: 10 ⁵ operations at rated load	12	285	12	9.6
Electrical	: 5 x 10 ⁶ operations	18	640	18	14.4
Mechanical		24	1150	24	19.2
Dielectric Strength		48	4600	48	38.4
Between open contacts	: 750 V RMS	60	7200	60	48.0
Between contact & coil	: 5000 V RMS				
Insulation Resistance	: 500 Meg ohms at 500 V DC 25°C & RH 50				
Operate Time (Max)	: 18 m sec (at nominal voltage)				
Release Time (Max)	: 8 m sec (at nominal voltage)				
Ambient Temperature	: -40°C to 70°C (with no ice)				
Sealed versions available on request.					
CONTACT RATING (Resistive)					
		@ 28 V DC	@ 230 V AC		
1 Form C (Std.)	10 A	10 A	10 A		
1 Form A (K type)	16 A	10 A	10 A		
1 Form C (K type)	10 A	10 A	10 A		

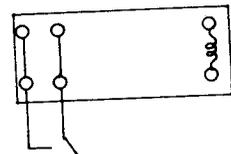
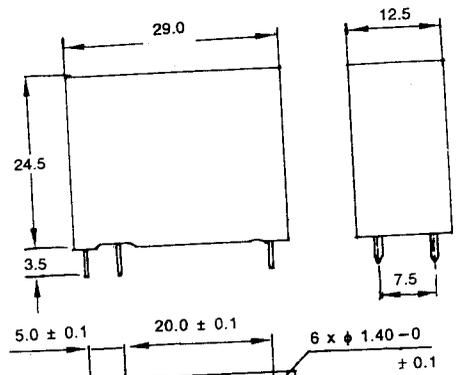
HOW TO ORDER	
58 - XX - XXX - XXXX	
	Provision for special if any eg. B-black or E-sealed Contact arrangement 1 C - 1 form (std) 1 AK - 1 form A (K) 1 CK - 1 form C (K) 2 C - 2 form C (K)
	Coil No (Ref coil d
	Product Series

SERIES - 58 RELAY
 Dimensions / P.C. Hole Layout / Circuit diagram



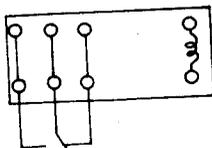
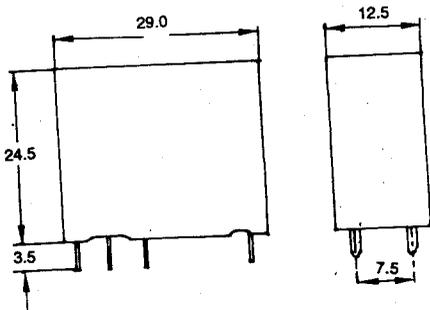
1 FORM C (STD.)

10A/28V DC
 10A/230VAC



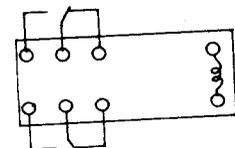
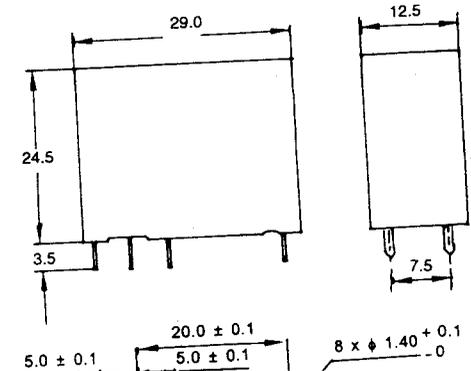
1 FORM A (K TYPE)

16A/28 VDC
 10A/230 VAC



1 FORM C (K TYPE)

10A/28VDC
 10A/230VAC



2 FORM C (STD.)

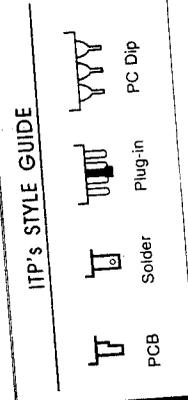
5A/28 VDC
 5A/230VAC

ALL DIMENSIONS GIVEN ARE IN MM. TOLERANCE UNLESS OTHERWISE SPECIFIED ± 0.5 MM

GRADUATED RELAYS

INDUSTRIAL

AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC		
40 x 40 x 67.45		33 x 36 x 54.5		35.5 x 35.5 x 57		39 x 39 x 47.6		25 x 20 x 31 30 x 20 x 31		30.2 x 19 x A A = 23.8 to 40.5	25 x 19 x 30 30 x 19 x 30	31 x 21 x 11.5 31 x 25 x 11.5	20 x 7.2 x 7.5	20.5 x 12 x 16							
1C, 2C, 3C	1C, 2C, 3C	1C, 2C, 3C	1C, 2C, 3C	2Z	5000	5000	24	2C, 4C	2C, 4C	2C, 4C, 6C, 8C ⁽¹⁾	2C, 4C	2C, 4C	2C, 4C	2C	2C, 4C	2C, 4C	2C, 4C	2C, 4C	2C, 4C	2C	
1380	1380	2300	2500	480	20 A at 24 VDC, 230 VAC	20 A at 24 VDC, 230 VAC	1 A at 24 VDC	30	30	3A 5A 7A at 28 VDC, 115 VAC	1A at 30 VDC	2A at 30 VDC	10 3	1A at 28 VDC, 115 VAC	2A at 30 VDC	Max. VDC: 100 28 Max. A: 1 1 Switching: 0.25A	5, 12, 24	5, 6, 12, 24, 48, 60	5, 12, 24	1A at 28 VDC, 115 VAC	
144	144	240	300	6A at 24 VDC, 230 VAC	6, 12, 24, 48, 60, 115, 240	6, 12, 24, 50, 115, 240	1 - 60 ⁽²⁾	2 - 230 ⁽³⁾	2 - 230 ⁽³⁾	2 - 230 ⁽³⁾	1 - 230 ⁽³⁾	1 - 230 ⁽³⁾	1 x 10 ⁶	2 - 230 ⁽³⁾	1 - 230 ⁽³⁾	1 - 230 ⁽³⁾	5, 12, 24	5, 6, 12, 24, 48, 60	5, 12, 24	3, 5, 6, 9, 12, 18, 24, 48	
6A at 24 VDC, 230 VAC	6A at 24 VDC, 230 VAC	6A at 24 VDC, 230 VAC	6A at 24 VDC, 230 VAC	20 A at 24 VDC, 230 VAC	6, 12, 24, 48, 60, 115, 240	6, 12, 24, 50, 110, 220, 250	1 - 60 ⁽²⁾	2 - 230 ⁽³⁾	2 - 230 ⁽³⁾	1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	2 - 230 ⁽³⁾	1 - 230 ⁽³⁾	1 - 230 ⁽³⁾	5, 12, 24	5, 6, 12, 24, 48, 60	5, 12, 24	3, 5, 6, 9, 12, 18, 24, 48	
6, 12, 18, 24, 48, 60, 115, 230	6, 12, 18, 24, 48, 60, 115, 230	6, 12, 18, 24, 48, 60, 115, 230	6, 12, 24, 48, 60, 110, 220	20 A at 24 VDC, 230 VAC	6, 12, 24, 50, 115, 240	6, 12, 24, 50, 110, 220, 250	1 - 60 ⁽²⁾	2 - 230 ⁽³⁾	2 - 230 ⁽³⁾	1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	2 - 230 ⁽³⁾	1 - 230 ⁽³⁾	1 - 230 ⁽³⁾	5, 12, 24	5, 6, 12, 24, 48, 60	5, 12, 24	3, 5, 6, 9, 12, 18, 24, 48	
1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	20 x 10 ⁶	5 x 10 ⁶	5 x 10 ⁶	5 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	2 - 230 ⁽³⁾	1 - 230 ⁽³⁾	1 - 230 ⁽³⁾	5, 12, 24	5, 6, 12, 24, 48, 60	5, 12, 24	3, 5, 6, 9, 12, 18, 24, 48	
1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	5 x 10 ⁶	5 x 10 ⁶	5 x 10 ⁶	5 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	1 x 10 ⁶	2 - 230 ⁽³⁾	1 - 230 ⁽³⁾	1 - 230 ⁽³⁾	5, 12, 24	5, 6, 12, 24, 48, 60	5, 12, 24	3, 5, 6, 9, 12, 18, 24, 48	
20.0	20.0	20.0	16.0	30.0	See footnote (3)	See footnote (3)	See footnote (3)	See footnote (3)	See footnote (3)	See footnote (3)	See footnote (3)	See footnote (3)	See footnote (3)	2C	4C	2C	4C	2C	4C	2C	4C
10.0	10.0	10.0	9.0	20.0	See footnote (3)	See footnote (3)	See footnote (3)	See footnote (3)	See footnote (3)	See footnote (3)	See footnote (3)	See footnote (3)	See footnote (3)	2C	4C	2C	4C	2C	4C	2C	4C



(1) Only available for DC coils.
 (2) Please see detailed catalogue for coil selection.
 (3) Operate and release time vary depending upon pile up and excitation.
 (4) Operate and release time vary depending upon contact arrangement.
 (5) Operate and release time vary depending upon contact arrangement.

Factory Sealed

Sealed

Sealed

