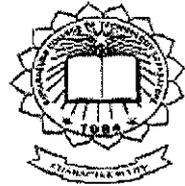P-3480

LOW POWER DELAY BUFFER USING GATED DRIVER TREE

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BONAFIDE CERTIFICATE

Certified that this project report entitled "**LOW POWER DELAY BUFFER USING GATED DRIVER TREE**" is the bonafide work of **C.Revathi** [Reg. no. 1020106016] who carried out the research under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other project or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

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Sho Llt

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The candidate with university Register no. **1020106016** is examined by us in the project viva-voce examination held on .23-05-2011.......

Internal Examiner

External Examiner

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ABSTRACT

The low-power delay buffer, proposed delay buffer uses several new techniques to reduce its power consumption. Since delay buffers are accessed sequentially, it adopts a ring-counter addressing scheme. In the ring counter, double-edge-triggered (DET) flip-flops are utilized to reduce the operating frequency by half and the C-element gated-clock strategy is proposed. A novel gated-clock-driver tree is then applied to further reduce the activity along the clock distribution network. Moreover, the gated-driver-tree idea is also employed in the input and output ports of the memory block to decrease their loading, thus saving even more power. Both simulation results and experimental results show great improvement in power consumption. A 256 x8 delay buffer is fabricated and verified in 0.18 um CMOS technology and it dissipates only 2.56 mW when operating at 135 MHz from 1.8-V supply voltage.

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CHAPTER 1

BUFFER

1.1 INTRODUCTION

A temporary storage area, usually in RAM. The purpose of most buffers is to act as a holding area, enabling the CPU to manipulate data before transferring it to a device.

Because the processes of reading and writing data to a disk are relatively slow, many programs keep track of data changes in a buffer and then copy the buffer to a disk. For example, word processors employ a buffer to keep track of changes to files. Then when you save the file, the word processor updates the disk file with the contents of the buffer. This is much more efficient than accessing the file on the disk each time you make a change to the file.

Buffers are commonly used when burning data onto a compact disc, where the data is transferred to the buffer before being written to the disc. Another common use of buffers is for printing documents. When you enter a PRINT command, the operating system copies your document to a print buffer (a free area in memory or on a disk) from which the printer can draw characters at its own pace.

1.2 SOFTWARE USED

> Modelsim XE 111 6.2g
> Xilinx ISE 9.2i

CHAPTER 2

SYSTEM ANALYSIS

2.1 Delay buffer implemented by shift registers

2.1.1 Flip-Flops

The memory elements in a sequential circuit are called flip-flops. A flip-flop circuit has two outputs, one for the normal value and one for the complement value of the stored bit. Binary information can enter a flip-flop in a variety of ways and gives rise to different types of flip-flops.

A flip-flop circuit can be constructed from two NAND gates or two NOR gates. Each flip-flop has two outputs, Q and Q', and two inputs, set and reset. This type of flip-flop is referred to as an SR flip-flop or SR latch. The flip-flop in has two useful states. When Q=1 and Q'=0, it is in the set state (or 1-state). When Q=0 and Q'=1, it is in the clear state (or 0-state). The outputs Q and Q' are complements of each other and are referred to as the normal and complement outputs, respectively.

2.1.2 D Flip-Flop

The edge-triggered D flip-flop is easily derived from its RS counterpart. The only requirement is to replace the R input with an inverted version of the S input, which thereby becomes D. This is only needed in the master latch section; the slave remains unchanged.

One essential point about the D flip-flop is that when the clock input falls to logic 0 and the outputs can change state, the Q output always takes on the state of the D input at the moment of the clock edge. This was not true of the RS and JK flip-flops. The RS master section would repeatedly change states to match the input signals while the clock line is logic 1, and the Q output would reflect whichever input most recently received an active signal. The JK master section would receive and hold an input to tell it to change state, and never

change that state until the next cycle of the clock. This behavior is not possible with a D flip-flop.

The D input goes directly into the S input and the complement of the D input goes to the R input. The D input is sampled during the occurrence of a clock pulse. If it is 1, the flip-flop is switched to the set state (unless it was already set). If it is 0, the flip-flop switches to the clear state. I

2.1.3 Description

The buffer length is and the word-length is then a total of DFFs are required, and it can be quite large if a standard cell for DFF is used. In addition, this approach can consume huge amount of power since on the average binary signals make transitions in every clock cycle.

As a result, this implementation is usually used in short delay buffers, where area and power are of less concern. SRAM-based delay buffers are more popular in long delay buffers because of the compact SRAM cell size and small total area. Also, the power consumption is much less than shift registers because only two words are accessed in each clock cycle: one for write-in and the other for read-out. A binary counter can be used for address generation since the memory words are accessed sequentially.

Though the SRAM-based delay buffers do away with many data transitions, there still can be considerable power consumption in the SRAM address decoder and the read/write circuits. In fact, since the memory words are accessed sequentially, we can use a ring counter with only one rotating active cell to point to the words for write-in and read- out.
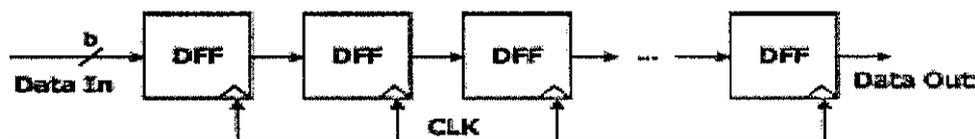

Fig.2.1 Delay buffer implemented by shift registers.

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2.2 Pointer- based delay buffer

The bottom row of D-type flip-flops is initialized with only one "1" (the active cell) and all the other DFFs are kept at "0." When a clock edge triggers the DFFs, this "1" signal is propagated forward. Consequently, the traditional binary address decoder can be replaced by this "unary-coded" ring counter. Compared to the shift register delay buffers, this approach propagates only one "1" in the ring counter instead of propagating -bit words.

Obviously, with much less data transitions, the pointer-based delay buffers can save a lot of power. By observing the fact that only one of the DFFs in the ring counter is activated, the gated-clock technique has then been proposed to be applied to the DFFs. In their approach, every eight DFFs in the ring counter are grouped into one block. Then, a "gate" signal is computed for each block to gate the frequently toggled clock signal when the block can be inactive so that unnecessary power wasted in clock signal transitions is saved.
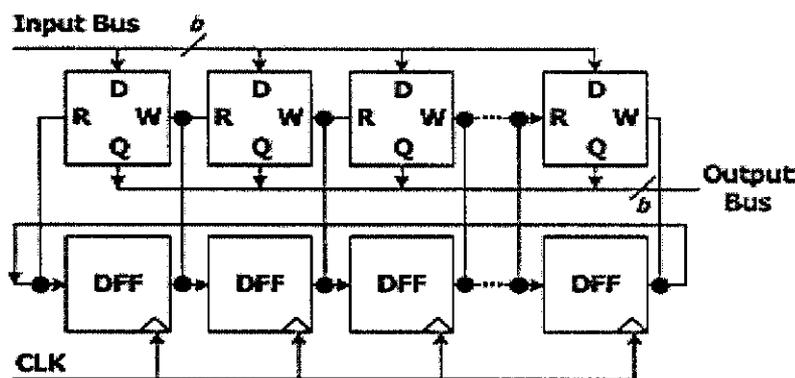
Fig. 2.2 Pointer- based delay buffer

2.3 Ring counter with clock gated by R–S flip-flop

The clocked SR flip-flop consists of a basic NOR flip-flop and two AND gates. The outputs of the two AND gates remain at 0 as long as the clock pulse (or CP) is 0, regardless of the S and R input values. When the clock pulse goes to 1, information from the S and R inputs passes through to the basic flip-flop. With both S=1 and R=1, the occurrence

of a clock pulse causes both outputs to momentarily go to 0. When the pulse is removed, the state of the flip-flop is indeterminate, ie either state may result, depending on whether the set or reset input of the flip-flop remains a 1 longer than the transition to 0 at the end of the pulse.

A ring counter is a type of counter composed of a circular shift register. The output of the last shift register is fed to the input of the first register. If the output of a shift register is fed back to the input. a ring counter results. The data pattern contained within the shift register will re circulate as long as clock pulses are applied. For example, the data pattern will repeat every four clock pulses in the figure below. However, we must load a data pattern. All 0's or all 1's does't count.
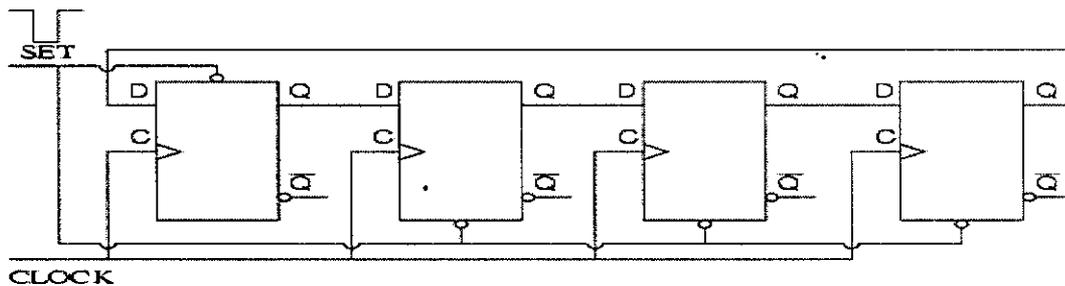
Fig 2.3 SET Flipflop

The input of the first DFF in a block is asserted, it sets the output of the R–S flip-flop to "1" at the next clock edge. Thus, the incoming "1" can be trapped in that block and continue to propagate inside the block. On the other hand, the successful propagation of "1" to the first DFF in the next block can henceforth shut down the unnecessary clock signal in the current block.

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Fig 2.4 Ring counter with clock gated by R–S flip-flop.

CHAPTER 3

LOW POWER DELAY BUFFER

3.1 OBJECTIVE

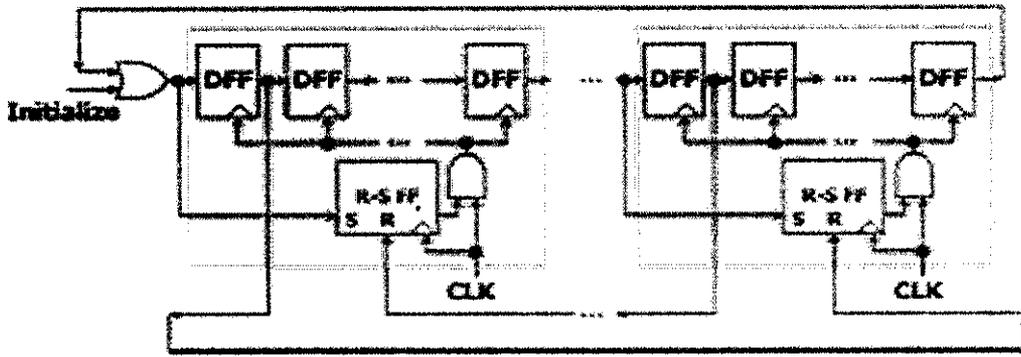The conventional delay buffers can consume huge amount of power and this implementation is usually used in short delay buffers. where area and power are of less concern. A delay buffer based on the SRAM cell array such as the one, the read/write circuitry is through the bit lines that work as data buses so, the loading is increased. The proposed system delay buffer designed to overcome this demerits.

The proposed system used the double-edge-triggered (DET) flip-flops instead of traditional DFFs in the ring counter to halve the operating clock frequency. A novel approach using the C-elements instead of the R–S flip-flops in the control logic for generating the clock-gating signals is adopted to avoid increasing the loading of the global clock signal. In addition to gating the clock signal going to the DET flip-flops in the ring counter, we also proposed to gate the drivers in the clock tree. The technique will greatly decrease the loading on distribution network of the clock signal for the ring counter and thus the overall power consumption. The same technique is applied to the input driver and output driver of the memory part in the delay buffer.

The proposed new delay buffer, we use a tree hierarchy for the read/write circuitry of the memory module. For the write circuitry, in each level of the driver tree, only one driver along the path leading to the addressed memory word is activated. Similarly, a tree of multiplexers and gated drivers comprise the read circuitry for the proposed delay buffer. Simulation results show the effectiveness of the above techniques in power reduction.

3.2 TECHNIQUES

We use several new techniques to reduce it's power consumption.

- ➢ Delay buffers are accessed sequentially and it adopts a ring counter addressing scheme.
- ➢ Double Edge Triggered (DET) flipflop and C-element techniques are used in this project.
- ➢ DET flipflops are utilized to reduce the operating frequency by half.
- ➢ C-element is used to reduce the loading in input and output ports of the memory block.
- ➢ The Gated driver tree is used as input driving circuitry.

3.2.1 Double Edge Triggered (DET) flipflop

The type of flip-flop that synchronizes the state changes during a clock pulse transition is the edge-triggered flip-flop. When the clock pulse input exceeds a specific threshold level, the inputs are locked out and the flip-flop is not affected by further changes in the inputs until the clock pulse returns to 0 and another pulse occurs. Some edge-triggered flip-flops cause a transition on the positive edge of the clock pulse (positive-edge-triggered), and others on the negative edge of the pulse (negative-edge-triggered) .When using different types of flip-flops in the same circuit, one must ensure that all flip-flop outputs make their transitions at the same time.

In order to reduce more power, we replace DFFs by double-edge-triggered flip-flops Double edge-triggered flip-flops are becoming a popular technique for low-power designs since they effectively enable a halving of the clock frequency. A single-edge triggered flip-flop can be implemented by two transparent latches in series, a double edge-triggered flip-flop can be implemented by two transparent latches in parallel. The clock signal is assumed to be inverted locally.
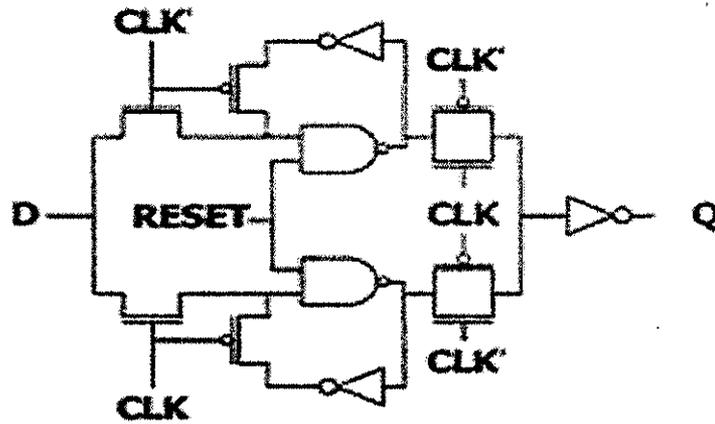
Fig 3.1 circuit diagram of DET

An apparatus comprising a clock for providing a clock signal, means for providing a delayed version of the clock signal, two transparent latches having clock inputs controlled by opposite polarities of the delayed clock signal, a multiplexer having, (i) inputs fed by outputs of the latches, and (ii) a select input fed by the clock signal, and means for providing a select signal for selecting the latch whose clock is inactive.

Each of the latches has a scan input gate and a scan output gate, and the scan output of the first latch is applied to the scan input of the second latch to form a scannable latch pair. Also, preferably, the apparatus further comprises a data port for applying data to the first and second latches, and an exclusive OR gate at the data port, whereby the apparatus produces a gated clock signal. Also disclosed is a method of operating this apparatus.

Double-edge-triggered flip flops (DET FF's) are recognized as power-saving flip flops. We study the same from a low voltage perspective [1-1.5V]. We combine a medium-to-high voltage, plain-MOS-style DETFF technique with a clock-skew technique to derive a new DETFF that is suited to low voltages. Speedwise, our result out performs existing static DETFFs convincingly in the low voltage range. Power wise, our flip flop beats others for dynamic input in the lower half of the same range. The dynamic counterpart of our static circuit also shows similar power superiority at low voltages.

The average power consumption using typical conditions and a 50MHz clock for the circuits with transmission gates, In each case, the inverse clock is generated by an inverter, and the input signals are driven by inverters so that the effects of input capacitance are included in the power measurement.

Power consumption
ECPDOT- 50V- Typ- 50MHz
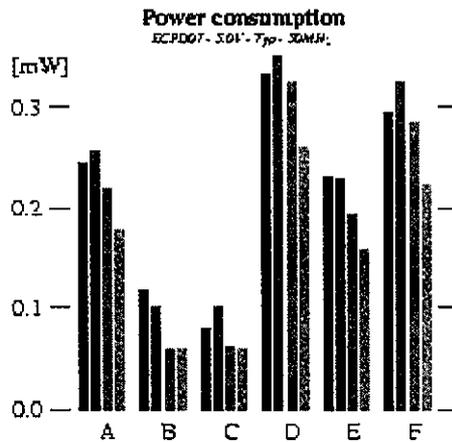
Fig 3.2 average power consumption

The effect of static-power consumption on the circuit can be seen in the different total-power consumption between a constant high (B) and a constant low (C) input. This effect, and the relatively high power-consumption of this circuit, were far more marked in simulations with lower clock frequencies: at 5MHz the power-consumption of more than double that of Fig. 2 for four out of the six simulation vectors.

In comparison to the use of transmission gates to eliminate static power consumption, the proposed circuits use less power with all simulation vectors; for instance, when the inputs to the flip flops do not change there is a 38% power reduction.

3.3 Ring counter with clock gated by c-element

3.3.1 Clock gating

Clock gating is one of the power-saving techniques used on many synchronous circuits. To save power, clock gating support adds additional logic to a circuit to prune the clock tree, thus disabling portions of the circuitry so that its flip-flops do not change state: their switching power consumption goes to zero, and only leakage currents are incurred.

Although asynchronous circuits by definition do not have a "clock", the term perfect clock gating is used to illustrate how various clock gating techniques are simply approximations of the data-dependent behavior exhibited by asynchronous circuitry. As the granularity on which you gate the clock of a synchronous circuit approaches zero, the power consumption of that circuit approaches that of an asynchronous circuit: the circuit only generates logic transitions when it is actively computing.

Chip families such as OMAP3, with a cell phone heritage, support several forms of clock gating. At one end is manual gating of clocks by software, where a driver enables or disables the various clocks used by a given idle controller. On the other end is automatic clock gating, where the hardware can be told to detect whether there's any work to do, and turn off a given clock if it isn't needed. These modes interact. For example, an internal bridge or bus might use automatic gating so that it's gated off until the CPU or a DMA engine needs to use it, while several of the peripherals on that bus might be permanently gated off if they are unused on that board.
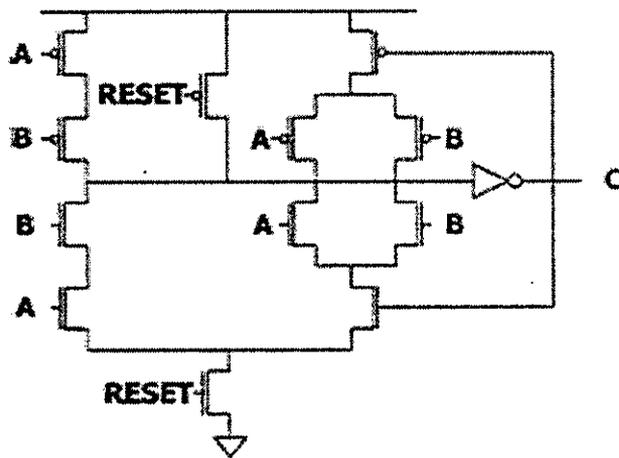
Fig 3.3 circuit diagram of c-Element

3.3.2 C-element

C-element is an essential element in asynchronous circuits for handshaking. One of its implementation is shown,The logic of the C-element is given by,

C+=AB+BC+CA

Where, as well as are its two inputs and as well as are the next and current outputs. If, then the next output will be the same as Otherwise, and remain unchanged. Since the output of C-element can only be changed when, it can avoid the possibility of glitches, a crucial property for a clock gating signal.

When the input of the last DET flip-flop in the previous block changes to "1" making both two inputs of the C-element the same, the clock signal in the current block will be turned on. When the output of the first DET flip-flop in the current block is asserted, then both inputs of the C-element in the previous block go to "0" and the clock for the previous block is disabled.

3.3.3 Gated-Clock Ring Counter

Although some power is indeed saved by gating the clock signal in inactive blocks, the extra R–S flip-flops still serve as loading of the clock signal and demand more than necessary clock power. We propose to replace the R–S flip-flop by a C-element and to use tree-structured clock drivers With gating so as to greatly reduce the loading on active clock drivers.

Additionally, DET flip-flops are used to reduce the clock rate to half and thus also reduce the power consumption on the clock signal.Each block contains one C-element to control the delivery of the local· clock signal "CLK " to the DET flip-flops, and only the "CKE" signals along the path passing the global clock source to the local clock signal are active.
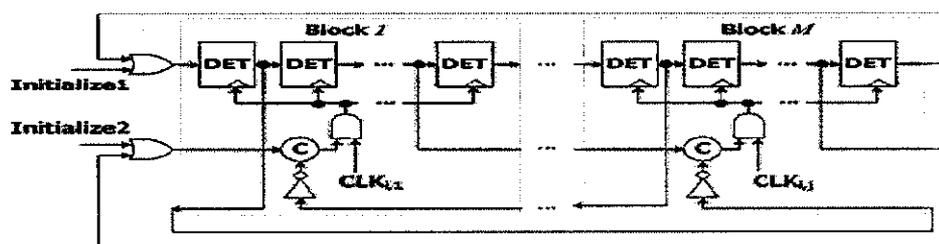

Fig 3.4 Ring counter with clock gated by C-elements

The "gate" signal (CKE) can also be derived from the output of the DET flip -flops in the ring counter. In order to further diminish the loading on the global clock signal ("CLK"), we propose to use a driver tree distribution network for the global clock and activate only those drivers along the path from the clock source to the blocks that need to be driven by the clock. The "gate" signal for those drivers can be derived from the same clock gating signals of the blocks that they drive.

Thus, in a quad-tree clock distribution network, the "gate" signal of the gate driver at the level (CKE) should be asserted when the active DET flip-flop (whose output is "1") in the ring counter is inside the group of blocks with index from to , where is the number of blocks. To be precise, every clock gating signal will be on for two more cases, when "1" is at the input of last DET flip-flop in block and when "1" is at the output of the first DET flip-flop of block .

The "gate" signal for those drivers can be derived from the same clock gating signals of the blocks that they drive. Thus, in a quad-tree clock distribution network, the "gate" signal of the gate driver at the level (CKE) should be asserted when the active DET flip-flop (whose output is "1") in the ring counter is inside the group of blocks with index from to , where is the number of blocks. To be precise, every clock gating signal will be on for two more cases, when "1" is at the input of last DET flip-flop in block and when "1" is at the output of the first DET flip-flop block .

In a quad-tree driver architecture with four times more drivers in each level, all drivers need be activated if no gating is applied and the number of active drivers is .On the other hand, only drivers are activated in the worst case for the proposed gated-clock tree when two drivers are activated in each of the level. On the average, there are no more than drivers that are turned on, where is the number of DET flip-flops in one block is, D=N/M. If the active"1" in the ring counter is propagated to the input of the last DET flip-flop, Q , then the clock enable signals, CKE and CKE , are turned on. Subsequently, CLK and CLK can be delivered.
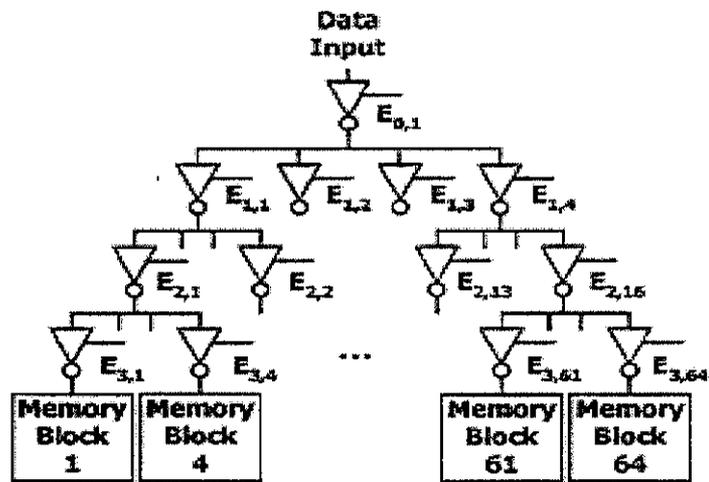
3.3.4 Gated-Driver Tree

Fig 3.5 Diagram of Gated-Driver Tree

To save area, the memory module of a delay buffer is often in the form of an SRAM array with input/output data bus. Special read/write circuitry, such as a sense amplifier, is needed for fast and low-power operations. However, of all the memory cells, only two words will be activated: one is written by the input data and the other is read to the output. Driving the input signal all the way to all memory cells seems to be a waste of power. The same can be said for the read circuitry of the output port. In light of the previous gated-clock tree technique, we shall apply the same idea to the input driving/output sensing circuitry in the memory module of the delay buffer.

The memory words are also grouped into blocks. Each memory block associates with one DET flip-flop block in the proposed ring counter and one DET flip-flop output addresses a corresponding memory word for read-out and at the same time addresses the word that was read one-clock earlier for write-in.

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3.4 THE PERFORMANCE OF PROPOSED DELAY BUFFER

Table 3.1 power consumption of three ring counters

Ring counter structure N=1024,M=128,D=8	Simulated power @1.8v,50MHz,0.18um	Estimated loading Ratio by equations
Traditional ring counter	2127uW	2048
Gated clock ring counter	433uW	400
Proposed ring counter	20uW	21

Table 3.1, represents the performance between the conventional and the proposed delay buffers. The proposed delay buffer is better than others where the power of the proposed delay buffer is 20μw and the loading ratio is 20.

Table 3.2 Power consumption of the input driver tree with and without the gating strategy

Input Driver Tree Structure N=512,M=64,D=8	Simulated power @1.8v,50MHz,0.18um	Estimated loading Ratio by equations
Without gated driver Tree	520uW	512
With gated driver Tree	44.2uW	44

Table 3.2 represents the power consumption between the using of ring counter with gated strategy and without the gated strategy. The proposed delay buffer needs only power in 1/11th power where it is in the without ring counter.

Table 3.3 comparison of measurement results with SRAM-based delay buffers

	Dual port SRAM Delay Buffer	Single port SRAM DelayBuffer	This work
Area	0.113mm^2	0.062mm^2	0.120mm^2
power	19913uW	15359uW	2556uW

Table 3.3 represents the comparison of SRAM based delay buffers. The proposed delay buffer have the highest level area to implement and the more power is saved. It consumes only 1/7th of dual port usage power or 1/6th of the single port usage power.
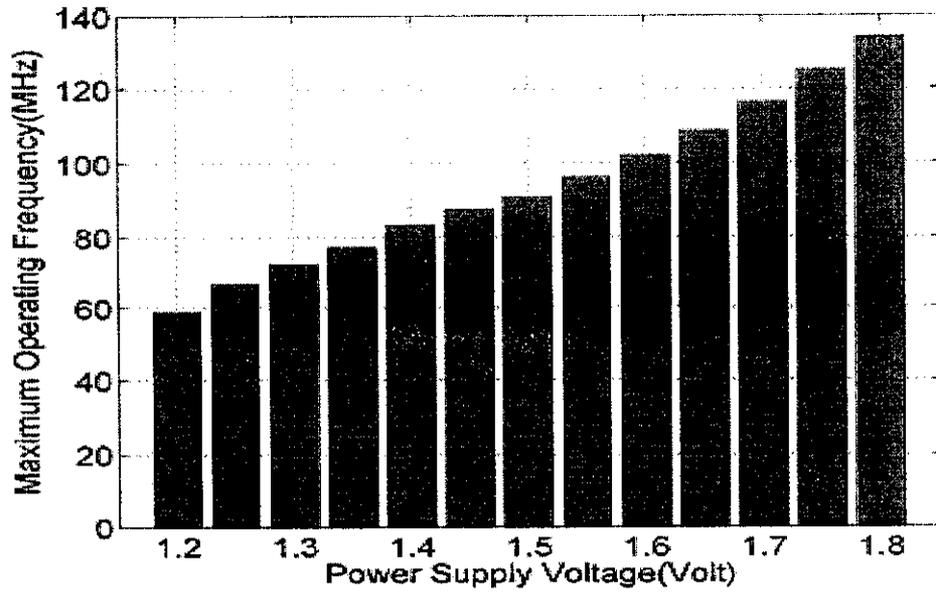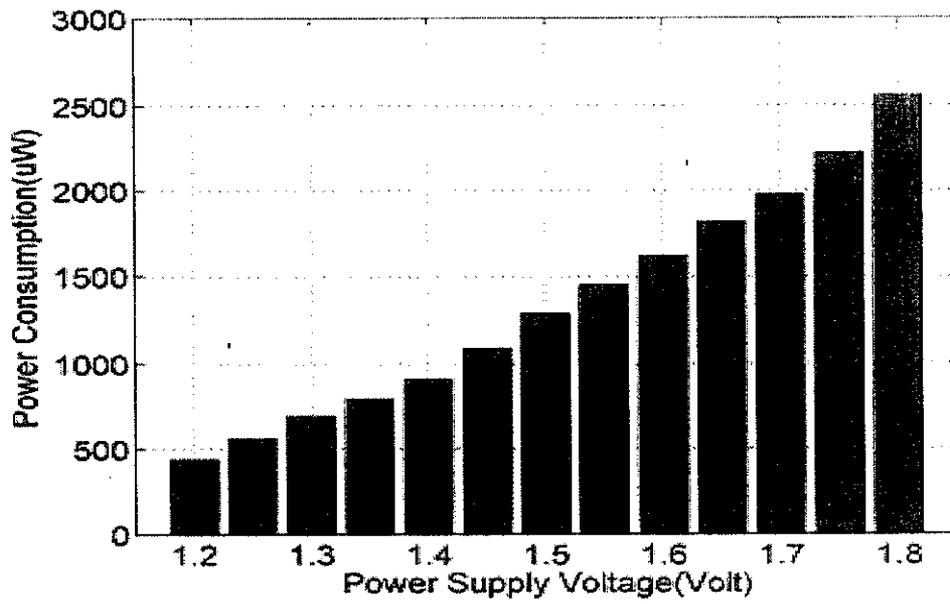
(a)

Fig 3.6 maximum clock rate

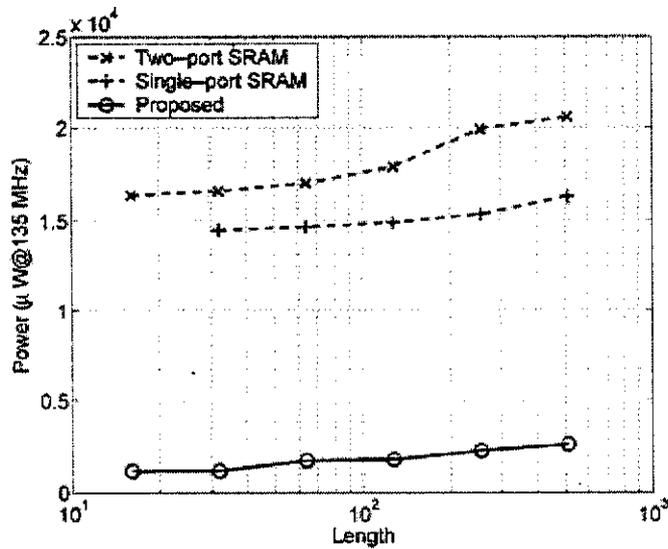Fig 3.7 power consumption at different supply voltage.
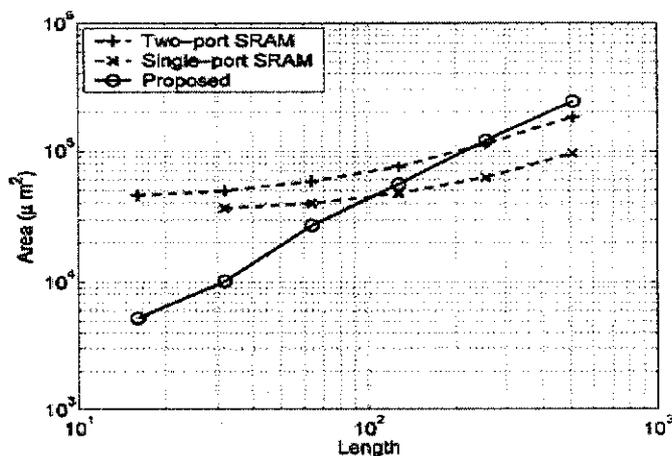
Fig 3.8 simulated results of power

Fig. 3.9 simulated results of area of various delay buffers versus different lengths.

The Total power consumption in normal operation mode and the leakage power consumption in idle (disabled clock) mode for 90-nm and 65-nm technology, respectively. Note that the total power consumption in normal operation mode is not logarithmically proportional to the length of the delay buffer. Instead, due to the quad tree structure for all the driving circuitry, delay buffers of length and have approximate dynamic power because basically these two cases activate the same number of drivers. We can see that the superiority of the proposed circuit is still obvious in 90-nm technology in that the leakage power is

almost negligible. Even in the more advanced 65-nm technology, the leakage power can be controlled to within an acceptable level for medium-length delay buffers with the dual-Voltage approach. For longer-length delay buffers and for more advanced technology, other leakage reductions techniques such as the "sleep" transistors in SRAM (Latch) cells can help to reduce leakage power .

CHAPTER 4

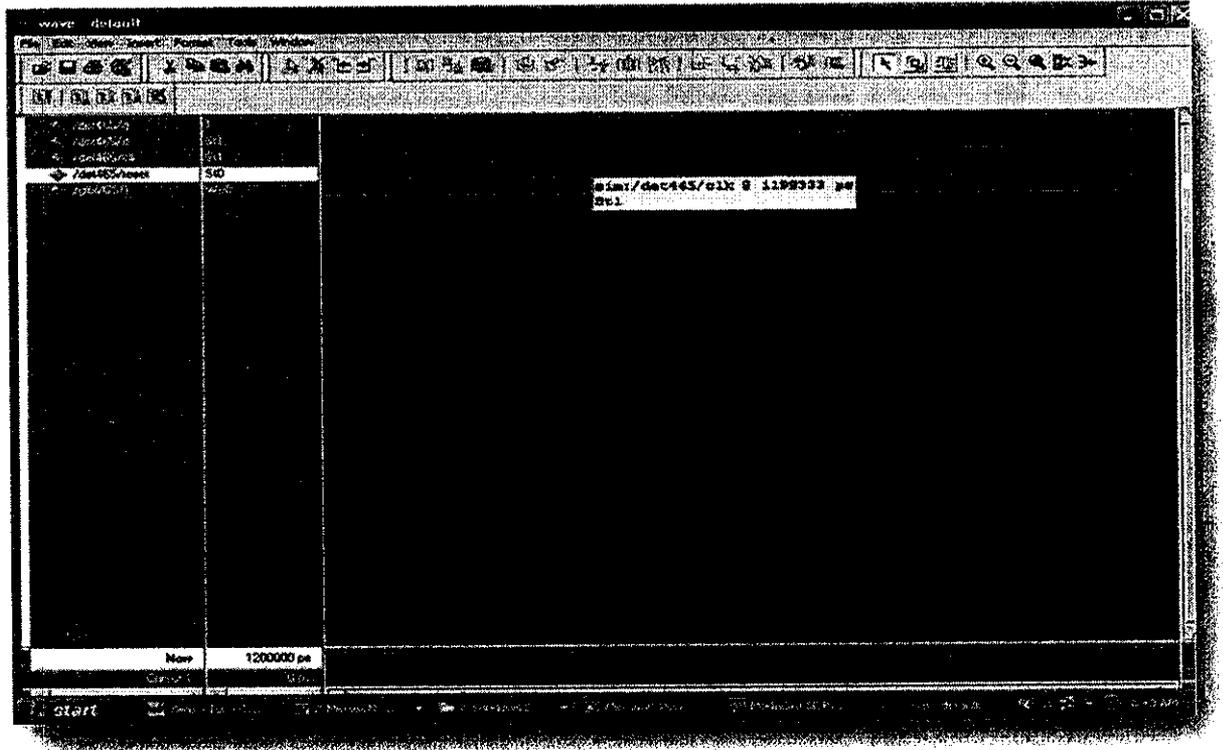# SIMULATION RESULTS AND DISCUSSIONS

4.1 DET

Fig 4.1 DET output

Fig 4.1 represents the output of the DET flip flop that means when the reset is 0' there is no output if the reset is 1' means the positive edge and negative edge transfer the data's.
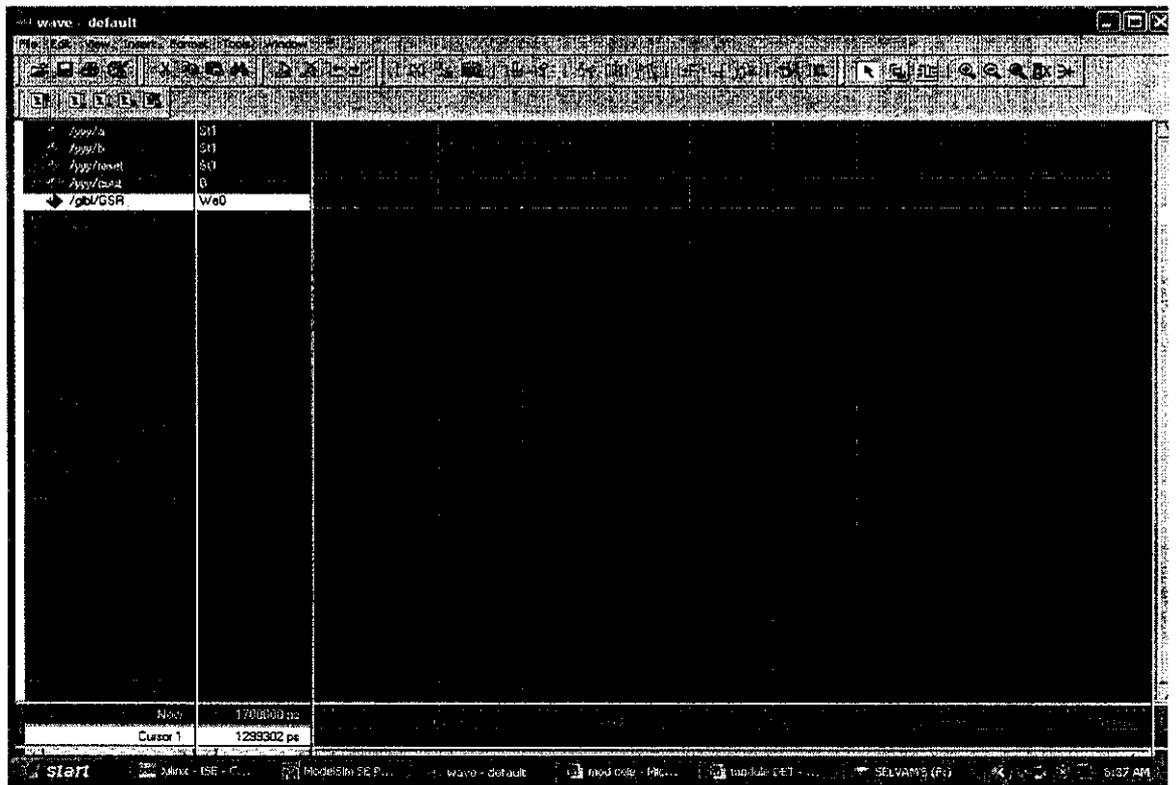
4.2 C-Element

Fig 4.2 C-Element output

Fig 4.2 represents the output of the c-element. If, the inputs of the c-element are same means the output is same as the one of the input. The inputs are different means the output is same as the previous output.

4.3 Clock gated by C-Element

Fig 4.3 Clock gated by C-Element output

Fig 4.3 represents the output of the delay buffer with clock gated by c-element which consists of both DET and c-element with gated driver tree.

CHAPTER 5

CONCLUSION

A low-power delay buffer architecture which adopts several novel techniques to reduce power consumption. The ring counter with clock gated by the C-elements can effectively eliminate the excessive data transition without increasing loading on the global clock signal. The gated-driver tree technique used for the clock distribution networks can eliminate the power wasted on drivers that need not be activated. Another gated-demultiplexer tree and a gated-multiplexer tree are used for the input and output driving circuitry to decrease the loading of the input and output data bus. All gating signals are easily generated by a C-element taking inputs from some DET flip-flop outputs of the ring counter. Measurement results indicate that the proposed architecture consumes only about 13% to 17% of the conventional SRAM-based delay buffers in 0.18- m CMOS technology. Further simulations also demonstrate its advantages in nanometer CMOS technology. The cell size of the proposed delay buffer can be further reduced, making it very useful in all kinds of multimedia/communication signal processing ICs.

In future we may design a large size delay buffers means that the clock gating level is increased and that also depends upon the increasing level of bits(32,64etc).

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