INTELLIGENT VEHICLE SYSTEM

By

PRATHISTA.I	**Reg No: 0710107068**
REKHA.T	**Reg No: 0710107080**
SANDHIYA.G	**Reg No: 0710107085**
SATHYA.M	**Reg No: 0710107094**

of

KUMARAGURU COLLEGE OF TECHNOLOGY,
COIMBATORE - 641 049.
(An Autonomous Institution affiliated to Anna University of Technology, Coimbatore)

A PROJECT REPORT

Submitted to the

FACULTY OF ELECTRONICS AND COMMUNICATION ENGINEERING

In partial fulfillment of the requirements
for the award of the degree

of

BACHELOR OF ENGINEERING
in
ELECTRONICS AND COMMUNICATION ENGINEERING

BONAFIDE CERTIFICATE

Certified that this project report titled **"Intelligent vehicle system"** is the bonafide work of **Ms.I.Prathista** [Reg. No. 0710107068], **Ms.T.Rekha** [Reg. No. 0710107080], **Ms.G.Sandhiya** [Reg. No. 0710107085], and **Ms.M.Sathya** [Reg. No. 0710107094] who carried out the research under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other project or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

Project Guide

Mrs.S.UmaMaheswari

Head of the Department

Dr. Rajeswari Mariappan

The candidates with **University Register Nos 0710107068, 0710107080, 0710107085 and 0710107094** are examined by us in the project viva-voce examination held on 19.04.2011

19/4/11

Internal Examiner

External Examiner

WE DEDICATE THIS PROJECT TO THOSE WHO ARE AFFECTED BY ACCIDENTS

ACKNOWLEDGEMENT

ACKNOWLEDGEMENT

First I would like to express my praise and gratitude to the Lord, who has showered his grace and blessing enabling me to complete this project in an excellent manner.

I express my sincere thanks to our beloved Director **Dr.J.Shanmugam**, Kumaraguru College of Technology, for his kind support and for providing necessary facilities to carry out the work.

I express my sincere thanks to our beloved Principal **Dr.S.Ramachandran**, Kumaraguru College of Technology, who encouraged me in each and every steps of the project work.

I would like to express my deep sense of gratitude to our HOD, the ever active **Dr.Rajeswari Mariappan**, Department of Electronics and Communication Engineering, for her valuable suggestions and encouragement which paved way for the successful completion of the project work.

In particular, I wish to thank with everlasting gratitude to the Project Coordinator **Ms.K.Kavitha,** Assistant Professor (SRG) , Department of Electronics and Communication Engineering, for her expert counseling and guidance to make this project to a great deal of success.

I am greatly privileged to express my heartfelt thanks to my project guide, **Ms.S.UmaMaheswari,** Assistant Professor (SRG), Department of Electronics and Communication Engineering, throughout the course of this project work and I wish to convey my deep sense of gratitude to all the teaching and non-teaching staffs of ECE Department for their help and cooperation.

Finally, I thank my parents and my family members for giving me the moral support and abundant blessings in all of my activities and my dear friends who helped me to endure my difficult times with their unfailing support and warm wishes.

ABSTRACT

ABSTRACT

This project is concerned with the aim to minimize the accident occurrences and to strictly implement the follow up of traffic rules. The basic idea is that one cannot use his vehicle without license and the violation of traffic rules by any vehicle will be reported immediately to the control room. In this project, we develop a prototype in which 3 main traffic rules are taken into consideration, driving license, speed limit and traffic signal. The owner of the vehicle can unlock it only if he has a license which means we are using license as a key to unlock the vehicle. Any vehicle violating these traffic rules will be reported immediately to the control room. If the control room gets any alert then that particular license will be invalidated which can be retrieved on justification.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

A/D	Analog To Digital
AC	Alternating Current
AES	Advanced Encryption Standard
AMR	Automatic Reading
BCD	Binary Coded Decimal
BOR	Brown-Out Reset
CMOS	Complementary Metal–Oxide–Semiconductor
DC	Direct Current
DPDT	Double Pole , Double Throw
DSSS	Direct-Sequence Spread Spectrum
EEPROM	Electrically Erasable Programmable Read-Only Memory
GNSS	Global Navigation Satellite Systems
GPS	Global Positioning System
HVAC	Heating, Ventilating, And Air Conditioning
I^2C	Inter-Integrated Circuit
IC	Integrated Circuits
ICD	In-Circuit Debug
ICSP	In-Circuit Serial Programming
IR	Infra Red
LC	Liquid Crystal
LCD	Liquid Crystal Display
M2M	Machine To Machine
N.C	Normally Closed
NV-SRAM	Non-Volatile Static Random-Access Memory
PIC	Peripheral Interface Controller
PSP	Parallel Slave Port

PWM	Pulse Width Modulation
QED	
R/W	Read/Write
RAM	Random Access Memory
RS-232	Recommended Standard-232
RTC	Real Time Clock
RTO	Regional Transport Office
SCI	Serial Communications Interface
SPDT	Single Pole, Double Throw
SPI	Serial Peripheral Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USART	Universal Synchronous Asynchronous Receiver/Transmitter
WDT	Watchdog Timer

INTRODUCTION

CHAPTER 1

INTRODUCTION

1.1 GENERAL VIEWS

In this fast moving world, people face with lots of accidents which results in heart-wrecking loss of precious lives and valuable properties. Traffic rules are framed in order to minimize the accidents but people don't tend to follow them just because they are in hurry concentrating on their work.

"Hurry makes one to worry"

It is mandatory to monitor and insist people to follow the traffic rules and regulations. Embedded systems pave way for implementing automatic control systems that can sense the activities, take decisions according to the pre-defined codes, and transfer it into actions. These actions may be issued as controlling commands to the people so that their activities, like violation of traffic rules, can be controlled.

Intelligent vehicle system is an initiative of implementing such an effective traffic control system which concentrates on monitoring the violation of traffic rules.

1.2 BASIC PRINCIPLE

This project "intelligent vehicle system" is mainly used to make a vehicle automatic in the world it is going to a dream come true in the near future that these intelligent vehicle systems are going to introduced into the present world. This project is mainly used to control the vehicle with the help of the remote computer, the user will be operating the car form the computer and the data will be transmitted through ZigBee transceiver.

1.3 WORKING

As soon as the driver inserts the license card in its holder, the vehicle controller asks for the password. The password entered is transmitted through ZigBee transmitter to the control room section for verification. Once the driver identity and password is true and valid, the driver is authenticated and hence the engine starts. Thus the rule of holding a driver's license is insisted here. In addition to this, theft protection is given by means of password request.

The first case of traffic violation considered here is the vehicle violating the RED signal. In this case a warning is displayed to the driver and to the control room. After the engine turns off, the next time, when the driver tries to access the license, the control room does not authenticate the license since there is a pending complaint against the driver. Only after the penalty is done, the license is authenticated.

The next case of traffic rule concentrated here is city speed limit control. In our project, the engine is directly controlled by the vehicle using GPS position for which the speed limit is fed in the memory. Say, the city speed limit is 45kmph, and then the speed of the vehicle doesn't exceed it.

1.4 ADVANTAGES

- No driver can drive without license
- Theft protection
- Accident prevention due to violation of traffic rules
- Fully automated traffic monitoring

1.5 APPLICATIONS

Intelligent vehicle system can be implemented in cities to automatically monitor the traffic.

SCHEMATIC OVERVIEW

CHAPTER 2

SCHEMATIC OVERVIEW

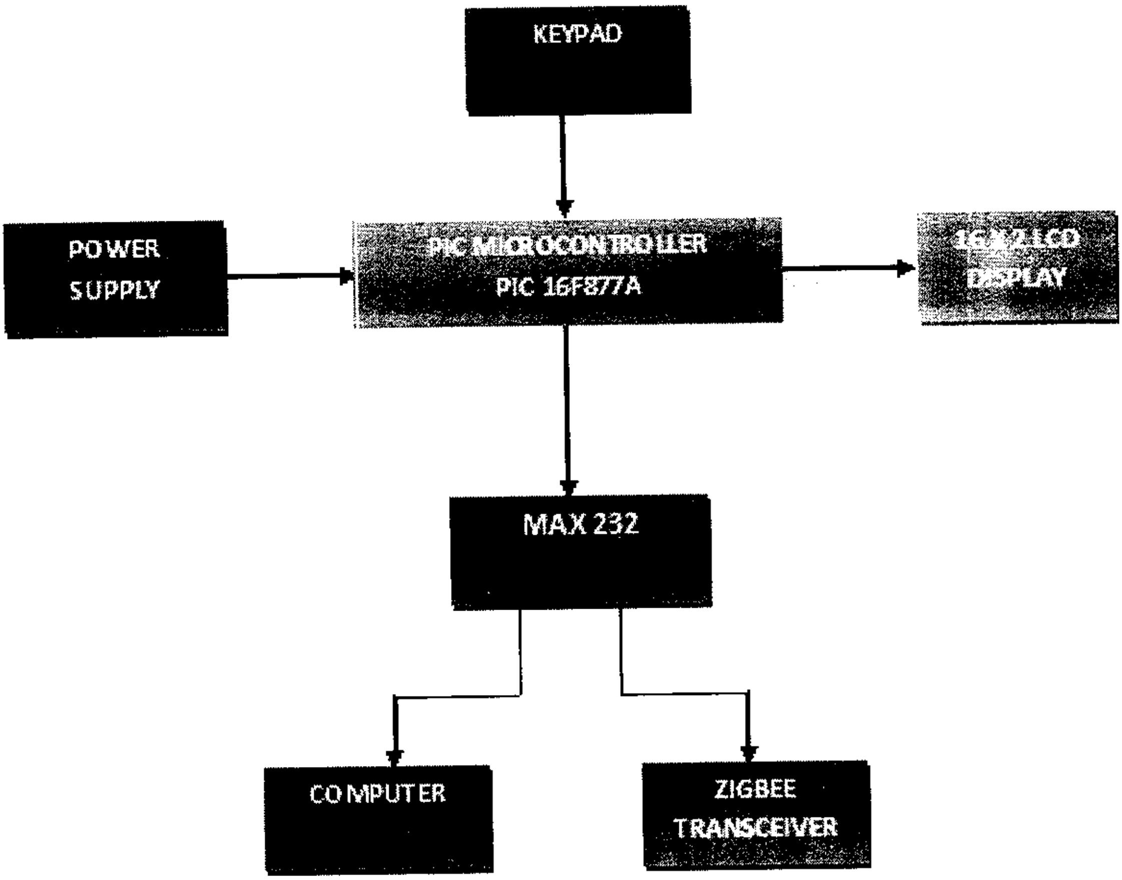


Fig 2.1 Block Diagram of Control Side

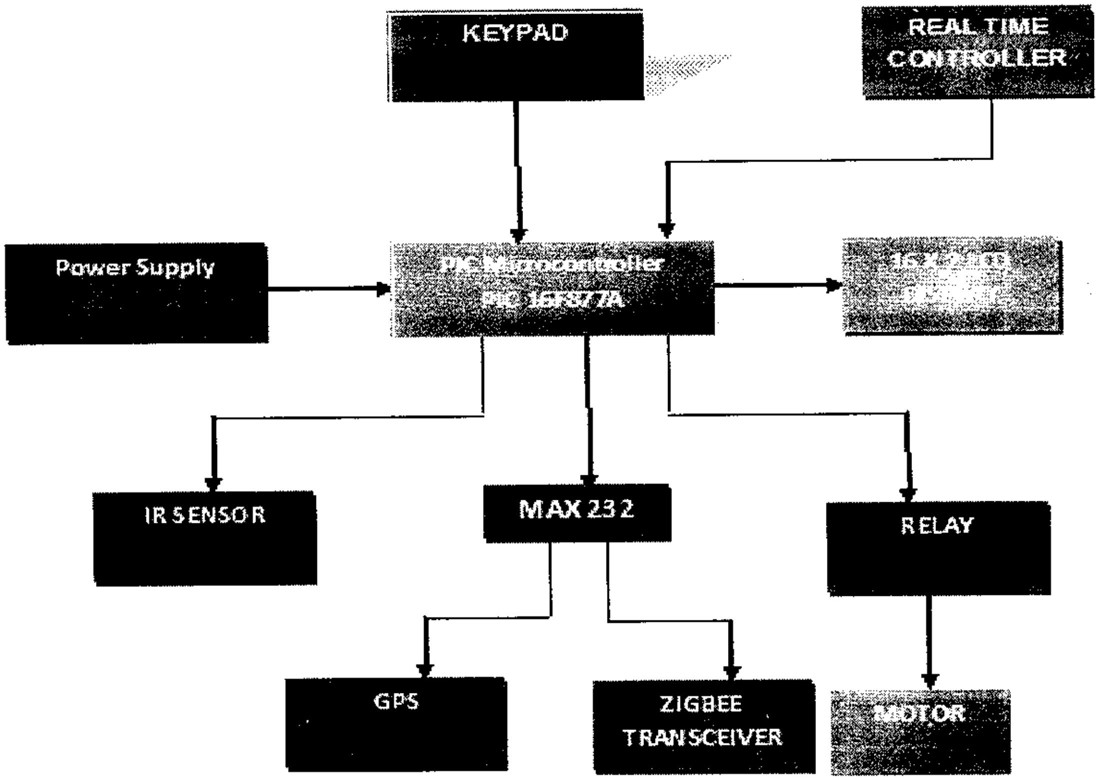


Fig 2.2 Block Diagram of Vehicle Side

2.1 POWER SUPPLY

A **power supply** is a device that supplies electrical energy to one or more electric loads. The term is most commonly applied to devices that convert one form of electrical energy to another, though it may also refer to devices that convert another form of energy (e.g., mechanical, chemical, solar) to electrical energy. A regulated power supply is one that controls the output voltage or current to a specific value; the controlled value is held nearly constant despite variations in either load current or the voltage supplied by the power supply's energy source. Every power supply must obtain the energy it supplies to its load, as well as any energy it consumes while performing that task, from an energy source. The basic block diagram of a power supply and its waveforms are shown in fig 2.3

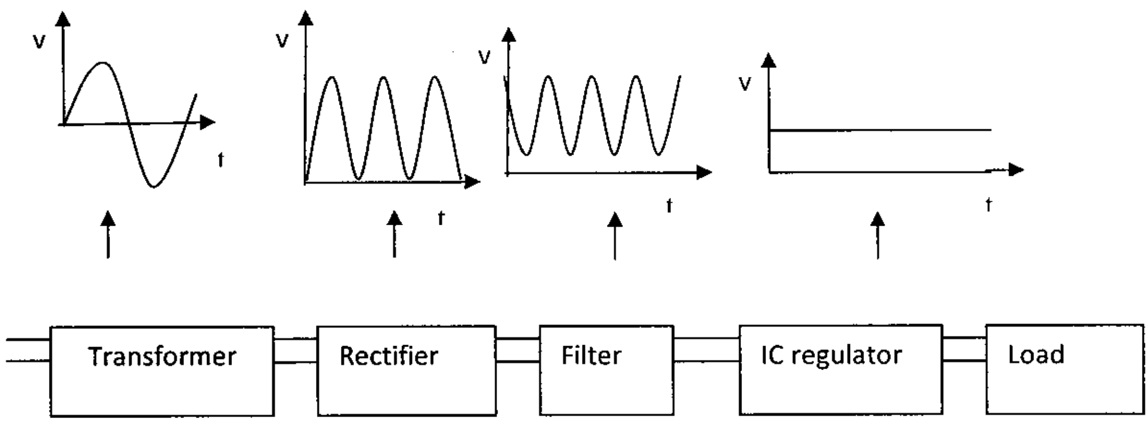


Fig 2.3 Block Diagram of Control Side

A power supply may be implemented as a discrete, stand-alone device or as an integral device that is hardwired to its load. In the latter case, for example, low voltage DC power supplies are commonly integrated with their loads in devices such as computers and household electronics.

2.2 BUZZER

A **buzzer** or **beeper** is an audio signaling device, which may be mechanical, electromechanical, or electronic. Typical uses of buzzers and beepers include alarms, timers and confirmation of user input such as a mouse click or keystroke. Early devices were based on an electromechanical system identical to an electric bell without the metal gong. Similarly, a relay may be connected to interrupt its own actuating current, causing the contacts to buzz. Often these units were anchored to a wall or ceiling to use it as a sounding board.

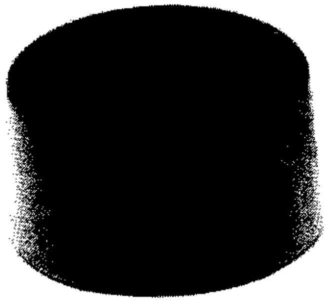


Fig 2.4 3v Pcb Mount Piezo Buzzer

The word "buzzer" comes from the rasping noise that electromechanical buzzers made. A piezoelectric element may be driven by an oscillating electronic circuit or other audio signal source. Sounds commonly used to indicate that a button has been pressed are a click, a ring or a beep. Electronic buzzers find many applications in modern days.

2.3 LCD DISPLAY

A **liquid crystal display (LCD)** is a thin, flat electronic visual display that uses the light modulating properties of liquid crystals (LCs). LCDs do not emit light directly. Liquid crystal displays (LCDs) are a passive display technology. This means they do not emit light; instead, they use the ambient light in the environment. By manipulating this light, they display images using very little power. This has made LCDs the preferred technology whenever low power consumption and compact size are critical. They are usually more compact, lightweight, portable, less expensive, more reliable, and easier on the eyes.

The LCD used here can display 16 × 2 alphanumeric characters as shown in fig 2.4.

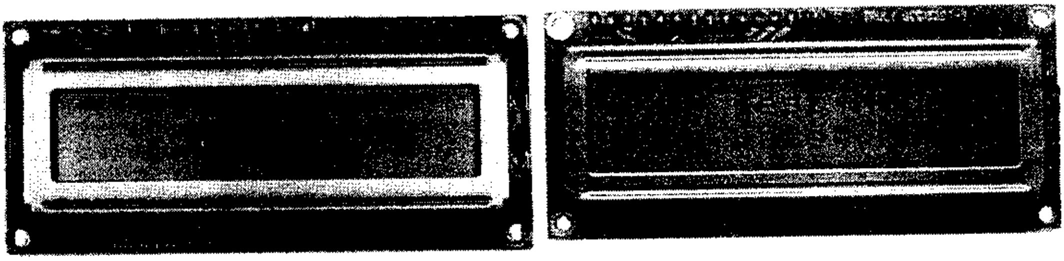


Fig 2.5 A Commercially Available LCD Display

2.4 PIC 16F877A MICROCONTROLLER

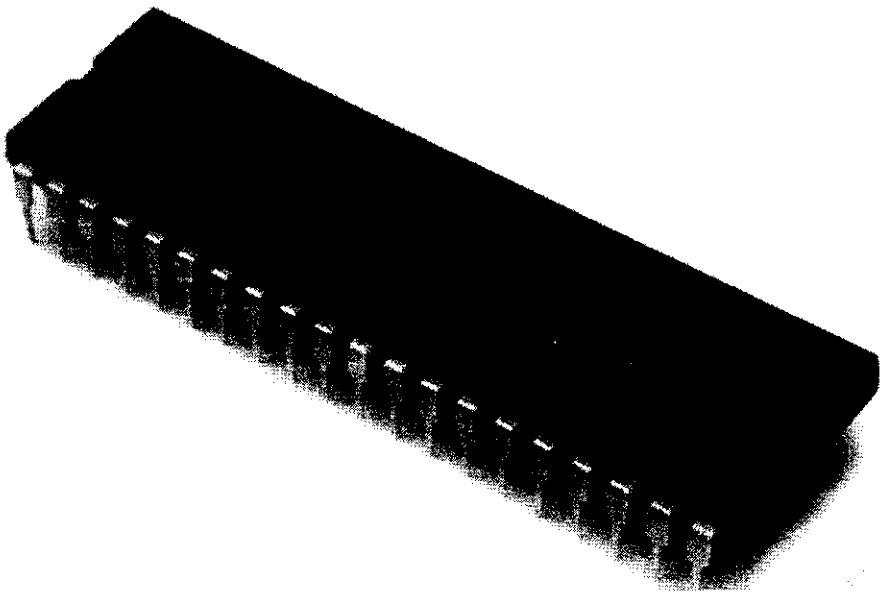


Fig 2.6 Picture of PIC 16F877 IC Microcontroller

PIC is a family of Harvard architecture microcontrollers made by Microchip Technology, derived from the PIC1640 originally developed by General Instrument's Microelectronics Division. The name PIC initially referred to "**Peripheral Interface Controller**". PICs are popular with both industrial developers and hobbyists alike due to their low cost, wide availability, large user base, extensive collection of application notes, availability of low cost or free development tools, and serial programming (and re-programming with flash memory) capability.

The powerful (200nanosecond instruction execution) yet easy-to-program (only 35 single word instructions) CMOS FLASH-based 8-bit *PIC 16F877A* microcontroller packs Microchip's powerful PIC® architecture into an 40- or 44-pin package and is upwards compatible with the PIC16C5X, PIC12CXXX and PIC16C7X devices. The PIC16F877A shown in fig 2.5 features 256 bytes of EEPROM data memory, self programming, 2 Comparators, 8 channels of 10-bit Analog-to-Digital (A/D) converter, 2 capture/compare/PWM functions, the synchronous serial port can be configured as either 3-wire SPI or the 2-wire I^2C bus and as USART. All of these features make it ideal for more advanced level A/D applications in automotive, industrial, appliances and consumer applications.

2.5 THE MAX232 IC

The MAX232 shown in fig 2.6 from Maxim was the first IC which, in one package contains the necessary drivers (two) and receivers (also two), to adapt the RS-232 signal voltage levels to TTL logic.

It became popular, because it just needs one voltage (+5V) and generates the necessary RS-232 voltage levels (approx. -10V and +10V) internally. This greatly simplified the design of circuitry. Circuitry designers no longer need to design and build a power supply with three voltages (e.g. -12V, +5V, and +12V), but could just provide one +5V power supply, e.g. with the help of a simple 78x05 voltage converter.

Fig 2.7 MAX232 IC

The MAX232 has a successor, the MAX232A. The ICs are almost identical, however, the MAX232A is much more often used (and easier to get) than the original MAX232, and the MAX232A only needs external capacitors 1/10th the capacity of what the original MAX232 needs.

2.6 ZIGBEE:

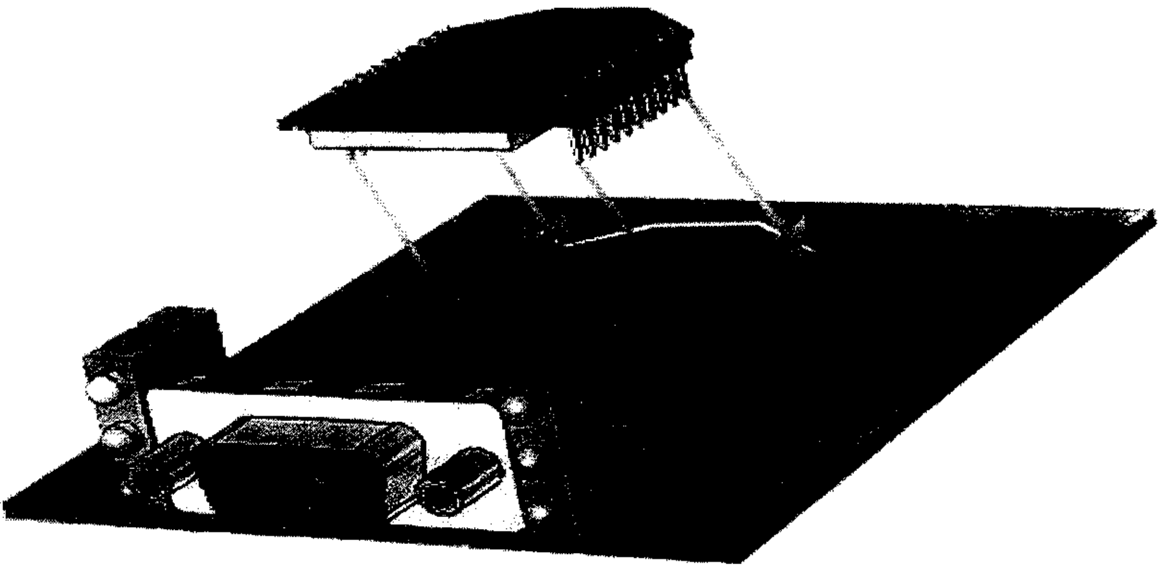


Fig 2.8 A Zigbee Module Mounting To An RS-232 Interface Board

ZigBee is a wireless technology developed as an open global standard to address the unique needs of low-cost, low-power wireless M2M networks. The ZigBee standard operates on the IEEE 802.15.4 physical radio specification and operates in unlicensed bands including 2.4 GHz, 900 MHz and 868 MHz. The ZigBee protocol is designed to communicate data through hostile RF environments that are common in commercial and industrial applications. Figure 2.8 shows a ZigBee module mounting to an RS-232 interface board.

ZigBee protocol features include:

- Support for multiple network topologies such as point-to-point, point-to-multipoint and mesh networks
- Low duty cycle – provides long battery life
- Low latency
- Direct Sequence Spread Spectrum (DSSS)
- Up to 65,000 nodes per network
- 128-bit AES encryption for secure data connections
- Collision avoidance, retries and acknowledgement

Smart energy/smart grid, AMR (Automatic Meter Reading), lighting controls, building automation systems, tank monitoring, HVAC control, medical devices and fleet applications are just some of the many spaces where ZigBee technology is making significant advancements.

2.7 MACHINE MOTOR [DC MOTOR]

Industrial applications use dc motors because the speed-torque relationship can be varied to almost any useful form -- for both dc motor and regeneration applications in either direction of rotation. Continuous operation of dc motors is commonly available over a speed range of 8:1. Infinite range (smooth control down to zero speed) for short durations or reduced load is also common.

2.8 RELAY

A relay is a simple **electromechanical switch** made up of an electromagnet and a set of contacts. Relays are found hidden in all sorts of devices. A relay is an **electrically operated switch**. Current flowing through the coil of the relay creates a magnetic field which attracts a lever and changes the switch contacts. The coil current can be on or off so relays have two switch positions and most have **double throw (changeover)** switch contacts as shown in the FIGURE 2.8

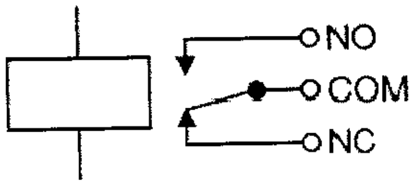


Fig 2.9 Relay

Relays are usually SPDT or DPDT but they can have many more sets of switch contacts, for example relays with 4 sets of changeover contacts are readily available. Relays are used where it is necessary to control a circuit by a low-power signal (with complete electrical isolation between control and controlled circuits), or where several circuits must be controlled by one signal. The first relays were used in long distance telegraph circuits, repeating the signal coming in from one circuit and re-transmitting it to another. Relays were used extensively in telephone exchanges and early computers to perform logical operations.

2.9 INFRA RED SENSORS

As the name implies, the sensor is always ON, meaning that the IR LED [4] is constantly emitting light. The circuit design is suitable for counting objects, or counting revolutions of a rotating object, that may be of the order 15,000 rpm or much more. However, this design is more power consuming and is not optimized for high ranges. In this design, range can be from 1 to 10 cm, depending on the ambient light conditions. A picture of QED 233 LED is shown in figure 2.10

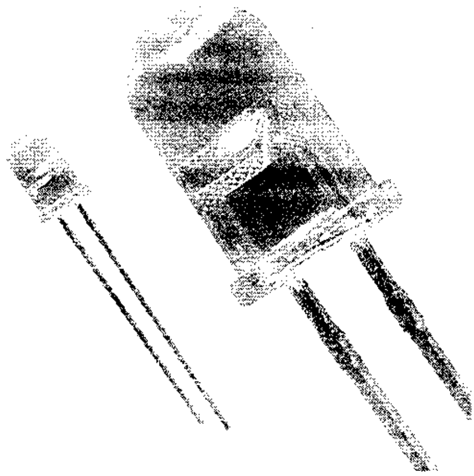


Fig 2.10 A Picture Of QED 233

2.10 GLOBAL POSOTIONING SYSTEM

The **Global Positioning System (GPS)** is a space-based global navigation satellite system (GNSS) that provides reliable location and time information in all weather and at all times and anywhere on or near the Earth when and where there is an unobstructed line of sight to four or more GPS satellites. It is maintained by the United States government and is freely accessible by anyone with a GPS receiver. Figure 2.10 shows a commercially available GPS receiver.

A GPS receiver calculates its position by precisely timing the signals sent by GPS satellites high above the Earth. Each satellite continually transmits messages that include

- the time the message was transmitted
- precise orbital information (the ephemeris)
- The general system health and rough orbits of all GPS satellites

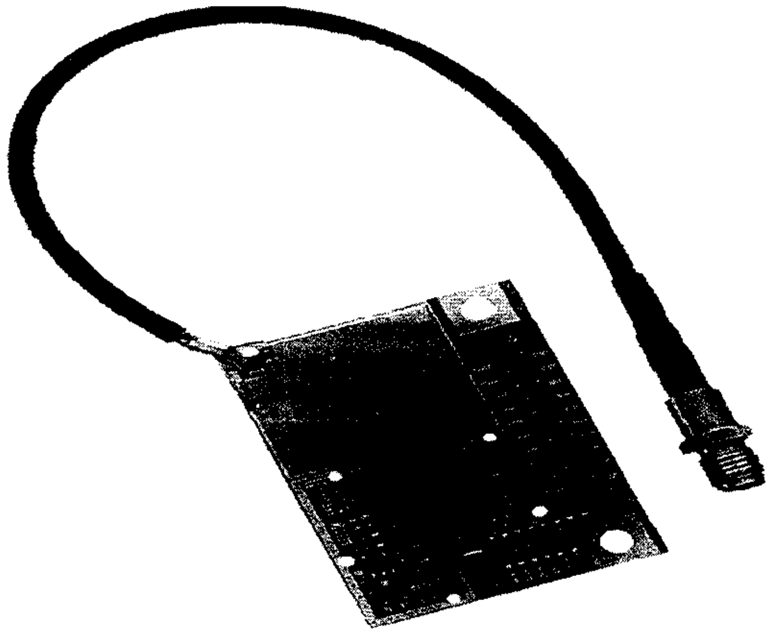


Fig 2.11 A GPS Receiver

The receiver uses the messages it receives to determine the transit time of each message and computes the distance to each satellite. These distances along with the satellites' locations are used with the possible aid of tri-lateration, depending on which algorithm is used, to compute the position of the receiver. This position is then displayed, perhaps with a moving map display or latitude and longitude; elevation information may be included. Many GPS units show derived information such as direction and speed, calculated from position changes.

2.11 REAL TIME CLOCK

A real-time clock (RTC) is a computer clock, most often in the form of an integrated circuit that keeps track of the current time. Although the term often refers to the devices in personal computers, servers and embedded systems, RTCs are present in almost any electronic device which ordinary hardware clocks which are only signals that govern digital electronics, and do not count time in human units. Although keeping time can be done without an RTC, using one has benefits namely:

- Low power consumption
- Frees the main system for time-critical tasks
- Sometimes more accurate than other methods

A GPS receiver can shorten its startup time by comparing the current time, according to its RTC, with the time at which it last had a valid signal.[2] If it has been less than a few hours then the previous ephemeris is still usable.

2.12 MATRIX KEYPADS

Matrix keypads are common devices where human has to interact with embedded system. Most common are scanning matrix keypads where rows or columns are constantly scanned to detect which buttons were pressed. A commercial 4×4 and 3×4 matrix keypad is shown in figure 2.9

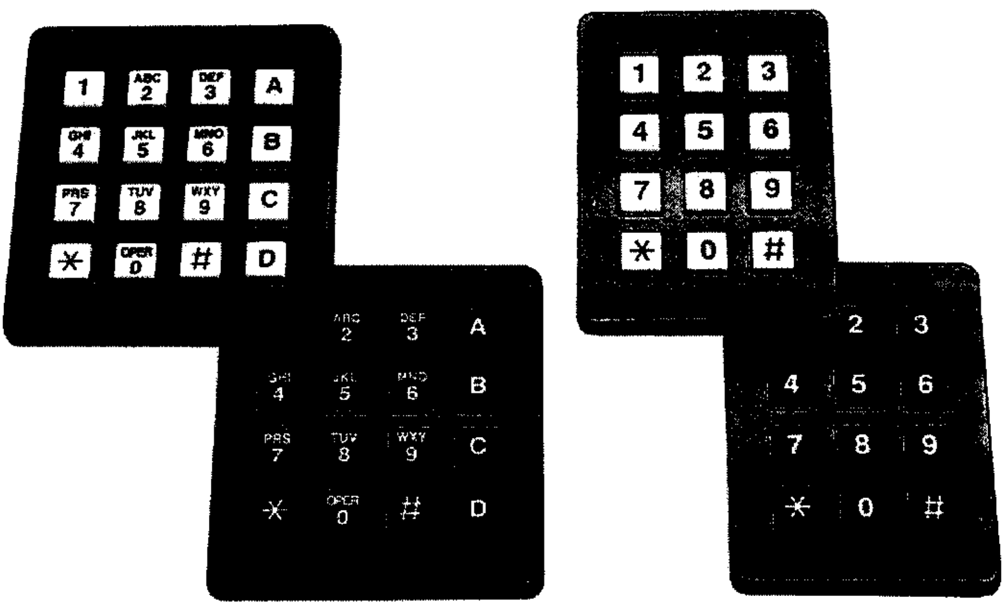


Fig 2.12 A Commercial 4×4 And 3×4 Matrix Keypad

HARDWARE DESCRIPTION

CHAPTER 3

HARDWARE DESCRIPTION

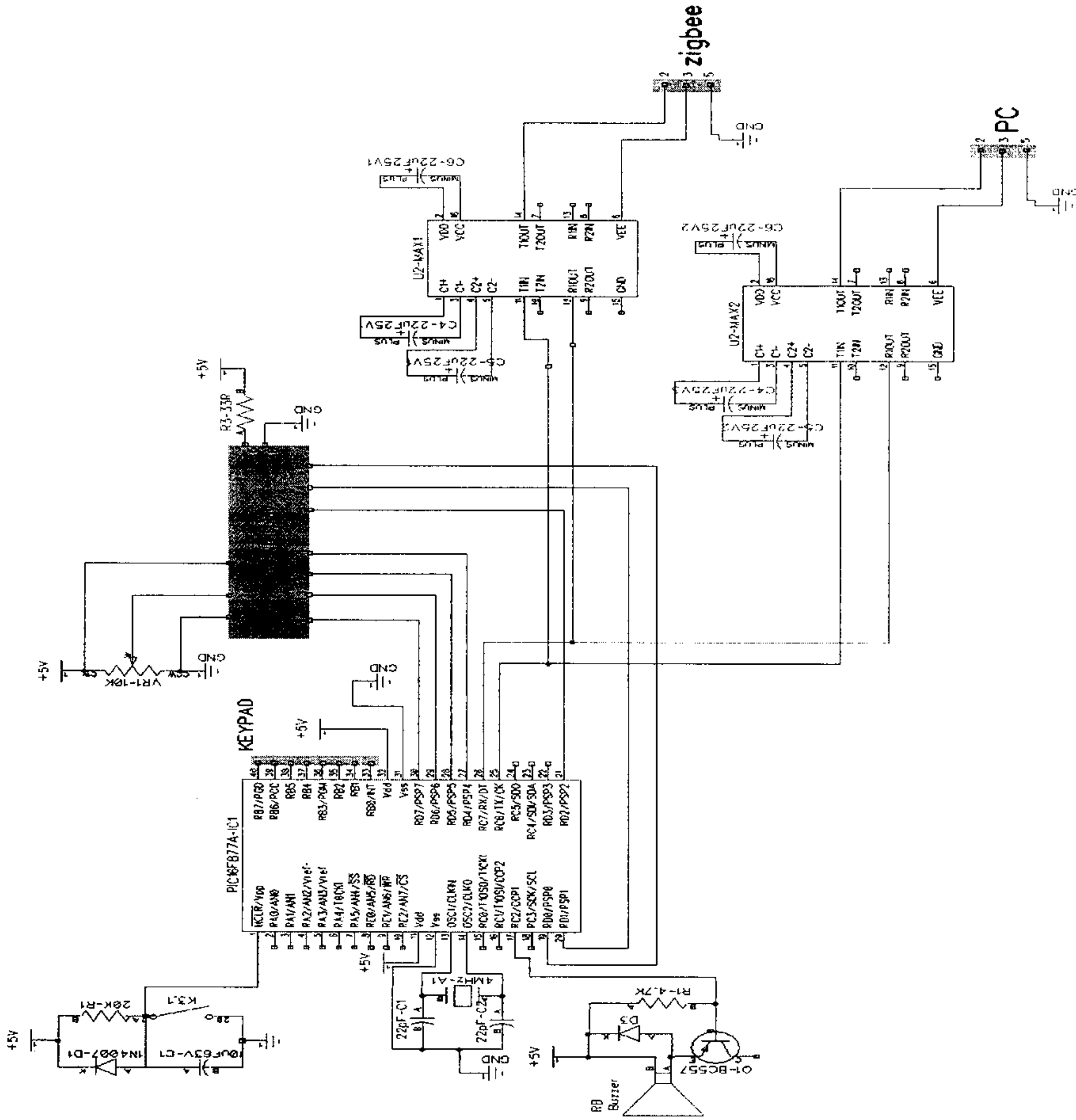


Fig 3.1 Circuit Diagram Of Controller Section

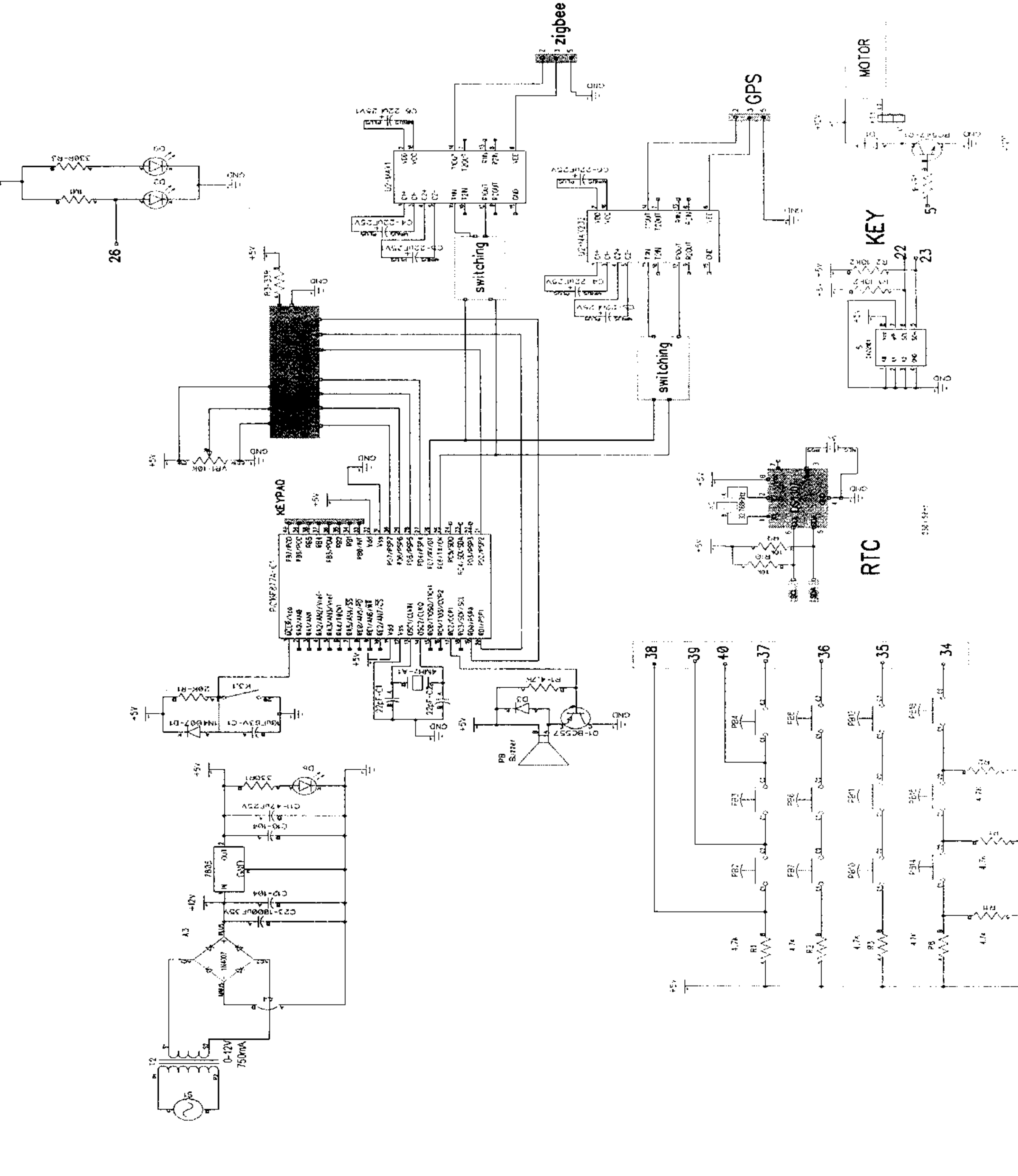


Fig 3.2 Circuit Diagram Of Vehicle Section

3.1 CIRCUIT DESCRIPTION

The needed DC voltage for the devices is obtained from the AC supply using the power supply circuit shown in figure 3.3. The PIC 16F877A Microcontroller is the CPU of the module. The necessary clock frequency for the microcontroller is given using crystal oscillator. The buzzer circuit is connected to the PWM output pin of the PIC. The data bus of LCD display is connected to the PORT D of PIC. In order to establish communication between PIC and PC, MAX232 IC is used which converts TTL/CMOS signals of PIC to RS232 signal level of computer system and vice versa.

Port C pins of PIC are connected to the driver pins of MAX232 IC. ZIGBEE module is also connected with PIC using MAX232 IC. The LEDs for RED, GREEN and YELLOW signals are connected to PORT A and PORT B of the PIC controller.

3.2 HARDWARE TOOLS

3.2.1 POWER SUPPLY

In fig 3.4.2 the actual power supply circuit is shown.

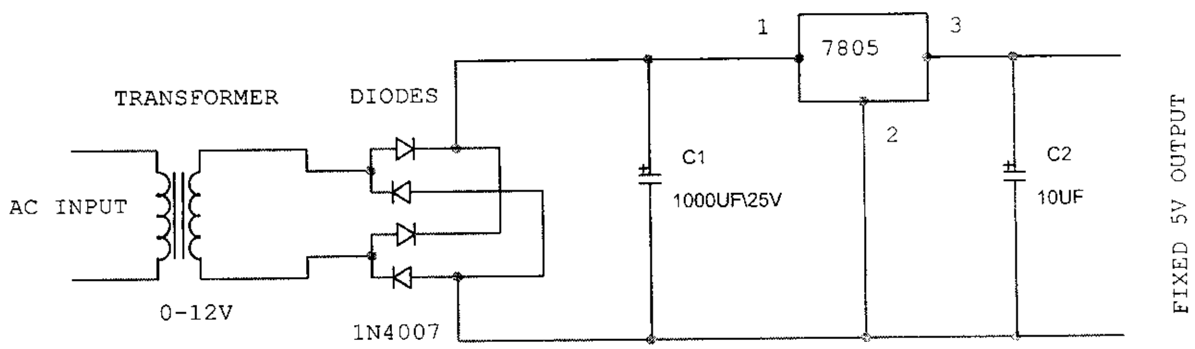


Fig 3.3 Power supply circuit diagram

The AC voltage, typically $120V_{rms}$, is connected to a transformer, which steps that AC voltage down to the level (0-12V) for the desired DC output. A diode rectifier constructed using IN4007 then provides a fullwave rectified voltage that is initially filtered by a simple capacitor filter to produce a DC voltage. This resulting DC voltage usually has some ripple or AC voltage variation. A regulator circuit can use this DC input to provide a DC voltage (fixed 5V output) that not only has much less ripple voltage but also remains the same DC value even if the input DC voltage varies somewhat, or the load connected to the output DC voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units 7805.

3.2.2 PIC MICROCONTROLLER

PIC 16F877 is one of the most advanced microcontroller from Microchip. This controller is widely used for experimental and modern applications because of its low price, wide range of applications, high quality, and ease of availability. It is ideal for applications such as machine control applications, measurement devices, study purpose, and so on.

3.2.2.1 HIGH-PERFORMANCE RISC CPU

- Only 35 single-word instructions to learn
- All single-cycle instructions except for program branches, which are two-cycle
- Operating speed: DC – 20 MHz clock input DC – 200 ns instruction cycle
- Up to 8K × 14 words of Flash Program Memory, Up to 368 × 8 bytes of Data Memory (RAM), Up to 256× 8 bytes of EEPROM Data Memory
- Pin out compatible to other 28-pin or 40/44-pin PIC16CXXX and PIC16FXXX microcontrollers.

3.2.2.2 PERIPHERAL FEATURES

- Timer0: 8-bit timer/counter with 8-bit pre-scaler
- Timer1: 16-bit timer/counter with pre-scaler, can be incremented during Sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, pre-scaler and post-scaler
- Two Capture, Compare, PWM modules
    - Capture is 16-bit, maximum resolution is 12.5 ns
    - Compare is 16-bit, maximum resolution is 200 ns
    - PWM maximum resolution is 10-bit
- Synchronous Serial Port (SSP) with SPI™
- (Master mode) and I2C™ (Master/Slave)
- Universal Synchronous Asynchronous Receiver
- Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) – 8 bits wide with external RD, WR and CS controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

3.2.2.3 ANALOG FEATURES

- 10-bit, up to 8-channel Analog-to-Digital Converter (A/D)
- Brown-out Reset (BOR)
- Analog Comparator module with:
    - Two analog comparators
    - Programmable on-chip voltage reference (VREF) module
    - Programmable input multiplexing from device inputs and internal voltage reference
    - Comparator outputs are externally accessible

3.2.2.4 SPECIAL FEATURES

- 100,000 erase/write cycle Enhanced Flash program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory typical
- Data EEPROM Retention > 40 years
- Self-reprogrammable under software control

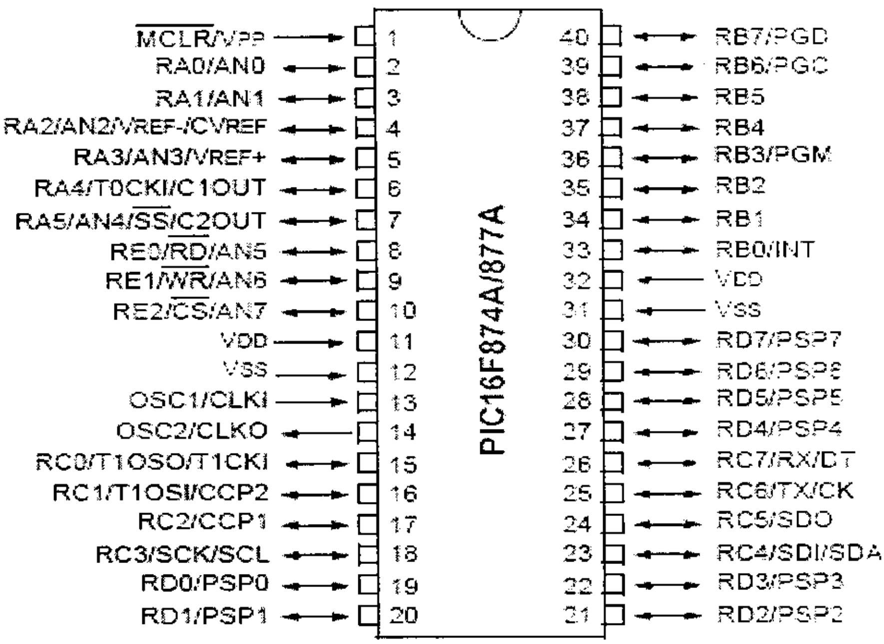


Fig 3.4 Pin details of PIC 16F877A Microcontroller

- In-Circuit Serial Programming™ (ICSP™) via two pins
- Single-supply 5V In-Circuit Serial Programming
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving Sleep mode
- Selectable oscillator options
- In-Circuit Debug (ICD) via two pins.

3.2.3 LCD DISPLAY

The pin details of LCD are shown in table 3.1

3.2.3.1 ALGORITHM TO SEND DATA TO LCD

1. Make R/W low
2. Make RS=0; if data byte is command RS=1; if data byte is data (ASCII)
3. Place data byte on data register
4. Pulse E (HIGH to LOW)
5. Repeat the steps to send another data byte

Table 3.1 Pin details of LCD

PIN NUMBER	SYMBOL	DETAILS
1	GND	Ground
2	VCC	Supply voltage
3	Vo	Contrast adjustment
4	RS	0 -> contol input 1 -> data input
5	R/W	Read/Write
6	E	Enable
7 TO 14	Do TO D7	Data
15	VB1	Backlight +5V
16	VB2	Backlight ground

3.2.3.2 LCD INITIALIZATION

Working of LCD depend on the how the LCD is initialized. We have to send few command bytes to initialize the LCD. Simple steps to initialize the LCD:

1. Specify function set:

Send **38H** for 8-bit, double line and 5×7 dot character format.

2. Display On-Off control:

Send **0FH** for display and blink cursor on.

3. Entry mode set:

Send **06H** for cursor in increment position and shift is invisible.

4. Clear display:

Send **01H** to clear display and return cursor to home position.

Table 3.2 Addresses of cursor position for 16×2 LCD

ine1	80H	81H	82H	83H	84H	85H	86H	87H	88H	89H	8AH	8BH	8CH	8DH	8EH	8F
ine2	C0H	C1H	C2H	C3H	C4H	C5H	C6H	C7H	C8H	C9H	CAH	CBH	CCH	CDH	CEH	CF

3.2.4 MAX 232 IC

The pin details of MAX 232 IC are shown in Table 3.3. The driver section consists of the pins 11 And 14 and the receiver section used comprises of the pins 13 and 12. The datasheet for MAX232 IC is attached to appendix

Table3.3 Pin details of MAX 232 IC		
Pin No	**Function**	**Name**
1	Capacitor connection pins	Capacitor 1 +
2		Capacitor 3 +
3		Capacitor 1 -
4		Capacitor 2 +
5		Capacitor 2 -
6		Capacitor 4 -
7 and 14	Output pin; outputs the serially transmitted data at RS232 logic level; connected to receiver pin of PC serial port	T_2 Out and T1out
8 and 13	Input pin; receives serially transmitted data at RS 232 logic level; connected to transmitter pin of PC serial port	R_2 In and R1 In
9 and 12	Output pin; outputs the serially transmitted data at TTL logic level; connected to receiver pin of controller.	R_2 Out and R1 out
10 and 11	Input pins; receive the serial data at TTL logic level; connected to serial transmitter pin of controller.	T_2 In and T1 In
15	Ground (0V)	Ground
16	Supply voltage; 5V (4.5V – 5.5V)	Vcc

3.2.5 ZIGBEE

The pin out details of the ZigBee module is shown in fig 3.3 The DTR, RTS, RESET and RX pins (going *into* the ZigBee) pass through a level converter chip that brings the levels to 3.3V. The data ranging between 2.7 to 5.5V can be used to communicate with the ZigBee.

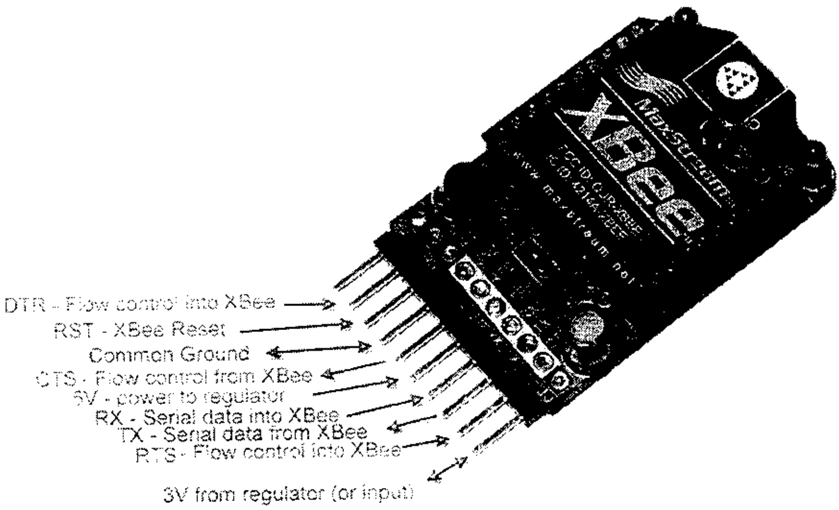


Fig 3.5 ZigBee pin out details.

3.2.6 RELAYS

A relay consists of a coil which may be energized by the low-voltage circuit and one or more sets of switch contacts which may be connected to the high-voltage circuit. In figure 3.6.a, the relay is off. The metal arm is at its rest position and so there is contact between the Normally Closed (N.C.) switch contact and the 'common' switch contact.

If a current is passed through the coil, the resulting magnetic field attracts the metal arm and there is now contact between the Normally Open (N.O.) switch contact and the common switch contact, as shown in figure 3.6.b

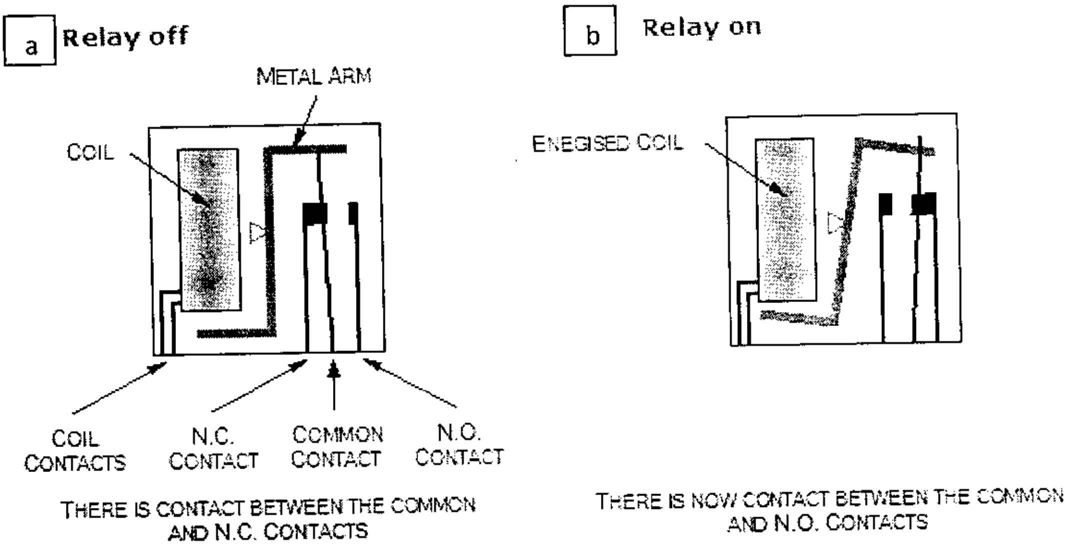


Fig 3.6 Operation Of Relay

3.2.7 REAL TIME CLOCK

The DS1307 serial real-time clock (RTC) shown in figure 3.5, is a low-power, full binary-coded decimal (BCD) Clock/calendar plus 56 bytes of NV SRAM. Address and data are transferred serially through an I2C™, bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24- hour or 12-hour format with AM/PM indicator. The DS1307 has a built-in power-sense circuit that detects power failures and automatically switches to the battery supply. The datasheet for RTC is attached in appendix

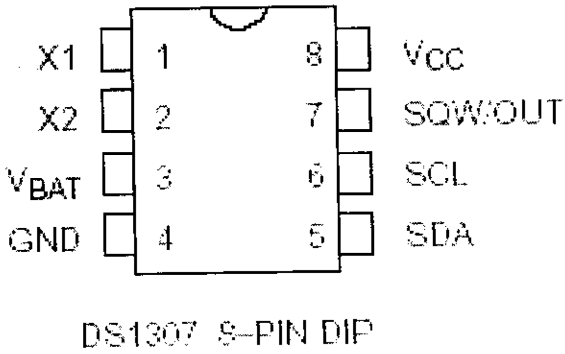


Fig 3.7 pin details of DS1307 RTC

3.3.8 GPS RECEIVER

A phase locked loop that can lock to either a positive or negative half-cycle (a bi-phase lock loop) is used to demodulate the 50 HZ navigation message from the GPS carrier signal. The same loop can be used to measure and track the carrier frequency (Doppler shift) and by keeping track of the changes to the numerically controlled oscillator, carrier frequency phase can be tracked and measured. A simplified GPS receiver block diagram is show in figure 3.6.

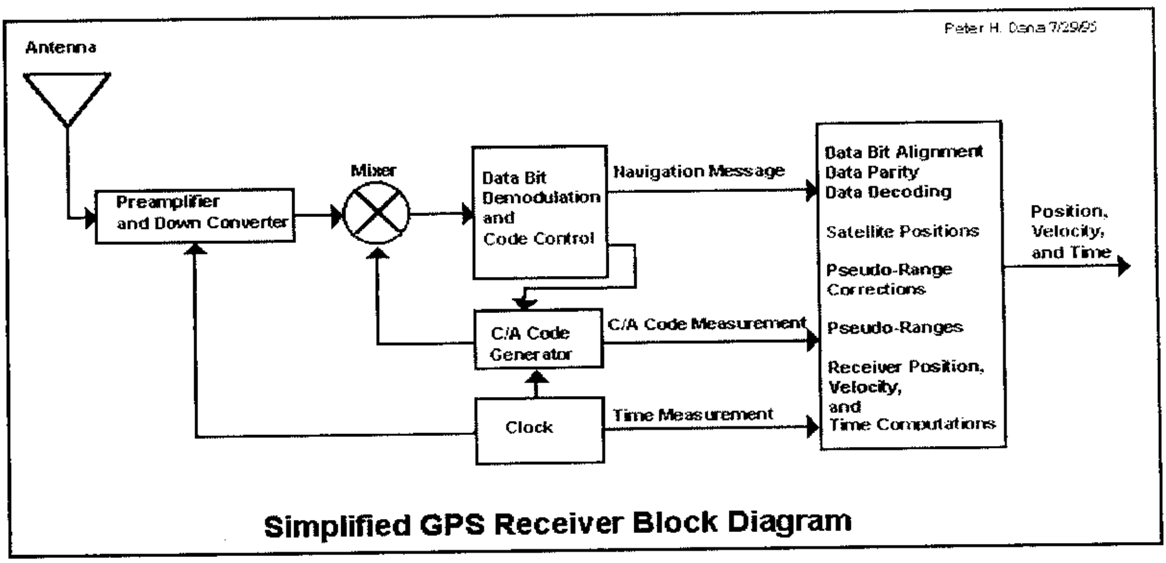


Fig 3.7 A simplified GPS receiver block diagram

SOFTWARE DESCRIPTION

CHAPTER 4

SOFTWARE DESCRIPTION

4.1 DRIVER AUTHENTICATION

4.1.1 ALGORITHM FOR DRIVER AUTHENTICATION

1. Start
2. Get password
3. Check if the password entered is correct else reenter password
4. To check the card details initiate ZigBee and transmit the data of the card holder to the service center. If the data are correct and authenticated a signal indicating permission to drive sent to the vehicle.
5. On the reception of signal, the motor turns on.
6. Now disable ZigBee and activate GPS to locate the vehicle.

4.1.2 FLOW CHART FOR DRIVER AUTHENTICATION

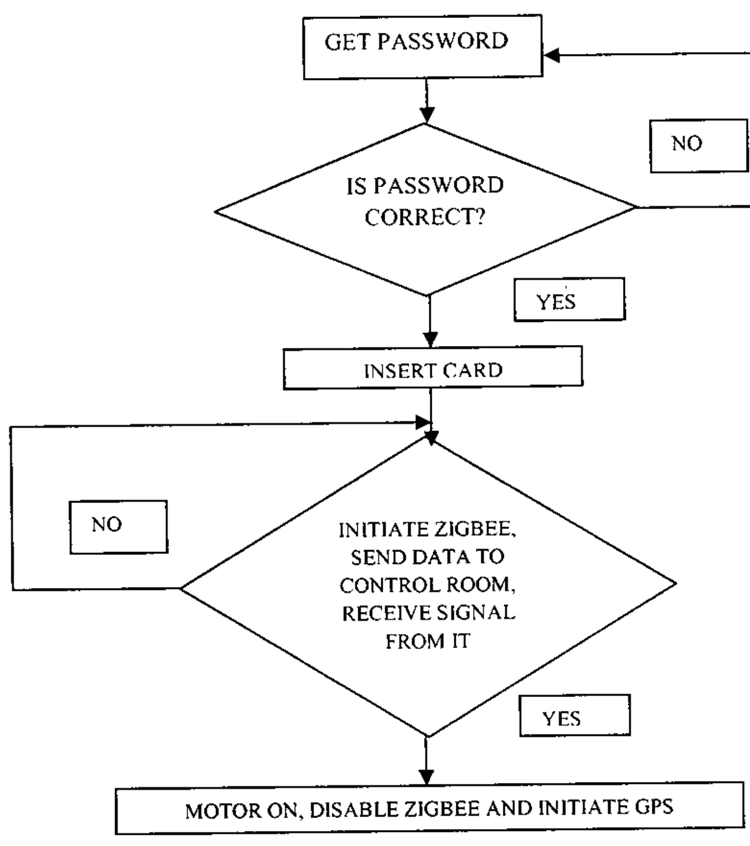


Fig 4.1 Flow Chart For Driver Authentication

4.2 TRAFFIC SIGNAL VIOLATION

4.2.1 ALGORITHM FOR TRAFFIC SIGNAL

1. Start
2. Motor will be in 'ON' condition.
3. Alert is initialized to 'zero'
4. In case of any traffic signal violation, ZigBee gets initiated.
5. An alert will be sent to the control center and the number of alerts is incremented by one.
6. In case of no violation, the system remains undisturbed.
7. If the motor turns OFF, then that license will be invalidated.
8. Motor ON
9. Request password
10. Display "Traffic signal violation."
11. Display "Please contact the nearest RTO."

4.2.2 FLOW CHART FOR TRAFFIC SIGNAL VIOLATION

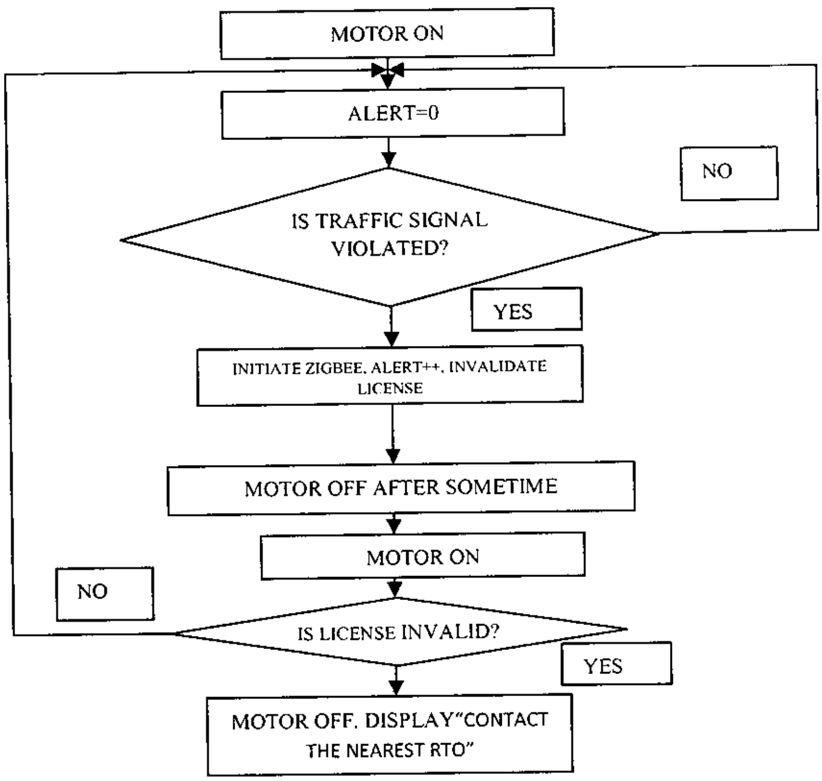


Fig 4.2 Flow Chart For Traffic Signal Violation

4.3 SPEED CONTROL

4.3.1 ALGORITHM FOR SPEED CONTROL

1. Start
2. The position is checked and if this position matches with the position in the program, then the speed is controlled.
3. Similarly the time along with the position is checked to stop the motor accordingly.

4.3.2 FLOW CHART FOR SPEED CONTROL

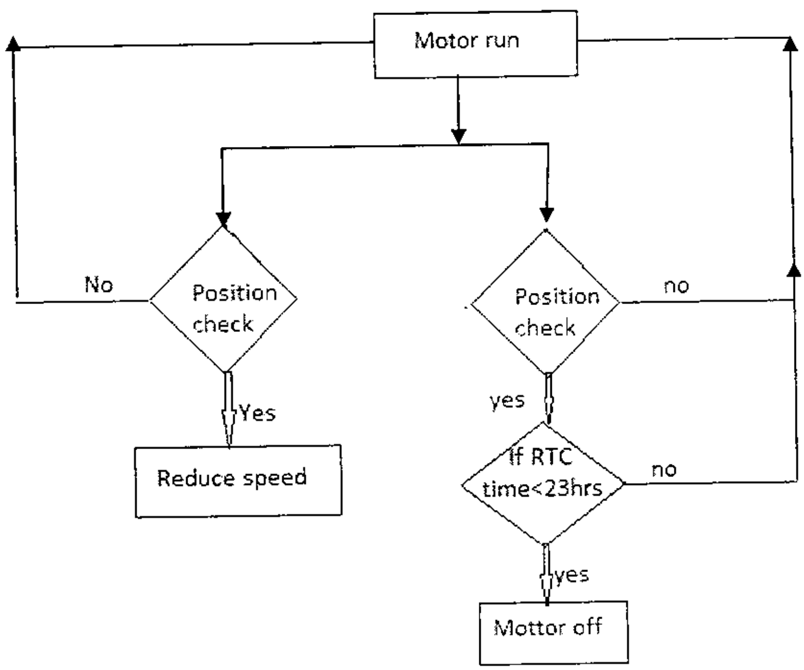


Fig 4.3 Flow Chart For Speed Control

CONCLUSION

CONCLUSION

This project, ***intelligent vehicle system***, is mainly designed to automatically control the traffic in cities without manual intervention for monitoring the violation of traffic rules and regulations and to reduce accidents.

The three ultimate aims of enquiry for license, traffic signal violation control and speed limit control are successfully implemented. This project not only tries to prevent accident occurrences, it also helps in theft prevention by password protection.

If implemented, intelligent vehicle system saves millions of precious lives and valuable properties.

REFERENCES

REFERENCES

[1] http://www.futurlec.com/Buzzers_PCB_Mount.shtml

[2] http://www.imagesco.com/microcontroller/lcd.html

[3] http://www.autoshop101.com/

[4] http://www.ictradenet.com/QED233/

[5] http://en.wikipedia.org/wiki/Real-time_clock

[6] http://www.datasheetcatalog.com/datasheets_pdf/MAX2/MAX232.html

[7] http://www.ladyada.net/make/xbee/

[8] http://www.eleinmec.com/article.asp?24

[9] http://avrmercubuana.files.wordpress.com/2010/07/ds1305_pinout.gif

[10] http://electronics.howstuffworks.com/gadgets/travel/gps.htm

APPENDICES

APPENDIX I

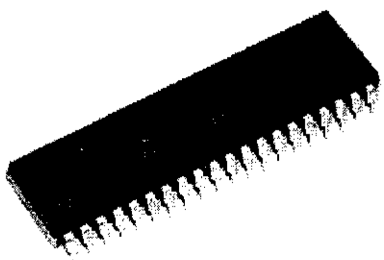
INTRODUCTION TO PIC 16F877

The basics of Peripheral Interface Controller have already been explained in recent posts. To know more about them, click on the links below.

TAKE A LOOK: PERIPHERAL INTERFACE CONTROLLER (PIC)

OVERVIEW OF PIC 16F877

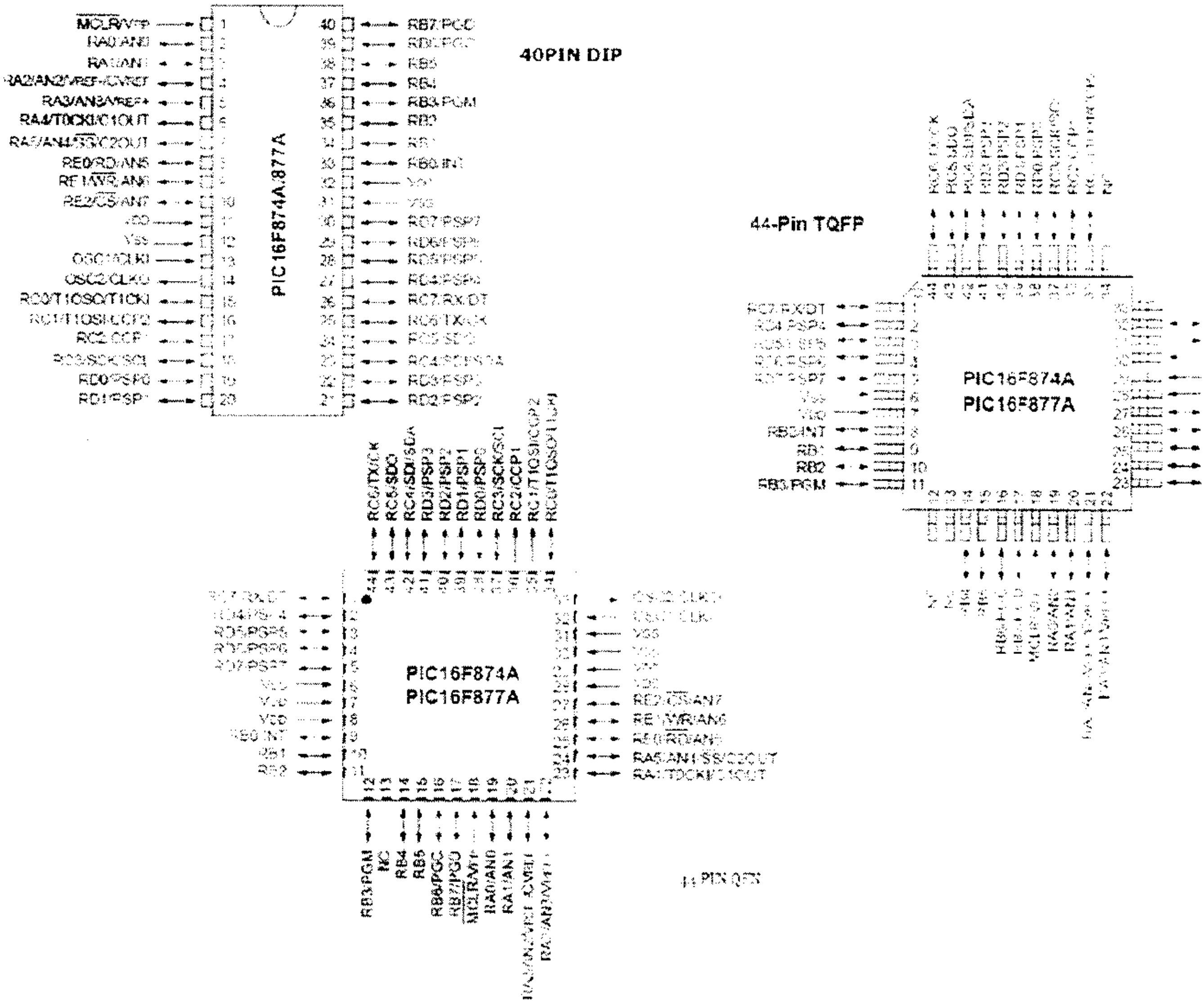
PIC 16F877 is one of the most advanced microcontroller from Microchip. This controller is widely used for experimental and modern applications because of its low price, wide range of applications, high quality, and ease of availability. It is ideal for applications such as machine control applications, measurement devices, study purpose, and so on. The PIC 16F877 features all the components which modern microcontrollers normally have. The figure of a PIC16F877 chip is shown below.



PIC 16F877

PIN DIAGRAMS

PIC16F877 chip is available in different types of packages. According to the type of applications and usage, these packages are differentiated. The pin diagram of a PIC16F877 chip in different packages is shown in the figure below.



Pin Diagrams of PIC 16F877 Chip

INPUT/OUTPUT PORTS

PIC16F877 has 5 basic input/output ports. They are usually denoted by PORT A (R A), PORT B (RB), PORT C (RC), PORT D (RD), and PORT E (RE). These ports are used for input/ output interfacing. In this controller, “PORT A” is only 6 bits wide (RA-0 to RA-7), ”PORT B” , “PORT C”,”PORT D” are only 8 bits wide (RB-0 to RB-7,RC-0 to RC-7,RD-0 to RD-7), ”PORT E” has only 3 bit wide (RE-0 to RE-7).

PORT-A	RA-0 to RA-5	6 bit wide
PORT-B	RB-0 to RB-7	8 bit wide
PORT-C	RC-0 to RC-7	8 bit wide
PORT-D	RD-0 to RD-7	8 bit wide
PORT-E	RE-0 to RE-2	3 bit wid

All these ports are bi-directional. The direction of the port is controlled by using TRIS(X) registers (TRIS A used to set the direction of PORT-A, TRIS B used to set the direction for PORT-B, etc.). Setting a TRIS(X) bit '1' will set the corresponding PORT(X) bit as input. Clearing a TRIS(X) bit '0' will set the corresponding PORT(X) bit as output.

(If we want to set PORT A as an input, just set TRIS(A) bit to logical '1' and want to set PORT B as an output, just set the PORT B bits to logical '0'.)

- Analog input port (AN0 TO AN7) : these ports are used for interfacing analog inputs.
- TX and RX: These are the USART transmission and reception ports.
- SCK: these pins are used for giving synchronous serial clock input.
- SCL: these pins act as an output for both SPI and I2C modes.
- DT: these are synchronous data terminals.
- CK: synchronous clock input.
- SD0: SPI data output (SPI Mode).

- SD1: SPI Data input (SPI mode).
- SDA: data input/output in I2C Mode.
- CCP1 and CCP2: these are capture/compare/PWM modules.
- OSC1: oscillator input/external clock.
- OSC2: oscillator output/clock out.
- MCLR: master clear pin (Active low reset).
- Vpp: programming voltage input.
- THV: High voltage test mode controlling.
- Vref (+/-): reference voltage.
- SS: Slave select for the synchronous serial port.
- T0CK1: clock input to TIMER 0.
- T1OSO: Timer 1 oscillator output.
- T1OS1: Timer 1 oscillator input.
- T1CK1: clock input to Timer 1.
- PGD: Serial programming data.
- PGC: serial programming clock.
- PGM: Low Voltage Programming input.
- INT: external interrupt.
- RD: Read control for parallel slave port.
- CS: Select control for parallel slave

- PSP0 to PSP7: Parallel slave port.
- VDD: positive supply for logic and input pins.
- VSS: Ground reference for logic and input/output pins.

ARCHITECTURE AND MEMORY ORGANIZATION OF PIC 16F877

The basic building block of PIC 16F877 is based on Harvard architecture. This microcontroller also has many advanced features as mentioned in the previous post. Here you can see the basic internal architecture and memory organisation of PIC16F877.

Take a look at the specifications of the PIC 16F87X Series

Key Features PICmicro™ Mid-Range Reference Manual (DS33023)	PIC16F873	PIC16F874	PIC16F876	PIC16F877
Operating Frequency	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz
RESETS (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
FLASH Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
EEPROM Data Memory	128	128	256	256
Interrupts	13	14	13	14
I/O Ports	Ports A,B,C	Ports A,B,C,D,E	Ports A,B,C	Ports A,B,C,D,E
Timers	3	3	3	3
Capture/Compare/PWM Modules	2	2	2	2
Serial Communications	MSSP, USART	MSSP, USART	MSSP, USART	MSSP, USART
Parallel Communications	—	PSP	—	PSP
10-bit Analog-to-Digital Module	5 input channels	8 input channels	5 input channels	8 input channels
Instruction Set	35 instructions	35 instructions	35 instructions	35 instructions

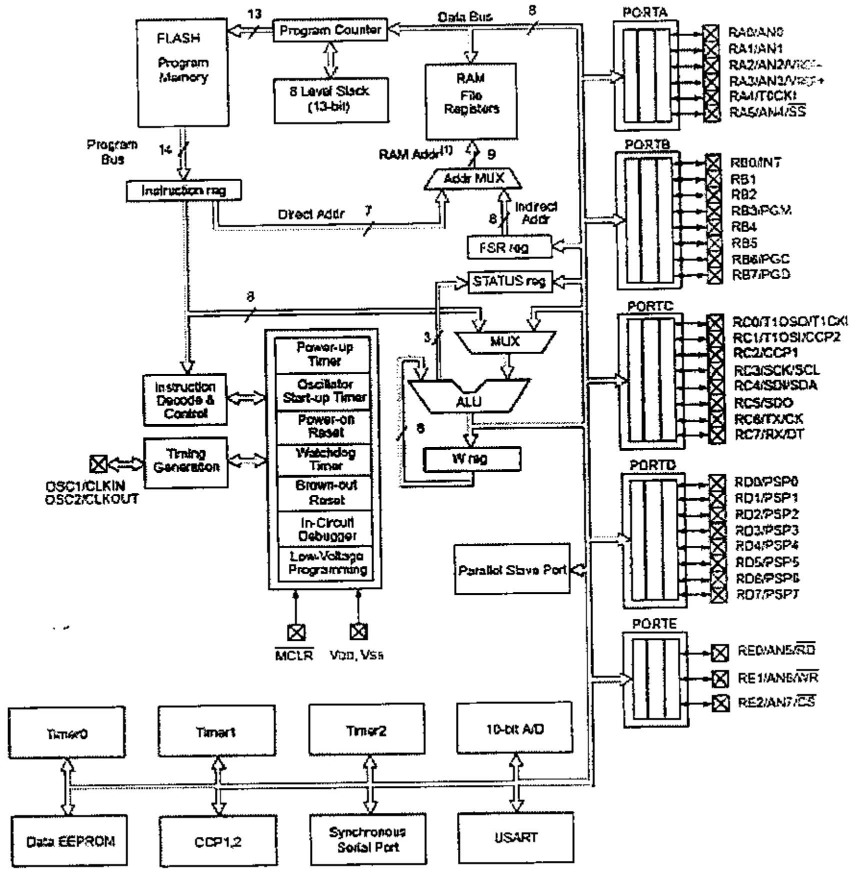
Wide operating voltage range: 2.0V to 5.5V
• High Sink/Source Current: 25 mA
• Commercial, Industrial and Extended temperature ranges
• Low-power consumption:
- < 0.6 mA typical @ 3V, 4 MHz
- 20 μA typical @ 3V, 32 kHz
- < 1 μA typical standby current

SOURCE : MICROCHIP PIC 16F87X DATA SHEET

ARCHITECTURE OF PIC16F877

The figure below shows the internal architecture of a PIC16F877A chip. The use ch functional block inside this controller has already been explained in the previous

Device	Program FLASH	Data Memory	Data EEPROM
PIC16F874	4K	192 Bytes	128 Bytes
PIC16F877	8K	368 Bytes	256 Bytes



Note 1: Higher order bits are from the STATUS register.

Internal Architecture of PIC16F877A Chip

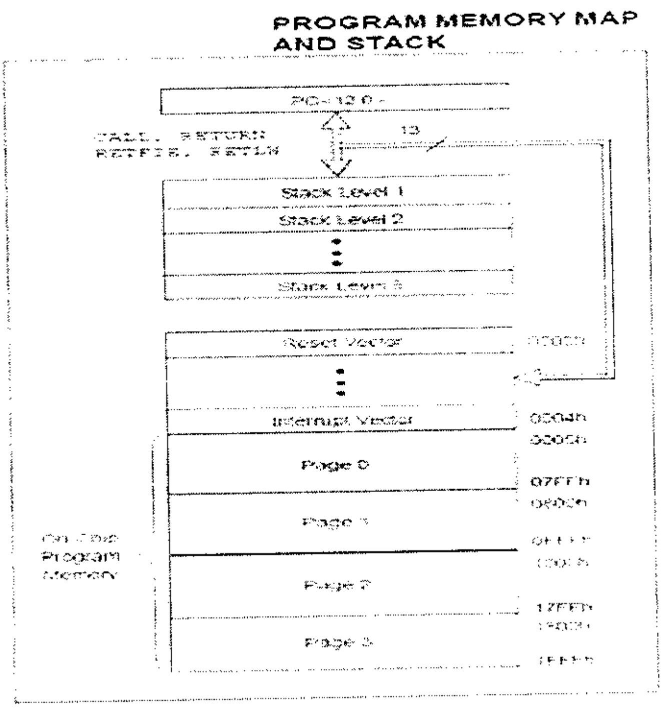
MEMORY ORGANIZATION OF PIC16F877

The memory of a PIC 16F877 chip is divided into 3 sections. They are

1. Program memory
2. Data memory and
3. Data EEPROM

1. PROGRAM MEMORY

Program memory contains the programs that are written by the user. The program counter (PC) executes these stored commands one by one. Usually PIC16F877 devices have a 13 bit wide program counter that is capable of addressing 8K×14 bit program memory space. This memory is primarily used for storing the programs that are written (burned) to be used by the PIC. These devices also have 8K*14 bits of flash memory that can be electrically erasable /reprogrammed. Each time we write a new program to the controller, we must delete the old one at that time. The figure below shows the program memory map and stack.



PIC16f877 Program Memory

Program counters (PC) is used to keep the track of the program execution by holding the address of the current instruction. The counter is automatically incremented to the next instruction during the current instruction execution.

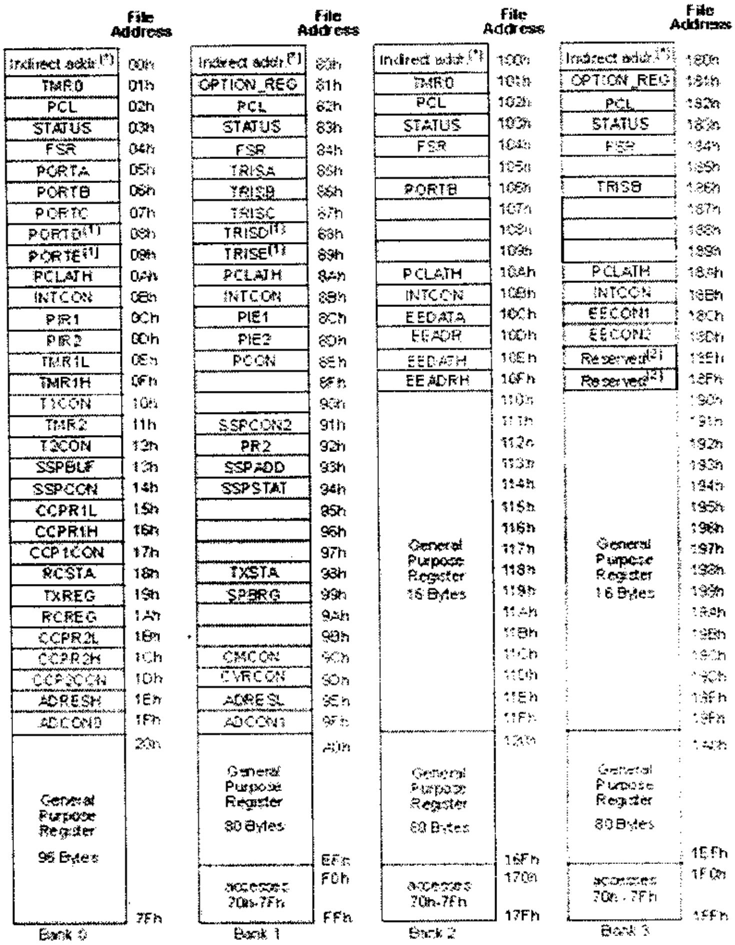
The PIC16F87XA family has an 8-level deep x 13-bit wide hardware stack. The stack space is not a part of either program or data space and the stack pointers are not readable or writable. In the PIC microcontrollers, this is a special block of RAM memory used only for this purpose.

Each time the main program execution starts at address 0000 – Reset Vector. The address 0004 is "reserved" for the "interrupt service routine" (ISR).

2. PIC16F87XA DATA MEMORY ORGANIZATION

The data memory of PIC16F877 is separated into multiple banks which contain the general purpose registers (GPR) and special function registers (SPR). According to the type of the microcontroller, these banks may vary. The PIC16F877 chip only has four banks (BANK 0, BANK 1, BANK 2, and BANK4). Each bank holds 128 bytes of addressable memory.

The banked arrangement is necessary because there are only 7 bits are available in the instruction word for the addressing of a register, which gives only 128 addresses. The selection of the banks are determined by control bits RP1, RP0 in the STATUS registers Together the RP1, RP0 and the specified 7 bits effectively form a 9 bit address. The first 32 locations of Banks 1 and 2, and the first 16 locations of Banks2 and 3 are reserved for the mapping of the Special Function Registers (SFR's).



Data Memory Organization

ANK	RP0	RP1
	0	0
	1	0
	0	1
	1	1

A bit of RP1 & RP0 of the STATUS register selects the bank access.

3. DATA EEPROM AND FLASH

The data EEPROM and Flash program memory is readable and writable during normal operation (over the full VDD range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are six SFRs used to read and write this memory:

- EECON1
- EECON2
- EEDATA
- EEDATH
- EEADR
- EEADRH

The EEPROM data memory allows single-byte read and writes. The Flash program memory allows single-word reads and four-word block writes. Program memory write operations automatically perform an erase-before write on blocks of four words. A byte write in data EEPROM memory automatically erases the location and writes the new data (erase-before-write). The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump, rated to operate over the voltage range of the device for byte or word operations.

REGISTER MEMORY ORGANIZATION IN PIC 16F877

a register is a place inside the pic which used to read or write the data/program. the memory of the pic is divided into a series of registers. Each of the registers has its own address and memory locations. These addresses are normally denoted by using hexadecimal numbers. According to the type of working and usage, the registers in PIC are classified into two categories.

GENERAL PURPOSE REGISTERS (GPR)

source : PIC16F877A data manual,microchip inc

FIGURE 2-3: PIC16F876A/877A REGISTER FILE MAP

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(1)	00h	Indirect addr.(1)	80h	Indirect addr.(1)	100h	Indirect addr.(1)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h		107h		187h
PORTD(1)	08h	TRISD(1)	88h		108h		188h
PORTE(1)	09h	TRISE(1)	89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved(2)	18Eh
TMR1H	0Fh		8Fh	EEADRH	10Fh	Reserved(2)	18Fh
T1CON	10h		90h	General Purpose Register 16 Bytes	110h	General Purpose Register 16 Bytes	190h
TMR2	11h	SSPCON2	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h		95h		115h		195h
CCPR1H	16h		96h		116h		196h
CCP1CON	17h		97h		117h		197h
RCSTA	18h	TXSTA	98h		118h		198h
TXREG	19h	SPBRG	99h		119h		199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh		19Bh
CCPR2H	1Ch	CMCON	9Ch		11Ch		19Ch
CCP2CON	1Dh	CVRCON	9Dh		11Dh		19Dh
ADRESH	1Eh	ADRESL	9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h	General Purpose Register 80 Bytes	A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h
			EFh		16Fh		1EFh
		accesses 70h-7Fh	F0h	accesses 70h-7Fh	170h	accesses 70h - 7Fh	1F0h
	7Fh		FFh		17Fh		1FFh

☐ Unimplemented data memory locations, read as '0'.
* Not a physical register

GPR is a small amount of storage that can be accessible more quickly than any other memory. These register files can be accessed either directly, or indirectly, through the File Select Register (FSR). The General Purpose Register (GPR) memory map (PIC16F877A) is shown in the figure below.

SPECIAL FUNCTION REGISTERS (SFR)

The special function registers are also memory registers which is used for special dedicated functions. These registers perform various dedicated functions inside the PIC chip. Each special function inside this PIC chip is controlled by using these registers. These registers are used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are normally implemented as in the form of static RAM memory. A list of these registers is given in the tables below. The Special Function Registers can be classified into two sets: core (CPU) and peripheral. Those registers associated with the core functions are described in detail in this section. The figures below shows SFR memory map of PIC16F877.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Deta on pa
Bank 0											
00h[3]	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	31, 1
01h	TMR0	Timer0 Module Register								xxxx xxxx	55, 1
02h[3]	PCL	Program Counter (PC) Least Significant Byte								0000 0000	30, 1
03h[3]	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	22, 1
04h[3]	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	31, 1
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--0x 0000	43, 1
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	45, 1
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	47, 1
08h[4]	PORTD	PORTD Data Latch when written: PORTD pins when read								xxxx xxxx	48, 1
09h[4]	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	49, 1
0Ah[1,3]	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	30, 1
0Bh[3]	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	24, 1
0Ch	PIR1	PSPIF[3]	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	26, 1
0Dh	PIR2	—	CMIF	—	EEIF	BCLIF	—	—	CCP2IF	-0-0 0--0	28, 1
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	60, 1
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	60, 1
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000	57, 1
11h	TMR2	Timer2 Module Register								0000 0000	62, 1
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	61, 1
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	79, 1
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	82, 9 15
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	63, 1
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	63, 1
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	64, 1
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	112, 1
19h	TXREG	USART Transmit Data Register								0000 0000	118, 1
1Ah	RCREG	USART Receive Data Register								0000 0000	118, 1
1Bh	CCPR2L	Capture/Compare/PWM Register 2 (LSB)								xxxx xxxx	63, 1
1Ch	CCPR2H	Capture/Compare/PWM Register 2 (MSB)								xxxx xxxx	63, 1
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	64, 1
1Eh	ADRESH	A/D Result Register High Byte								xxxx xxxx	133, 1
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	—	ADON	0000 00-0	127, 1

Special Function Registers (SFR) - PIC 16F877

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR. BOR	Details on page:
Bank 1											
80h(3)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	31, 150
81h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	23, 150
82h(3)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	30, 150
83h(3)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	22, 150
84h(3)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	31, 150
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	43, 150
86h	TRISB	PORTB Data Direction Register								1111 1111	45, 150
87h	TRISC	PORTC Data Direction Register								1111 1111	47, 150
88h(4)	TRISD	PORTD Data Direction Register								1111 1111	48, 151
89h(4)	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction bits			0000 -111	50, 151
8Ah(1,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	30, 150
8Bh(3)	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	24, 150
8Ch	PIE1	PSPIE(2)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	25, 151
8Dh	PIE2	—	CMIE	—	EEIE	BCLIE	—	—	CCP2IE	-0-0 0--0	27, 151
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	---- --qq	29, 151
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	83, 151
92h	PR2	Timer2 Period Register								1111 1111	62, 151
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	79, 151
94h	SSPSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	79, 151
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	111, 151
99h	SPBRG	Baud Rate Generator Register								0000 0000	113, 151
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	135, 151
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	141, 151
9Eh	ADRESL	A/D Result Register Low Byte								xxxx xxxx	133, 151
9Fh	ADCON1	ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0	00-- 0000	128, 151

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note

1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.

2: Bits PSPIE and PSPIF are reserved on PIC16F873A/876A devices; always maintain these bits clear.

3: These registers can be addressed from any bank.

4: PORTD, PORTE, TRISD and TRISE are not implemented on PIC16F873A/876A devices, read as '0'.

5: Bit 4 of EEADRH implemented only on the PIC16F876A/877A devices.

source: PIC16F877A data manual, microchip.inc

Special Function Registers (SFR) - PIC 16F877

STATUS REGISTER

Status register is an eight bit register that contains the arithmetic status of the arithmetic logic unit (ALU), the reset status and the bank select bits for the data memory. The detailed explanation of status register is given below.

Status registers (address 03h, 83h, 103h, and 183h)

R/W*-0	**R/W-0**	**R/W-0**	**R-1**	**R-1**	**R/W-x****	**R/W-x**	**R/W-x**
IRP	**RP1**	**RP0**	**TO**	**PD**	**Z**	**DC**	**C**

Bit7

Bit 0

(*R/W-readable/writable, **x-unknown bit)

- Bit 7 – (IRP): this is a Register Bank Select Bit usually used for indirect addressing mode.
- Bit 6-5 (RP1:RP0): these bits are Register Bank Select bits commonly used for direct addressing mode (each banks in this mode carry 128 byes)

(11 = Bank 3 (180h-1FFh)

10 = Bank 2 (100h-17Fh)

01 = Bank 1 (80h-FFh)

00 = Bank 0 (00h-7Fh))

- Bit 4, (TO): this is a time-out bit used for timing and counting, sleep and reset functions.

(1 = after power-up, CLRWDT instruction or SLEEP instruction

0 = A WDT time-out occurred)

- Bit 3, (PD): Power-down bit

(1 = after power-up or by the CLRWDT instruction

0 = by execution of the SLEEP instruction)

- Bit 2, (Z): Zero bit

(1 = the result of an arithmetic or logic operation is zero

0 = the result of an arithmetic or logic operation is not zero.)

- Bit 1 DC: Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)

(For borrow, the polarity is reversed)

(1 = A carry-out from the 4th low order bit of the result occurred

0 = No carry-out from the 4th low order bit of the result.)

- Bit 0 (C): Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)

(1 = A carry-out from the Most Significant bit of the result occurred

0 = No carry-out from the Most Significant bit of the result occurred.)

OPTION REGISTER

The option Register is a readable and writable register, which contains various control bits to configure the TMR0 prescaler/WDT postscaler (single assignable register known also as the pre-scaler), the external INT interrupt andTMR0 and the weak pull-ups on PORTB. Structure of option register is shown below.

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU(inverting)	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Bit7 Bi

t 0

- Bit 7 (RBPU): This is a PORTB Pull-up Enable bit. If this bit is '1' then PORTB pull-up function disabled. If this bit is '0', it enabled the pull-up function by individual port-latch values.

(1 = PORTB pull-ups are disabled.

0 = PORTB pull-ups are enabled by individual port latch values.)

- Bit 6 (INTEDG): This is an Interrupt Edge Select bit. This bit decided if the interrupt is on either raisin edge or falling edge. The function of this bit is given below.

(1 = Interrupt on rising edge of RB0/INT pin.

0 = Interrupt on falling edge of RB0/INT pin.)

- Bit 5 (T0CS): this is a timer-0(TMR0) Clock Source Select bit and

(1 = Transition on RA4/T0CKI pin.

0 = Internal instruction cycle clock (CLKO).)

- Bit 4 (T0SE): TMR0 Source Edge Select bit which select the timer 0 source edge.

(1 = Increment on high-to-low transition on RA4/T0CKI pin.

0 = Increment on low-to-high transition on RA4/T0CKI pin.)

- Bit 3 (PSA): Prescaler Assignment bit.

(1 = Prescaler is assigned to the Watch Dog Timer (WDT).

0 = Prescaler is assigned to the Timer0 module.)

- Bit 2-0 (PS2:PS0): Prescaler Rate Select bits.

INTCON REGISTER

The INTCON register is a readable and writable register, which contains various enable and flag bits for the

TMR0 register overflow, RB port change and external RB0/INT pin interrupts. The architecture of this register is given below.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF

- Bit 7 GIE: Global Interrupt Enable bit. If this bit is enable ('1'), which also enable all unmasked interrupts and if it is zero ('0'), which disable all interrupts.

(1 = Enables all unmasked interrupts.

0 = Disables all interrupts.)

- Bit 6 (PEIE): this is a Peripheral Interrupt Enable bit which used for controlling peripheral interrupts. If this bit is enable('1'), also enable all unmasked peripheral interrupts and if it is disable('0'), also disable all active peripheral interrupt actions.

(1 = Enables all unmasked peripheral interrupts

0 = Disables all peripheral interrupts)

- Bit 5 (TMR0IE): This is timer 0(TMR0) Overflow Interrupt Enable bit which control the overflow interrupt in timer 0.

(1 = Enables the TMR0 interrupt

0 = Disables the TMR0 interrupt)

- Bit 4 (INTE): This is an RB0/INT External Interrupt Enable bit which used for enable/disable external interrupts.

(1 = Enables the RB0/INT external interrupt

0 = Disables the RB0/INT external interrupt)

- Bit 3 (RBIE): RB Port Change Interrupt Enable bit which control PORTB change interrupt.

(1 = Enables the RB port change interrupt.

0 = Disables the RB port change interrupt.)

- Bit 2 (TMR0IF): TMR0 Overflow Interrupt Flag bit which controls the overflow of timer 0.

(1 = TMR0 register has overflowed [must be cleared in software]

0 = TMR0 register did not overflow)

- Bit 1 (INTF): RB0/INT External Interrupt Flag control bit.

(1 = The RB0/INT external interrupt occurred (must be cleared in software)

0 = The RB0/INT external interrupt did not occur).

- Bit 0 (RBIF): RB Port Change Interrupt Flag bit.

(1 = At least one of the RB7:RB4 pins changed state; a mismatch condition will continue to set that bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared

[Must be cleared in software]).

PIE1 REGISTER

The PIE1 register contains the individual enable bits for the peripheral interrupts. The structure of this register is shown below.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE

- Bit 7 (PSPIE): this bit is the Parallel Slave Port Read/Write Interrupt Enable bit

(1 = Enables the PSP read/write interrupt

0 = Disables the PSP read/write interrupt)

- Bit 6 (ADIE): A/D Converter Interrupt Enable bit which control the analog to digital converter interrupt.

(1 = Enables the A/D converter interrupt

0 = Disables the A/D converter interrupt)

- Bit 5 (RCIE): USART Receive Interrupt Enable bit which control the USART data reception interrupt.

(1 = Enables the USART receive interrupt

0 = Disables the USART receive interrupt)

- Bit 4 (TXIE): USART Transmit Interrupt Enable bit that control USART data transmission.

(1 = Enables the USART transmit interrupt

0 = Disables the USART transmit interrupt)

- Bit 3 (SSPIE): Synchronous Serial Port Interrupt Enable bit that control SSP data interrupt.

(1 = Enables the SSP interrupt

0 = Disables the SSP interrupt)

- Bit 2 (CCP1IE): CCP1 Interrupt Enable bit which control the capture-compare-pulse width modulation interrupt.

(1 = Enables the CCP1 interrupt

0 = Disables the CCP1 interrupt)

- Bit 1 (TMR2IE): TMR2 to PR2 Match Interrupt Enable bit.

(1 = Enables the TMR2 to PR2 match interrupt

0 = Disables the TMR2 to PR2 match interrupt)

- Bit 0 (TMR1IE): TMR1 Overflow Interrupt Enable bit that control the overflow interrupt of timer 1 module.

(1 = Enables the TMR1 overflow interrupt

0 = Disables the TMR1 overflow interrupt)

PIR1 REGISTER

The PIR1 register contains the individual flag bits for the peripheral interrupt. The structure of PIR1 register is given below.

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF

- Bit 7 (PSPIF): Parallel Slave Port Read/Write Interrupt Flag bit.

(1 = A read or a write operation has taken place (must be cleared in software)

0 = No read or write has occurred)

- Bit 6 (ADIF): A/D Converter Interrupt Flag bit that control the interrupt flag for that analog to digital converter.

(1 = An A/D conversion completed

0 = The A/D conversion is not complete)

- Bit 5 (RCIF): USART Receive Interrupt Flag bit.

(1 = The USART receive buffer is full

0 = The USART receive buffer is empty)

- Bit 4 (TXIF): USART Transmit Interrupt Flag bit.

(1 = The USART transmit buffer is empty

0 = The USART transmit buffer is full)

- Bit 3 (SSPIF): Synchronous Serial Port (SSP) Interrupt Flag bit that control the SSP interrupt flag in a PIC.

(1 = The SSP interrupt condition has occurred and must be cleared in software before returning from the Interrupt Service Routine. The conditions that will set this bit are:

• SPI – A transmission/reception has taken place.

• I2C Slave – A transmission/reception has taken place.

• I2C Master

- A transmission/reception has taken place.

- The initiated Start condition was completed by the SSP module.

- The initiated Stop condition was completed by the SSP module.

- The initiated Restart condition was completed by the SSP module.

- The initiated Acknowledge condition was completed by the SSP module.

- A Start condition occurred while the SSP module was Idle (multi-master system).

- A Stop condition occurred while the SSP module was Idle (multi-master system).

0 = No SSP interrupt condition has occurred)

- Bit 2 (CCP1IF): CCP1 Interrupt Flag bit that control capture-compare-pulse width modulation interrupt flag. It works in three modes. They are given below.

1. Capture mode:

1 = A TMR1 register capture occurred (must be cleared in software)

0 = No TMR1 register capture occurred

2. Compare mode:

1 = A TMR1 register compare match occurred (must be cleared in software)

0 = No TMR1 register compare match occurred

3. PWM mode:

- Bit 1 (TMR2IF): TMR2 to PR2 Match Interrupt Flag bit

(1 = TMR2 to PR2 match occurred (must be cleared in software)

0 = No TMR2 to PR2 match occurred)

- Bit 0 (TMR1IF): TMR1 Overflow Interrupt Flag bit.

(1 = TMR1 register overflowed (must be cleared in software)

0 = TMR1 register did not overflow)

PIE2 REGISTER

The PIE2 register contains the individual enable bits for the CCP2 peripheral interrupt, the SSP bus collision

Interrupt, EEPROM write operation interrupt and the comparator interrupt. The structure of this register is given below.

U-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0
—	CMIE	—	EEIE	BCLIE	—	—	CCP2IE

- Bit 7 Unimplemented: Read as '0'
- Bit 6 (CMIE): Comparator Interrupt Enable bit

(1 = Enables the comparator interrupt

0 = Disable the comparator interrupt)

- Bit 5 Unimplemented: Read as '0'

Bit 4 (EEIE): EEPROM Write Operation Interrupt Enable bit

(1 = Enable EEPROM write interrupt

0 = Disable EEPROM write interrupt)

- Bit 3 (BCLIE): Bus Collision Interrupt Enable bit.

(1 = Enable bus collision interrupt

0 = Disable bus collision interrupt)

- Bit 2-1 Unimplemented: Read as '0'
- Bit 0 (CCP2IE): CCP2 Interrupt Enable bit.

(1 = Enables the CCP2 interrupt

0 = Disables the CCP2 interrupt)

PIR2 REGISTER

The PIR2 register contains the flag bits for the CCP2 interrupt, the SSP bus collision interrupt, EEPROM write operation interrupt and the comparator interrupt. The structure of this register is given below.

U-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0
—	CMIF	—	EEIF	BCLIF	—	—	CCP2IF

- Bit 7 Unimplemented: Read as '0'
- Bit 6 (CMIF): Comparator Interrupt Flag bit

(1 = the comparator input has changed (must be cleared in software)

0 = the comparator input has not changed)

- Bit 5 Unimplemented: Read as '0'
- Bit 4 (EEIF): EEPROM Write Operation Interrupt Flag bit.

(1 = the write operation completed (must be cleared in software)

0 = the write operation is not complete or has not been started)

- Bit 3 (BCLIF): Bus Collision Interrupt Flag bit.

(1 = A bus collision has occurred in the SSP when configured for I2C Master Mode

0 = No bus collision has occurred)

- Bit 2-1 Unimplemented: Read as '0'
- Bit 0 (CCP2IF): CCP2 Interrupt Flag bit. This also works in three modes. They ere

1. Capture mode:

1 = A TMR1 register capture occurred (must be cleared in software)

0 = No TMR1 register capture occurred

Compare mode:

1 = A TMR1 register compare match occurred (must be cleared in software)

0 = No TMR1 register compare match occurred

2. PWM mode:

This mode is not used.

PCON REGISTER

The Power Control (PCON) register contains flag bits to allow differentiation between a Power-on Reset

(POR), a Brown-out Reset (BOR), a Watchdog Reset (WDT) and an external MCLR Reset. The structure of this register is given below.

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-1
____	____	____	____	____	____	POR(inverting)	BOR(inverting)

- Bit 7-2 Unimplemented: Read as ‘0’
- Bit 1 (POR): Power-on Reset Status bit

(1 = No Power-on Reset occurred

0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

Bit 0 (BOR): Brown-out Reset Status bit

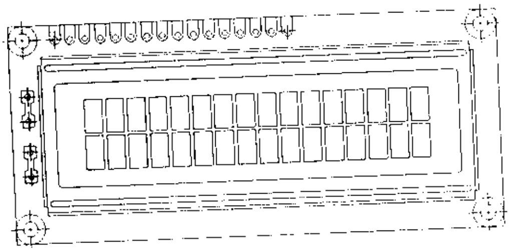
(1 = No Brown-out Reset occurred

0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs).

APPENDIX II

VISHAY

16 x 2 Character LCD



FEATURES

- 5 x 8 dots with cursor
- Built-in controller (KS 0066 or Equivalent)
- + 5V power supply (Also available for + 3V)
- 1/16 duty cycle
- B/L to be driven by pin 1, pin 2 or pin 15, pin 16 or A.K (LED)
- N.V. optional for + 3V power supply

MECHANICAL DATA

ITEM	STANDARD VALUE	UNIT
Module Dimension	80.0 x 36.0	mm
Viewing Area	66.0 x 16.0	mm
Dot Size	0.56 x 0.66	mm
Character Size	2.96 x 5.56	mm

ABSOLUTE MAXIMUM RATING

ITEM	SYMBOL	STANDARD VALUE			UNIT
		MIN.	TYP.	MAX.	
Power Supply	VDD-VSS	- 0.3	–	7.0	V
Input Voltage	VI	- 0.3	–	VDD	V

NOTE: VSS = 0 Volt, VDD = 5.0 Volt

ELECTRICAL SPECIFICATIONS

ITEM	SYMBOL	CONDITION		STANDARD VALUE			UNIT
				MIN.	TYP.	MAX.	
Input Voltage	VDD	VDD = + 5V		4.7	5.0	5.3	V
		VDD = + 3V		2.7	3.0	5.3	V
Supply Current	IDD	VDD = 5V		–	1.2	3.0	mA
Recommended LC Driving Voltage for Normal Temp. Version Module	VDD - V0	- 20 °C		–	–	–	V
		0°C		4.2	4.8	5.1	
		25°C		3.8	4.2	4.6	
		50°C		3.6	4.0	4.4	
		70°C		–	–	–	
LED Forward Voltage	VF	25°C		–	4.2	4.6	V
LED Forward Current	IF	25°C	Array	–	130	260	mA
			Edge	–	20	40	
EL Power Supply Current	IEL	Vel = 110VAC:400Hz		–	–	5.0	mA

DISPLAY CHARACTER ADDRESS CODE:

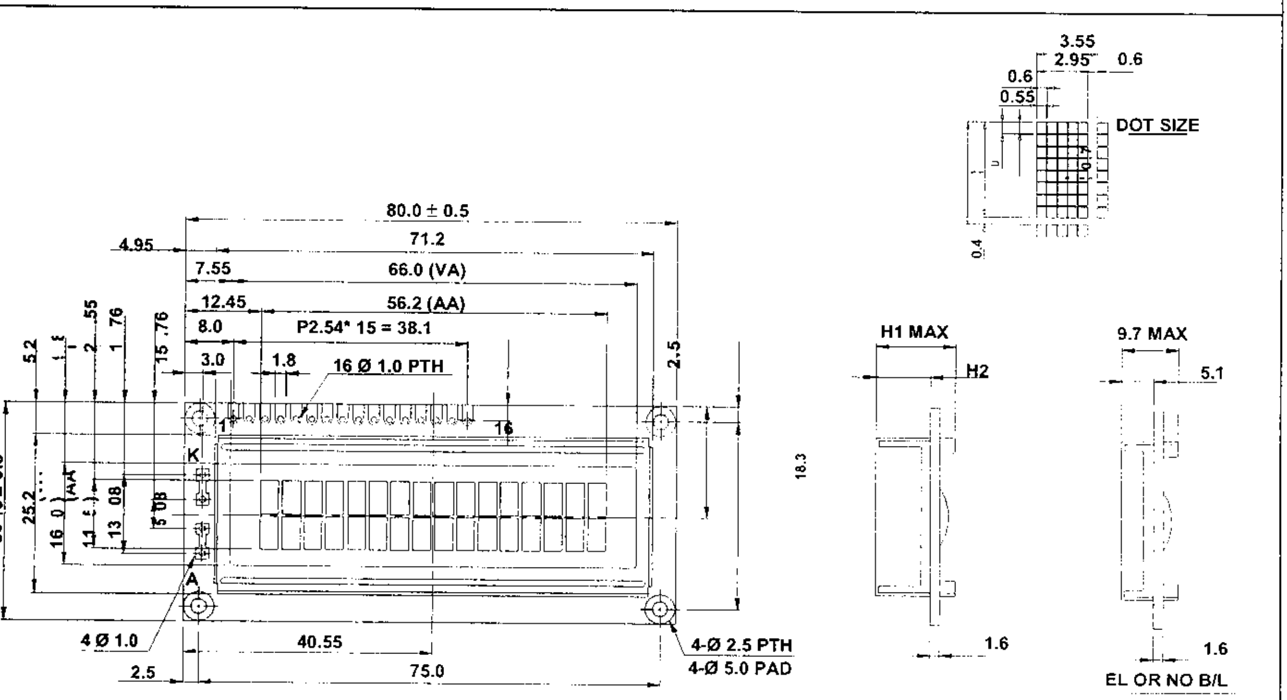
Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM Address	00	01														0F
DD RAM Address	40	41														4F

CD-016M002B

ishay — 16 x 2 Character LCD

PIN NUMBER	SYMBOL	FUNCTION
	Vss	GND
2	Vdd	+ 3V or + 5V
3	Vo	Contrast Adjustment
4	RS	H/L Register Select Signal
5	R/$\overline{W}$	H/L Read/Write Signal
6	E	H → L Enable Signal
7	DB0	H/L Data Bus Line
8	DB1	H/L Data Bus Line
9	DB2	H/L Data Bus Line
0	DB3	H/L Data Bus Line
1	DB4	H/L Data Bus Line
2	DB5	H/L Data Bus Line
3	DB6	H/L Data Bus Line
4	DB7	H/L Data Bus Line
5	A/Vee	+ 4.2V for LED/Negative Voltage Output
6	K	Power Supply for B/L (OV)

DIMENSIONS in millimeters



LED - H/L B/L		
	HIGH	LOW
H1	13.2	12.1
H2	8.6	7.5

APPENDIX III

SIEMENS

Small Relay D2

Product Information

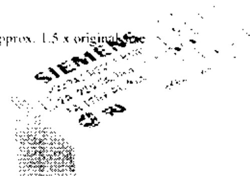
PCB relay for DC voltage, polarized, monostable or bistable

Features

- Universally applicable in the most varied circuit functions in the field of telecommunications and small signal technology
- Versatile design as it can be delivered with different power consumptions (P_N = 150 to 250 mW) as well as with reversed coil polarity
- High reliability due to slide-free operation of the middle spring
- High-voltage resistance according to FCC Part 68

ECR0983-1

Approx. 1.5 x original size



Typical applications

- Standard telecommunication relay for public and private networks and terminal equipment
- Interface relay for microcomputer systems
- Storage element for input and output equipment (bistable version)
- Measurement and control
- Automobile technology
- Entertainment electronics
- Signalling systems
- Medical equipment

Versions

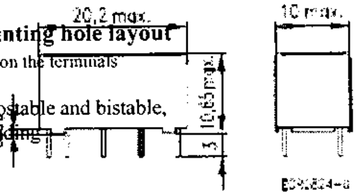
- Relay types: monostable with 1 winding or bistable with 2 windings or bistable with 1 winding
- With 2 changeover contacts
- With double contacts
- For printed circuit assembling
- Immersion cleanable

Approvals

UL	File E 48393
CSA	File LR 50227-7

all relay D2

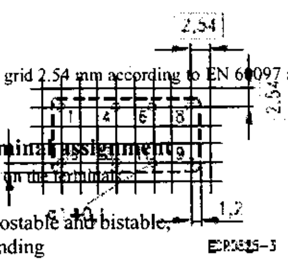
ension drawing (in mm)



nting hole layout
on the terminals

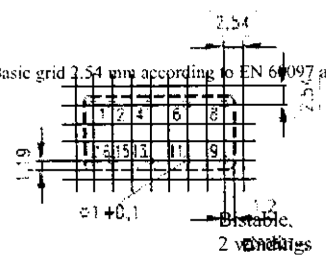
stable and bistable,
ding

Bistable,
2 windings



grid 2.54 mm according to EN 60097 and DIN 40803, fine

Basic grid 2.54 mm according to EN 60097 and DIN 40803, fine



minal assignment
on the terminals

ostable and bistable,
nding

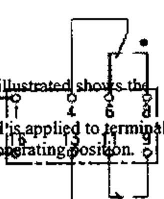
42-A2III
42-C2III

Monostable and bistable,
1 winding

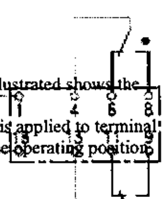
V23042-A3III
V23042-C3III

Bistable,
2 windings

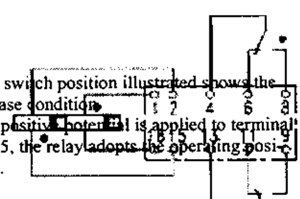
V23042-B2III



witch position illustrated shows the
se condition.
ositive potential is applied to terminal 1,
lay adopts the operating position.



The switch position illustrated shows the release condition.
If a positive potential is applied to terminal 16, the relay adopts the operating position.



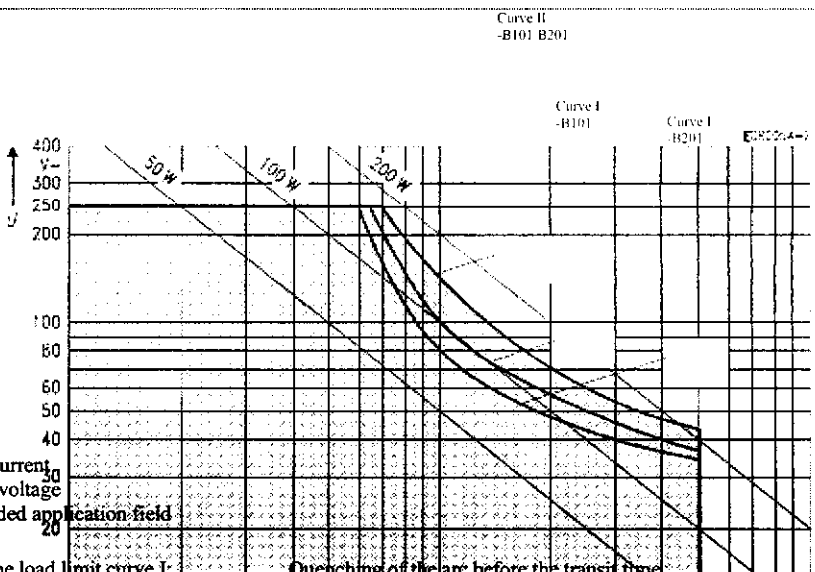
The switch position illustrated shows the release condition.
If a positive potential is applied to terminal 1 or 15, the relay adopts the operating position.

Small relay D2

Contact data

Ordering code block 3	B101	B201
Number of contact and type	2 changeover contacts	
Contact assembly	Double contacts	
Contact material	Gold-plated silver against palladium silver	Gold-plated palladium silver against palladium silver
Max. continuous current at max. ambient temperature	2A	
Maximum switching current	5A	
Maximum switching voltage	250 V– 220 V~	
Maximum switching voltage according to VDE 0110, insulation group A	150 V– 125 V~	
Maximum switching capacity DC voltage AC voltage	50 ... 150 W, see load limit curve 250 VA	
Recommended for load voltages greater than	100 ∝ς	
Thermoelectric potential	δ 10 ∝ς	
Contact resistance (initial value) / measuring current / driver voltage	δ 50 mΩ / 10 mA / 20 mV	

Load limit curve



I = switching current
U = switching voltage
= recommended application field

Definition of the load limit curve I: Quenching of the arc before the transit time

il data

ninal energizing voltage	From 3V– to 48V–
ical nominal power consumption	
nostable with 1 winding	150 ... 250 mW
table with 2 windings	150 ... 200 mW
~~table with 1 winding~~	~~75 ... 100 mW~~
	(depending on the coil version, ~~see table)~~
ximum operating voltage	70 ... 80 % of the nominal energizing voltage, depending on the coil version
ximum reverse voltage (bistable)	75 % of the nominal energizing voltage
imum release voltage (monostable)	10 % of the nominal energizing voltage
ximum holding voltage (non-releasing, monostable)	35 % of the nominal energizing voltage

= minimum voltage at 20 °C after pre-energizing with nominal energizing voltage without contact current

= maximum continuous voltage at 20 °C

~~operating voltage limits UI and UII are dependent on the~~ erature according to the formulae:

mb = $k_I \cdot U_{I\ 20\ °C}$

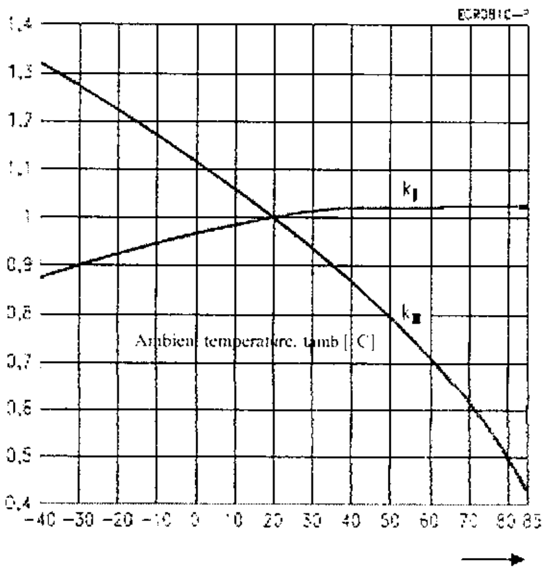
mb = $k_{II} \cdot U_{II\ 20\ °C}$

= ambient temperature

mb = minimum voltage at ambient temperature, tamb

mb = maximum voltage at ambient temperature, tamb

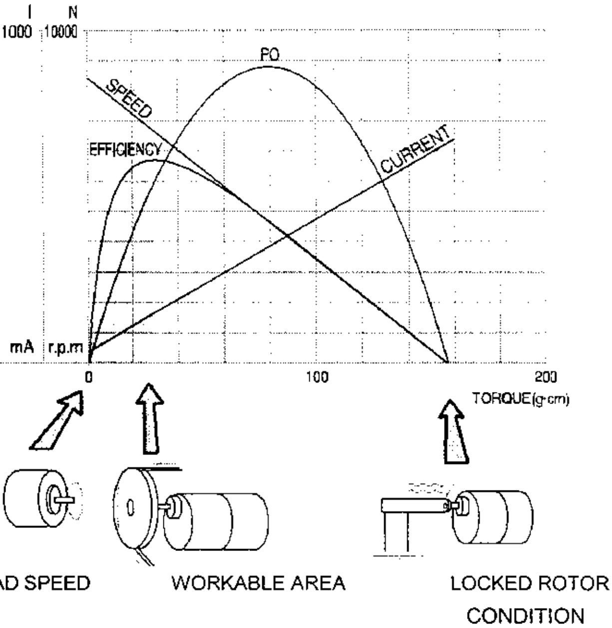
kII = factors (temperature dependent), see diagram



APPENDIX IV

DC MOTOR SPECIFICATIONS

EED AND LOAD CHARACTERISTICS



The relationship between torque vs speed and current is linear as shown left;as the load on a motor increases, Speed will decrease. The graph pictured here represents the characteristics of a typical motor.

As long as the motor is used in the area of high efficiency (as represented by the shaded area) long life and good performance can be expected. However, using the motor outside this range will result in high temperature rises and deterioration of motor parts.

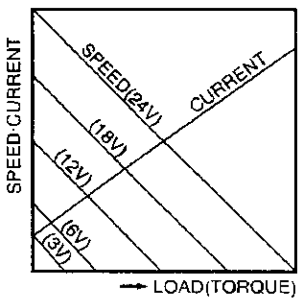
If voltage in continuous applied to a motor in a locked rotor condition, the motor will heat up and fail in a relatively short time. Therefore it is important that there is some form of protection against high temperature rises.

A motor's basic rating point is slightly lower than its maximum efficiency point.

Load torque can be determined by measuring the current drawn when the motor is attached to a machine whose actual load value is known.

We will select the most suitable motor for your application after receiving your information.

APPLIED VOLTAGE WILL BE CHANGED



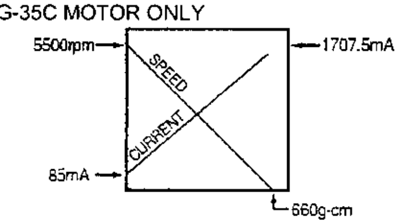
As shown left, if the applied voltage is changed, no load speed and starting torque also change in proportion to the voltage.

Speed characteristics at a given voltage are parallel to those at other voltages.

Thus, a DC motor can be used at a voltage lower than the rated voltage. But, below 1000 rpm, the speed becomes unstable, and the motor will not run smoothly.

ARACTERISTICS AND RATED PERFORMANCE OF A GEARED MOTOR

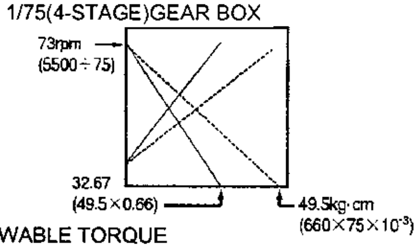
G-35C MOTOR ONLY



Speed reduction by means of a gear box results in increased torque.

The reduction/increase is determined by the gear ratio and efficiency of the gear box.

1/75(4-STAGE)GEAR BOX



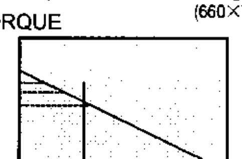
Over-all efficiency depends on the number of reduction stages : one average is 90% per stage. Therefore: a two stage reduction gives 90 90=80%; 3 stages will be 72.9% and a 4-stage reduction 66%.

The above mechanical loss effects the stall torque as shown left.

Stall torque of a geared motor can be calculated using the following formula:

—Motor stall× torque× gear ratio efficiency.

WABLE TORQUE



The output loading on a gear box must never exceed the manufactures "specified rated torque" as this will cause premature gear failure.

It is particularly important to observe this at slow output speeds when the calculated output torque exceeds the specified rated torque.

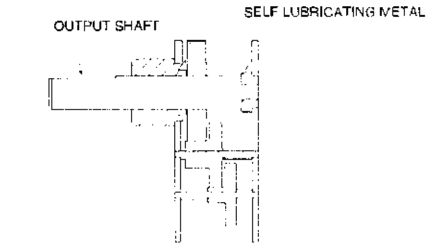
;EAR BOX CONSTRUCTION AND FEATURES

ERMITTENT DUTY

able for less than 2sec.)
& long enough off time

ANDARD TYPE

AG, SG, BG ⇨
VG, VM, LG



STANDARD GEAR MECHANISM

Other than the output gear, the gears rotate around a shaft that is fixed to the plate.

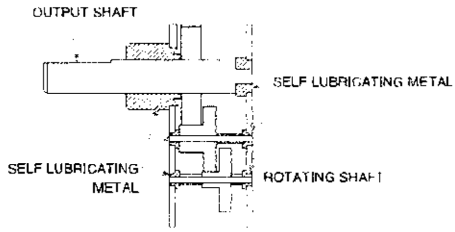
AVY LOAD

'self lubricating metal type.

SM, AM, BE, BM ⇨

'ballbearing at all stages

AP ⇨



NON-LUBRICATED METAL BEARING GEAR MECHANISM

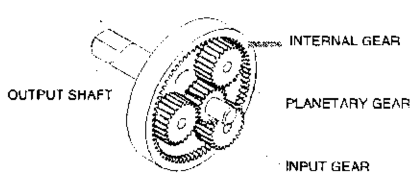
All gears, including the output gear, are attached to the shaft and supported by non-lubricated metal bearings. This type of mech-anism is suitable for medium load applications and continuous duty cycle operation.

W COST VERSION—Plastic or sinterd metal. EU, RU, LG, VG

MPACT SIZE TYPE

—Planetary

GU, FU, EU, RU ⇨



PLANETARY GEAR MECHANISM

A heavy duty type gear mechanism using 3 mating gears to transmit torque to the output shaft. This type of mechanism is suitable for limited space applications.

otection against overload and locked rotor

n the rotor is locked and voltage is applied to the motor terminals, the temperature of the motor windings will rise and eventually short-circuit.

:ime until a short-circuit condition appears differs per motor type.
recommended that the motor is protected against such an overload by means of a fuse, current limiter or mechanical protection.

otection against RFI/EMI caused by PWM control

nternally installed suppressor reduces electrical commutation noise caused by the brushes. Depending on the requirements, extra precautions sometimes are nmended such as an external capacitor, or filter circuit.
n driven in PWM at certain Frequencies it may occur that a motor does not start due to the combination of driving frequency and internally fitted capacitive : suppressor.

ecautions for instantaneous reversing and dynamic braking

n the power supply to the motor is switched off, it is advisable to allow the motor to stop rotating before reversing the supply polarity. Failure to do this result in a very high instantaneous current.
possible to stop the motor within a few revolutions by applying a short-circuit across the motor terminals immediately after the motor is switched off. This od is very effective but may shorten brush life.

rtical mounting with shaft up

me cases when a motor-gear is mounted in this position, traces of lubrication oil can contaminate the brushes and commutator thus shortening brush life or ng a short-circuit. Please contact us when vertical mounting is required.