INTERACTIVE VOICE RESPONSE SYSTEM FOR COLLEGE AUTOMATION

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BONAFIDE CERTIFICATE

Certified that this project report titled **"INTERACTIVE VOICE RESPONSE SYSTEM FOR COLLEGE AUTOMATION"**, is the bonafide work of **Ms.R.RAMAPRIYA**[Reg.No.0710107088],**Ms.R.SARANYA**[Reg.No.0710107088],**Ms.T.SUGANYA**[Reg. No. 0710107102], and **Ms.G.SUJITHRA** [Reg. No. 0710107103] who carried out the research under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other project or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

18/4/11

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18/4/11

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18/4/11

External Examiner

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ABSTRACT

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In today's competitive world any business must build flexible systems that adapt easily to evolving requirements of the critical business processes. IVRS is one such system that transforms the traditional business model into customer centric model. IVRS is historically interactive speech memory driven that walk the caller through a series of prompts where they respond to questions by pressing the combination of one or more buttons of the phone keypad.

The decision tree associated with the prompts and the responses will route the caller to information they desire. These IVRS systems are typically utilized to check bank account balance, buy and sell stocks, check the show times for your favorite movie.

In telephony, Intelligent Voice Response, or IVR, is a phone technology that allows a computer to detect voice and touch tones using a normal phone call. The IVR system can respond with pre-recorded or dynamically generated audio to further direct callers on how to proceed. IVR systems can be used to control almost any function where the interface can be broken down into a series of simple menu choices. Once constructed IVR systems generally scale well to handle large call volumes.

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INTRODUCTION

1.1 GENERAL VIEWS

Today technology has made our life simple and easy in communication world. IVRS is an important development in the field of interactive communication which makes use of the most modern technology available today. IVRS is a unique blend of both the communication field and the software field, incorporating the best features of both these streams of technology. IVRS is an electronic device through which information is available related to any topic about a particular organization with the help of telephone lines anywhere in the world. IVRS provides a friendly and faster self service alternative to speaking with customer service agents. Thus communication leads troop of developments in the recent trends.

1.2 BASIC PRINCIPLE

Interactive voice response refers to technology supporting the interaction of customer with the service provider generally over the telephone lines.

When a person wants to access any of the services of the Interactive Voice Response System, he presses a number through his telephone keypad. The pressed number appears across the line and the ring detector circuit senses this ring. After a specified number of rings the relay is activated through the microcontroller, which in turn connects the line to DTMF decoder.The activation of relay causes the number pressed to appear across the DTMF decoder.The decoder decodes the number pressed and then the decoder output is passed through the microcontroller to the computer. Now, when the caller presses a number, the number pressed is decoded by the DTMF decoder and passed to the computer through the microcontroller using MAX232.The computer recognizes the number and accesses the particular file from the database .

The output voice is passed through the voice card where the digitized serial data is converted into analog voice form and passed to the line. The caller gets the information through the line.

1.3 BASIC BLOCK DIAGRAM

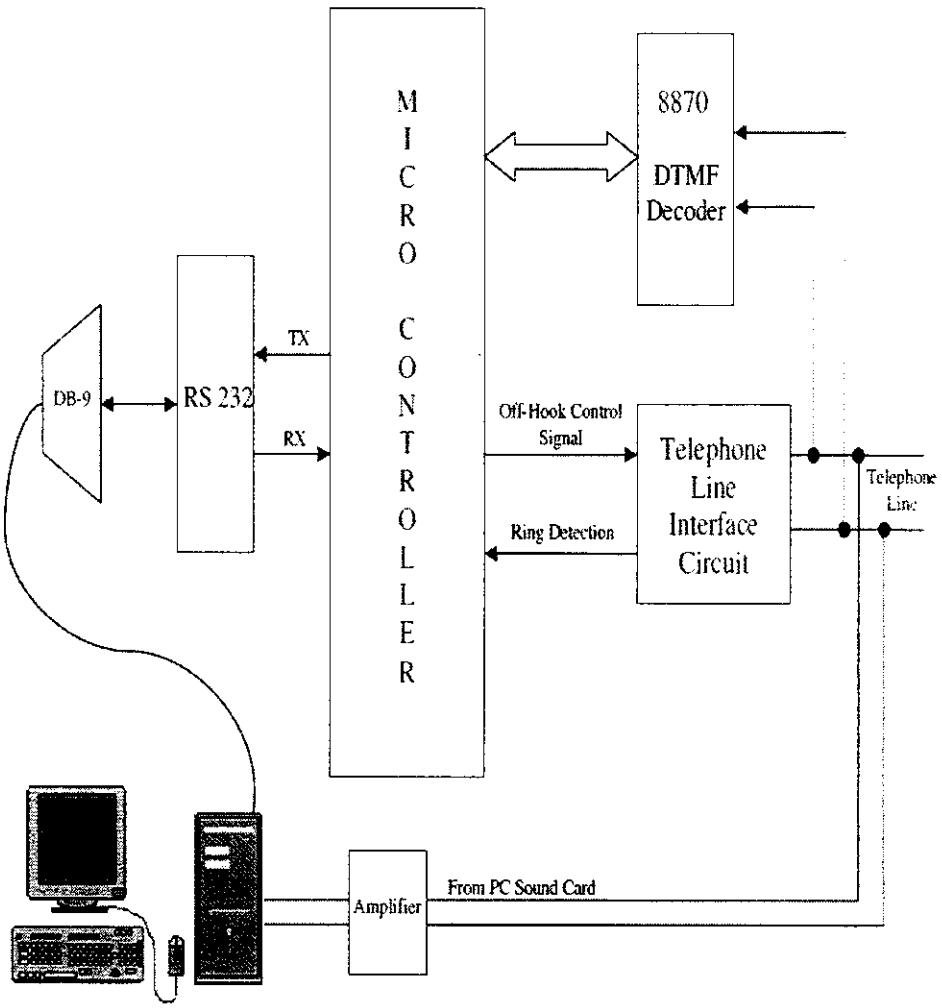


FIG 1.1 BASIC BLOCK DIAGRAM

1.3.1 WORKING

•When the telephone is in the idle condition, the voltage will be -48V.

• When the ringing occurs, it will be 125V peak to peak AC signal superimposed on -48V.

• The opto isolator is used to isolate the microcontroller from high voltage AC signals and it consists of GaAs infrared emitting diode optically coupled to a monolithic silicon phototransistor.

• The microcontroller will detect the ring through the port 1.5 and it will count the number of rings.

• After a fixed number of rings, the microcontroller will send a signal to the relay and then the automatic off-hooking of the telephone takes place.At the same time, microcontroller will transmit '#' to the computer which is an indication to play the 'Welcome' message.

• The relay used is DPDT type and after automatic off-hooking takes place, the relay connects the telephone lines to the decoder IC 8870 and isolation transformer.

• The transformer used is a line transformer used to isolate voice card from high voltages.

• As the telephone lines are connected to the voice card, the caller gets to hear the stored messages and asks the caller to enter the roll number of the student whose result is to be known. After the caller dials the roll number from the touch tone keypad of his telephone, that number will be decoded by the decoder IC 8870 and the decoded information will be sent to the computer via the microcontroller.

• Computer on receiving the decoded information will check the database to access the result of the student whose roll number is entered.

• Then the computer will send the desired information to the voice card and the caller will get to hear the result of the student on his telephone through the voice card.

1.4 ADVANTAGES OF IVR SYSTEM

The biggest advantage of IVR for small and large organizations is to save time and money. Answering phone calls takes a lot of time, and not every phone call deserves the attention of a trained employee. IVR systems can take care of most of the frequently asked questions that an organization receives (office hours, directions, phone directory, common tech support questions, et cetera) and allow customer service representatives, salesmen and tech support specialists to concentrate on the harder stuff. If a large company is able to save even a second off the average length of each phone call with a live operator, it can save them hundreds of thousands or even millions of dollars a year [source: Human Factors International]. IVR systems have the advantage of making callers and customers feel like they're being attended to, even if it's just by a machine. If you have a simple question, it's better to get a quick answer from a computerized operator than to wait ten minutes on hold before talking to a human being.

Another advantage is that IVR systems don't sleep. They don't take lunch breaks. They don't go on vacations to the Bahamas. An IVR system can be available 24 hours a day to field questions and help customers with simple tasks. An IVR system can make a small company look bigger. Some IVR hosting plans even set you up with an 800 number to look more official. Subscription IVR hosting plans make it easier for businesses and organizations to use these automated phone services. This is a big advantage of days past, when only large companies with big telecommunications and computing budgets could afford the hardware, software and staff to run in-house IVR systems.

1.5 APPLICATIONS

- Schools,Colleges and Educational Institutions
- Bank and Stock account balances and transfers
- Surveys and polls
- Call center forwarding

SCHEMATIC OVERVIEW

CHAPTER 2

SCHEMATIC OVERVIEW

2.1 BLOCK DIAGRAM DISCRIPTION

The main blocks of IVR system are as follows:

- Ring Decoder
- DTMF Decoder
- Microcontroller
- MAX 232
- Relay
- Isolation Transformer
- Voice Card

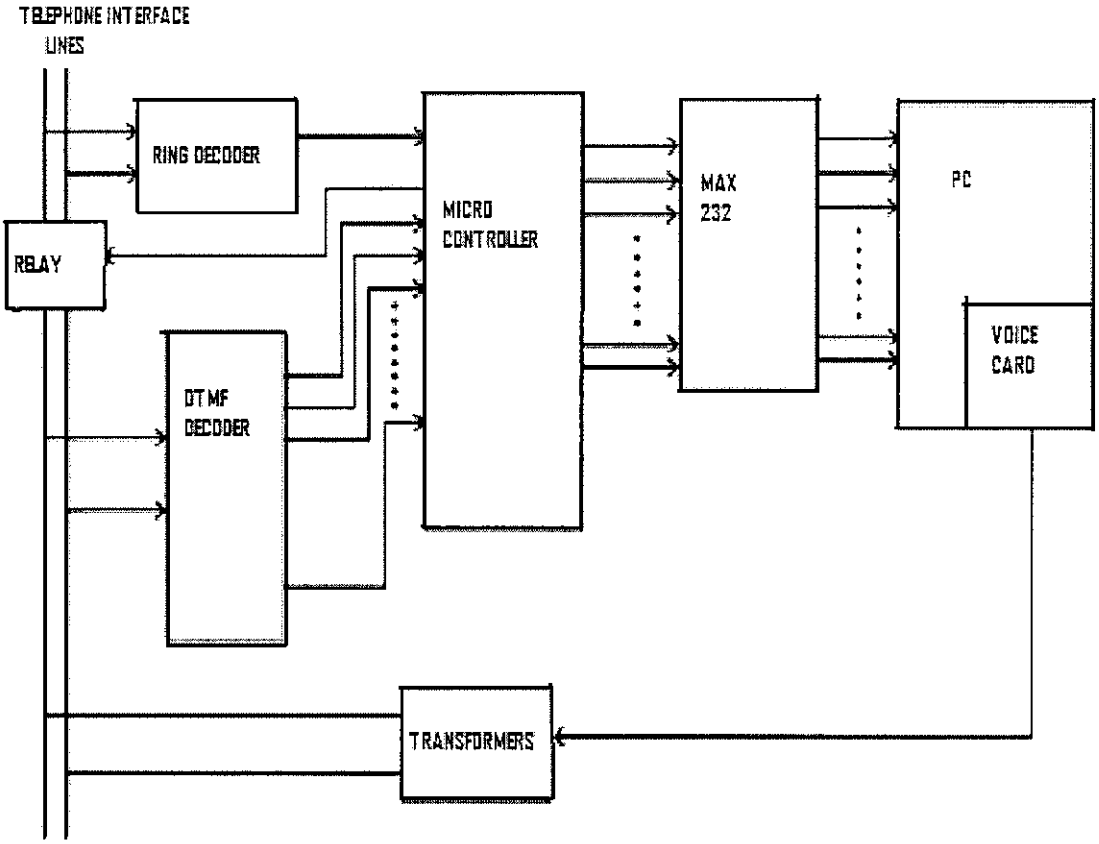


FIG 2.1 BLOCK DIAGRAM

2.1.1 Ring Decoder

Ring decoder consists of:

- Bridge Rectifier
- Capacitor Filter
- Opto Isolator

2.1.2 DTMF Decoder

In DTMF signaling, two frequencies are allocated to each digit in the push button keypad. The main function of the DTMF decoder is to detect the two frequencies and until and unless these two frequencies allocated for a particular digit are obtained, that particular digit will not be recognized by the DTMF decoder. The decoder uses digital counting technique to detect and decode all 16 DTMF tone pairs into 4 bit code.

Its features are:-

- Complete DTMF Receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode

2.1.3 Microcontroller

AT89S52 microcontroller is used in IVR system. It is the central controller of the whole project. It scans all channels continuously. It transfers the logical values serially to the PC. Various tasks are assigned to peripherals.

2.1.4 Relay

Relay is used as a switch to provide the connection between the telephone line and the voice card as well as the DTMF decoder.

2.1.5 MAX 232

MAX232 is used to convert the voltage levels. Dual driver/receiver that includes capacitive voltage generator to supply 232 voltage levels from single 5V supply. Each receiver converts 232 inputs to 5V TTL/CMOS levels. Each driver converts TTL/CMOS input levels into 232 levels.

2.1.6 Isolation Transformer

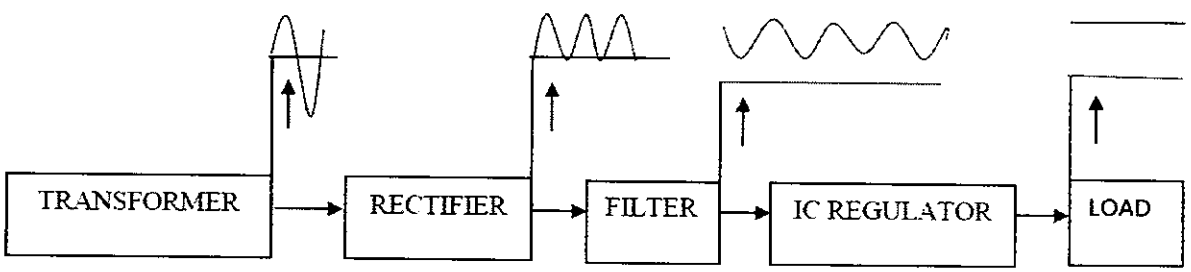
The simplest and the most common way to do the isolation is by using audio transformer which is a 1:1 isolation transformer.

2.1.7 Voice Card

Voice card is the output device of IVR system. The caller will get to hear the information through the voice card.

2.1.8 Power supply

The ac voltage, typically 220V rms, is connected to a transformer, which steps that ac voltage down to the level of the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage.



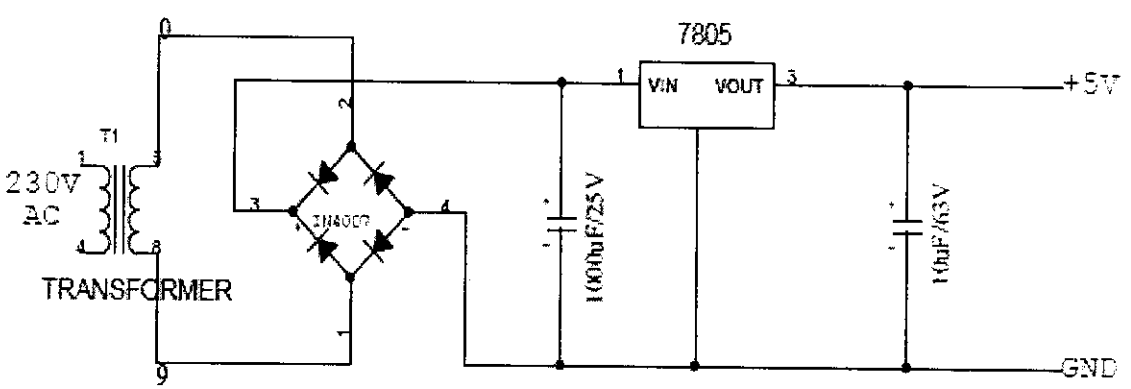


FIG 2.2 POWER SUPPLY BLOCK DIAGRAM

WORKING PRINCIPLE

TRANSFORMER

The potential transformer will step down the power supply voltage (0-230V) to (0-6V) level. Then the secondary of the potential transformer will be connected to the precision rectifier, which is connected with the help of op-amp. The advantages of using precision rectifier, it will give peak voltage output as DC, rest of the circuits will give only RMS output.

BRIDGE RECTIFIER

When four diodes are connected as shown in figure, the circuit is called as bridge rectifier. The input to the circuit is applied to the diagonally opposite corners of the network, and the output is taken from the remaining two corners.

Let us assume that the transformer is working properly and there is positive potential, at point A and a negative potential at point B. The positive potential at point A will forward bias D3 and reverse bias D4.

The negative potential at point B will forward bias D1 and reverse bias D2. At this time D3 and D1 are forward biased and will allow current flow to pass through them; D4 and D2 are reverse biased and will block current flow.

One advantage of a bridge rectifier over a conventional full-wave rectifier is that with a given transformer the bridge rectifier produces a voltage output that is nearly twice that of the conventional full-wave circuit.

FILTERS

Capacitors are used as filters in the power supply unit. Shunting the load with the capacitor affects filtering. The action of the system depends upon the fact the capacitor stores energy during the conduction period and delivers this energy to the load during the inverse or non-conducting period. In this way, time during which the current passes through the load prolonged and ripple is considerably reduced.

IC VOLTAGE REGULATORS

Voltage regulators comprise a class widely used ICs. Regulator IC unit contain the circuitry for reference source, comparator amplifier, control device and overload protection all in a single IC. IC units provide regulation of either a fixed positive voltage, a fixed negative , or an adjustably set voltage. The regulators can be selected for operation with load currents from hundreds of milli amperes, corresponding to power ratings from milli watts to ten of watts.

2.1.9 RELAY CIRCUIT

Relays are components, which allow a low power circuit to switch a relatively high current ON and OFF, or to control signals that must be electrically isolated from the controlling circuit itself. Relays are composed of a coil of wire around a steel core, a switch, and a spring that hold one or more contacts.

When an electrical flows through the coil it becomes energized, acting like an electromagnet. The refuse field opens the contacts, and close the circuit. When electrical current stops flowing, the opposite occurs.

2.2 CIRCUIT DIAGRAM

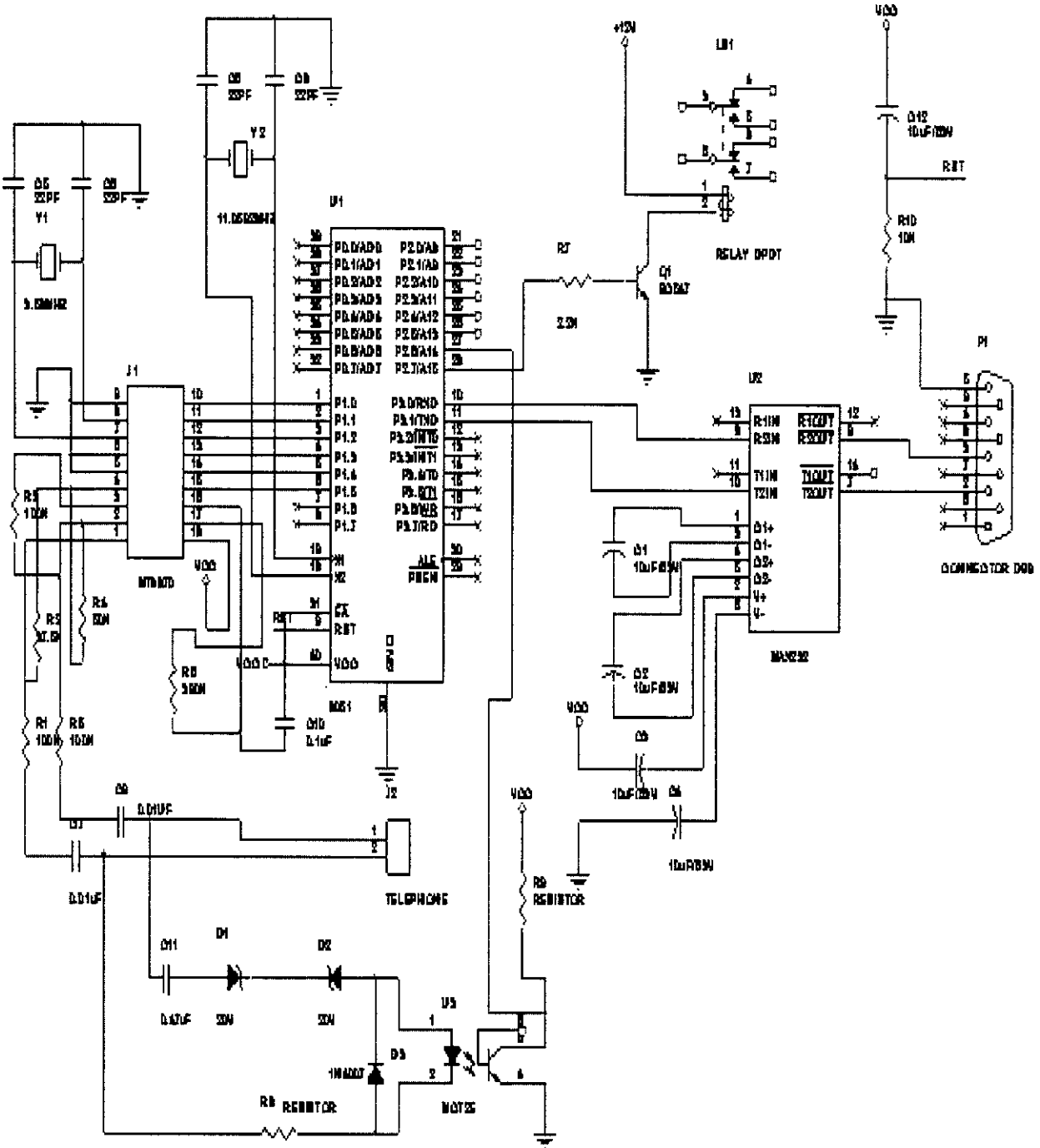


FIG 2.3 CIRCUIT DIAGRAM

CIRCUIT DESCRIPTION

Whenever the call is coming ,the ring circuit is used to inform the microcontroller about the details. Ring circuit along with the optocoupler is used. DPST switch is connected to the controller,which decodes the information and send to the controller. MAX 232 is used which is an level converter ,converts the voltage and data to a form which a computer can understand. The voltage level for this IC is -3 to+25. A relay circuit is used which makes the computer to attend the call after a fixed number of rings.

The hook switch will be on whenever the call is not coming, if any call comes then automatically the hook switch will be off after attending the call. MAX 232 is a serial communication IC which communicates between the controller and computer. The recorded voices stored in the memory will be sent for the callers to listen initially. After that the callers inputs are accepted through MAX 232 and based on that ,the information stored in the database is converted into voice and again sent. Only inputs through keypad will be accepted. The connector DB9 is used to connect the hardware to computer. DPST switch decodes all data from the telephone line and sends as an useful information to the controller in the form which it can understand, because the controller cannot accept or understand the data directly from the telephone line. The controller then informs MAX 232 ,which is a serial communication between the controller and computer,to get the required data from the computer. MAX 232 converts the data into 0and 1s ,then send to computer. The computer inturn checks the database and sends required data to the MAX 232. It sends the data to the controller. The controller sends the data to DPST and from that to the telephone line . Thus the circuit works for getting the information from the computer and sending to the telephone through the controller, MAX 232 and DPST.

CHAPTER 3

PCB DESIGN

3.1 INTRODUCTION

The PCB layout is designed using the protel software. The bottom layer is used for drawing and the track which minimises the cost for the fabrication. The track width of 1mm for the power supply track and 0.5mm width for the oher tracks.

3.2 PRINTED CIRCUIT BOARD

Making of PCB is as much an art as a technique partially,so they are to fabricated in very small numbers. There are several ways of drawing PCB patterns and making the final board. But the method likely to interest people in need of just a few PCBs which are simple and economical. The making of PCB drawing. Fabricating the PCB itself from drawing.

The traditional method of making a PCB drawing with complete placement of parts. Taking a photographic negative of the drawing. Developing the image of the negative formed on the photosensitized copper plate and dissolving the excess copper by etching in the standard practice being followed in large scale operations.

This procedure has its own advantages,as the lateralinversion problem is overcome. Also tracing of the circuit and fault finding is made easy,as the exactly matches with the original circuit so that one does not have to constantly look for positions to drill holes and place components.

3.3 PCB DRAWING

Making of PCB drawing involves some preliminary considerations such as placement of components on a piece of paper location of holes. The optimum area of each components. The shape and location of islands for two or more components at a place. Full place utilization and prevention of over crowding of components at a particular place.

There is no other way to arrive at the components,one mm dia hole and for fixing PCB holding screws to the chairs 3 mm diameter hole are recommended.

This sketch may be redrawn neatly in the fresh piece of paper,if desired this sketch is the mirror image of the PCB pattern desired,it shows the component placement on the other side of the PCB laminate.

The mirror image of this sketch,the pattrn can now be drawn with the help of thick tracing paper. The sketch is redrawn on a tracing paper would appear as the PCB pattern when viewed from the other side. To save time and effort,the sketch on the tracing paper itself right in beginning.

Alternatively,the PCB can be drawn from the sketch with the help of a carbon paper. A fresh carbon paper may be face upon a flat surface and coverd with a plain sheet of paper. On this sheet the sketch may be placed. Now,by carefully tracing the sketch with a ball pen or hard pencil,the mirror image of the sketch may be obtained on the lower sheet of the paper.

3.4 PCB FABRICATION

The copper clad PCB laminate may now be prepared by rubbing away the oxide,grenade and dirt etc,with fine emery paper or sand paper. On this the final PCB drawing may be traced this time by using the carbon paper in the normal way clip should be used to prevent the carbon and the paper from slipping while the PCB pattern is being traced on the laminate. Only the connecting line in PCB island and hole should be traced tracing the position of the components are not required. The component position may be marked on the PCB reverse side,if desired. The marked holes in PCB may be drilled using 1mm or 3mm drill bits and the traced PCB pattern coating with black,quick enamel points,using a thin brush and a small metal scale. In case there is shooting of line due to spilling of points,there may be removed by scraping with a blade or knife after the point had dried.

CHAPTER 4

HARDWARE TOOLS

4.1 MICROCONTROLLER

4.1.1 INTRODUCTION

The AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the indus-try-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory pro-grammer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications

4.1.2 FEATURES

Compatible with MCS®-51 Products

• 8K Bytes of In-System Programmable (ISP) Flash Memory – Endurance: 10,000 Write/Erase Cycles

• 4.0V to 5.5V Operating Range

• Fully Static Operation: 0 Hz to 33 MHz

• Three-level Program Memory Lock

• 256 x 8-bit Internal RAM

• 32 Programmable I/O Lines

• Three 16-bit Timer/Counters

• Eight Interrupt Sources

• Full Duplex UART Serial Channel

• Low-power Idle and Power-down Modes

• Interrupt Recovery from Power-down Mode

• Watchdog Timer

• Dual Data Pointer

• Power-off Flag

• Fast Programming Time

4.1.3 PIN DIAGRAM

AT89S52

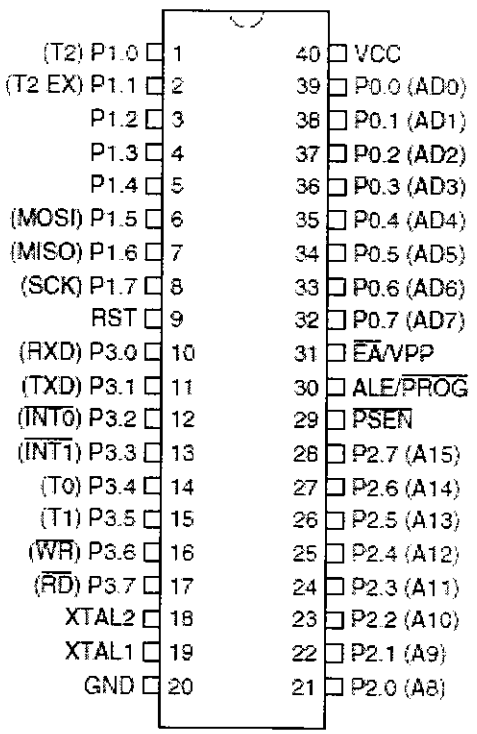


FIG 4.1 PIN OUT OF AT89S52

4.2 GENERAL DESCRIPTION ABOUT TELEPHONY

Any telephone set will always be in any of the conditions mentioned below:

4.2.1 ON-HOOK

It is the state whenever telephone handset is placed on the cradle. During this state, the telephone line is open circuit with the exchange and the voltage of –48 V is available on each telephone line from the exchange.

4.2.2 OFF-HOOK

This is the state whenever telephone handset is displaced from the cradle. During this state the voltage level is between ± 5V to ± 12 V. The telephone OFF – HOOK resistance is typically 600 Ω .

2. 4.3 SIGNALING TONES

• Dial tone

This tone indicates that the exchange is ready to accept dialed digits from the subscriber. The subscriber should start dialing only after hearing the dial tone. Otherwise, initial dialed pulse may be missed by the exchange that may result in the call landing on the wrong number. The dialed tone is 33 Hz or 50 Hz or 400 Hz continuous tones.

• Ring tone

When the called party is obtained, the exchange sense out the ringing current to the telephone set of the called party. This ringing current has the familiar double ring pattern. Simultaneously, the exchange sends out the ringing tone to the calling subscriber, which has the pattern similar to that of ringing current, the two rings in the double ring pattern are separated by a time gap of 0.2s and two double rings patterns by a time gap of 2s.The burst has duration of 0.4s. The frequency of the ringing tone is 133 Hz or 400 Hz.

• Busy tone

Busy tone is bursty 400 Hz signal with silence period in between. The burst and silence duration has the same value of 0.75s. A busy tone is sent out to the calling subscriber whenever the switching equipment or junction line is not available to put through the call or called subscriber line is engaged.

• Number unobtainable tone

The number unobtainable tone is a continuous 400 Hz signal. This tone may be sent to the calling subscriber due to a variety of reasons. In some exchanges this tone is 400 Hz intermittent with 2.5s ON period and 0.5s OFF period.

• Routing tone

The routing tone or call – in – progress tone is 400 Hz or 800 Hz intermittent patterns. In an electromechanical system it is usually 800Hz with 50% duty ratio and 0.5s ON-OFF period. In analog electronic exchange it is 400 Hz pattern with 0.5s ON period and 0.5s OFF period. In digital exchange it has 0.1s ON-OFF period at 400 Hz.

• **TOUCH –TONE KEY PAD**

Touching a button generates a ' tone', which is a combination of two frequencies, one from lower band and other from upper band. For e.g. pressing push button '7' transmits 852 and 1209 Hz.

	1209Hz	1336Hz	1477Hz
697Hz	1	2	3
770Hz	4	5	6
852Hz	7	8	9
941Hz	*	0	#

4.3 TELEPHONE INTERFACE SECTION

It consists of following subsections:

4.3.1Ring Detector Section

Ring detector circuit does the function of detecting the ring activating signals and then counts the number of rings.

4.3.2Ring activating signals

This is sent by telephone exchange to the subscriber. This signal causes an audio tone in the subscriber's telephone set. This ring tone is an alarming signal, which diverts the attention of the subscriber towards the instrument. The ring signal produced at the central office is composed of a 10v ac, 400Hz signal that is always present on the telephone line with the handset in ON-HOOK position.

The ring-activating signal is ON for 0.2 sec and the subscriber can hear the sound of ring in that duration of time. For next 0.4 sec the ring-activating signal goes OFF. Now the subscriber can't hear the sound. Again this repeats for six times with the pause of 2 sec. Thus the subscriber hears six rings.

4.3.3 Optocoupler

In the same application it is necessary to isolate input and output. The isolation can be achieved in many ways. One of these is to use an Opto-coupler. Opto-coupler is controlled by optical energy.

4.3.4 Construction

Optocoupler is MCT2E. The device consists of GaAs infra red emitting diode optically coupled to a monolithic silicon phototransistor detector.

4.4 DTMF (Dual Tone Multiple Frequency) MT8870:

Today, most telephone equipment use a DTMF receiver IC. One common DTMF receiver IC is the Motorola MT8870 that is widely used in electronic communications circuits. The MT8870 is an 18-pin IC. It is used in telephones and a variety of other applications. When a proper output is not obtained in projects using this IC, engineers or technicians need to test this IC separately. A quick testing of this IC could save a lot of time in research labs and manufacturing industries of communication instruments. Here's a small and handy tester circuit for the DTMF IC. It can be assembled on a multipurpose PCB with an 18-pin IC base. One can also test the IC on a simple breadboard.

The AT89S52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator disabling all other chip functions .

4.5 SERIAL INTERFACE – RS 232:

4.5.1 INTRODUCTION:

Serial data is any data that is sent one bit at a time using a single electrical signal. In contrast, parallel data is sent 8,16, 32, or even 64 bits at a time using a single line for each bit. Data that is sent without the use of a master clock is said to be asynchronous serial data.

Several communications standards exists for the transfer of asynchronous serial data. Common PC's transfer data using the EIARS-232C (also known as V.28 or V.24). Updated versions of this standards include RS-232D and EIA/TIA-232E, but most literature still refers to the RS-232 or RS-232 standard.

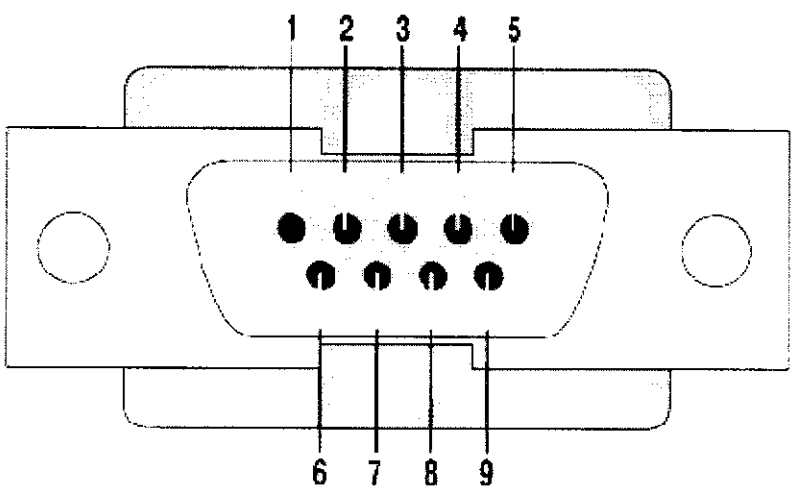
The baud rate for a serial connection is the number of bits that are transmitted per second. It is specified in bits/second or baud.

VOLTAGE LEVELS IN RS 232:

1. Logic high (1) represented as -3 to -25
2. Logic low (0) represented as +3 to +25
3. -3 to +3V not defined

4.5.2 RS 232 PINS:

The table provides the pins and the labels for RS 232 cable, commonly referred to as DB-25 connector.



Pin	Signal	Pin	Signal
1	Data Carrier Detect	6	Data Set Ready
2	Received Data	7	Request to Send
3	Transmitted Data	8	Clear to Send
4	Data Terminal Ready	9	Ring Indicator
5	Signal Ground		

FIG 4.2 RS 232 PINS

The standards for RS 232 and similar interfaces usually restrict RS 232 to 20Kbps or less and line length of 15m or less. RS 232 is fair more robust than the traditional limits of 20kbps over a 15m line would imply RS 232 as perfectly adequate at speed upto 200kbps.

4.5.3 SERIAL PORT OF PC:

IBM PC/compatible computers based on x86(8086, 286,386,486 and pentium) microprocessors normally have two COM (read:COMMUNICATION) ports. Both COM ports have RS 232 type connectors. Many PCs use one each of DB-25 and DB-9 RS 232 connectors. The COM ports are designated as COM 1 , COM 2 etc.. One can utilize COM X port of a PC for serial communication experiments, where X designates a particular port. The RS 232 standard is not TTL compatible, therefore, it requires the line driver such as MAX 232 chip to convert the RS 232 voltage levels to TTL levels and vice versa.

4.5.4 MAX 232:

MAX 232 is primary used for people building electronics with an RS 232 interface. Serial RS-232communications works with voltages (-15V ... -3V for high) and (+3V ... +15V for low) which are not compatible with normal computer logic voltages. To receive serial data from an RS-232 interface, the voltages have to be reduced, and low and high voltage levels are to inverted inverted. In the other direction (sending data from some logic over RS-232) the logic voltage has to be "bumped up", and a negative voltages have to be generated, too.

The MAX232 has two sets of the line drivers for transferring and receiving data. The line drivers used for TxD are called T1 and T2, while the line drivers for RxD designated as R1 and R2. In many applications only one of each is used. For example T1 and R1 are used together for TxD and RxD of the PIC and second set is left unused. Notice in MAX232 that the T1 line driver is designated to T1IN and T1OUT on pin numbers 11 and 14 respectively.

The T1 in pin is the TTL side is connected to TxD of the microcontroller, while T1 out is the RS232 side that is connected to the RxD pin of the RS232 DB connector. The R1 line driver has a designation of R1 in R1 out pin numbers 13 and 12 respectively.

The R1 in pin 13 is the RS232 DB connected to the TxD pin of the RS232 DB connector and R1 out(pin 12) in the TTL side that is connected MAX232 requires 4 capacitors ranging from 1 to 22 micro farad. The most widely used value for this capacitor is 22 microfarad.

No	Name	Purpose	Signal Voltage
1	C1+	+connector for capacitor C1	Capacitor should stand at least 16V
2	V+	Output of voltage pump	+10V
3	C1-	-connector for capacitor C1	Capacitor should stand at least 16V
4	C2+	+connector for capacitor C2	Capacitor should stand at least 16V
5	C2-	-connector for capacitor C2	
6	V-	Output of voltage pump/inverter	-10V
7	T2out	Driver 2 output	RS232
8	R2in	Receiver 2 input	RS232
9	R2out	Receiver 2 output	TTL
10	T2in	Driver 2 output	TTL
11	T1in	Driver 1 input	TTL
12	R1out	Receiver 1 output	TTL
13	R1in	Receiver 1 input	RS-232
14	T1out	Driver 1 output	RS-232
15	GND	Ground	0V
16	Vcc	Power supply	+5V

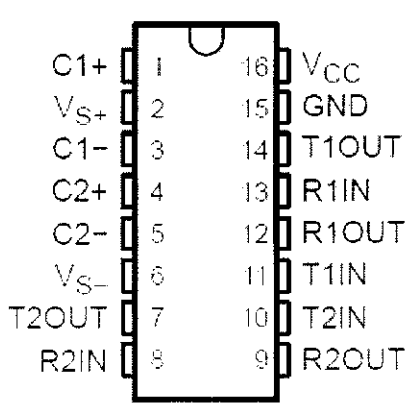


FIG 4.3 PIN OUT OF MAX 232

Features

- Operate from single +5V power supply
- Low-power receive mode in shut down
- Multiple drivers and receivers
- 3-state drivers and Receiver outputs
- Open line detection

4.5.5 MAX 232 INTERFACING

The data from microcontroller is made available to the serial port. The encoded RS232 level signal from pin 3 is given to pin 13 of MAX232 IC. The TTL level signal is obtained across pin 12 of the IC and is directly given to the microcontroller. Thus with this signal level conversion, the data is now ready to be transmitted.

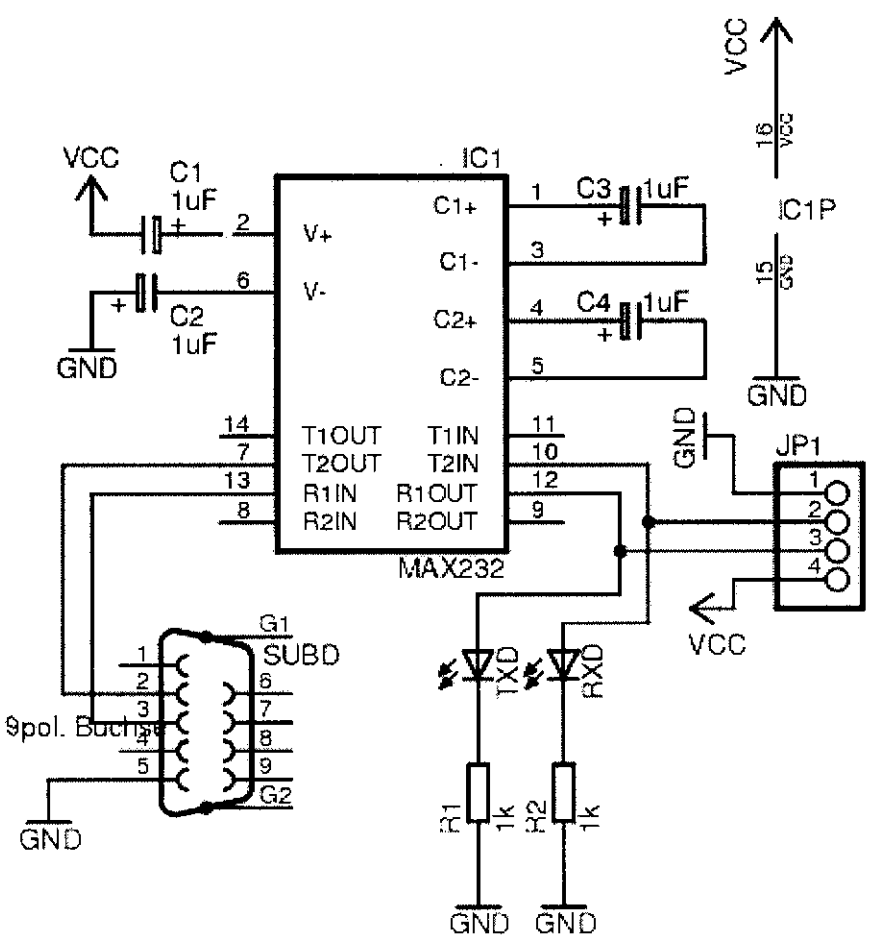


FIG 4.4 MAX 232 INTERFACING

4.5.6 LCD DISPLAY:

LCD's also are used as numerical indicators, especially in digital watches. LCD needs much smaller current than LED displays (microamperes compared with mill amperes) prolong battery life. Liquid crystals are organic (carbon) compounds, which exhibit both solid and liquid properties. A 'cell' with transparent metallic conductors, called electrodes, on opposite faces, containing a liquid crystal, and on which light falls, goes 'dark' when a voltage is applied across the electrodes. The effect is due to molecular rearrangement within the liquid crystal. The LCD display used in our project consists of 2 rows. Each row consists of maximum 16 characters. So using maximum of 32 characters can be displayed.

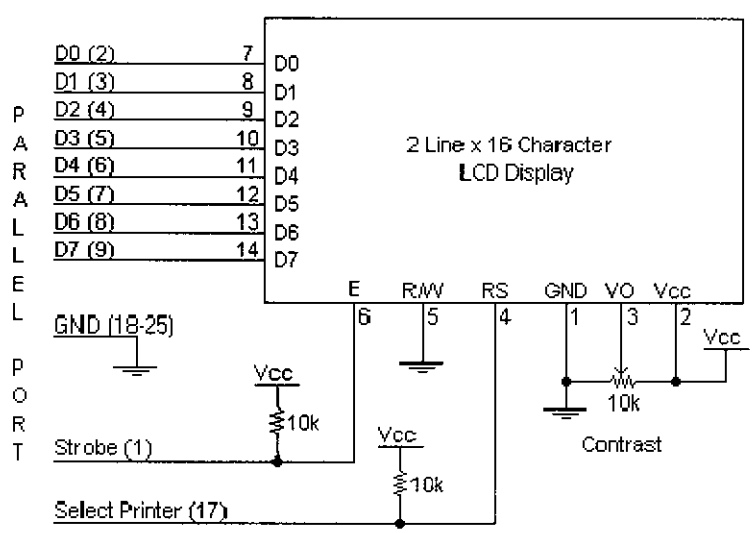


FIG 4.5 LCD DISPLAY

CHAPTER 5
SOFTWARE DESCRIPTION

5.1 SOFTWARE TO BE USED:

- Visual Basic 6.0
- Embedded C for microcontroller

5.2 INTRODUCTION OF VISUAL BASIC 6.0

Visual Basic is an ideal programming language for developing sophisticated professional applications for Microsoft Windows. Visual Basic programming introduces a variety of features that make it easier to create powerful, flexible applications. It makes use of Graphical User Interface for creating robust and powerful applications. The Graphical User Interface uses illustration for text, which enables users to interact with an application.

Visual Basic has evolved from the original BASIC language and now contains several hundred statements, functions, and keywords, many of which relate directly to the Windows GUI. Visual Basic software is developed in Windows operating system.

FEATURES OF VISUAL BASIC

- Easier comprehension.
- User-friendliness.
- Faster application development.
- Introduction to ActiveX-Technology.
- Internet Features.

ADVANTAGES OF USING VISUAL BASIC 6.0

- **Office/VSTO development.**

The Office object model was created with optional parameters, a feature of VBA, in mind and makes heavy use of it. As Visual Basic supports thus it has an advantage over C#

- **COM inter-op with older applications.**

And in this case it is specifically referred to COM interop without a complete type library, something common in VB6 or Visual FoxPro. This is where Option Explicit Offis a great helper and time saver.

5.3 ADVANTAGES OF USING MS-ACCESS 2003

Although there is always overlap, the following rules might help when deciding when or when not to use MS Access:

- MS Access is best used for long-term data storage and/or data sharing.
- MS Excel is best used for minor data collection, manipulation, and especially visualization.
- SPSS is best used for minor data collection and especially data analysis.
- Cheap, readily available (packaged with MS-Office Premium).
- Easy to use (relative to other systems –Oracle may require one FTE to maintain the server as a database administrator and another FTE to serve as an application developer).

5.4 ALGORITHM

Step1: Start the program

Step2: Initialise all the variabes

Step3: Wait for the call

Step4 : If there is a call attend the call using hook on or else go to step 3

Step5: When the hook is on check for the dtmf signal

Step6: If any number is pressed by the user the DTMF decoder sends the corresponding signal to the PC thorugh the microcontroller

Step7: Corresponding to the pressed number the pre recorded voice in the PC responds to the user.

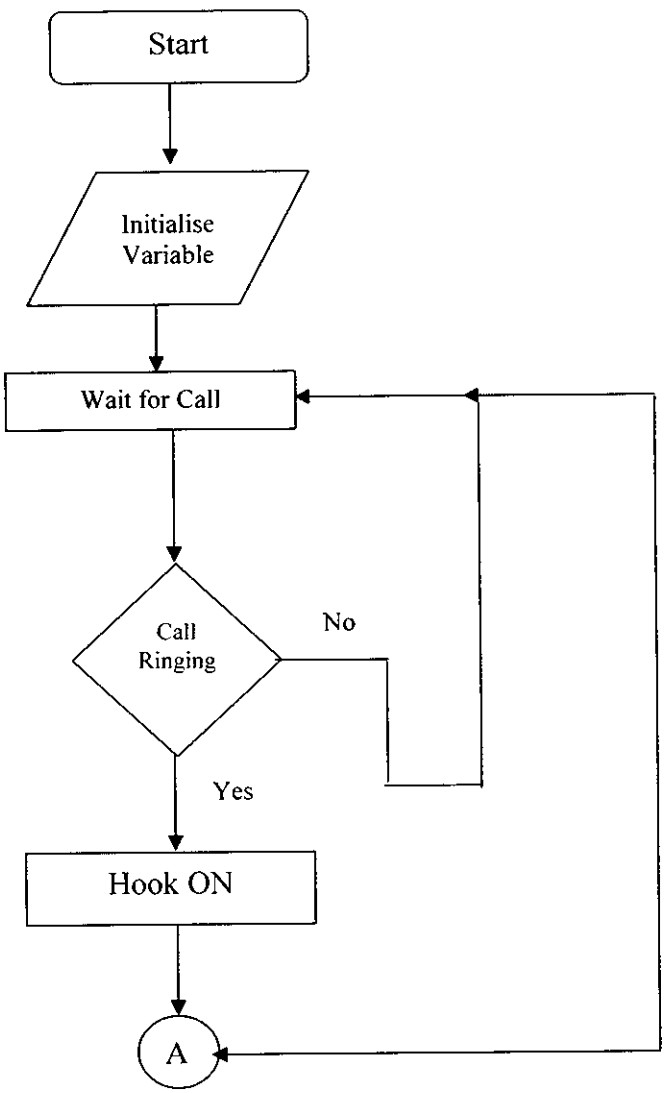
Step8: The user follows the instructions given by the PC.

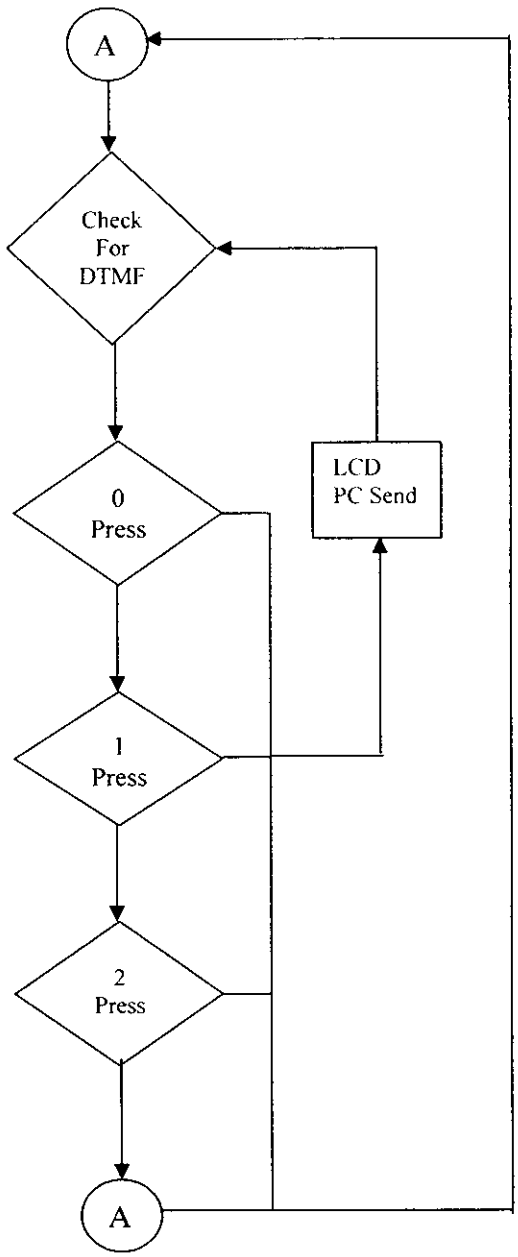
Step9: The access code given to the user is entered.

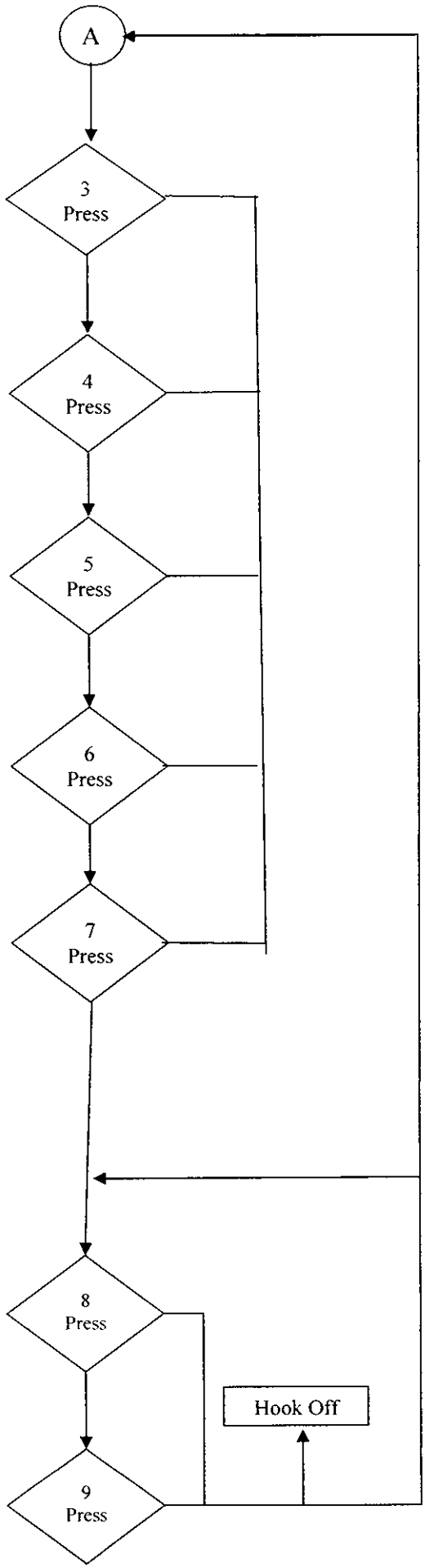
Step10: Then the corresponding information from the data base is retrieved and then sent to the user by the voice card in the form of voice

Step11: After the access has been completed the PC gives instructions to the user to disconnect the call.

5.5 FLOW CHART

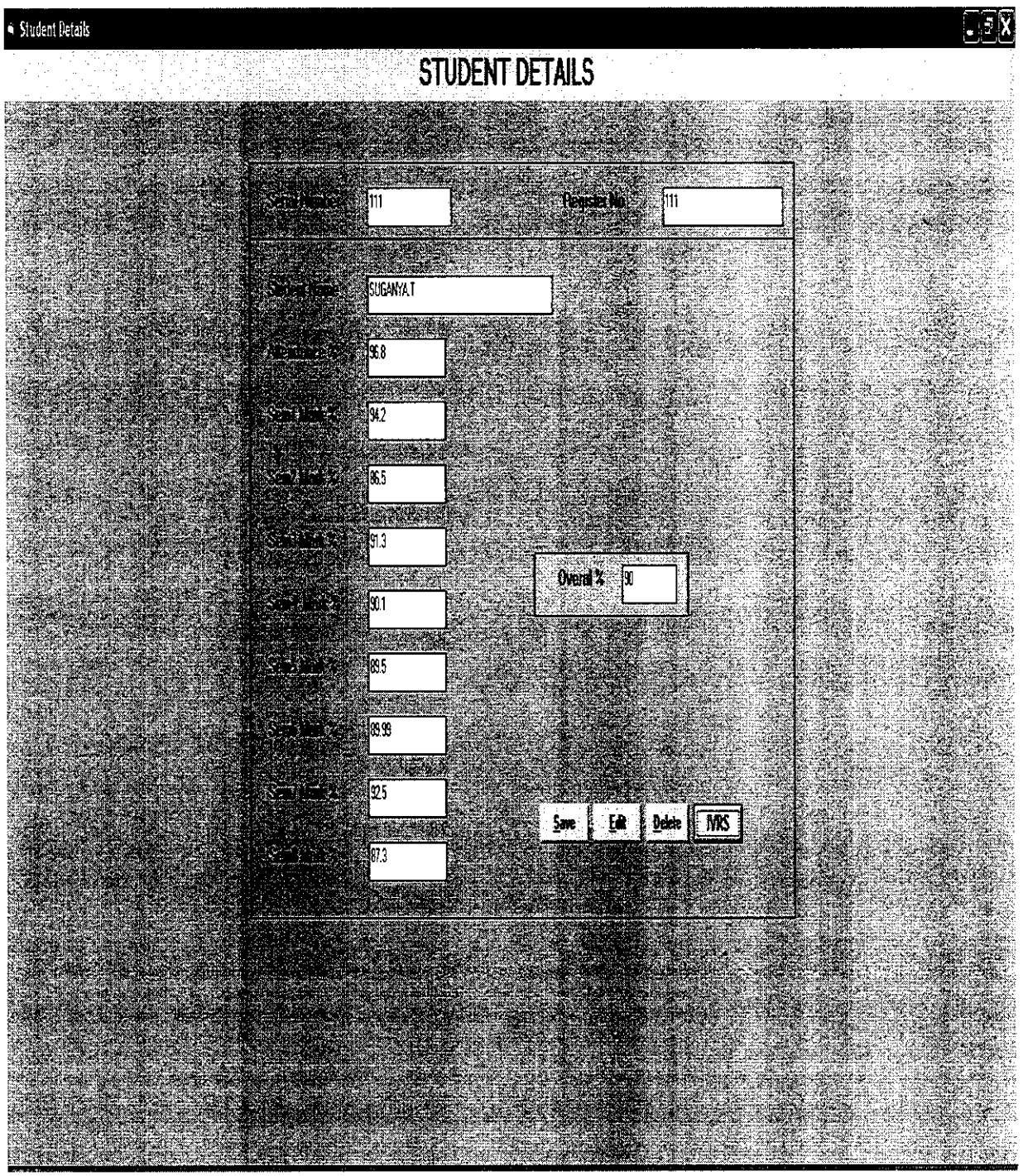


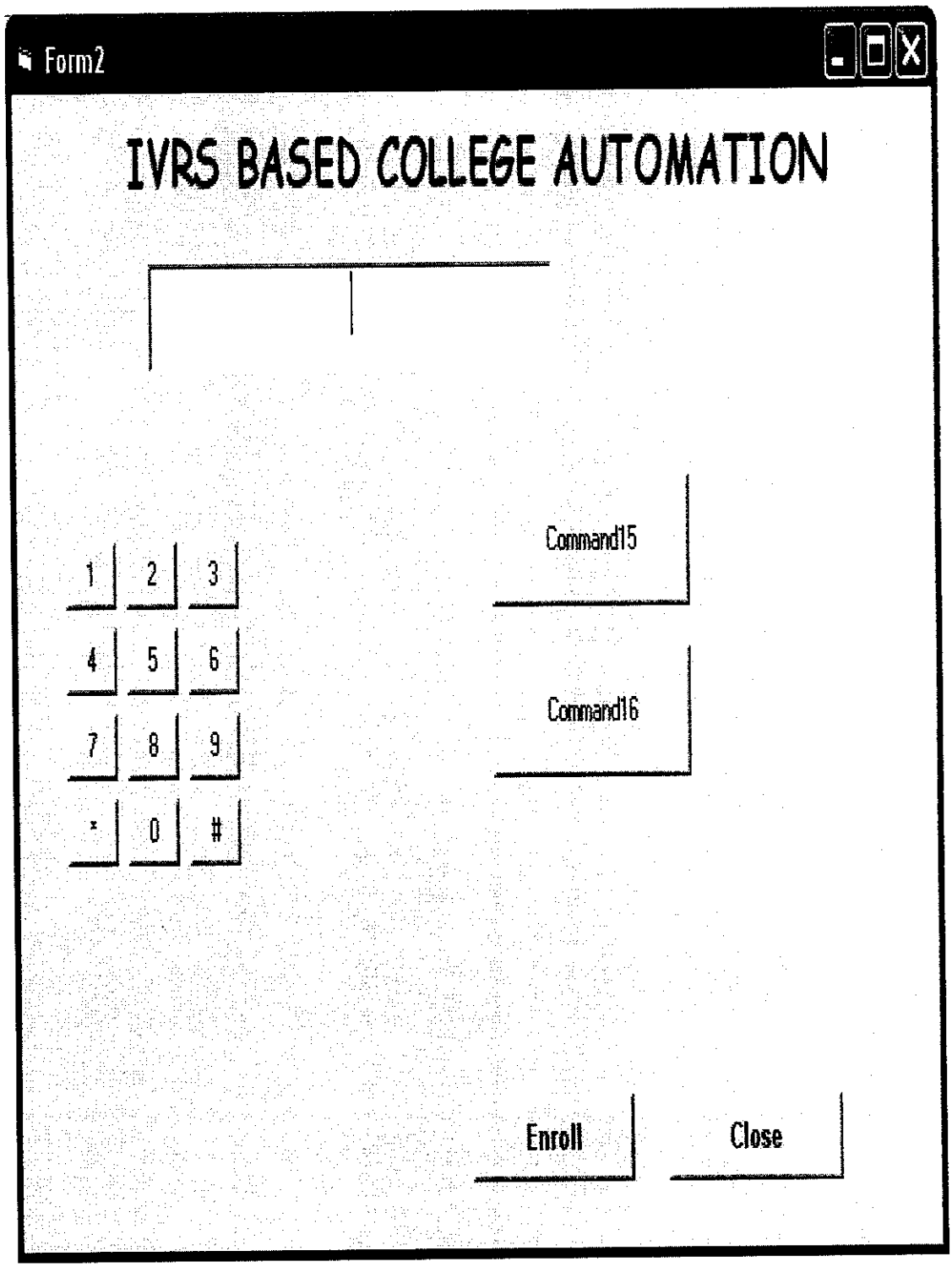

A
Check
For
DTMF
0
Press
LCD
PC Send
1
Press
2
Press
A


A
3
Press
4
Press
5
Press
6
Press
7
Press
8
Press
9
Press
Hook Off

RESULTS

RESULTS


Student Details
STUDENT DETAILS
111
111
SUGANYA.T
96.8
94.2
86.5
91.3
90.1
88.5
88.99
92.5
87.3
Overall %
90
Save
Edit
Delete
MARKS


Form2
IVRS BASED COLLEGE AUTOMATION
1
2
3
4
5
6
7
8
9
*
0
#
Command15
Command16
Enroll
Close

CONCLUSION

CONCLUSION

The system designed will be intelligent for interaction and will suitably provide a good response to the caller who will access it. It will be truly a responsible system for human mankind. The advancements made in such provisions help people in making good use of them whenever and wherever needed. IVR system make the work of parents easier to know their wards marks and other details regarding him or her from the good without making a visit to college. In fact IVR system can also be designed in such a manner that there is a responder on the other side of the line when the parent calls to respond to the questions apart from the information obtained from the database through the pre-recorded voice system.

REFERENCES

REFERENCES

Books:

1. Thiagarajan Vishwanathan" Telecommunication Switching System & Networks", Second Edition

2. Kenneth J.Ayala"The 8051 Microcontroller Architecture ,Programming and Applications"Second Edition

3. Douglas V.Hall"Microcontroller and Interfacing"Second Edition

Websites:

1. http://en.wikipedia.org/wiki/Interactive_voice_response
2. http://web.cmc.net.in/products/ivrs/ivrs.asp
3. http://www.blissit.org/ivrs.htm
4. http://www.kleward.com/ivr_solutions.htm
5. http://en.wikipedia.org/wiki/Special:Search?search=information+on+IVR+system

APPENDIX 1

Features

- Compatible with MCS®-51 Products
- 8K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 10,000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Eight Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)
- Green (Pb/Halide-free) Packaging Option

8-bit Microcontroller with 8K Bytes In-System Programmable Flash

AT89S52

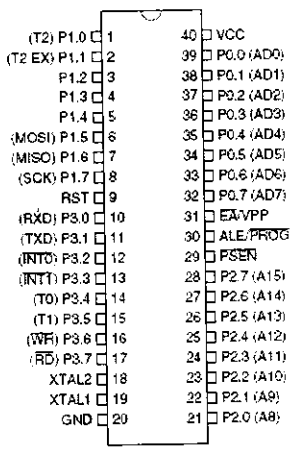
1. Description

The AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

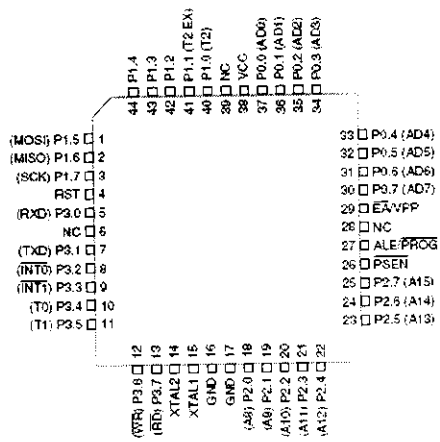
The AT89S52 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

2. Pin Configurations

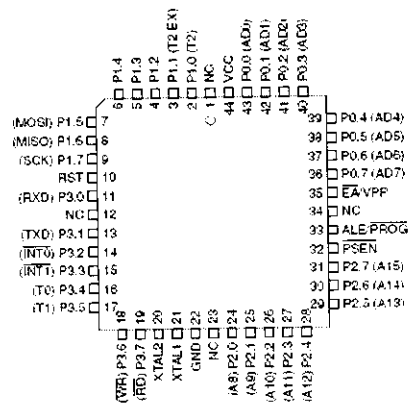
2.1 40-lead PDIP



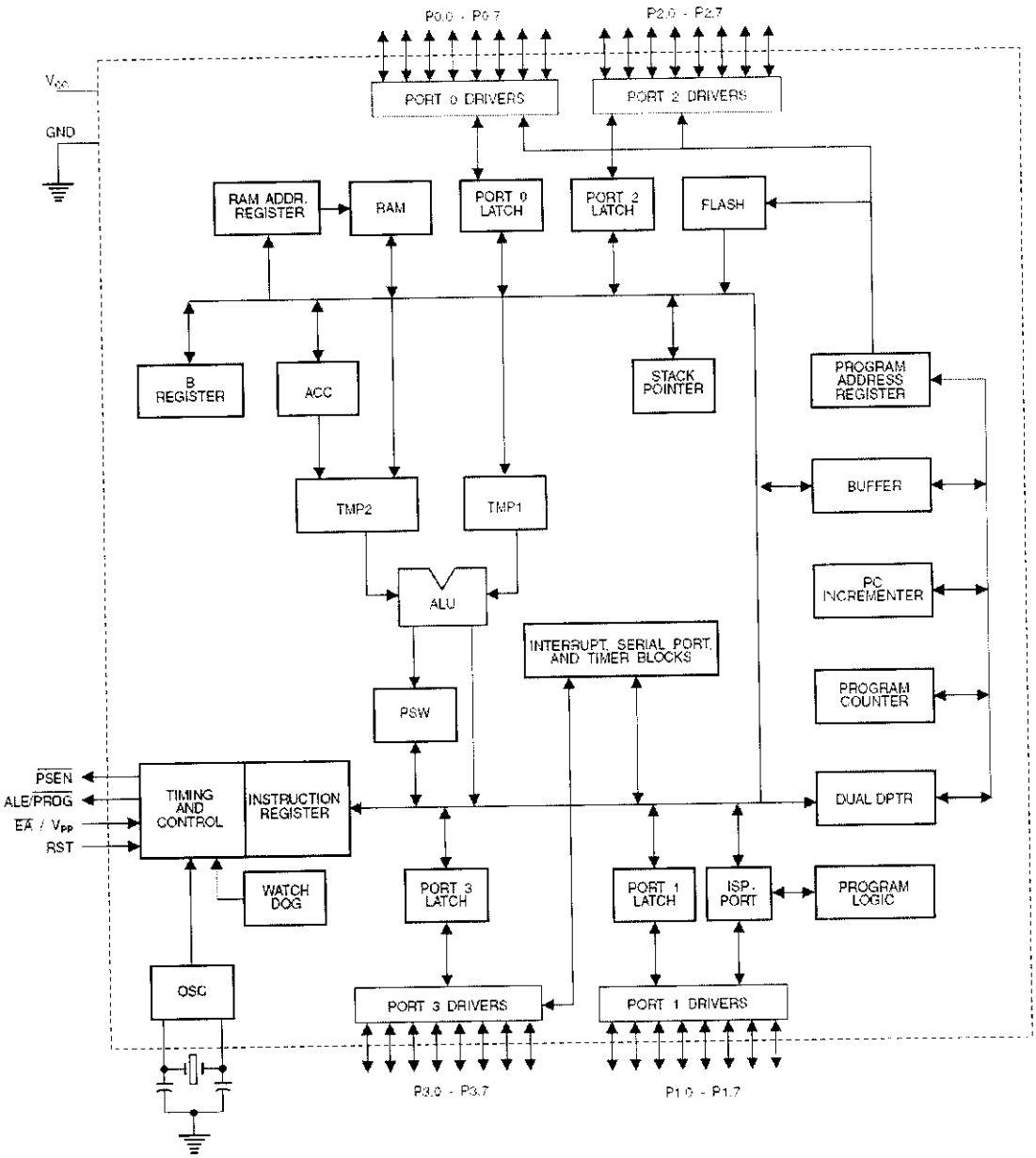
2.2 44-lead TQFP



2.3 44-lead PLCC



3. Block Diagram



4. Pin Description

4.1 VCC

Supply voltage.

4.2 GND

Ground.

4.3 Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

4.4 Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

4.5 Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

4.6 Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S52, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

4.7 RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives high for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

4.8 ALE/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

4.6 Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

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P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
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4.9 $\overline{\text{PSEN}}$

Program Store Enable ($\overline{\text{PSEN}}$) is the read strobe to external program memory.

When the AT89S52 is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

4.10 $\overline{\text{EA}}$/VPP

External Access Enable. $\overline{\text{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be internally latched on reset.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

4.11 XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

4.12 XTAL2

Output from the inverting oscillator amplifier.

11. Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 5-2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 11-1.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

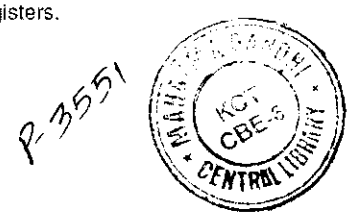
The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536\text{-RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 11-1. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus, when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.



14. Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 16-1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 16-2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

15. Idle Mode

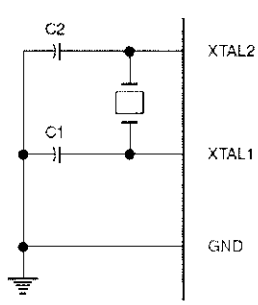
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

16. Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 16-1. Oscillator Connections



Note: 1. C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 16-2. External Clock Drive Configuration

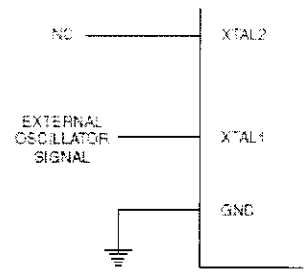


Table 16-1. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

17. Program Memory Lock Bits

The AT89S52 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in Table 17-1.

Table 17-1. Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

22. Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 22-1. Flash Programming Modes

Mode	V_{CC}	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.4-0 Address	P1.7-0 Address
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A12-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A12-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2 P0.3 P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	X 0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	52H	X 0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	X 0010	00H

Notes:
1. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{BSY}$ signal is output on P3.0 during programming.
5. X = don't care.

23. Flash Programming and Verification Characteristics (Parallel Mode)

T_A = 20°C to 30°C, V_{CC} = 4.5 to 5.5V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	11.5	12.5	V
I_{PP}	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
t_{GHAX}	Address Hold After $\overline{PROG}$	48 t_{CLCL}		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
t_{GHDX}	Data Hold After $\overline{PROG}$	48 t_{CLCL}		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48 t_{CLCL}		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	0.2	1	µs
t_{AVQV}	Address to Data Valid		48 t_{CLCL}	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		48 t_{CLCL}	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	48 t_{CLCL}	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		50	µs

Figure 23-1. Flash Programming and Verification Waveforms – Parallel Mode

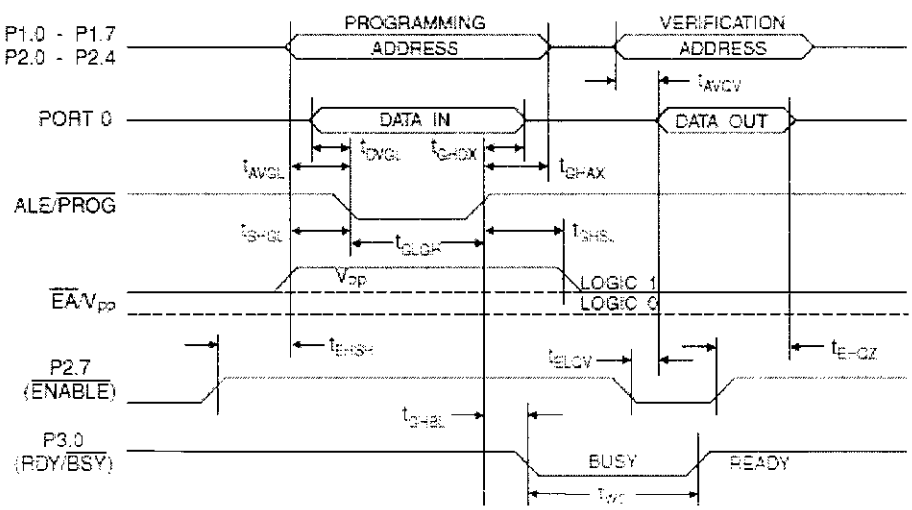


Table 24-1. Serial Programming Instruction Set

Instruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output on MISO)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
Write Lock Bits[1]	1010 1100	1110 00m2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (1).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xxx LB1 LB2 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
Read Signature Bytes	0010 1000	xxx A12 A11 A10 A9 A8	A7 xxx xxx0	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

Note: 1. B1 = 0, B2 = 0 ---> Mode 1, no lock protection
B1 = 0, B2 = 1 ---> Mode 2, lock bit 1 activated
B1 = 1, B2 = 0 ---> Mode 3, lock bit 2 activated
B1 = 1, B2 = 1 ---> Mode 4, lock bit 3 activated

} Each of the lock bit modes needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

25. Serial Programming Characteristics

Figure 25-1. Serial Programming Timing

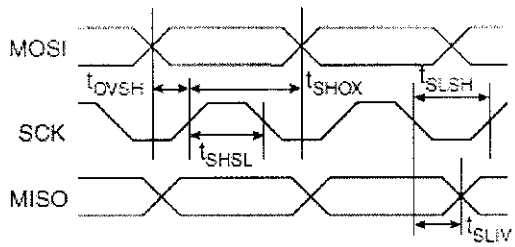


Table 25-1. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	3		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	$8\ t_{CLCL}$			ns
t_{SLSH}	SCK Pulse Width Low	$8\ t_{CLCL}$			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	$2\ t_{CLCL}$			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			$64\ t_{CLCL}$ + 400	µs

26. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

27. DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	kΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

28. AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

28.1 External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	33	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-25		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-25		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

APPENDIX 2

ZARLINK SEMICONDUCTOR

MT8870D/MT8870D-1
ISO²-CMOS Integrated DTMF Receiver

Data Sheet

May 2005

Features

- Complete DTMF Receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode
- Backward compatible with MT8870C/MT8870C-1

Applications

- Receiver system for British Telecom (BT) or CEPT Spec (MT8870D-1)
- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote control
- Personal computers
- Telephone answering machine

Ordering Information

MT8870DE	18 Pin PDIP	Tubes
MT8870DS	18 Pin SOIC	Tubes
MT8870DN	20 Pin SSOP	Tubes
MT8870DSR	18 Pin SOIC	Tape & Reel
MT8870DNR	20 Pin SSOP	Tape & Reel
MT8870DN1	20 Pin SSOP*	Tubes
MT8870DE1	18 Pin PDIP*	Tubes
MT8870DS1	18 Pin SOIC*	Tubes
MT8870DNR1	18 Pin SSOP*	Tape & Reel
MT8870DSR1	18 Pin SOIC*	Tape & Reel
MT8870DE1-1	18 Pin PDIP*	Tubes
MT8870DS1-1	18 Pin SOIC*	Tubes
MT8870DSR1-1	18 Pin SOIC*	Tape & Reel

*Pb Free Matte Tin

-40°C to +85°C

Description

The MT8870D/MT8870D-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code.

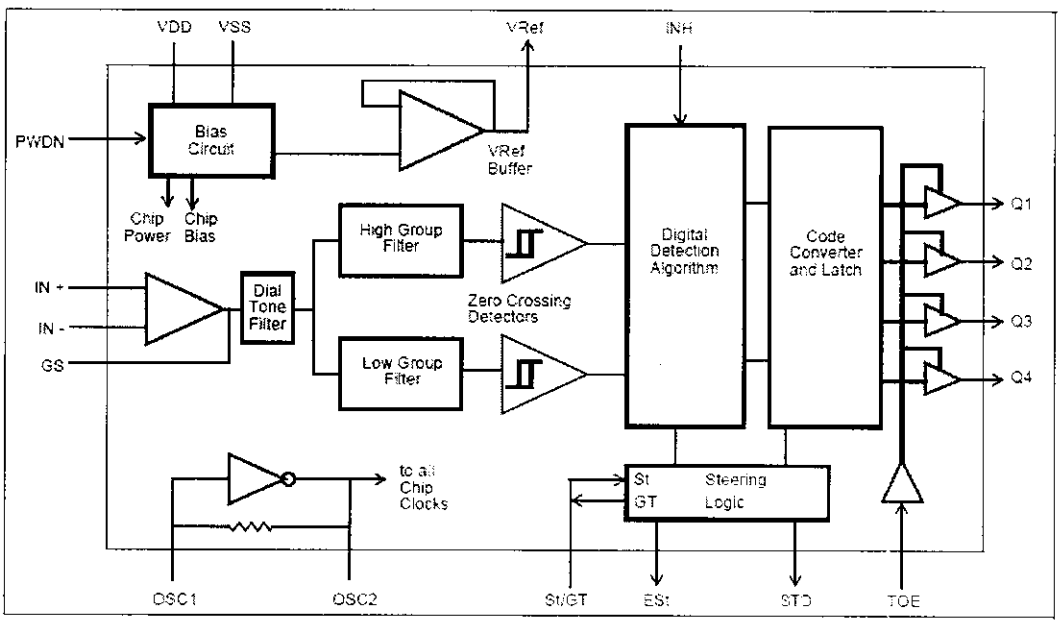


Figure 1 - Functional Block Diagram

External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

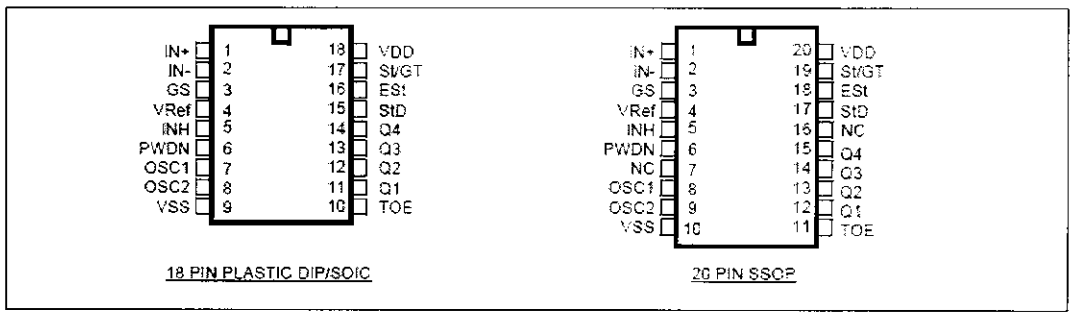


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
18	20		
1	1	IN+	**Non-Inverting Op-Amp (Input).**
2	2	IN-	**Inverting Op-Amp (Input).**
3	3	GS	**Gain Select.** Gives access to output of front end differential amplifier for connection of feedback resistor.
4	4	V_{Ref}	**Reference Voltage (Output).** Nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig. 6 and Fig. 10).
5	5	INH	**Inhibit (Input).** Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down.
6	6	PWDN	**Power Down (Input).** Active high. Powers down the device and inhibits the oscillator. This pin input is internally pulled down.
7	8	OSC1	**Clock (Input).**
8	9	OSC2	**Clock (Output).** A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
9	10	V_{SS}	**Ground (Input).** 0 V typical.
10	11	TOE	**Three State Output Enable (Input).** Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
11-14	12-15	Q1-Q4	**Three State Data (Output).** When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.
15	17	StD	**Delayed Steering (Output).** Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt}.
16	18	ESt	**Early Steering (Output).** Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.

Pin Description

Pin #		Name	Description
18	20		
17	19	St/GT	**Steering Input/Guard time (Output) Bidirectional.** A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	20	V_{DD}	**Positive power supply (Input).** +5 V typical.
	7, 16	NC	No Connection.

Functional Description

The MT8870D/MT8870D-1 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Figure 3). Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

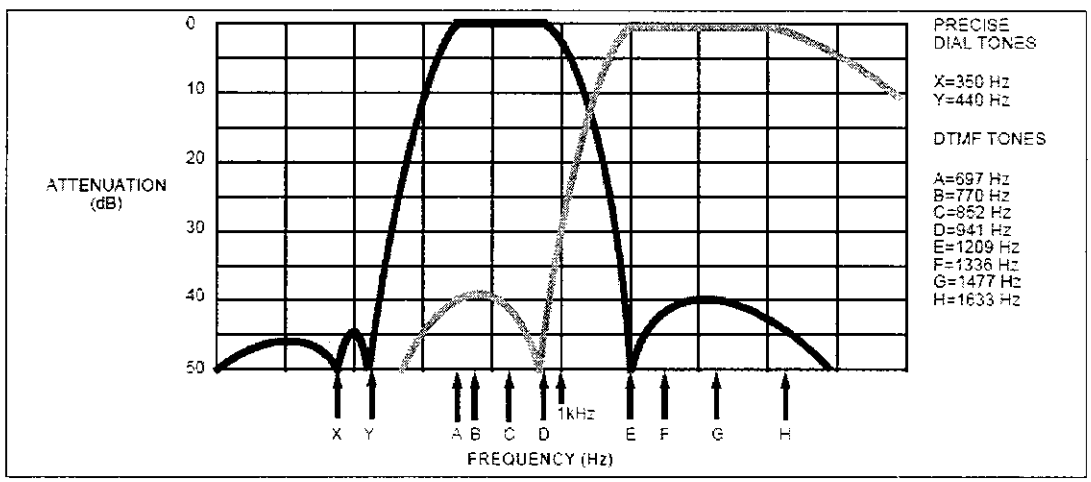


Figure 3 - Filter Response

The value of t_{DP} is a device parameter (see Figure 11) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 µF is recommended for most applications, leaving R to be selected by the designer.

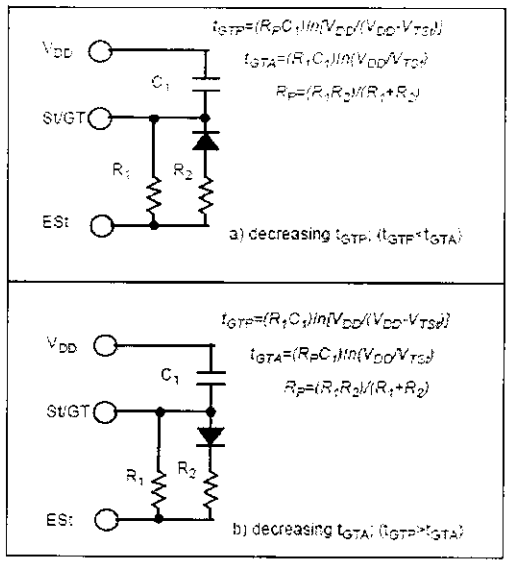


Figure 5 - Guard Time Adjustment

Digit	TOE	INH	ESt	Q_4	Q_3	Q_2	Q_1
ANY	L	X	H	Z	Z	Z	Z
1	H	X	H	0	0	0	1
2	H	X	H	0	0	1	0
3	H	X	H	0	0	1	1
4	H	X	H	0	1	0	0
5	H	X	H	0	1	0	1
6	H	X	H	0	1	1	0
7	H	X	H	0	1	1	1
8	H	X	H	1	0	0	0
9	H	X	H	1	0	0	1
0	H	X	H	1	0	1	0
*	H	X	H	1	0	1	1
#	H	X	H	1	1	0	0
A	H	L	H	1	1	0	1
B	H	L	H	1	1	1	0
C	H	L	H	1	1	1	1
D	H	L	H	0	0	0	0
A	H	H	L	undetected, the output code will remain the same as the previous detected code			
B	H	H	L				
C	H	H	L				
D	H	H	L				

Table 1 - Functional Decode Table

L=LOGIC LOW, H=LOGIC HIGH, Z=HIGH IMPEDANCE
X = DON'T CARE

Parameter	Unit	Resonator
R1	Ohms	10.752
L1	mH	.432
C1	pF	4.984
C0	pF	37.915
Qm	-	896.37
Δf	%	±0.2%

Table 2 - Recommended Resonator Specifications

Note: Qm=quality factor of RLC model, i.e., $1/2\Pi fR1C1$.

Applications

Receiver System for British Telecom Spec POR 1151

The circuit shown in Fig. 9 illustrates the use of MT8870D-1 device in a typical receiver system. BT Spec defines the input signals less than -34 dBm as the non-operate level. This condition can be attained by choosing a suitable values of R_1 and R_2 to provide 3 dB attenuation, such that -34 dBm input signal will correspond to -37 dBm at the gain setting pin GS of MT8870D-1. As shown in the diagram, the component values of R_3 and C_2 are the guard time requirements when the total component tolerance is 6%. For better performance, it is recommended to use the non-symmetric guard time circuit in Fig. 8.

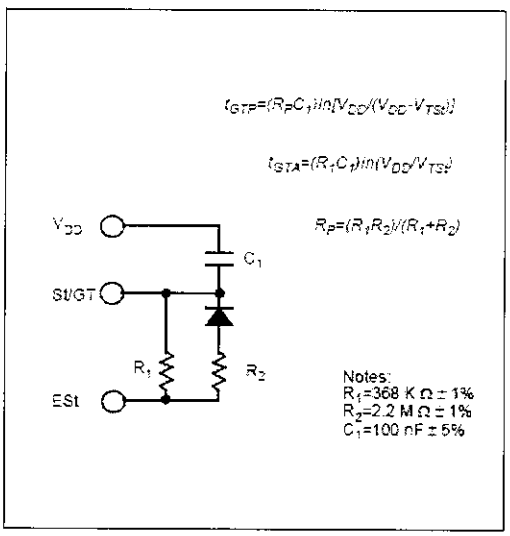


Figure 8 - Non-Symmetric Guard Time Circuit

Absolute Maximum Ratings†

	Parameter	Symbol	Min.	Max.	Units
1	DC Power Supply Voltage	V_{DD}		7	V
2	Voltage on any pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin (other than supply)	I_I		10	mA
4	Storage temperature	T_{STG}	-65	+150	°C
5	Package power dissipation	P_D		500	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Derate above 75°C at 16 mW / °C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	DC Power Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2	Operating Temperature	T_O	-40		+85	°C	
3	Crystal/Clock Frequency	fc		3.579545		MHz	
4	Crystal/Clock Freq.Tolerance	Δfc		±0.1		%	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

DC Electrical Characteristics - V_{DD}=5.0V± 5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	SUPPLY	Standby supply current	I_{DDQ}		10	25	µA	PWDN=V_{DD}
2		Operating supply current	I_{DD}		3.0	9.0	mA	
3		Power consumption	P_O		15		mW	fc=3.579545 MHz
4	INPUTS	High level input	V_{IH}	3.5			V	V_{DD}=5.0 V
5		Low level input voltage	V_{IL}			1.5	V	V_{DD}=5.0 V
6		Input leakage current	I_{IH}/I_{IL}		0.1		µA	V_{IN}=V_{SS} or V_{DD}
7		Pull up (source) current	I_{SO}		7.5	20	µA	TOE (pin 10)=0, V_{DD}=5.0 V
8		Pull down (sink) current	I_{SI}		15	45	µA	INH=5.0 V, PWDN=5.0 V, V_{DD}=5.0 V
9		Input impedance (IN+, IN-)	R_{IN}		10		MΩ	@ 1 kHz
10		Steering threshold voltage	V_{TSt}	2.2	2.4	2.5	V	V_{DD} = 5.0 V

DC Electrical Characteristics - V_{DD}=5.0V±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
11	OUTPUTS	Low level output voltage	V_{OL}			V_{SS}+0.03	V	No load
12		High level output voltage	V_{OH}	V_{DD}-0.03			V	No load
13		Output low (sink) current	I_{OL}	1.0	2.5		mA	V_{OUT}=0.4 V
14		Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT}=4.6 V
15		V_{Ref} output voltage	V_{Ref}	2.3	2.5	2.7	V	No load, V_{DD} = 5.0V
16		V_{Ref} output resistance	R_{OR}		1		kΩ	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Operating Characteristics - V_{DD}=5.0V±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated.
Gain Setting Amplifier

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Input leakage current	I_{IN}			100	nA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input resistance	R_{IN}	10			MΩ	
3	Input offset voltage	V_{OS}			25	mV	
4	Power supply rejection	PSRR	50			dB	1 kHz
5	Common mode rejection	CMRR	40			dB	0.75 V ≤ V_{IN} ≤ 4.25 V biased at V_{Ref} =2.5 V
6	DC open loop voltage gain	A_{VOL}	32			dB	
7	Unity gain bandwidth	f_C	0.30			MHz	
8	Output voltage swing	V_O	4.0			V_{pp}	Load ≥ 100 kΩ to V_{SS} @ GS
9	Maximum capacitive load (GS)	C_L			100	pF	
10	Resistive load (GS)	R_L			50	kΩ	
11	Common mode range	V_{CM}	2.5			V_{pp}	No Load

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