FLC BASED TEMPERATURE CONTROLLER USING LABVIEW

A Project Report

Submitted By

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BONAFIDE CERTIFICATE

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External Examiner

ABSTRACT

The objective of this project is to simulate a Fuzzy Logic temperature control system that can be used in boilers, furnaces and other industrial applications. The project aims to simulate the entire process of temperature control, its variations and as to how fuzzy controller determines its response in LABVIEW.

The temperature is received from the sensor i.e is a thermistor in this case, kept in boiler setup. The signal received is signal conditioned, amplified and converted to a digital signal using a Analog To Digital Converter. The digital signal is transmitted through the parallel port of the computer to the LabVIEW platform and processed based on fuzzy algorithm. The controlled output is sent to the control circuit which regulates the heater to maintain the temperature at predetermined setpoint.

ACKNOWLEDGEMENT

The completion of this project can be attributed to the combined efforts made by us and the contribution made in one form or the other by the individuals we hereby acknowledge.

We thank our beloved Principal **Dr.S.Ramachandran** for providing all facilities all facilities to carry out this project work.

We express our heart felt gratitude and thanks to the HOD of Electronics & Instrumentation Engineering. **Prof.R.Annamalai** , for encouraging us and for being with us right from the beginning of the project and guided us at every step.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

CHAPTER 1

INTRODUCTION

1.1 GENERAL BLOCK DIAGRAM

The block diagram of the FLC based temperature controller is shown in Fig1.1

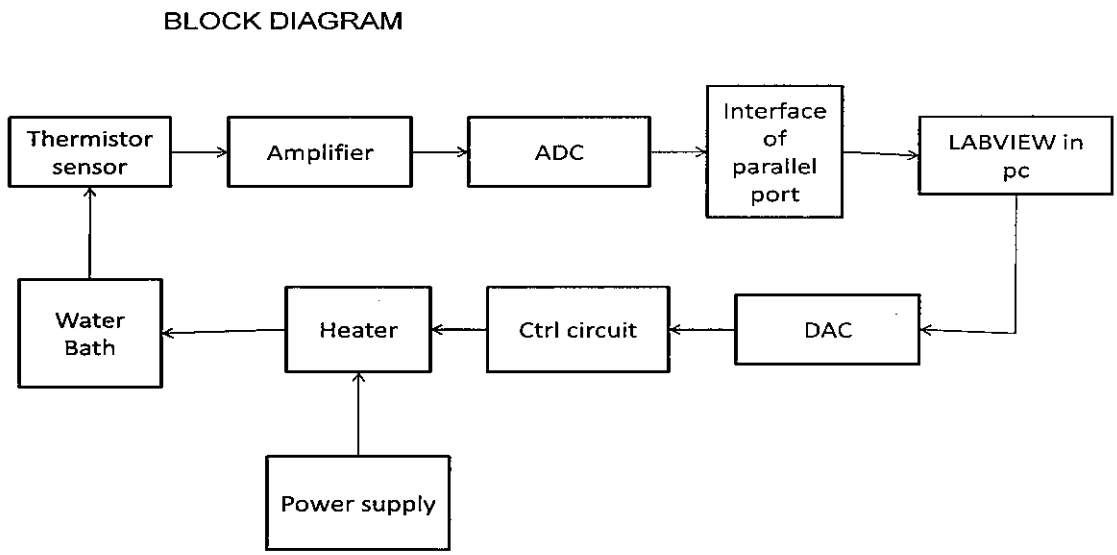

FIG 1.1 FLC BASED TEMPERATURE CONTROL

It consists of four main functions. They are

- **TEMPERATURE SENSING**
- **SIGNAL CONDITIONING AND AMPLIFICATION**
- **INTERFACING**
- **CONTROL AND IMPLEMENTATION**

The above individual sections are explained in detail further on.

1.2 SENSING

The project makes use of a thermistor type sensor to detect the temperature from the requisite test location, which can be a boiler, a furnace or any other industrial application needing temperature control. The sensed signal is then sent to the signal conditioned circuit.

1.3 SIGNAL CONDITIONING AND AMPLIFICATION

The signal received from the thermistor setup is then filtered, amplified and then sent to the interfacing circuit.

1.4 INTERFACING CIRCUIT

The input signals that is obtained after being processed and amplified are connected to PC (Lab VIEW software) through a interfacing unit. The interfacing unit consists of LPT (line printer terminal) which is used to interface the computer and the kit. For the channel selection, data bus is taken through a latch (74LS273) and it is converted here as data bus and address bus. Then the address bus is given to selection of channels in the ADC. Then the converted digital signal from ADC is is given to the parallel port of computer.

1.5 CONTROL AND IMPLEMENTATION

The controller plays a major role in controlling the overall process. The fuzzy controller is implemented using FLC toolbox .The temperature sensed by thermistor is controlled by the fuzzy controller and given to the heater control circuit. If the temperature reaches the above the set point, the controller controls the TRIAC control circuit to turn off the heater and if the temperature reaches below the set point it will make the TRIAC to turn on.

CHAPTER 2

CHAPTER 2

FUZZY LOGIC CONTROL

2.1 FUZZY LOGIC CONTROL

The fuzzy logic is a unique concept.

Fuzzy" the term indicates indistinct or haziness. The Fuzzy logic was invented by professor **L.A.Zadeh** of California University at Berkeley in the year 1965. The invention was not recognized globally until it was implemented practically by **Dr.E.H.Mamdani** a professor at London University. Fuzzy controller is an automatic controller that can be used in control application to control the object based on its desired behavior. Unlike the traditional 'yes' or 'no' decisions the fuzzy logic allows a graduation from 'yes' to 'no'. The fuzzy logic works on set of rules and these will be created by the engineers.

For example if you take a fuzzy controlled air conditioner, the rules behind them are less precise. For instance if the room temperature is warm then the controller will automatically increase the cooling. Fuzzy logic systems are not only used for smaller application but it's also used for complex applications. Some complex problems can be solved only using fuzzy logic due its rules and sets and the one more thing is that it is faster compared to the conventional controllers. In this project fuzzy control is implemented with PI control for position control of the DC motor.

2.2 IMPORTANT TERMS

Some important terms related to fuzzy logic are briefly summarized below.

FUZZY SET: The values or the parameters used in fuzzy control are put together to form fuzzy set and they are usually described in qualitative terms like large, medium, small, Zero, positive and negative.

MEMBERSHIP VALUE: The degree a control variable or parameters belongs to a fuzzy set is denoted by a membership value between 0 and 1.

MEMBERSHIP FUNCTION: A membership function associated with the fuzzy set maps a control variable or parameter to its appropriate membership value.

FUZZY RULE: The fuzzy rule is usually in the form: if X is A and Y is B and Z is C where x and y are inputs and z is output. The if then statements are combined by using either and or or connection.

DEFUZZIFICATION: The output of fuzzy should be converted in to a single value so that it can be used as a control signal to control the plant and Defuzzification block do this process.

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2.3 FUZZY CONTROLLER THEORY

The block diagram of fuzzy control is shown next.

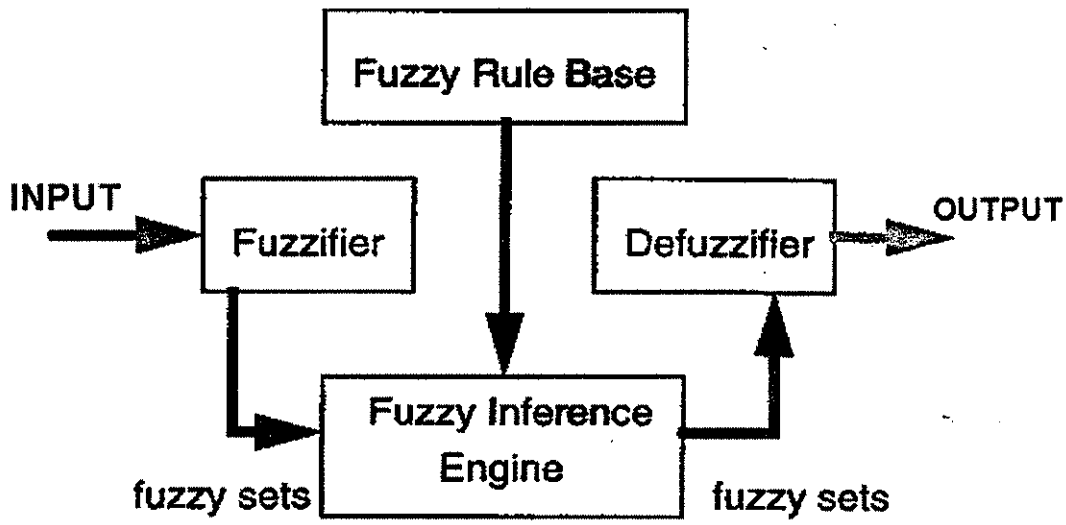


FIG 2.1 BLOCK DIAGRAM OF FLC

2.4 FUZZY CONTROLLER COMPONENTS

The fuzzy controller is made up of Fuzzification block, Rule base block, Interference engine block and the Defuzzification block. Fuzzification block converts each and every input into a look up table in the membership functions to derive the membership grades.

Rule base block consists of set of rules that links the input and the output. The rules are formed using if then statements and are connected using either and or or connection. Interference engine block is the one which links the Fuzzification and Defuzzification block. Defuzzification block converts the output to a single value so that it can be used as a control signal to the plant.

2.5 ADVANTAGES OF FUZZY LOGIC

Here is a list of general observations about fuzzy logic:

- Fuzzy logic is conceptually easy to understand.

  The mathematical concepts behind fuzzy reasoning are very simple. Fuzzy logic is a more intuitive approach without the far-reaching complexity.

- Fuzzy logic is flexible.

  With any given system, it is easy to layer on more functionality without starting again from scratch.

- Fuzzy logic is tolerant of imprecise data.

  Everything is imprecise if you look closely enough, but more than that, most things are imprecise even on careful inspection. Fuzzy reasoning builds this understanding into the process rather than tacking it onto the end.

- Fuzzy logic can model nonlinear functions of arbitrary complexity.

  You can create a fuzzy system to match any set of input-output data. This process is made particularly easy by adaptive techniques like Adaptive

Neuro-Fuzzy Inference Systems (ANFIS), which are available in Fuzzy Logic Toolbox software.

- In direct contrast to neural networks, which take training data and generate opaque, impenetrable models, fuzzy logic lets you rely on the experience of people who already understand your system.
- Fuzzy logic can be blended with conventional control techniques.

  Fuzzy systems don't necessarily replace conventional control methods. In many cases fuzzy systems augment them and simplify their implementation.

- Fuzzy logic is based on natural language.

  The basis for fuzzy logic is the basis for human communication. This observation underpins many of the other statements about fuzzy logic. Because fuzzy logic is built on the structures of qualitative description used in everyday language, fuzzy logic is easy to use.

The last statement is perhaps the most important one and deserves more discussion. Natural language, which is used by ordinary people on a daily basis, has been shaped by thousands of years of human history to be convenient and efficient. Sentences written in ordinary language represent a triumph of efficient communication.

CHAPTER 3

CHAPTER 3

TEMPERATURE MEASUREMENT

3.1 TEMPERATURE MEASUREMENT

The temperature measurement device used here is the Themistor type.

A **Thermistor** is a type of resistor used to measure temperature changes, relying on the change in its resistance with changing temperature.

The relationship between resistance and temperature is linear (i.e. A first-order approximation), then it can be said that:

$$\Delta R = k\Delta T$$

Where

ΔR = change in resistance

ΔT = change in temperature

k = first-order temperature coefficient of resistance

Thermistors can be classified into two types depending on the sign of k. If k is positive, the resistance increases with increasing temperature, and the device is called a positive temperature coefficient (**PTC**) Thermistor, **Posistor**. If k is negative, the resistance decreases with increasing temperature, and the device is called a negative temperature coefficient (**NTC**) Thermistor. Resistors that are not Thermistors are designed to have the smallest possible k, so that their resistance remains almost constant over a wide temperature range.

3.1.1 THERMISTOR

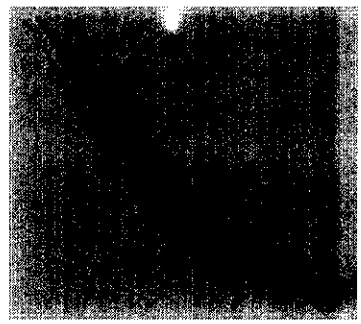


FIG 3.1 THERMISTER

3.1.2 SYMBOL

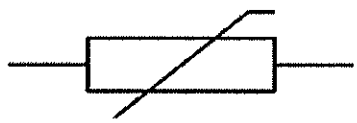
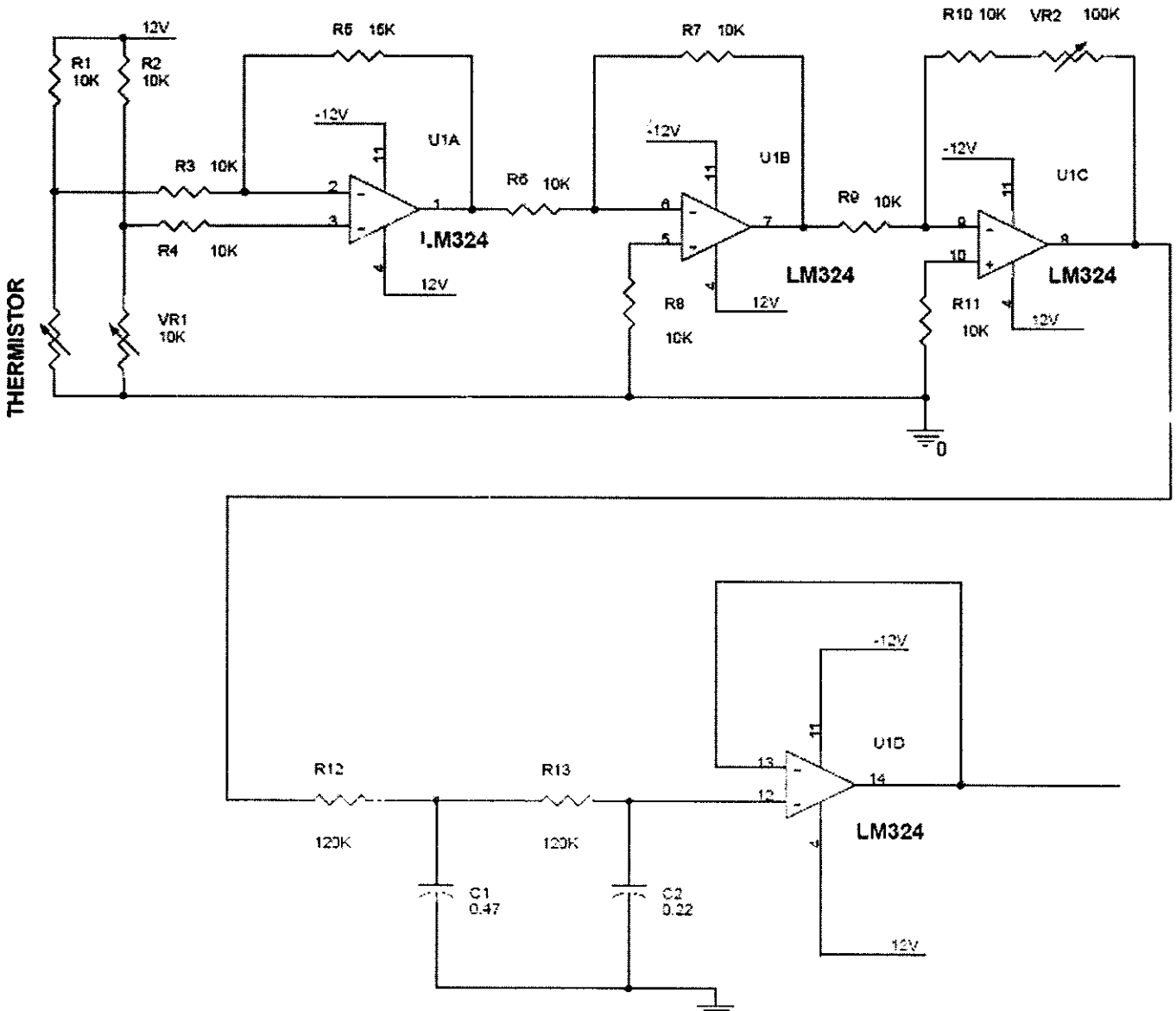


FIG 3.2 SYMBOL

3.2 CIRCUIT DESCRIPTION:

In this circuit the Thermistor is used to measure the temperature. Thermistor is nothing but temperature sensitive resistor. There are two types of Thermistors available such as positive temperature co-efficient and negative temperature co-efficient. Here the negative temperature co-efficient is used in which the resistance value is decreased when the temperature is increased.

THERMISTER CIRCUIT



Here the Thermistor is connected with resister bridge network. The bridge terminals are connected to inverting and non-inverting input terminals of comparator. The comparator is constructed by LM 324 operational amplifier.

The LM 324 consists of four independent, high gains, internally frequency compensated operational amplifier which were designed specifically to operate from a single power supply over a wide voltage range.

The first stage is a comparator in which the variable voltage due to Thermistor is given to inverting input terminal and reference voltage is given to non-inverting input terminal.

Initially the reference voltage is set to room temperature level so the output of the comparator is zero. When the temperature is increased above the room temperature level, the Thermistor resistance is decreased so variable voltage is given to comparator. Now the comparator delivered the error voltage at the output. Then the error voltage is given to next stage of preamplifier. Here the input error voltage is amplified then the amplified voltage is given to next stage of gain amplifier. In this amplifier the variable resistor is connected as feedback resistor. The feedba feedback resistor is adjusted to get desired gain. Then the AC components in the output are filtered with the help of capacitors. Then output voltage is given to final stage of DC voltage follower through this the output voltage is given to ADC or other circuit.

CHAPTER 4

CHAPTER 4

ANALOG TO DIGITAL CONVERSION

4.1 INTRODUCTION

The functional components involved in analog to digital conversion circuit: ADCO0809, 555 Timer, 74HC240 and 74HC245.

The interfacing circuit consists of two buffers IC's 74HC244 which is similar to 74HC240 but non-inverting. With the help of these buffers the input to the computer is given.

4.2 DESCRIPTION

The analog to digital conversion circuit transforms the analog signal from the sensors in to digital signals, to be interfaced with the parallel port.

The analog signals: drum level, furnace pressure, super heater pressure and drum level set point are connected to the input terminals of the ADC0809 as in the figure.

The ADC0809 converts the analog input signals (A_0 to A_7) into digital outputs by successive approximation method. The 555 timer is used to generate the clock pulses for the ADC0809. Some of the features are listed below

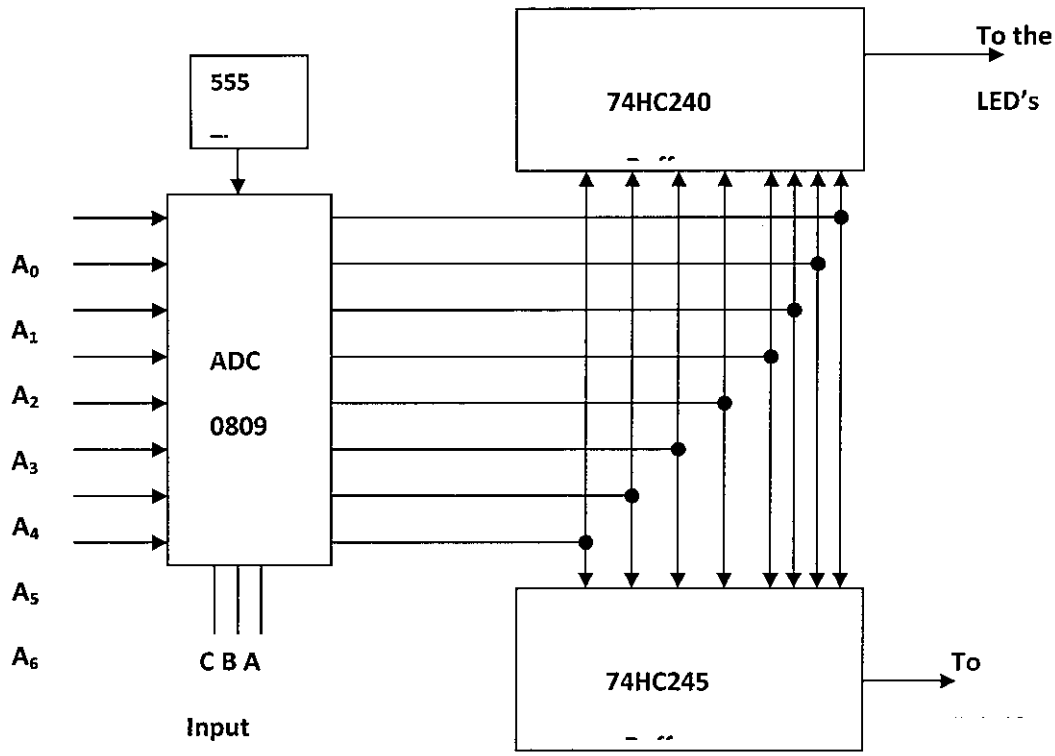


FIG 4.1 ADC CIRCUIT WITH BUFFER

The digital output lines (D_0 to D_7) are connected to the inverting buffer 74HC240 and non inverting buffer 74HC245. The output terminals of the inverting buffer 74HC240 are connected to the LED's for on-spot detection of the output. The non inverting buffer is connected to the main interfacing buffer 74HC244. It acts as a protection circuit for the ADC0809. The circuit is provided with a power supply of +5V and the ADC0809 input address pins (A, B, C) are connected to parallel port.

4.3 ADC 0809

The ADC0803, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register.

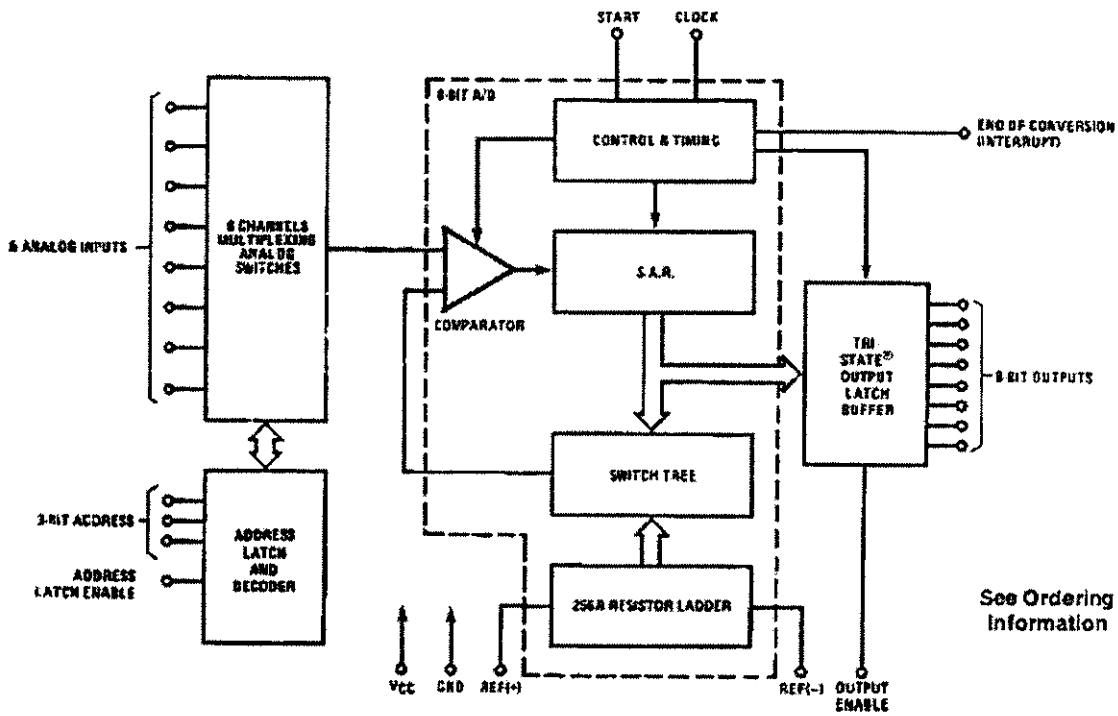


FIG 4.2 ADC CONVERSION

The 8-channel multiplexer can directly access any of 8-single-ended analog signals. The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and

decoded multiplexer address inputs and latched TTL TRI-STATE... outputs. The design of the ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0809 offers high-speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications.

4.4 FEATURES

1. Easy interface to all microprocessors.
2. Operates ratiometrically or with 5 VDC or analog span adjusted voltage reference.
3. No zero or full-scale adjust required.
4. 8-channel multiplexer with address logic.
5. 0V to 5V input range with single 5V power supply.
6. Outputs meet TTL voltage level specifications.

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4.5 FUNCTIONAL DESCRIPTION

4.5.1 MULTIPLEXER

The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. The table shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

SELECTED	ADDRESS LINE		
ANALOG CHANNEL	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

TABLE 4.1 CHANNEL SELECTION

4.6 CONVERTER CHARACTERISTICS

4.6.1 THE CONVERTER

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register

and the comparator. The converter's digital outputs are positive true. The 256R ladder network approach was chosen over the conventional R/2R ladder because of its inherent monotonic, which guarantees no missing digital codes.

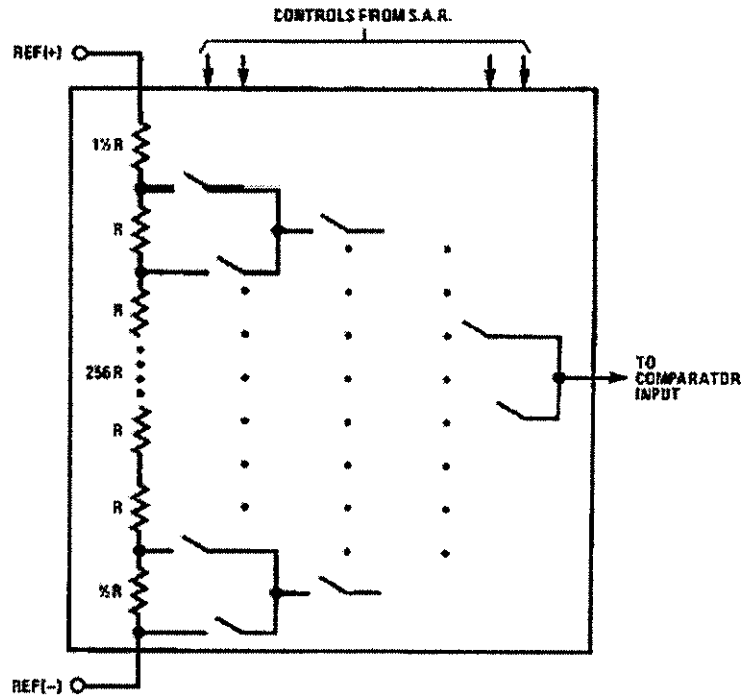


FIG 4.3 R/2R LADDER DIAGRAM

Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system.

Additionally, the 256R network does not cause load variations on the reference voltage. The bottom resistor and the top resistor of the ladder network in figure are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full

scale points of the transfer curve. The first output transition occurs when the analog signal has reached a (/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. Figure shows a typical example of a 3-bit converter.

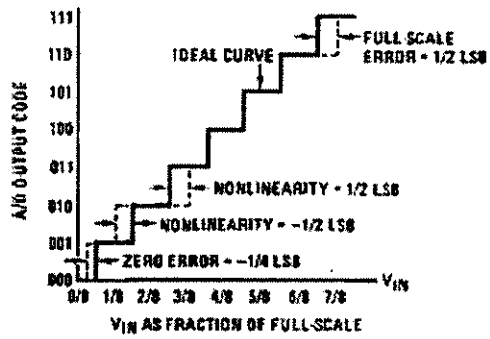


FIG 4.4 OUTPUT OF SAR

In the ADC0809, the approximation technique is extended to 8 bits using the 256R network. The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors. The timing diagram of the analog to digital converter (ADC0809) is shown below in the fig.4.5

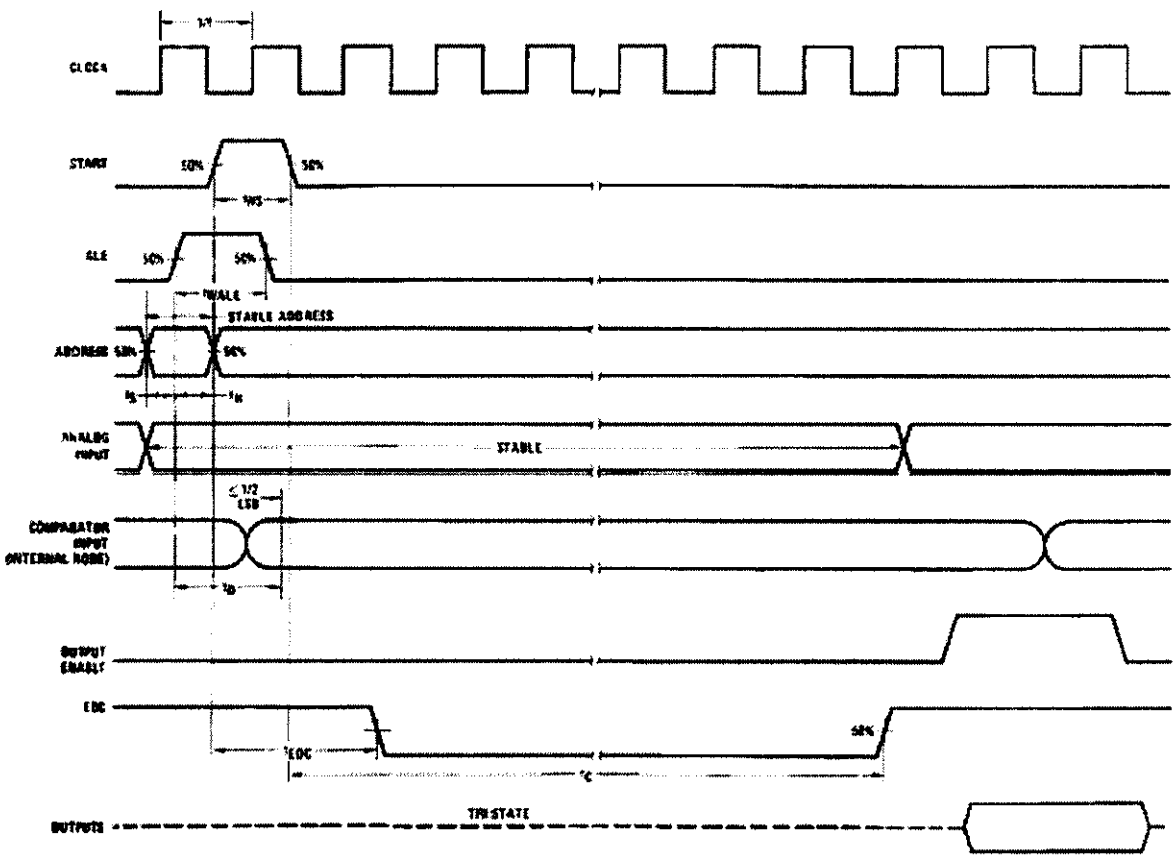


FIG 4.5 TIMING DIAGRAM PIN DIAGRAM

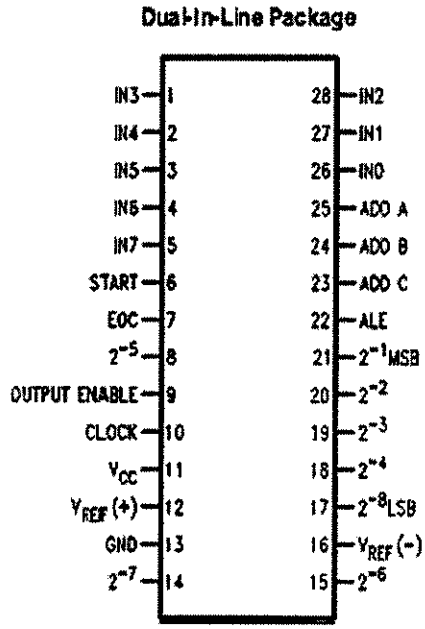


FIG 4.6 PIN DIAGRAM

4.7 IC 555 TIMERS

4.7.1 GENERAL DESCRIPTION

The 555 timer is a highly stable device for generating accurate time delay or oscillation. It can provide time delay ranging from microseconds to hours. It is used to generate clock pulses for ADC0809.

4.7.2 PIN DIAGRAM

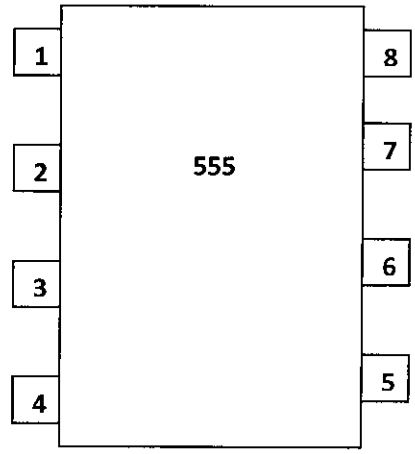


FIG 4.7 PIN DIAGRAM OF TIMER

4.7.3 PIN DESCRIPTION

Pin no:	Description
1	Ground
2	Trigger
3	Output
4	Reset
5	Control Voltage
6	Threshold
7	Discharge
8	V_{cc}

TABLE 4.2 PIN DESCRIPTION

4.7.4 FEATURES

Its main features make it more preferable in the circuit integration.

1. Compatible with CMOS/TTL logics.
2. Supply voltage in the range of +5V to +18V.
3. It can drive load up to 200mA.
4. It can be used as pulse generator, voltage monitor etc.

4.8 INVERTING BUFFER 74HC240

4.8.1 GENERAL DESCRIPTION

The 74HC240 3-STATE buffer utilizes advanced silicon-gate CMOS technology. It possesses high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity and low power consumption. It has a fanout of 15 LS-TTL equivalent inputs. The 74HC240 is an inverting buffer and has two active LOW enables (1G and 2G). Each enable independently controls 4 buffers. All inputs are protected from damage due to static discharge by diodes to VCC and ground.

The connection diagram and the truth table of 74HC240 are shown in the figures.

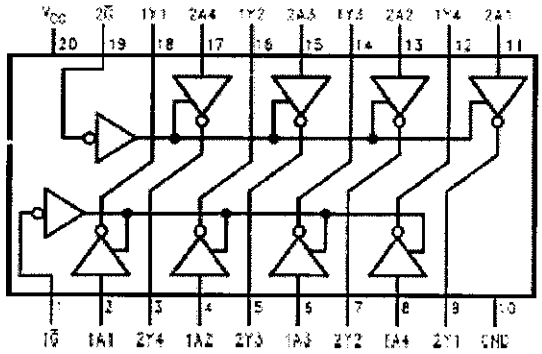


FIG 4.8 CONNECTION DIAGRAM

Truth Table

$\overline{1G}$	1A	1Y	$\overline{2G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = HIGH Level
L = LOW Level
Z = HIGH Impedance

TABLE 4.3 TRUTH TABLE

4.8.2 FEATURES

1. Typical propagation delay: 12 ns.
2. 3-STATE outputs for connection to system buses.
3. Wide power supply range: 2–6V.
4. Low quiescent supply current: 80 μA (74 Series).
5. Output current: 6 mA.

4.9 NON INVERTING BUFFER 74HC245

4.9.1 GENERAL DESCRIPTION

The 74HC/HCT245 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). The 74HC245 are octal trans

ceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The "245" features an output enable (OE) input for easy cascading and a send/receive (DIR) for direction control. OE controls the outputs so that the buses are effectively isolated. The "245" has true (non-inverting) outputs.

4.9.2 PIN DIAGRAM AND DESCRIPTION

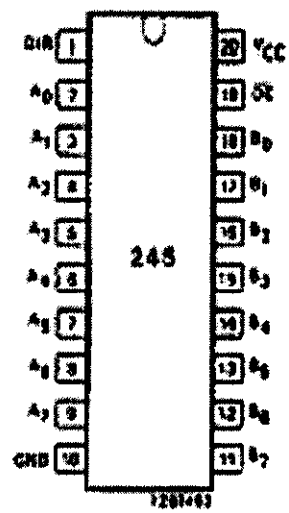


FIG 4.9 PIN DIAGRAM

Pin No.	Symbol	Name and Function
1	DIR	Direction control
2,3,4,5,6,7,8,9	A_0 to A_7	Data inputs/outputs
10	GND	Ground(0V)
18,17,16,15,14,13,12,11	B_0 to B_7	Data inputs/outputs
19	OE (Active low)	Output enable input (active low)
20	V_{cc}	Positive supply voltage

TABLE 4.4 PIN DESCRIPTION

4.9.3 FEATURES

Octal bidirectional bus interface.

1. Non-inverting 3-state outputs.
2. Output capability: bus driver.
3. ICC category: MSI.

4.10 INTERFACING BUFFER 74HC244

4.10.1 GENERAL DESCRIPTION

The 74HCT244 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). The 74HC244 has octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs 1OE and 2OE. A HIGH on nOE (active low) causes the outputs to assume a high-impedance OFF-state. The 74HC244 is identical to the 74HC240 but has non-inverting outputs. The interfacing buffer 74HC244 is used to protect the hardware components from overloading currents and to interface 4 bits to the data register of the printer port.

4.10.2 FEATURES

1. Octal bus interface.
2. Non-inverting 3-state outputs.
3. Complies with JEDEC standard no. 7A.
4. ESD protection.
5. HBM EIA/JESD22-A114-C exceeds 2000 V.
6. MM EIA/JESD22-A115-A exceeds 200 V.
7. Multiple package options.
8. Specified from -40 °C to +85 °C and from -40 °C to +125 °C.

4.10.3 PIN DIAGRAM

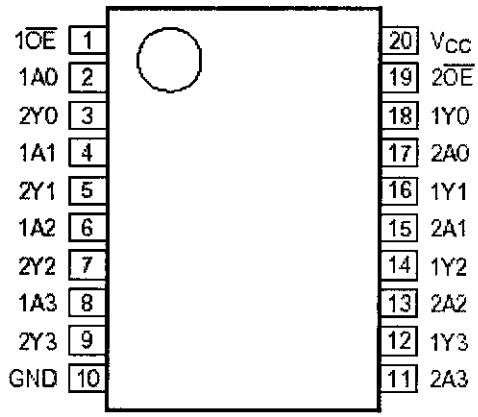


FIG 4.10 PIN DIAGRAM

4.10.4 FUNCTIONAL TABLE

Control	Input	Output
nOE	nAn	nYn
L	L	L
	H	H
H	X	Z

TABLE 4.5 FUNCTIONAL TABLE

Where, H = HIGH voltage level;

L = LOW voltage level;

X = don't care;

Z = high-impedance OFF-state.

4.10.5 PIN DESCRIPTION

Symbol	Pin	Description
1OE	1	output enable input (active LOW)
1A0	2	1 data input 0
2Y0	3	2 bus output 0
1A1	4	1 data input 1
2Y1	5	2 bus output 1
1A2	6	1 data input 2
2Y2	7	2 bus output 2
1A3	8	1 data input 3
2Y3	9	2 bus output 3
GND	10	ground (0 V)
2A3	11	2 data input 3
1Y3	12	1 bus output 3
2A2	13	2 data input 2
1Y2	14	1 bus output 2

TABLE 4.6 PIN DESCRIPTION

4.10.6 OUTPUT OF 74HC244

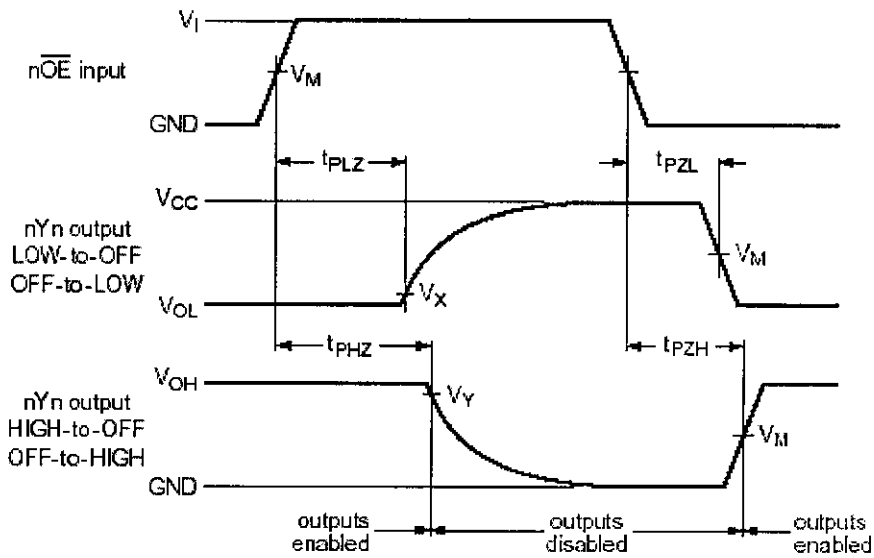


FIG 4.11 OUTPUT OF INTERFACING BUFFER

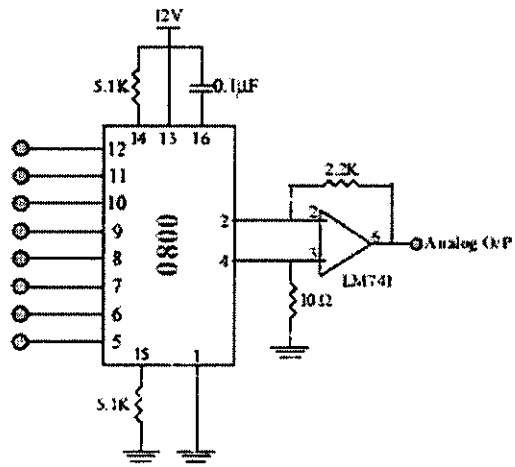
CHAPTER 5

CHAPTER 5

DIGITAL TO ANALOG CONVERSION

5.1 DIGITAL TO ANALOG CONVERTER

The schematic representation of the digital to analog converter is shown in figure. The DAC circuit will convert the digital signals coming out of microcontroller into analog signals in which the actuator devices could be operated.



Digital to Analog Converter

FIG 5.1 DAC

DAC

In electronics, a digital-to-analog converter (DAC or D-to-A) is a device for converting a digital (usually binary) code to an analog signal (current, voltage or electric charge). Digital-to-analog converters are interfaces between the abstract digital world and analog real life. An analog-to-digital converter (ADC) performs

DAC usually deals with pulse-code modulation (PCM)-encoded signals. The job of converting various compressed forms of signals into PCM is left to codec.

5.2 BASIC OPERATION

The DAC fundamentally converts finite-precision numbers (usually fixed-point binary numbers) into a physical quantity, usually an electrical voltage. Normally the output voltage is a linear function of the input number. Usually these numbers are updated at uniform sampling intervals and can be thought of as numbers obtained from a sampling process. These numbers are written to the DAC, sometimes along with a clock signal that causes each number to be latched in sequence, at which time the DAC output voltage changes rapidly from the previous value to the value represented by the currently latched number. The effect of this is that the output voltage is *held* in time at the current value until the next input number is latched resulting in a piecewise constant output. This is equivalently a zero-order hold operation and has an effect on the frequency response of the reconstructed signal.

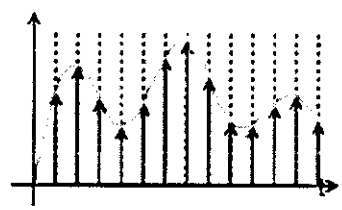


FIG 5.2 FREQUENCY RESPONSE

The fact that practical DAC's do not output a sequence of dirac impulses (that, if ideally low-pass filtered, result in the original signal before sampling) but instead output a sequence of piecewise constant values or rectangular pulses, means that there is an inherent effect of the zero-order hold on the effective

frequency response of the DAC resulting in a mild roll-off of gain at the higher frequencies (a 3.9224 dB loss at the Nyquist frequency).

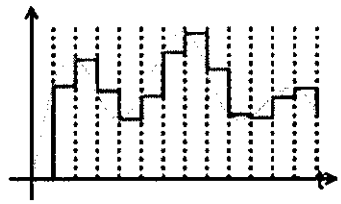


FIG 5.3 FREQUENCY RESPONSE

5.3 DAC0800

The DAC0800 series are monolithic 8 bit high speed current output digital to analog factoring typical setting times of 100ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high complementary current output to allow differential output voltages of 20 Vp-p with simple resistor loads. The reference to full scale current matching of better than l LAB eliminates the need for full scale trims in most application while the nonlinearities of better than 0.1 over temperature minimize system error accumulations.. The performance and characteristics of the device are essentially unchanged over the full 4.5v to 18v power supply range power dissipation is only 33mvw with +5v supplies and is independent of the logic input states. The output of the DAC is current signal. So it is given to current voltage converter which is constructed by the LM 741 operational amplifier. Finally the analog voltage is given to Triac or SCR control circuit.

CHAPTER 6

CHAPTER 6

INTERFACING DETAILS

6.1 LPT INTERFACE

To interface any external device to a computer has many ways. Few of them are ISA interface, PCI interface, LPT interface, USB interface and serial com port interface. Out of the above five methods first three methods are parallel methods and last two are serial methods. Normally the serial methods are comparatively slower than the parallel methods. In parallel methods, PCI is comparatively faster than the other methods. However, we decided to go with LPT interface. The main reason behind our selection is safety use of the computer. For our project, we will work with the newly designed circuits for the projects. It will create critical problems inside the system when we use ISA and PCI cards. It will cause major problems for hard disk, motherboard and processor. In LPT interface the risk factor is very low and to interface any hardware there is no need to open the CPU.

LPT (Line Printer Terminal) is a bidirectional interface port, it has three different I/O ports they are Status port, control port and data port. In these ports data port has eight-bit bi-directional bits that is data port can be used for inputs as well as outputs. Status port is a five bit port which is a unify-directional port which can be used only to get inputs. Control port is a four bit port which is also a uni-directional port but it is used to give only outputs. By using above three ports, we can do many wonders. In our board we decided to interface the following inputs and outputs

- Eight channel analog inputs with eight bit resolution
- Eight digital inputs with byte operation
- One analog output with eight bit resolution
- Eight digital outputs with byte operation

Normally in the LPT port the address of all three ports are common for all PCs, but for some exceptional cases, it may differ. In most of the PCs one LPT port is available which is named as LPT1 and in some cases there will be two the other one is named as LPT2. The addresses of the ports are as follows.

LPT1

Data port : 0x378

Status port : 0x379

Control port : 0x37a

LPT2

Data port : 0x278

Status port : 0x279

Control port : 0x27

6.2 PORT DESCRIPTION

As previously stated we decided to go with eight channel ADC interface, eight bit digital input, one channel DAC and eight bit digital output.

The complete circuit is designed with the help of control port and the data port itself. We have not used status port in our design. But we have terminated the status port in to a connecter for the purpose of future use. The selection of all the

input and outputs are based on a PAL chip which is programmed with the help of VHDL. In this selection logic we used three control port pins and two external input pins. According to the control port signal ADC or DAC or Digital input or digital output pins are selected, all these pins are connected to the corresponding ICs selection pins. Except the ADC all other will have only one selection pin. ADC will have three selection pins named as start of conversion, output enable and ALE. An ADC0809 chip for analog to digital conversion part is used. It has a resolution of 8bit and the conversion time of 100microseconds. The ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter,8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals. The device eliminates the need for external zero and full-scale adjustments. For the start of conversion and the output read (output enable) are selected from the PAL decoding logic which we have discussed earlier. For the channel selection we take data bus into a latch (74LS273) and we convert here as databus and address bus. Then the address bus is given to selection of channels in the ADC section. Then the converted digital signal is fed the PC through the data bus. Then for the digital to analog converter the chip selection is done from the PAL decoding logic. The selection is done through a latch 74LS273 and the databus from the computer is given to the DAC 0800 through the latch. Then the output is amplified with the help of general purpose amplifier LM741. The final output will be 0 to 5 volts DC.

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in Figure 1. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations. The digital input is done through a buffer 74LS244 which is selected with the help of the PAL logic and the input from the buffer is sent to the PC through databus. These buffers/line drivers are designed to improve both the performance and PC board density of 3-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133W, so that a pull up resistor along with the input terminals and the buffer.

Digital output is also selected with the help of PAL decoding logic and the latch 74ls273 and the final output can be taken here or the relay driver chip ULN2003 to connect directly to the relay and other devices.

These high speed octal D-type latches (74LS273) utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the 3-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system

CHAPTER 7

CHAPTER 7

CONTROL CIRCUIT

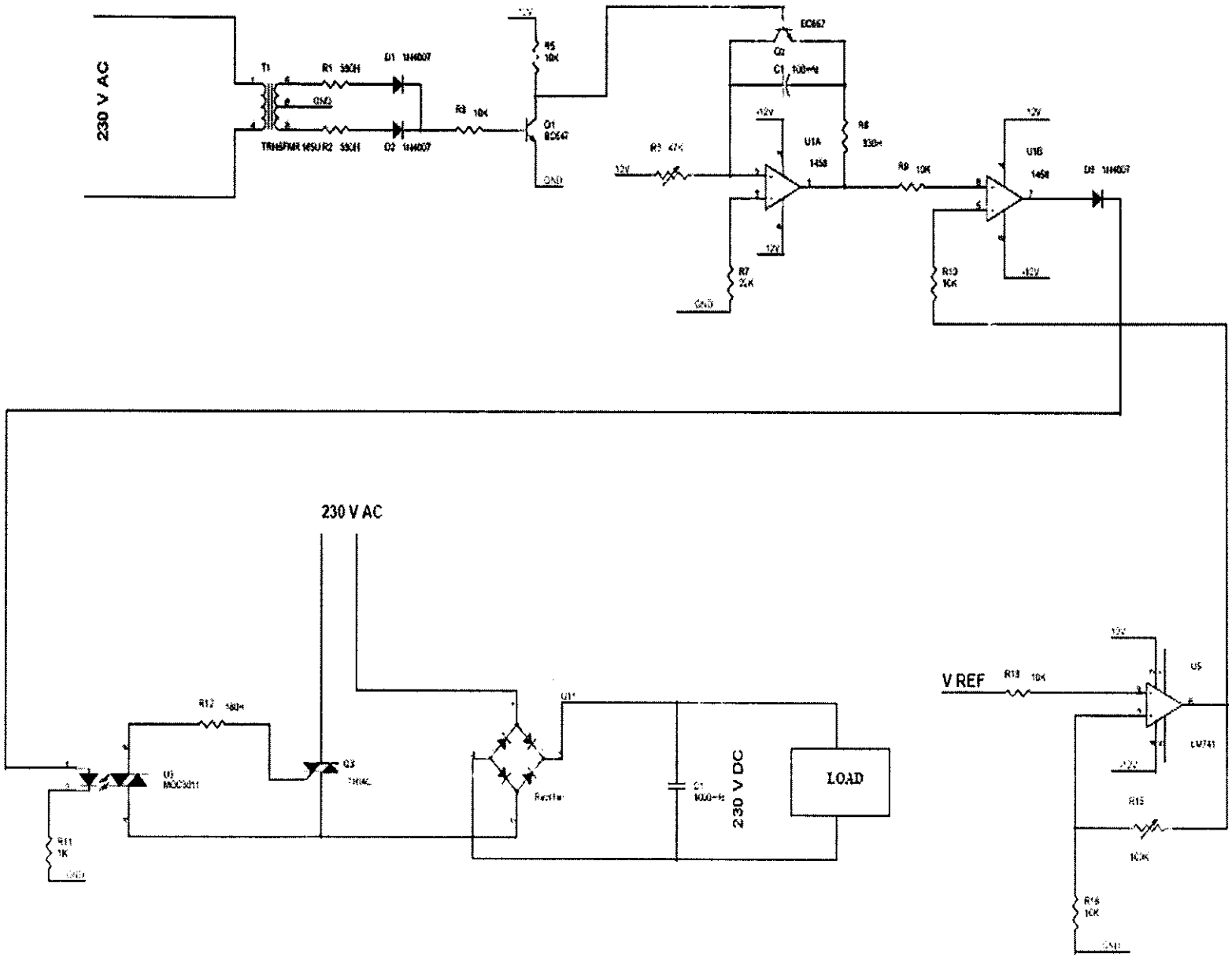
7.1 TEMPERATURE CONTROL

In our process, temperature is to be controlled through controlling the flow of current through the heater. In this case, TRIAC can be used as on/off switch, on controlling the current.

7.1.1 TRIAC

A TRIAC, or TRIode for Alternating Current is an electronic component approximately equivalent to two silicon-controlled rectifiers (SCRs/thyristors) joined in inverse parallel (paralleled but with the polarity reversed) and with their gates connected together. This results in a bidirectional electronic switch which can conduct current in either direction when it is triggered (turned on). It can be triggered by either a positive or a negative voltage being applied to its *gate* electrode. Once triggered, the device continues to conduct until the current through it drops below a certain threshold value, such as at the end of a half-cycle of alternating current (AC) mains power. This makes the TRIAC a very convenient switch for AC circuits, allowing the control of very large power flows with milliampere-scale control currents. In addition, applying a trigger pulse at a controllable point in an AC cycle allows one to control the percentage of current that flows through the TRIAC to the load (so-called *phase control*).

TRIAC CONTROL CIRCUIT



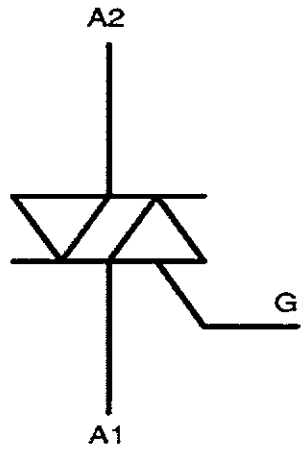


FIG 7.1 TRIAC

7.1.2 APPLICATION

Low power TRIACs are used in many applications such as light dimmers, speed controls for electric fans and other electric motors, and in the modern computerized control circuits of many household small and major appliances. However, when used with inductive loads such as electric fans, care must be taken to assure that the TRIAC will turn off correctly at the end of each half-cycle of the ac power.

7.2 CIRCUIT WORKING DESCRIPTION

This circuit is designed to control the 230V AC load such as heater, motor etc. The 230V AC voltage is step down with help of step down transformer. The step down voltage is rectified by the full wave rectifier. After the rectification the pulsating rectified voltage is given to base of the transistor Q1. Whenever peak pulse is come the transistor Q1 is conducting and ground voltage is given to Q2 transistor base. Rest of the time 12V is given to base of the Q2 transistor which is connected across the feedback capacitor of U1A saw tooth generator. The saw tooth generator is constructed by LM1458 operational amplifier.

The LM1458 is the general purpose duel operational amplifier with sharing common supply. U1A delivered the saw tooth wave output which is given to non inverting input terminal of comparator. The comparator is constructed by the U1B.

The 12V square wave signal is given to inverting input terminal. The 12V square wave signal is generated by the comparator U5 which is constructed by LM 741 operational amplifier.

The U1B comparator compares the input saw tooth wave and square wave signal and outputs the +12V to -12V square pulse. The -12V square pulse is rectified by D3 diode.

The positive 12 square pulse is given to isolation circuit. The isolation is constructed by the MOC3011 Opto coupler.

The isolation is used to separate the 230V AC voltage and DC voltages. The opto coupler consists of photo LED and photo transistor. Whenever the 12V signal is given to photo LED the light rays' falls on the photo transistor. Now the photo transistor is conducting and high pulse is given to Triac gate. So the Triac is conducting and 230V AC voltage is given to load. Depending on the pulse given to Triac gate the conduction angel is varied. Then the variable AC voltage is rectified by the full wave rectifier unit. So that DC voltage flowing through load varied in order to control the load to desired level.

CHAPTER 8

CHAPTER 8

LABVIEW

8.1 INTRODUCTION TO LABVIEW

LabVIEW (Laboratory Virtual Instrument Engineering Workbench) is a graphical programming language that uses icons instead of lines of text to create applications. In contrast to text-based programming languages, where instructions determine the order of program execution, LabVIEW uses dataflow programming, where the flow of data through the nodes on the block diagram determines the execution order of the VIs and functions. VIs, or virtual instruments, is LabVIEW programs that imitate physical instruments.

In LabVIEW, you build a user interface by using a set of tools and objects. The user interface is known as the front panel. You then add code using graphical representations of functions to control the front panel objects. This graphical source code is also known as G code or block diagram code. The block diagram contains this code. In some ways, the block diagram resembles a flowchart.

LabVIEW is integrated fully for communication with hardware such as GPIB, VXI, PXI, RS-232, RS-485, and data acquisition control, vision, and motion control devices. LabVIEW also has built-in features for connecting your application to the Internet using the LabVIEW web server and software standards such as TCP/IP networking and ActiveX.

Using LabVIEW, you can create 32-bit compiled applications that give you the fast execution speeds needed for custom data acquisition, test, measurement, and control solutions. You also can create stand-alone executables and shared libraries, like DLLs, because LabVIEW is a true 32-bit compiler.

LabVIEW contains comprehensive libraries for data collection, analysis, presentation, and storage. LabVIEW also includes traditional program development tools. You can set breakpoints, animate program execution, and single-step through the program to make debugging and development easier.

LabVIEW also provides numerous mechanisms for connecting to external code or software through DLLs, shared libraries, ActiveX, and more. In addition, numerous add-on tools are available for a variety of application needs.

8.2VIRTUALINSTRUMENTS

LabVIEW programs are called virtual instruments, or VIs, because their appearance and operation imitate physical instruments, such as oscilloscopes and multimeters.

A VI contains the following three components:

- Front panel Serves as the user interface.
- Block diagram contains the graphical source code that defines the functionality of the VI.
- Icon and connector pane identifies the interface to the VI so that you can use the VI in another VI.

8.3 FRONT PANEL

The front panel is the user interface of the VI. The following figure shows an example of a front panel.

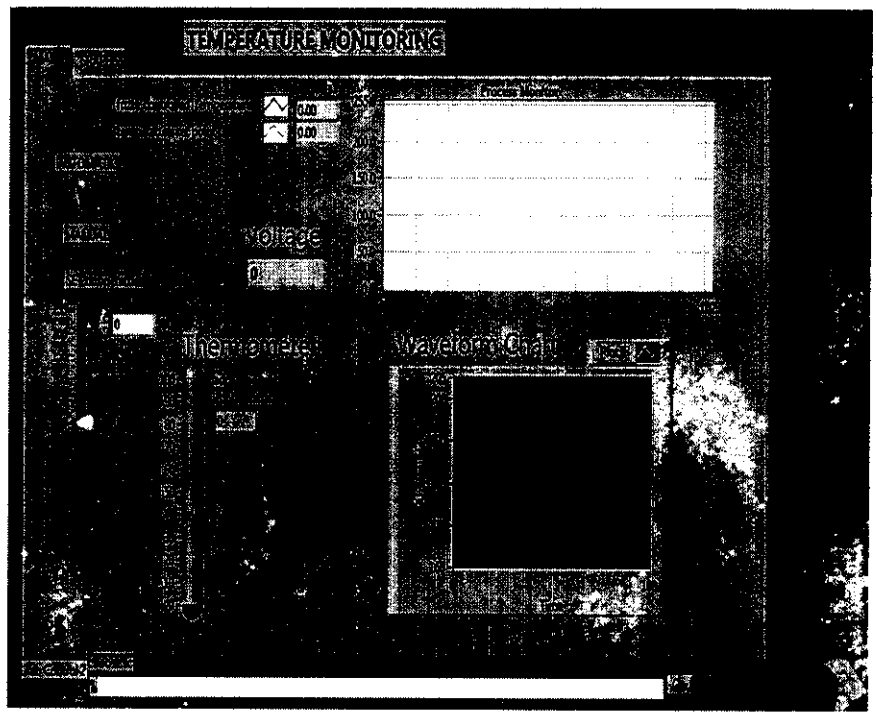


FIG 8.1 FRONT PANEL

You build the front panel using controls and indicators, which are the interactive input and output terminals of the VI, respectively. Controls are knobs, push buttons, dials, and other input mechanisms. Indicators are graphs, LEDs, and other output displays. Controls simulate instrument input mechanisms and supply data to the block diagram of the VI. Indicators simulate instrument output mechanisms and display data the block diagram acquires or generates.

8.4 BLOCK DIAGRAM

After you build the front panel, you add code using graphical representations of functions to control the front panel objects. The block diagram contains this graphical source code, also known as G code or block diagram code. Front panel objects appear as terminals on the block diagram. The following VI contains several primary block diagram objects—terminals, functions, and wires.

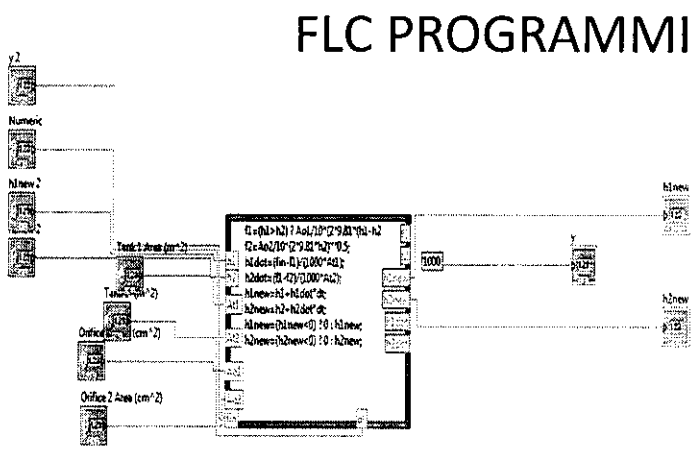
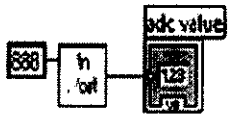


FIG 8.2 BLOCK DIAGRAM

8.5 TERMINALS

The terminals represent the data type of the control or indicator. You can configure front panel controls or indicators to appear as icon or data type terminals on the block diagram. By default, front panel objects appear as icon terminals. For example, a knob icon terminal, shown as follows, represents a knob on the front panel.



The DBL at the bottom of the terminal represents a data type of double-precision, floating-point numeric. A DBL terminal, shown as follows, represents a double-precision, floating-point numeric control.

Terminals are entry and exit ports that exchange information between the front panel and block diagram. Data you enter into the front panel controls (**a** and **b** in the previous figure) enter the block diagram through the control terminals. The data then enter the Add and Subtract functions. When the Add and Subtract functions complete their calculations, they produce new data values. The data values flow to the indicator terminals, where they update the front panel indicators (**a+b** and **a-b** in the previous figure).

8.5.1 NODES

Nodes are objects on the block diagram that have inputs and/or outputs and perform operations when a VI runs. They are analogous to statements, operators, functions, and subroutines in text-based programming languages. The Add and Subtract functions in the previous figure are examples of nodes.

8.5.2 WIRES

You transfer data among block diagram objects through wires. In the previous figure, wires connect the control and indicator terminals to the Add and Subtract functions. Each wire has a single data source, but you can wire it to many VIs and functions that read the data. Wires are different colors, styles, and thicknesses, depending on their data types. A broken wire appears as a dashed black line with a red X in the middle. Broken wires occur for a variety of reasons, such as when you try to wire two objects with incompatible data types.

8.5.3 STRUCTURES

Structures are graphical representations of the loops and case statements of text-based programming languages. Use structures on the block diagram to repeat blocks of code and to execute code conditionally or in a specific order.

8.5.4 ICON AND CONNECTOR PANE

After you build a VI front panel and block diagram, build the icon and the connector pane so you can use the VI as a subVI. The icon and connector pane correspond to the function prototype in text-based programming languages. Every VI displays an icon, such as the one shown as follows, in the upper right corner of the front panel and block diagram windows.

An icon is a graphical representation of a VI. It can contain text, images, or a combination of both. If you use a VI as a subVI, the icon identifies the subVI on the block diagram of the VI. You can double-click the icon to customize or edit it.

You also need to build a connector pane, shown as follows, to use the VI as a subVI.

The connector pane is a set of terminals that correspond to the controls and indicators of that VI, similar to the parameter list of a function call in text-based programming languages. The connector pane defines the inputs and outputs you can wire to the VI so you can use it as a subVI. A connector pane receives data at its input terminals and passes the data to the block diagram code through the front panel controls and receives the results at its output terminals from the front panel indicators.

8.6 LABVIEW ENVIRONMENT

It is possible to use the LabVIEW palettes, tools, and menus to build the front panels and block diagrams of VIs. LabVIEW includes three palettes: the **Controls** palette, the **Functions** palette, and the **Tools** palette. LabVIEW also includes the **Getting Started** window, the **Context Help** window, the **Project Explorer** window, and the **Navigation** window. You can customize the **Controls** and **Functions** palettes, and it is possible to set several work environment options.

8.7 IMPLEMENTATION OF FUZZY LOGIC USING LABVIEW

The idea of fuzzy logic is to model a subjective, indeterminate concept such *as temperature too high, temperature change too low,* and so on, with intermediate values. These values are expressions of the colloquial language, what means that anybody can understand and handle it. But a computer can not deal these fuzzy arguments. It needs sharp values which define clear facts to decide upon them. Fuzzy logic extends here the classic set theory with the help of membership functions as a part of the fuzzy set theory. The expression *temperature too high* is a different subjective statement, which can not be limited with fixed temperature points. A person would decide in regard to this expression, that the temperature belongs more or less to the variable. The degree of the membership in the fuzzy set theory is defined as a continuous function between no membership (0) and full membership (1), in comparison to the binary values (0, l) in the classic set theory.Fuzzification here means to classify a value to the degree of its membership function in regard to express humanlike linguistic variables. The next step in fuzzy logic is to make decisions based upon the linguistic variables (inference). They are made in IF-THEN-rules, were the IF-part describes a situation and the THEN-part contains the wished action. Methods of Defuzzification try to find a compromise from all fuzzy sets to suggest at least aprecise value. Several methods of defuzzification exist to produce an exact output value. The typical value for every single result of the rules is determined in the centre of maximum method(COM). Thus the linguistic variables in the composition are not fuzzy sets but fixed values (typical values). The outputs of the single rules are added up with their weight from the aggregation. The received exact value is consequently the mean of the weighted values. Another well known method is the Center of Gravity (COG).

8.8 CONTROLLER DESIGN

The output from the temperature sensor is in the form of analog voltage ranges 0-0.15 V, which is digitalized by DAQ. The input variables are fuzzified and after proper defuzzification using rule base and aggregation methods, the output is evaluated which is used in control action. To achieve the accurate output from the fuzzy inference system, following steps are designed:

- Step One: Define Inputs and Outputs for the Fuzzy Logic Controller
- Step Two: Define frame for fuzzy variables
- Step Three: Assign membership values to fuzzy variable
- Step Four: Create a rule base
- Step Five: Fuzzify inputs to the fuzzy logic controller
- Step Six: Determine which rule fires
- Step Seven: Infer the output recommended by each rule
- Step Eight: Aggregate the fuzzy outputs recommended by each Rule
- Step Nine: Defuzzify the aggregated fuzzy set to form crisp output from the fuzzy logic controller.

The input variables of the fuzzy logic controller are:

Error = Set point – Measured temperature

Change in error = Current error – Previous error

First fuzzy input represents the error between measured temperature and set point. Figure shows the membership function and table 1 gives the linguistic variables for error. The crisp input for second input membership function is change in error. The triangular seven-level membership function and table gives the linguistic variables for change in error. Input variables are scaled to the intervals [-0.2, 1] and [-1, 0] respectively. Rule evaluation part has 49 fuzzy rules. Fuzzy logic controller's output is voltage level which is applied to voltage controlled current source circuit.

FUZZY TABLE:

Temperature (Celsius)	Voltage (Volts)
0	0
10	0.5
20	1
30	1.5
40	2
50	2.5
60	3
70	3.5
80	4
90	4.5
100	5

TABLE 8.1 FUZZY TABLE

8.9 FLOW OF PROCESS

The flow of process begins in the following format.

1. The data from the sensor (Thermistor) is first captured.
2. The signal is conditioned for unwanted noise.
3. It is sent for amplification.
4. The Fuzzy algorithms present in the LabVIEW block receives this signal.
5. The formula

$$Error = Set\ point - Measured\ temperature$$

6. The error is compared with a table of values comprising of variation in voltage values. (refer appendix)
7. The voltage is sent to the Triac circuit to turn on or off the heater.

8.10 MEMBERSHIP FUNCTION

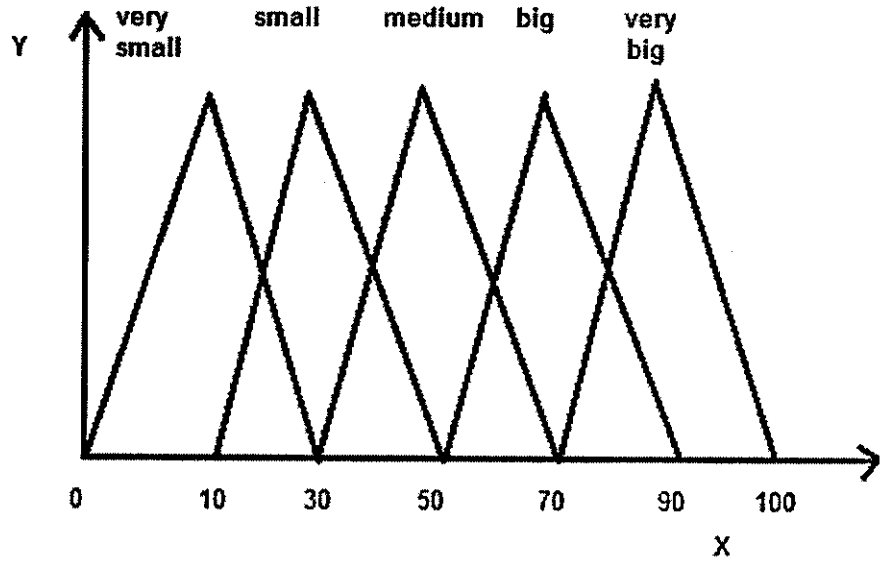


FIG 8.3 MEMBERSHIP FUNCTION

8.11 RULE BASE

M.V/S.P	VERY SMALL	SMALL	MEDIUM	BIG	VERY BIG
Very small	Ze	Very small	Small	Medium	Big
Small	Ze	Ze	Very small	Small	Medium
Medium	Ze	Ze	Ze	Very small	Small
Big	Ze	Ze	Ze	Ze	Small
Very big	Ze	Ze	Ze	Ze	Ze

TABLE 8.2 RULEBASE

CONCLUSION

CHAPTER 9

CONCLUSION

The Fuzzy Logic based temperature control system using LabVIEW was implemented and tested in real time in lab setup. The results were successfully obtained with high degree of accuracy and consistency. The project can be scaled up to meet the industrial requirements to suit equipments such as boilers, furnaces etc. Further improvements on the fuzzy algorithm can also be carried out.

REFERENCES

REFERENCES

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Jonconway's " A Software Engineering To Labview"

David Jave Ritter's " Labview Essential Techniques"

WEBSITES

www.datasheetcatalog.com

www.howstuffworks.com

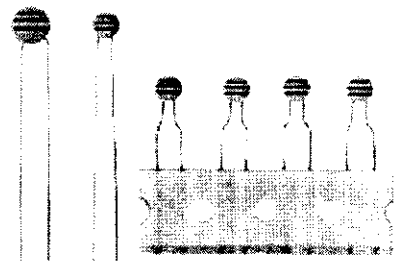
www.microchip.com

www.nationalinstruments.com

APPENDICES

Disc Type NTC Thermistors

Type: **ERTD**



Disc type negative temperaturecoefficient thermistors. Resistance values from 8 Ω to 150 kΩ and B Values are from 3000 K to5000 K.

■ Features

- Wide selection of temperature coefficients
- Excellent electrical and thermal stability

■ Recommended Applications

- Temperature detection
- Temperature compensation for measuring instruments
- Temperature compensation for deflection coil in TV

■ Explanation of Part Numbers

1	2	3	4	5	6	7	8	9	10	11	12
E	R	T	D								

Product Code	
ERT	NTC Thermistors

Disc Dim	
2	ϕ5.0 mm
3	ϕ7.5 mm

Shape	
D	Disc Type

Lead Style	
F	Straight Lead
Z	"Z" Crimped Lead

Center B Value (K)	
E	2501–3000
F	3001–3500
G	3501–4000
H	4001–4500
I	4501–5000

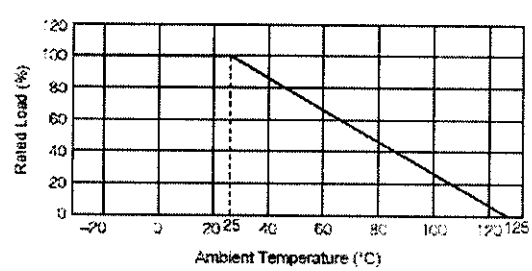
Resistance Tolerance	
J	± 5 %
K	±10 %
L	±15 %

Resistance R_{25} (Ω)
The first two digits are significant figures of resistance and the third one denotes number of zeros following them. Decimal point is expressed by R as 1.4 =1R4.

Option	
S	Standard
T	Taping Type

■ Derating Curve for the NTC Thermistor

For the NTC Thermistor operated in ambient temperature above 25 °C, power rating should be derated in accordance with the right figure.



■ Ratings and Characteristics

Part No.	Zero-Power Resistance at 25 °C(Ω)	B Value*a (K)	Maximum Permissible Power(W)	Heat Dissipation Constant (mW/°C)	Thermal Time Constant (s)	Resistance Ratio R_{25}/R_{50}	Table A/B Curve No.
ERTD2FE□*200S	20	3000				2.18	—
ERTD2FF□*400S	40	3200				2.30	—
ERTD2FG□*750S	75	3700				2.62	1
ERTD2FF□*101S	100	3500				2.48	—
ERTD2FG□*101S	100	3700				2.62	2
ERTD2FG□*171S	170	3700				2.62	3
ERTD2FF□*251S	250	3500				2.48	—
ERTD2FG□*251S	250	3900				2.76	4
ERTD2FG□*301S	300	3900				2.76	—
ERTD2FF□*351S	350	3500				2.48	5
ERTD2FG□*601S	600	4000				2.83	6
ERTD2FG□*801S	800	3900	0.4	4.5	20	2.76	7
ERTD2FG□*102S	1000	3700				2.61	—
ERTD2FG□*142S	1400	3900				2.76	—
ERTD2FG□*202S	2000	4000				2.83	8
ERTD2FG□*332S	3300	4000				2.83	9
ERTD2FH□*462S	4600	4100				2.90	—
ERTD2FH□*802S	8000	4100				2.90	10
ERTD2FH□*103S	10000	4100				2.90	—
ERTD2FH□*153S	15000	4200				2.98	11
ERTD2FH□*333S	33000	4500				3.22	12
ERTD2FH□*503S	50000	4500				3.22	13
ERTD2FI□*154S	150000	4800				3.48	14
ERTD3FE□*8R0S	8	3000				2.18	15
ERTD3FF□*130S	13	3200				2.30	16
ERTD3FF□*160S	16	3200				2.30	—
ERTD3FF□*200S	20	3200				2.30	—
ERTD3FF□*300S	30	3200				2.30	—
ERTD3FF□*400S	40	3200				2.30	—
ERTD3FG□*750S	75	3700	0.6	7.0	27	2.62	—
ERTD3FG□*800S	80	3700				2.62	—
ERTD3FG□*131S	130	3700				2.62	—
ERTD3FG□*501S	500	4000				2.83	—
ERTD3FH□*402S	4000	4100				2.90	—
ERTD3FH□*203S	20000	4500				3.22	—
ERTD3FI□*803S	80000	5000				3.70	17

*Resistance Tolerance Code

J	K	L
±5 %	±10 %	±15 %

*a Tolerance of "B value": ±10 %

$$B = \frac{\ell n\,(R_{25}/R_{50})}{\frac{1}{T_{25}} - \frac{1}{T_{50}}}$$

R_{25}=Resistance at 25.0 °C

R_{50}=Resistance at 50.0 °C

T_{25}=Absolute temperature at 25.0 °C (K)

T_{50}=Absolute temperature at 50.0 °C (K)

● Operating Temperature Range: −30 to +125 °C

National Semiconductor

November 1995

ADC0808/ADC0809 8-Bit μP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

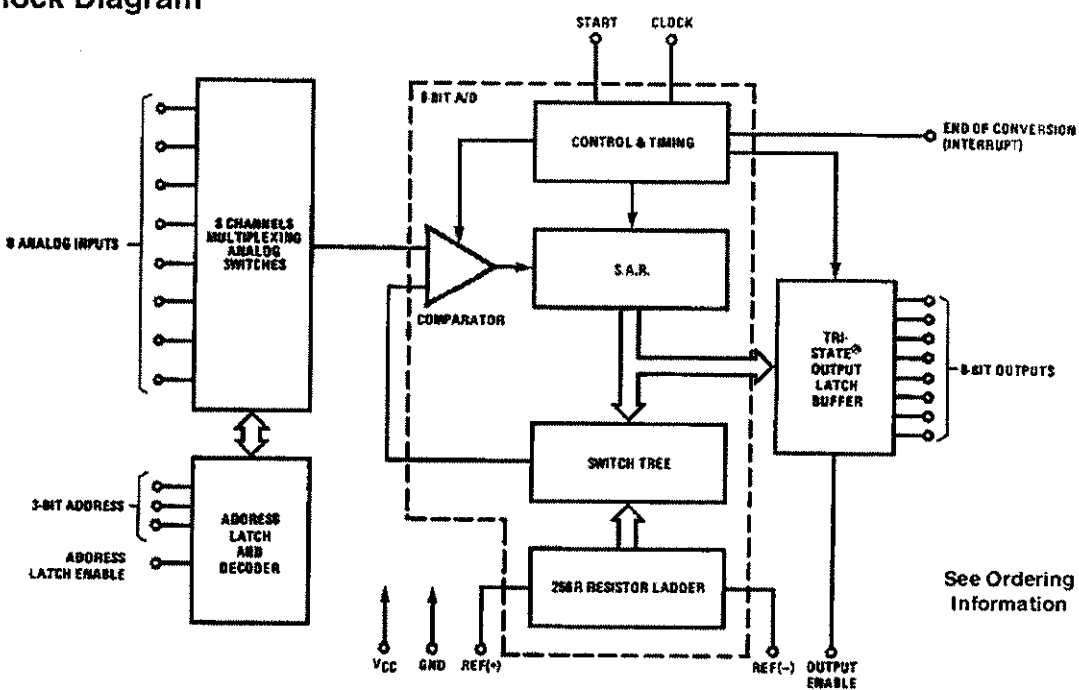
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 μs

Block Diagram



See Ordering Information

National Semiconductor

June 1999

DAC0800/DAC0802
8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in *Figure 1*. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{LC}, grounded. Changing the V_{LC} potential will allow direct interface to other logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33 mW with ±5V supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, and DAC-08H, respectively.

Features

- Fast settling output current: 100 ns
- Full scale error: ±1 LSB
- Nonlinearity over temperature: ±0.1%
- Full scale current drift: ±10 ppm/°C
- High output compliance: −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range: ±4.5V to ±18V
- Low power consumption: 33 mW at ±5V
- Low cost

Typical Applications

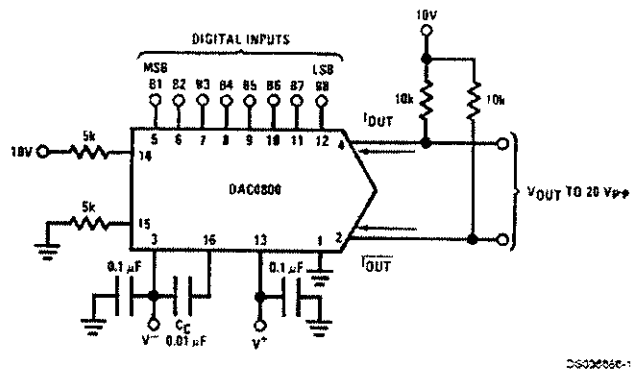


FIGURE 1. ±20 V_{P-P} Output Digital-to-Analog Converter (Note 5)

Ordering Information

Non-Linearity	Temperature Range	Order Numbers				
		J Package (J16A) (Note 1)		N Package (N16E) (Note 1)		SO Package (M16A)
±0.1% FS	0°C ≤ T_A ≤ +70°C	DAC0802LCJ	DAC-08HQ	DAC0802LCN	DAC-08HP	DAC0802LCM
±0.19% FS	−55°C ≤ T_A ≤ +125°C	DAC0800LJ	DAC-08Q			
±0.19% FS	0°C ≤ T_A ≤ +70°C	DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP	DAC0800LCM

Note 1: Devices may be ordered by using either order number.

has power. 1284 Type C connectors are recommended for new designs, so we can look forward on seeing these new connectors in the near future.

Pin No (D-Type 25)	Pin No (Centronics)	SPP Signal	Direction In/out	Register	Hardware Inverted
1	1	nStrobe	In/Out	Control	Yes
2	2	Data 0	Out	Data	
3	3	Data 1	Out	Data	
4	4	Data 2	Out	Data	
5	5	Data 3	Out	Data	
6	6	Data 4	Out	Data	
7	7	Data 5	Out	Data	
8	8	Data 6	Out	Data	
9	9	Data 7	Out	Data	
10	10	nAck	In	Status	
11	11	Busy	In	Status	Yes
12	12	Paper-Out PaperEnd	In	Status	
13	13	Select	In	Status	
14	14	nAuto-Linefeed	In/Out	Control	Yes
15	32	nError / nFault	In	Status	
16	31	nInitialize	In/Out	Control	
17	36	nSelect-Printer nSelect-In	In/Out	Control	Yes
18 - 25	19-30	Ground	Gnd		

Table 1. Pin Assignments of the D-Type 25 pin Parallel Port Connector.