SMART HELMET

A PROJECT REPORT

Submitted by

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in partial fulfillment for the award of the degree

of

BACHELOR OF ENGINEERING

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

KUMARAGURU COLLEGE OF TECHNOLOGY

COIMBATORE-641049

(An Autonomous Institution Affiliated to Anna University, Chennai)

APRIL 2015

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BONAFIDE CERTIFICATE

Certified that this project report titled **"SMART HELMET"** is the bonafied work of "**S.P.PRASAANTH"** who carried out the project work under my supervision.

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INTERNAL EXAMINER **EXTERNAL EXAMINER**

ACKNOWLEDGEMENT

First I would like to express my praise and gratitude to the Lord, who has showered his grace and blessing enabling me to complete this project in an excellent manner. He has made all things in beautiful in his time.

I express my sincere thanks to my beloved Joint Correspondent, **Shri. Shankar Vanavarayar** for his kind support and for providing necessary facilities to carry out the project work.

I would like to express my sincere thanks to my beloved Principal **Dr. R.S.Kumar M.E, Ph.D.,** who encouraged me with his valuable thoughts.

I would express my sincere gratitude to **Soliton Technologies** who allowed me to complete the project at their esteemed company with all possible support.

I would like to express my sincere thanks and deep sense of gratitude to my HOD, **Dr.Rajeswari Mariappan M.E, Ph.D** for her valuable suggestions and encouragement which paved way for the successful completion of the project.

I am greatly privileged to express my deep sense of gratitude to the Project Guide **Dr.A.Vasuki M.E, Ph.D**, Professor, for her expert counselling in each and every steps of the project work.

Further, I wish to thank and express my everlasting gratitude to the Project Coordinator **Ms. A.Kalaiselvi M.E, (Ph.D)**, Assistant Professor for her continuous support throughout the project course and I wish to convey my deep sense of gratitude to all teaching and non-teaching staff members of ECE Department for their help and cooperation.

Finally, I thank my parents and my family members for giving me the moral support in all of my activities and my dear friends who helped me to endure the difficult times with their unfailing support and warm wishes.

ABSTRACT

India is one of the countries where there is high incidence of road accidents. The high casualty rate in these accidents can be attributed to the delay in medical assistance reaching the victims. One of the reasons for the delay is that the information about the accident might not reach the hospital/ ambulance faster. Hence, a system to ensure that medical help arrives in time to the site of the accident is required. The objective of this project is to create a SMART HELMET which intimates the medical helpline about the occurrence of an accident, thereby reducing the delay in rescue operation.

The normal helmet which we use just provides a protection to the head but the smart helmet adds a feature of informing the medical helpline if an accident occurs. The project incorporates a Controller equipped with Accelerometer, GPS and GSM module placed inside the helmet. The accelerometer sends instantaneous data regarding the rider's acceleration to the controller. The controller calculates the net 'g' force from the acceleration data and checks whether the value crosses the safety limit. The safety limit is the predetermined threshold for accident occurrence. When the net ‘g’ force is equal to or above the threshold, there is a high chance for an accident to have occurred. The controller then obtains the location of the victim from the GPS module and then triggers the GSM module to send the distress signal along with the location details in terms of longitude and latitude to the helpline which thus facilitates a faster rescue.

This project will definitely reduce the fatalities in the road accidents that occur almost every day.

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LIST OF ABBREVIATIONS

AIIMS	-	**A**ll **I**ndia **I**nstitute of **M**edical **S**ciences
GPS	-	**G**lobal **P**ositioning **S**ystem
GSM	-	**G**lobal **S**ystem for **M**obiles
HUD	-	**H**eads **U**p **D**isplay
I2C	-	**I**nter **I**ntegrated **C**ircuits
ICSP	-	**I**n **C**ircuit **S**erial **P**rogramming
IDE	-	**I**ntegrated **D**evelopment **E**nvironment
PWM	-	**P**ulse **W**idth **M**odulation
Rx	-	Receiver
SPI	-	**S**erial **P**eripheral **I**nterface
Tx	-	Transmitter
UART	-	**U**niversal **A**synchronous **R**eceiver **T**ransmitter
WHO	-	**W**orld **H**ealth **O**rganization

CHAPTER 1

INTRODUCTION

The crucial time between the occurrence of an accident and the victim getting medical attention can often be the difference between life and death. Unfortunately not many people value that precious time. It will require a Good Samaritan to inform the helpline regarding the accident so that the rescue measures can be initiated. *"If the patients are not arriving at the hospital in time, then it becomes complicated. A simple thing like bringing a patient in time can result in a question of life and death"* said AIIMS doctor Dr.Amit Gupta.

The reasons for the accidents can be many such as no proper driving knowledge, rash driving, drunken driving etc. But in some cases the person injured in the accident may not be directly responsible for the accident, it may be fault of the other rider, but end of the day it's an accident. If accidents are one issue, delay in treatment/first aid is another reason for deaths. This scenario is something that usually is undervalued. This is where smart helmet comes in where it will automatically detect the accident and send a distress call and the accident location to the helpline.

In the proceedings to detect the occurrence of an accident, the project Smart Helmet incorporates an accelerometer to detect instantaneous acceleration of the rider i.e. the vehicle , a GSM module to transmit distress signal, a GPS receiver to locate the accident and a push button to detect whether the rider is wearing the helmet or not. The reason for such a design is that, unless mandatory, about 65 % of Indians don't wear helmet. Further according to a WHO report, wearing a helmet reduces chances of death by 40 per cent and that of severe injury by 70 per cent. Thus the **SMART HELMET** provides a pavement for better society, with less vulnerability on roads.

1.1 EXISTING PRODUCTS

The existing specially designed helmets are:

- Skully
- LifeBEAM

1.1.1 SKULLY

The Skully AR-1 (AR stands for Augmented Reality) is the first helmet from the team at Skully and features the first HUD system available for a motorcycle helmet. Its two main features are

- 180-degree, rear-facing camera
- A little screen placed in the bottom right portion of your field of view.

The screen allows you to see everything behind you, no matter which direction your helmet is facing, without any blind spots. Skully has also developed its own interface to bring turn-by-turn directions and a few other basic pieces of information to the screen, all with the purpose of reducing the mental load placed on the rider. Connectivity will come through pairing with your phone via Bluetooth, but that doesn't mean you'll be relying on Siri, necessarily. Further the helmet is also equipped with a GPS for navigation.

The entire helmet is custom fabricated accordingly so that it could accommodate all the electronics into it.

1.1.2 LifeBEAM

The LifeBEAM helmet is exclusively modelled for bicycle riders with health related features. It provides details regarding heart rate and blood pressure without any strap-on. It suites for all the weather conditions and is entirely wireless.

1.1.3 COMPARISON

The table 1.1 provides the comparison between the smart helmet and the existing products.

Table 1.1 Comparison of Existing Products and Smart Helmet

Smart Helmet	LifeBEAM	Skully
It is modelled for all two wheeler rider.	It is modelled for cyclists only.	It is modelled for professional motorcyclists
A helmet with simple electronics.	A helmet for measuring health parameters like blood pressure and heart rate.	A helmet with high end features.
It has an emergency distress call mechanism.	It does not have any such feature.	It does not have any such feature.
It has a GPS to trace location.	It does not have any type of location finder	Has GPS module to trace location
Mobile phones are not required for the operation.	A mobile phone is required to provide Bluetooth connectivity.	A mobile phone is required to provide Bluetooth or Siri connectivity
Targeted for common person	Targeted for health conscious cyclists	Mainly made for professional motorcyclists
Lower cost (1500 INR)	High cost ($ 1100 approx)	High cost ($ 1499 approx)

1.2 PROJECT BLOCK DIAGRAM

The project consists of an accelerometer which provides the instantaneous acceleration of the rider in terms of ‘g’. The controller obtains these values and calculates the ‘g’ force. If the ‘g’ force exceeds the threshold value then the controller triggers the GPS module and obtains the accident location from it. The controller then triggers the GSM module to send the distress signal along with the accident location. The detailed descriptions of the various modules are presented in the following chapters.

The block diagram of the project is shown in fig 1.1

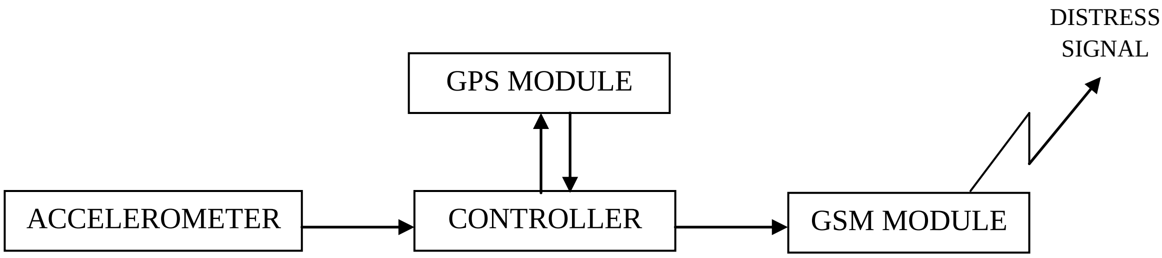


Fig 1.1 Block Diagram of the Project

Chapter 2 presents the hardware description of the project which provides a detailed description on the hardware components used. Chapter 3 deals with the software segment of the project which describes the software used to code the controller. The working of the project is presented in chapter 4. Chapter 5 describes algorithm of the project and chapter 6 concludes the work.

CHAPTER 2

HARDWARE DESCRIPTION

This chapter describes the hardware segment of the project. The project consists of the following modules:

- A controller
- Accelerometer
- GSM module
- GPS module

The detailed description of these modules will be dealt in the following sections.

2.1 CONTROLLER: ARDUINO NANO

2.1.1OVERVIEW

The Arduino Nano is a small, complete, and breadboard-friendly board based on the ATmega328 (Arduino Nano 3.x) or Atmega168 (Arduino Nano 2.x). It has only a DC power jack, and works with a Mini-B USB cable instead of a standard one. The Nano was designed and is being produced by Gravitech. The Arduino Nano ver 3 is shown in fig 2.1.

Fig 2.1 Arduino Nano

2.1.2 POWER:

The Arduino Nano can be powered by

- The Mini-B USB connection.
- 6-20V unregulated external power supply (pin 30).
- 5V regulated external power supply (pin 27).

The power source is automatically selected to the highest voltage source.

2.1.3 MEMORY

The ATmega168 has 16 KB of flash memory for storing code (of which 2 KB is used for the boot loader); the ATmega328 has 32 KB, (also with 2 KB used for the boot loader). The ATmega168 has 1 KB of SRAM and 512 bytes of EEPROM (which can be read and written with the EEPROM library); the ATmega328 has 2 KB of SRAM and 1 KB of EEPROM.

2.1.4 I/O

Each of the 14 digital pins on the Nano can be used as an input or output, using

- pinMode().
- digitalWrite().
- digitalRead() functions.

They operate at 5 volts. Each pin can provide or receive a maximum of 40 mA and has an internal pull-up resistor (disconnected by default) of 20-50 kOhms. The Arduino Nano pinout is shown in fig 2.2.

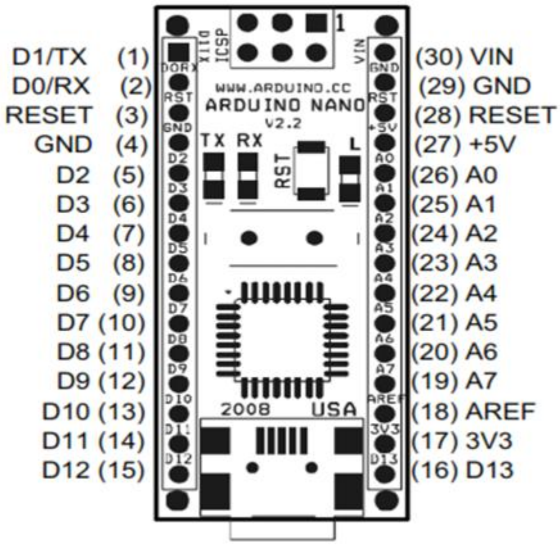


Fig 2.2 Arduino Nano Pin Layout

In addition, some pins have specialized functions:

Serial- 0 (RX) and 1 (TX)

These are used to receive (RX) and transmit (TX) TTL serial data. These pins are connected to the corresponding pins of the FTDI USB-to-TTL Serial chip.

External Interrupts- 2 and 3

These pins can be configured to trigger an interrupt on a low value, a rising or falling edge, or a change in value.

PWM- 3, 5, 6, 9, 10, and 11

They provide 8-bit PWM output with the analogWrite() function.

SPI- 10 (SS), 11 (MOSI), 12 (MISO), 13 (SCK)

These pins support SPI communication, which, although provided by the underlying hardware, is not currently included in the Arduino language.

LED- 13:

There is a built-in LED connected to digital pin 13. When the pin is HIGH value, the LED is on, when the pin is LOW, it's off.

The Nano has 8 analog inputs, each of which provides 10 bits of resolution (i.e. 1024 different values). By default they measure from ground to 5 volts, though is it possible to change the upper end of their range using the analogReference() function. Analog pins 6 and 7 cannot be used as digital pins. Additionally, some pins have specialized functionality:

I2C- 4 (SDA) and 5 (SCL):

They support I2C (TWI) communication using the Wire library.

There are a couple of other pins on the board:

AREF - Reference voltage for the analog inputs. Used with analogReference().

Reset- Bring this line LOW to reset the microcontroller. Typically used to add a reset button to shields which block the one on the board.

2.1.5 COMMUNICATION

The Arduino Nano has a number of facilities for communicating with a computer, another Arduino, or other microcontrollers. The ATmega168 and ATmega328 provide UART TTL (5V) serial communication, which is available on digital pins 0 (RX) and 1 (TX). An FTDI FT232RL on the board channels this serial communication over USB and the FTDI drivers (included with the Arduino software) provide a virtual com port to software on the computer.

The Arduino software includes a serial monitor which allows simple textual data to be sent to and from the Arduino board. The RX and TX LEDs on the board will flash when data is being transmitted via the FTDI chip and USB connection to the computer (but not for serial communication on pins 0 and 1).

A SoftwareSerial library allows for serial communication on any of the Nano's digital pins. ATmega328 also support I2C and SPI communication. The Arduino software includes a Wire library to simplify use of the I2C bus.

2.1.6 PROGRAMMING

The Arduino Nano can be programmed with the Arduino software (IDE). The ATmega168 or ATmega328 on the Arduino Nano comes pre-burned with a boot loader that allows you to upload new code to it without the use of an external hardware programmer. It communicates using the original STK500 protocol.

The boot loader can also be bypassed and the microcontroller can be programmed through the ICSP (In-Circuit Serial Programming) header using Arduino ISP or similar. Fig 2.3 shows the Arduino IDE.

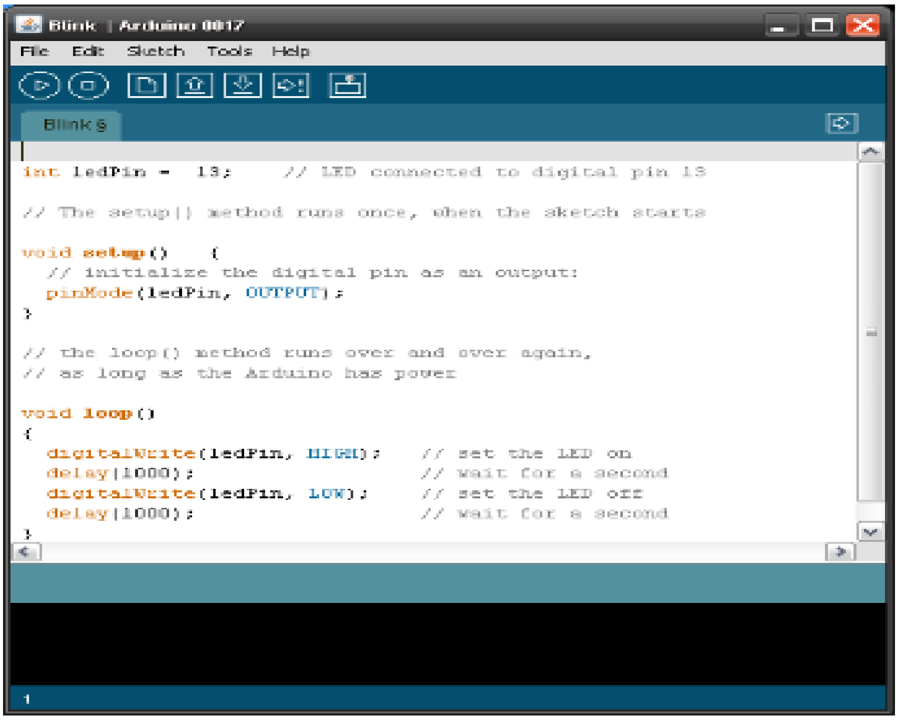


Fig 2.3 Arduino IDE

2.1.7 SPECIFICATIONS

The Table 2.1 provides the Specification for Arduino Nano.

Table 2.1 Arduino Nano Specification

Microcontroller	Atmel ATmega168 or ATmega328
Operating Voltage	5 V (logic level)
Input Voltage	7-12 V(recommended)
Input Voltage(limits)	6-20 V
Digital I/O Pins	14 (of which 6 provide PWM output)
Analog Input Pins	8
DC Current per I/O Pin	40 mA
Flash Memory	16 KB (ATmega168) or 32 KB (ATmega328) of which 2 KB used by boot loader
SRAM	1 KB (ATmega168) or 2 KB (ATmega328)
EEPROM	512 bytes (ATmega168) or 1 KB (ATmega328)
Clock Speed	16 MHz
Dimensions	0.73" x 1.70"

2.1.8 ATmega 328
PERIPHERAL FEATURES

- Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
- One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and
- Capture Mode
- Real Time Counter with Separate Oscillator
- Six PWM Channels
- 8-channel 10-bit ADC in TQFP and QFN/MLF package
- 6-channel 10-bit ADC in PDIP Package
- Programmable Serial USART
- Master/Slave SPI Serial Interface
- Byte-oriented 2-wire Serial Interface (Philips I2C compatible)
- Programmable Watchdog Timer with Separate On-chip Oscillator

- On-chip Analog Comparator
- Interrupt and Wake-up on Pin Change

The fig 2.4 provides the block diagram of the micro-controller atmega328.

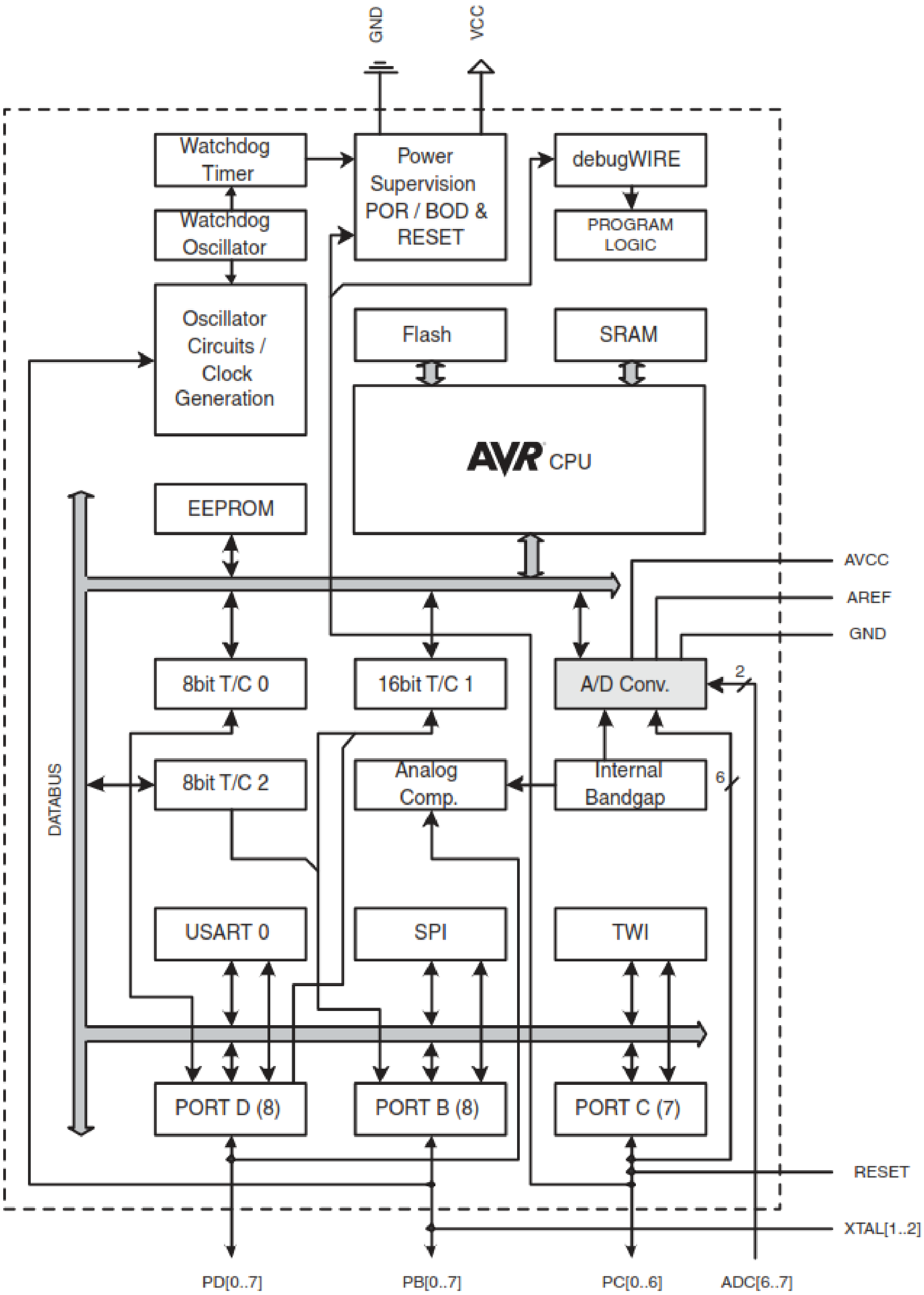


Fig 2.4 Block Diagram: ATmega 328

2.2 ACCELEROMETER: ADXL345

2.2.1 OVERVIEW

The ADXL345 is a small, thin, ultralow power, 3-axis accelerometer with high resolution (13-bit) measurement up to ±16 g. Digital output data is formatted as 16-bit twos complement and is accessible through either a SPI (3- or 4- wire) or I2C digital interface with data rates ranging from 10 Hz to 3200 Hz. The fig 2.5 shows the ADXL345 accelerometer.

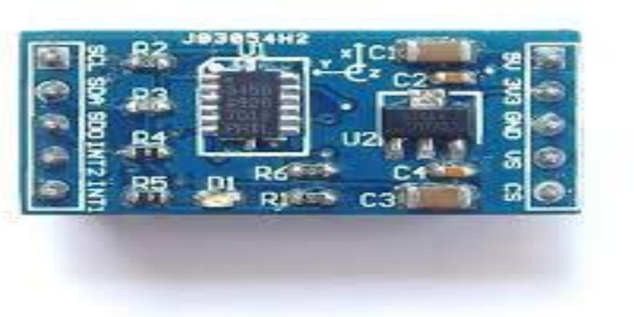


Fig 2.5 Accelerometer: ADXL345

The ADXL345 is well suited for mobile device applications. It measures the static acceleration of gravity in tilt-sensing applications, as well as dynamic acceleration resulting from motion or shock. Its high resolution (4mg /LSB) enables resolution of inclination changes of as little as 0.25°.

Several special sensing functions are provided. Activity and inactivity sensing detect the presence or lack of motion and if the acceleration on any axis exceeds a user-set level. Tap sensing detects single and double taps. Free-Fall sensing detects if the device is falling. These functions can be mapped to interrupt output pins. An integrated 32 level FIFO can be used to store data to minimize host processor intervention. Low power modes enable intelligent motion-based power management with threshold sensing and active acceleration measurement at extremely low power dissipation.

Fig 2.6 shows the block diagram of ADXL345.

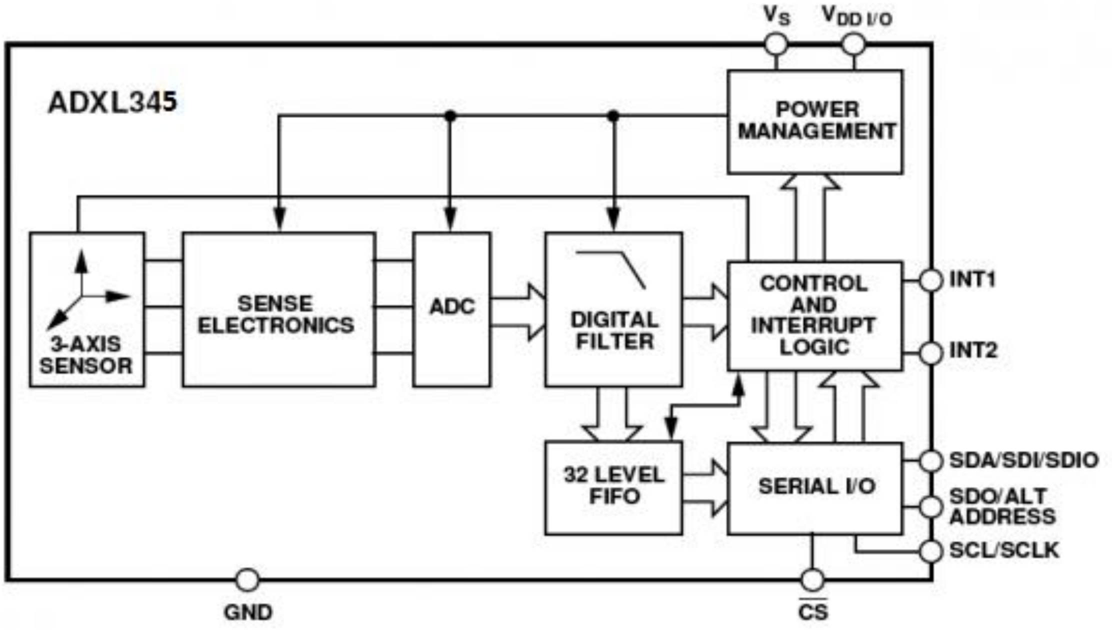


Fig 2.6 Block Diagram: ADXL345

Pin out configuration of ADXL345 breakout board is shown in the fig 2.7.

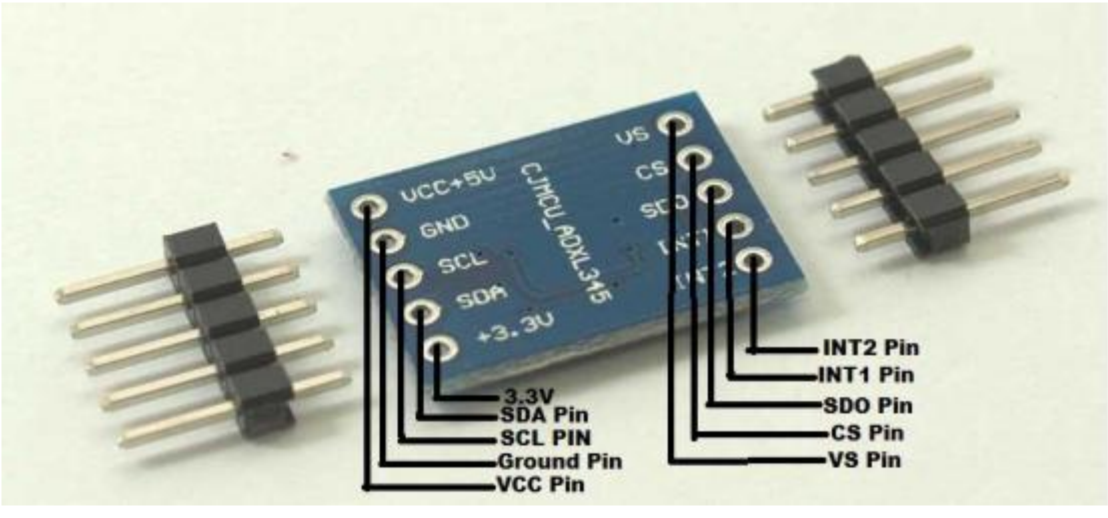


Fig 2.7 Pin Configuration: ADXL345

2.2.2 WORKING

The sensor consists of a micro machined structure on a silicon wafer. The structure is suspended by polysilicon springs which allow it to deflect smoothly in any direction when subject to acceleration in the X, Y and/or Z axis. Deflection causes a change in capacitance between fixed plates and plates attached to the suspended structure. This change in capacitance on each axis is converted to an output voltage proportional to the acceleration on that axis.

2.2.3 DIMENSIONS (Without Header)

- Length:25mm/0.95in
- Width:19mm/0.75in
- Height:3.14mm/0.12in
- Weight:1.27g/0.04oz
- This board/chip uses I2C 7-bit address 0x53.

2.2.4 HARDWARE FEATURES

- Ultra low power
- Power consumption scales automatically with bandwidth
- User selectable fixed 10-bit resolution or 4 mg /LSB scale factor in all g-ranges, up to 13-bit resolution at ±16 g
- 32 level output data FIFO minimizes host processor load
- Built in motion detection functions
    - Tap/Double Tap detection
    - Activity/Inactivity monitoring
    - Free-Fall detection
- Supply and I/O voltage range: 1.8 V to 3.6 V
- SPI (3 and 4 wire) and I2C digital interfaces
- Flexible interrupt modes – Any interrupt mappable to either interrupt pin
- See data sheet for additional features

2.2.5 DRIVER FEATURES

- Driver supports both SPI (3 and 4 wire) and I2C digital interface
  - I2C client using the 2.6 new style binding driver model
  - SPI using the generic Linux SPI Bus Driver Model
- Support for Linux Power Management (PM) suspend resume
- User selectable Sample Rate / Bandwidth
- User selectable resolution
- Support for 32 level output data FIFO that minimizes host processor load
- Option to report acceleration as Linux Input Absolute or Relative events.
- Motion detection functions
  - Tap/Double Tap detection
    - User selectable Linux Input Event Codes for TAP x,y,z axis
  - Activity/Inactivity monitoring
    - User selectable Linux Input Event Code for Activity/Inactivity reporting
    - Option to minimize host processor load and save additional power by automatically switch to sleep mode during periods of inactivity.
- Free-Fall detection
  - User selectable Linux Input Event Code for Free-Fall reporting

2.3 GSM MODULE

2.3.1 OVERVIEW

GSM is a digital, mobile radio standard developed for mobile, wireless, voice communications. GSM uses a combination of both the time division multiple access (TDMA) and frequency division multiple access (FDMA). With this combination, more channels of communications are available, and all channels are digital.

The GSM service is available in following frequency bands:

- 850 MHz
- 900 MHz
- 1800 MHz
- 1900 MHz

2.3.2 GSM MODEM

GSM/GPRS RS232 Modem is built with **SIMCOM SIM900** a **Quad-band** GSM/GPRS engine, works on frequencies 850MHz, 900MHz, 1800MHz and 1900MHz.It is very compact in size and easy to use as plug in GSM Modem. The Modem is designed with RS232 Level converter circuitry, which allows you to directly interface PC Serial port. The baud rate can be configurable from 9600-115200 through AT commands. The GSM/GPRS RS232 Modem have internal TCP/IP stack to enable you to connect with internet via GPRS.

It is suitable for SMS as well as DATA transfer application in M2M interface. The modem needs only 3 wires (Tx, Rx, and GND) except Power supply to interface with microcontroller/Host PC. The built in voltage regulator allows you to connect wide range of unregulated power supply (4.2V - 13V).Using this modem, you will be able to Send & Read SMS, connect to Internet via GPRS through simple AT commands. The fig 2.8 shows the GSM module.

Fig 2.8 GSM Module

2.3.3 SIM900

Featuring an industry-standard interface, the SIM900 delivers GSM/GPRS 850/900/1800/1900MHz performance for voice, SMS, Data, and Fax in a small form factor and with low power consumption. With a tiny configuration of 24mm x 24mm x 3 mm, SIM900 can fit almost all the space requirements in any M2M application, especially for slim and compact demand of design.

- SIM900 is designed with a very powerful single-chip processor integrating AMR926EJ-S core
- Quad - band GSM/GPRS module with a size of 24mmx24mmx3mm
- SMT type suit for customer application
- An embedded Powerful TCP/IP protocol stack.

The fig 2.9 shows a SIM900 GSM modem.

Fig 2.9 SIM900 GSM Modem

2.3.4 GENERAL FEATURES

- Quad-Band 850/ 900/ 1800/ 1900 MHz
- GPRS multi-slot class 10/8
- GPRS mobile station class B
- Compliant to GSM phase 2/2+[Class 4 (2 W @850/ 900 MHz)][Class 1 (1 W @ 1800/1900MHz)]

- Dimensions: 24* 24 * 3 mm
- Weight: 3.4g
- Control via AT commands (GSM 07.07 ,07.05 and SIMCOM enhanced AT Commands)
- SIM application toolkit
- Supply voltage range 3.4 to 4.5 V
- Low power consumption
- Operation temperature: -30 °C to +80 °C

2.3.5 SPECIFICATIONS FOR DATA:

- GPRS class 10: max. 85.6 kbps (downlink)
- Coding schemes CS 1, 2, 3, 4
- CSD up to 14.4 kbps
- USSD
- Non transparent mode
- PPP-stack

2.3.6 SPECIFICATIONS FOR SMS VIA GSM / GPRS

- Point-to-point MO and MT
- SMS cell broadcast
- Text and PDU mode

2.3.7 INTERFACES:

- Interface to external SIM 3V/ 1.8V
- analog audio interface
- RTC backup
- SPI interface
- Serial interface
- Antenna pad
- I2C
- GPIO

2.4 GLOBAL POSITIONING SYSTEM (GPS)

2.4.1 OVERVIEW

The Global Positioning System (GPS) is a space-based satellite navigation system that provides location and time information in all weather conditions, anywhere on or near the Earth where there is an unobstructed line of sight to four or more GPS satellites. The system provides critical capabilities to military, civil and commercial users around the world. It is freely accessible to anyone with a GPS receiver. The fig 2.10 shows the position of the satellites in a GPS system.

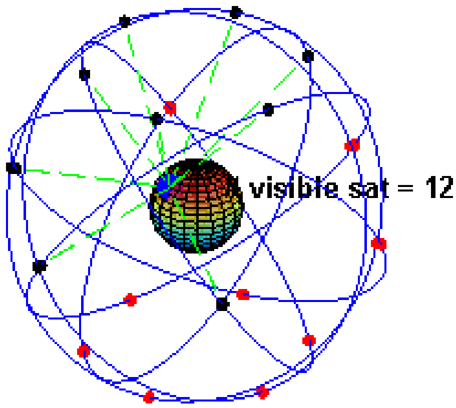


Fig 2.10 Satellite Position in GPS System

In the GPS system, a constellation of 24 satellites circles the earth in near-circular inclined orbits. By receiving signals from at least four of these satellites, the receiver position (latitude, longitude, and altitude) can be determined accurately. In effect, the satellites substitute for the geodetic position markers used in terrestrial surveying. In terrestrial surveying, it is only necessary to have three such markers to determine the three unknowns of latitude, longitude, and altitude by means of triangulation. With the GPS system, a time marker is also required, which necessitates getting simultaneous measurements from four satellites.

The GPS system uses one-way transmissions, from satellites to users, so that the user does not require a transmitter, only a GPS receiver. The only quantity the receiver has to be able to measure is time, from which propagation delay, and hence the range to each satellite, can be determined. Each satellite broadcasts its ephemeris (which is a table of the orbital elements as described), from which its position can be calculated. Knowing the range to three of the satellites and their positions, it is possible to compute the position of the observer (user). The geocentric-equatorial coordinate system is used with the GPS system, where it is called the earth-centred, earth-fixed (ECEF) coordinate system.

2.4.2 GPS ACCURACY

For the moment, knowing the positions of three satellites and the measured range to each, the position of the observer relative to the coordinate system can be calculated. Of course, the satellites are moving, so their positions must be tracked accurately. The satellite orbits can be predicted from the orbital parameters. These parameters are continually updated by a master control station which transmits them up to the satellites, where they are broadcast as part of the navigational message from each satellite. Just as in a land-based system, better accuracy is obtained by using reference points well separated in space.

2.4.3 POSITION DETERMINATION & TIMING

The GPS constellation consists of 24 satellites in six near-circular orbits, at an altitude of approximately 20,000 km. The ascending nodes of the orbits are separated by 60°, and the inclination of each orbit is 55°. Time enters into the position determination in two ways.

First, the ephemerides must be associated with a particular time or epoch. The standard timekeeper is an atomic standard, maintained at the U.S. Naval

Observatory, and the resulting time is known as GPS time. Each satellite carries its own atomic clock. The time broadcasts from the satellites are monitored by the control station, which transmits back to the satellites any errors detected in timing relative to GPS time. No attempt is made to correct the clocks aboard the satellites; rather, the error information is rebroadcast to the user stations, where corrections can be implemented in the calculations. It can be assumed, therefore, that the satellite position relative to the ECEF coordinate system (the geocentric-equatorial coordinate system), is accurately known.

Second, time markers are needed to show when transmissions leave the satellites so that, by measuring propagation times and knowing the speed of propagation, the ranges can be calculated. Therein lies a problem, since the user stations have no direct way of telling when a transmission from a satellite commenced.

The problem is overcome by having the satellite transmit a continuous-wave carrier, which is modulated by a pseudo-random code, timing for the carrier and the code being derived from the atomic clock aboard the satellite. At a user station, the receiver generates a replica of the modulated signal from its own (nonatomic) clock, which is correlated with the received signal in a correlator. A delay is introduced into the replica signal path and is adjusted until the two signals show maximum correlation. If the receiver clock started at exactly the same time as the satellite clock, the delay in the replica path would be equal to the propagation delay.

2.4.4 GPS SIGNAL

GPS satellites transmit two radio signals. These are designated as L1 and L2. A Civilian GPS uses the L1 signal frequency (1575.42 MHz) in the UHF band. The signals travel by line of sight, meaning they will pass through clouds, glass, plastic etc but will not travel through solid objects such as buildings and mountains.

The GPS signal contains three different bits of information — a pseudo random code, almanac data and ephemeris data.

- The **pseudo random code** is simply an I. D. code that identifies which satellite is transmitting information. You can often view this number on your GPS unit's satellite information page; the number attached to each signal bar identifies which satellites it's receiving a signal from.
- **Almanac data** is data that describes the orbital courses of the satellites. Every satellite will broadcast almanac data for every satellite. Your GPS receiver uses this data to determine which satellites it expects to see in the local sky. It can then determine which satellites it should track. With Almanac data the receiver can concentrate on those satellites it can see and forget about those that would be over the horizon and out of view. Almanac data is not precise and can be valid for many months.
- **Ephemeris data** is data that tells the GPS receiver where each GPS satellite should be at any time throughout the day. Each satellite will broadcast its own ephemeris data showing the orbital information for that satellite only. Because ephemeris data is very precise orbital and clock correction data necessary for precise positioning, its validity is much shorter. It is broadcast in three six second blocks repeated every 30 seconds.

2.4.5 GPS STATUS

- **Factory Start**: All data is considered invalid.
- **Cold Start**: Almanac data is current but Ephemeris is not or has expired.
- **Warm Start**: Both Almanac and Ephemeris data is current.

2.4.6 UBLOX GPS MODEM

UBLOX GPS Receiver with ceramic POT Antenna provides reliable positioning, navigation, and timing services to worldwide users on a continuous basis in all weather, day and night, anywhere on the Earth. Global Positioning System (GPS) satellites broadcast signals from space that GPS receivers, use to provide three-dimensional location (latitude, longitude, and altitude) plus precise time. GPS UBLOX receiver can acquire GPS signals from 65 channels of satellites and output position data with high accuracy.

The output is serial data of 9600 baud rate which is standard NMEA 0183 v3.0 protocol offering industry standard data messages and a command set for easy interface to mapping software like Trimble Studio and embedded devices like Microcontrollers. Fig 2.11 shows the GPS module.

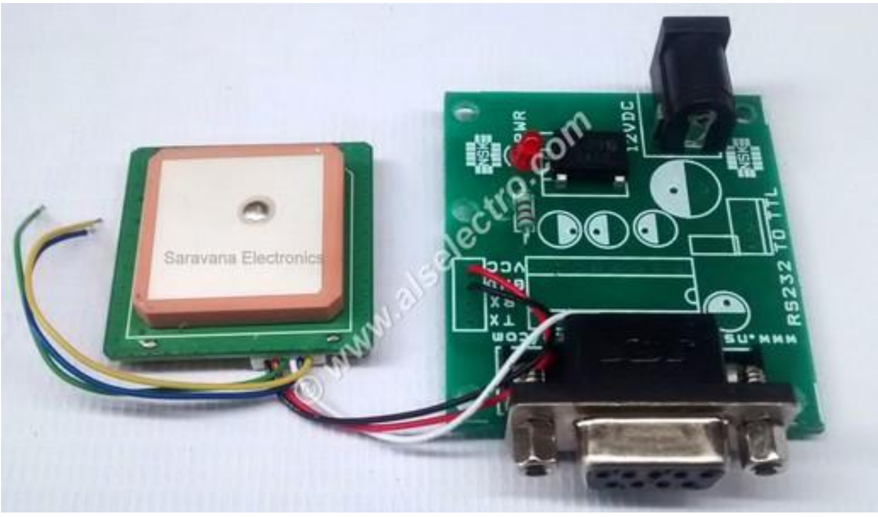


Fig 2.11 GPS Module

FEATURES

- Both RS232 & TTL signal outputs. Very easy to interface with Microcontrollers.
- High sensitivity -160dBm & Searching up to 65 Channel of satellites.
- Low power consumption.

- GPS L1 C/A Code.
- Supports NMEA0183 V 3.01 data protocol.
- Real time navigation for location based services.
- Works from +5V DC signal and outputs 9600 bps serial data.
- Ceramic POT antenna built on module.
- Used in Car Navigation and Marine Navigation, Fleet Management & Vehicle Tracking.

SPECIFICATION

- Operating Voltage 5 V DC Regulated Power Supply & Operating Current 150 mA.
- Sensitivity -160 dBm, Channels 65. 65 parallel channels all in view searching.
- L1 C/A code Protocol output baud rate 9600 bps no handshaking.
- Protocol format NMEA0183 V 3.01 GGA, GLL, GSA, GSV, RMC, VTG.
- Output Voltage level 3.3V signals. Serial UART interfacing directly to microcontrollers working at 5V and 3V.
- Frequency 1, 1575.42 MHz.
- C/A Code 1.023Mhz chip rate.
- Accuracy in Position 5 Meters, Accuracy in Velocity 0.1 Meters/Second, Accuracy in Time 0.1 Microsecond.
- Time to First Fix for first power on 33 Second approx, Time to Reacquisition 2 Second.
- Update Rate 1 Hz.

DATA FORMAT

Eg:

$GPRMC,225446,A,4916.45,N,12311.12,W,000.5,054.7,190215,020.3,E*68

Legend:

225446	Time of fix 22:54:46 UTC
A	Navigation receiver warning A = OK, V = warning
4916.45,N	Latitude 49 deg. 16.45 min North
12311.12,W	Longitude 123 deg. 11.12 min West
000.5	Speed over ground, Knots
054.7	Course Made Good, True
190215	Date of fix 19 February 2015
020.3,E	Magnetic variation 20.3 deg East
*68	mandatory checksum

2.5 PUSH BUTTON

The main ideology behind including a push button is to detect the presence of human inside the helmet. Various cases are witnessed where people do not wear a helmet but place it in front of them while driving or hang it along the rear view mirror. If the helmet falls down under such cases, the distress signal must not be triggered. Precautions must be enforced to avoid such situations. Hence we require a mechanism to detect the human presence.

There are multiple ways to detect the presence of human. Certain methods are:

- PIR sensor
- IR pulse detector
- Push buttons

2.5.1 PIR:

PIRs are basically made of a pyroelectric sensor, which can detect levels of infrared radiation.

2.5.2 IR PULSE DETECTOR

The sensor itself consists of an infrared emitter and detector mounted side-by-side and pressed closely against the skin. When the heart pumps, there is an amount of blood pressure, which increases the amount of infrared light from the emitter that gets reflected back to the detector. The detector passes more current when it receives more light, which in turn causes a voltage drop to enter the amplifier circuitry. This can be used to detect the presence of head inside the helmet.

The major reason for avoiding their use is

- The sensors are bulkier. Sensor - 10mm

  Module - 29 to 40 mm

So when this is placed inside the helmet, it becomes protruding and affects the ease of driver.

- Since the helmet is exposed to the sunlight the rise in temperature will also trigger the sensors.
- It gets easily affected by the ambient radiations from the sun. High degree of ambiguity will be present, thus reducing the sensitivity and accuracy.

2.5.3 5500 SERIES PUSH BUTTONS

LL1105 switch SPECIFICATIONS

- Contact rating: 50mA 12VDC
- Mechanical life: 5,000,000 Cycles
- Contact Resistance: 50mΩ at 5VDC, 10mA
- Insulation Resistance: 100MΩ Min. at 100V
- Dielectric Strength: 250VAC (50Hz., 1 Minute)
- Force: 65 ± 20 gram force
- Operating Temperature: -20°C to 70°C
- Size: 6X6 mm

2.6 BATTERY SPECIFICATIONS

The table 2.2 provides the specifications for the Li-ion 18650 battery.

Table 2.2 Battery Specification

Item		Specification	Remarks
4.1	Typical capacity	2200mAh	0.2 C_5A discharge
4.2	Minimum Capacity	2150mAh	
4.2 Nominal Voltage		3.7V	
4.3 Discharging Voltage (Min)		2.75V	
4.4 Charging Voltage (Max.)		4.2±0.03V	
4.5 Charging Current（Std.）		0.5 C_5A	
4.6 Discharging Current（Std.）		0.2 C_5A	
4.7 Charging Current (Fast）		1 C_5A	0 ~ 40°C, ≤95%RH
4.8 Discharging Current（Fast）		1 C_5A	
4.9 Discharging Current（Max.）		2 C_5A	
4.10 Internal Impedance		≤70mΩ	AC impedance 1kHz Difference among cells should be less than 10mΩ in a shipment.
4.11 Weight		45.0±2.0g	
4.12 Outline dimension (see figure)	Diameter	ф 18.0±0.2mm	
	Length	64.8±0.5mm	
4.13 Battery cell storage and transportation environment and temperature ranges	Min 1 Month	-20 ~ +60°C, <75%RH*	Initial status of cell 3.80V and 50% of charge, the capacity lost during shipment < 20%. Capacity recover rate > 80%.
	Min 3 Months	-20 ~ +45°C, <75%RH*	
	Min 12 Months	-20 ~ +25°C, <75%RH*	

This chapter explained the specification and the functionality of every module present in the project. The operation of these modules will be dealt in further chapters.

CHAPTER 3

SOFTWARE DESCRIPTION

Arduino is an open-source computer hardware and software company, project and user community that designs and manufactures kits for building digital devices and interactive objects that can sense and control the physical world. This chapter provides an brief outline of Arduino IDE.

An integrated development environment (IDE) is a software application that provides comprehensive facilities to computer programmers for software development. An IDE normally consists of a source code editor, build automation tools and a debugger. Most modern IDEs have intelligent code completion.

3.1 ARDUINO IDE

The Arduino development environment contains a text editor for writing code, a message area, a text console, a toolbar with buttons for common functions, and a series of menus. It connects to the Arduino hardware to upload programs and communicate with them.

The toolbar buttons allow you to verify and upload programs, create, open, and save sketches, and open the serial monitor.

Verify 

Checks your code for errors.

Upload 

Compiles your code and uploads it to the Arduino I/O board.

New 

Creates a new sketch.

Open 

Presents a menu of all the sketches in your sketchbook.

Clicking one will open it within the current window.

Save 

Saves your sketch (code).

Serial Monitor 

Opens the serial monitor.

Additional commands are found within the five menus: File, Edit, Sketch, Tools, and Help. The menus are context sensitive which means only those items relevant to the work currently being carried out are available.

3.1.1 Edit

Copy for Forum

Copies the code of your sketch to the clipboard in a form suitable for posting to the forum, complete with syntax colouring.

Copy as HTML

Copies the code of your sketch to the clipboard as HTML, suitable for embedding in web pages.

3.1.2 Sketch

Verify/Compile

Checks your sketch for errors.

Show Sketch Folder

Opens the current sketch folder.

Add File

Adds a source file to the sketch

Import Library

Adds a library to your sketch by inserting #include statements at the start of your code.

3.1.3 Tools

Auto Format

This formats your code nicely: i.e. indents it so that opening and closing curly braces line-up and that the statements inside curly braces are indented more.

Archive Sketch

Archives a copy of the current sketch in .zip format. The archive is placed in the same directory as the sketch.

3.1.4 Board

Select the board that you're using.

Serial Port

This menu contains all the serial devices (real or virtual) on your machine. It should automatically refresh every time you open the top-level tools menu.

Programmer

For selecting a hardware programmer when programming a board or chip and not using the onboard USB-serial connection. Normally you won't need this, but if you're burning a bootloader to a new microcontroller, you will use this.

Burn Bootloader

The items in this menu allow you to burn a bootloader onto the microcontroller on an Arduino board. This is not required for normal use of an Arduino board but is useful if you purchase a new ATmega microcontroller (which normally comes without a bootloader).

This chapter dealt with the outline of Arduino IDE and programming the controller to perform the operation. The operation of the module is described in the following chapter.

CHAPTER 4

OPERATION

The basic operation of the Smart Helmet is as follows. When the push button is enabled the circuit is powered up and the controller obtains the acceleration data and calculates the ‘g’ force. If the force exceeds the threshold then the location is obtained from GPS and is transmitted by GSM to the helpline. The details of operation of each module are presented in the following sections. Fig 4.1 shows the operational flow chart of the project

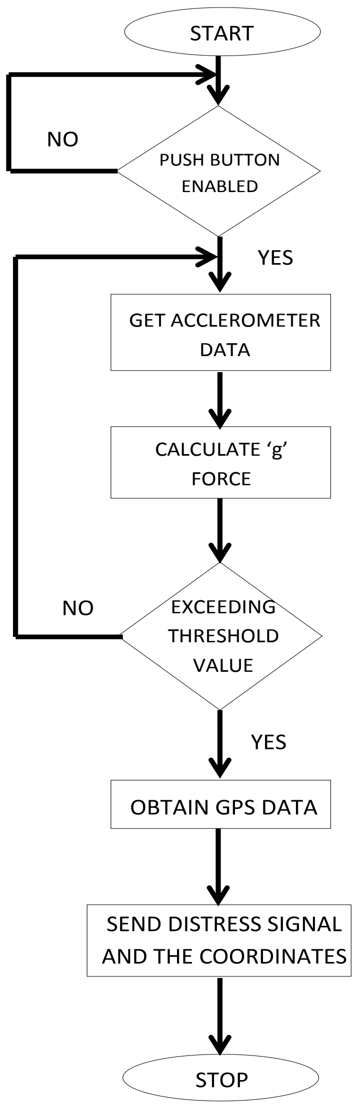


Fig 4.1 Operational Flowchart

The Smart Helmet consists of the following hardware components:

- Arduino
- Push Button
- Accelerometer
- GSM Module
- GPS Module

The working of each is given below.

4.1 ARDUINO NANO

Arduino is an open source platform which has an Atmega328 controller embedded in it. This controller controls the other modules of the smart helmet. It obtains the raw accelerometer reading from the accelerometer ADXL345 through I2C and converts it into 'g' force along all the 3 axes using the following calculations:

Gx = Raw_x/(2^(R-1))

Gy = Raw_y/(2^(R-1))

Gz = Raw_z/(2^(R-1))

R- Resolution = 12 bits.

G(x) – 'g' force in one axis

Raw _ (x) – Accelerometer output of one axis.

From this the resultant 'g' force acting on the human is found by:

Net 'g' force = Sqrt (Gx^2+Gy^2+Gz^2).

The resultant 'g' force is compared with a predetermined value and if it exceeds that value there is a high chance of an accident to have occurred. The Arduino now obtains the coordinates of the accident using the GPS module through software UART which gives latitude, longitude position in GPRMC format from which the actual values are determined.

After the position of the accident is obtained, the GSM is triggered by the Arduino through the hardware UART to call to the emergency helpline and send the accident location by an SMS stating that an accident has occurred and the position of the accident to provide faster rescue.

4.2 PUSH BUTTON AND POWER

The push button is used switch on the module whenever the rider wears the helmet. The push button is positioned such that, it is pressed when the rider wears the helmet. The size of LL1105 switch is 6X6mm hence it does not protrude out causing discomfort to the rider. The actuating force, to change the state of the switch is less enough which is sufficient to get the switch activated when the rider wears it, avoiding any interaction with the user in terms of the driver taking measures to switch it on whenever he is about to drive.

When the button is pressed, the power is fed to the Arduino from the battery thus switching it on. All other modules are powered from the Arduino. By this way, power is conserved when the helmet is not under operation.

4.3 ACCELEROMETER

The accelerometer is a MEMS device that measures the acceleration in all the three coordinates. The sensor consists of a micro machined structure on a silicon wafer. The structure is suspended by polysilicon springs which allow it to deflect smoothly in any direction when subjected to acceleration in the X, Y and Z axis. Deflection causes a change in capacitance between fixed plates and plates attached to the suspended structure. This change in capacitance on each axis is converted to an output voltage proportional to the acceleration on that axis. This output of the accelerometer will be in digital. The accelerometer sends the measured instantaneous acceleration of the 3 coordinates to the Arduino which is interfaced using I2C.The accelerometer sends about 200 values for every second.

4.4 GSM MODULE

The GSM module is used to communicate about the accident to the medical helpline. The module can send an SMS and make an emergency call regarding the situation. It is powered by a 12v 1A supply. It is usually programmed using the AT commands to perform its operation. The interfacing of the GSM module is very simple with Arduino Nano. Briefly, an activated SIM card should be inserted in its defined slot and wait for the signal LED to stop blinking which indicates that the signals are received. After this the AT commands are specified for the necessary actions. The following commands are used in Smart Helmet.

- AT – Initializes the GSM module
- ATD – Calls the specified number
- ATH – Hangs the call
- AT+CMGF – To send text message

4.5 GPS MODULE

GPS is used to provide the position of the accidents using the satellite coordinates. It usually provides output in the GPRMS format. The position can be decoded by using necessary software steps. Initially when the GPS is provided with the supply the signal LED starts blinking to indicate that it is searching for the signal, but when it stabilizes the GPS receives the coordinates about the location, which is fed to the Arduino via software UART. The received data is usually of the form:

Time/status of GPS/latitude/(N/S)/longitude/(E/W)/ground speed/tracking angle/date of fix/empty/check sum.

4.6 PROJECT SCHEMATIC

The fig 4.2 shows the project schematic and the interfacing of the various modules.

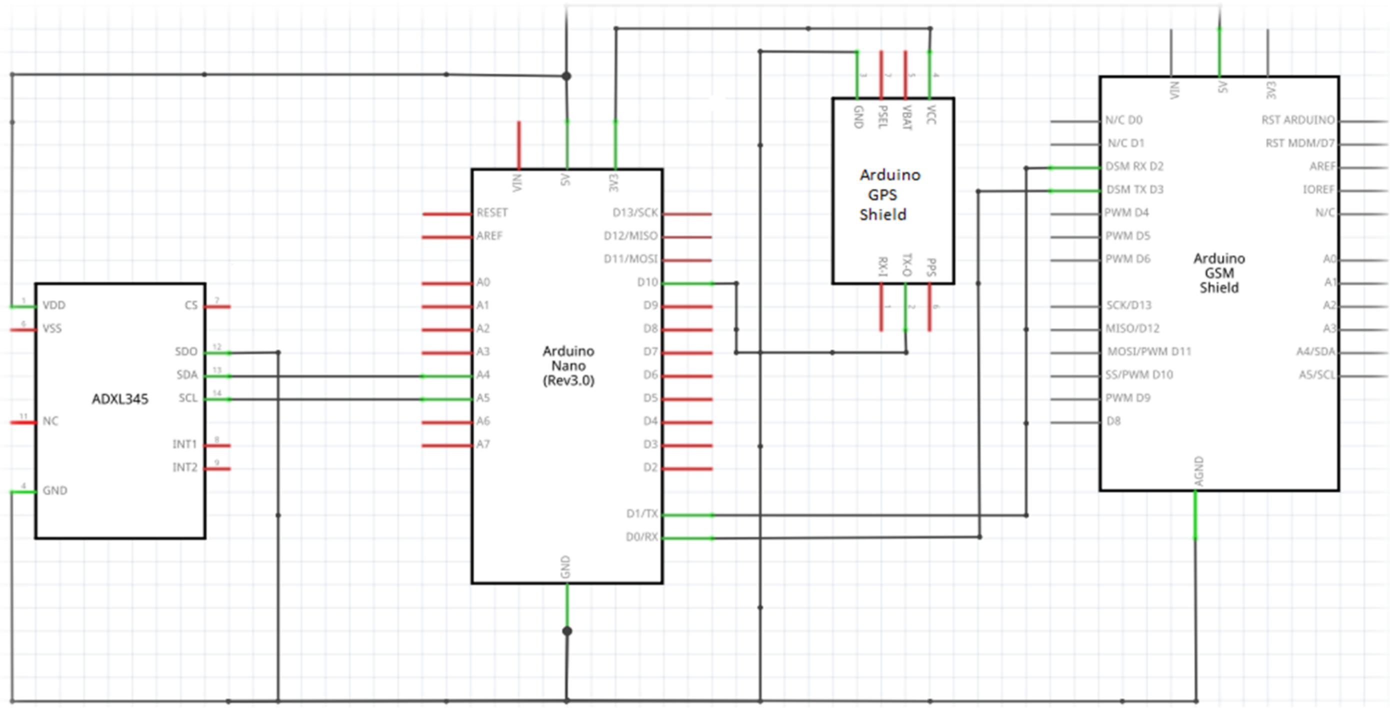


Fig 4.2 Project schematic

This section dealt with the interfacing of the various modules together and their operation. The following chapter describes how the modules are controlled using the software codes and the algorithm behind the accident detection.

CHAPTER 5

DETECTING ACCIDENTS

The real scenario accident cannot be easily detected because it involves the prediction of the circumstance of the event and the human tolerance. Moreover the situation of one accident may not suite for the other. But the threshold of the accident can be reverse engineered by calculating the human tolerance level of various common road events like

- Sudden braking
- Speed breaker
- Pot hole

All these events involve a certain threshold for its occurrence. Their values were tentatively found from various experimental trails.

- Sudden braking : 2.25 g
- Speed breaker : 2.65 g
- Pot hole : 3.25 g

The experimental results are shown in the following figures where the values are calculated by using Dynamic Length Moving Average in order to remove rapid fluctuation and to calculate an effective force over the period of the event.

There are no significant variations in the accelerometer output when the vehicle is running normally. But a spike occurs when ever the above mentioned event occurs ,from there the moving average order changes depending upon the value obtained. But the riders are able withstand this force, so the threshold for the occurrence of the accident must be a value greater than it.

It was found that the maximum time duration that an event persists is around 2.5 Sec. And the maximum ‘g’ force experienced during experimentation was just below 3.5 g. By calculations a human can withstand about 8 g for 5 sec depending upon their individual capability. So an event like accident would be sustained for about 5sec and the force experienced will also be high.

If these conditions are satisfied then it can be concluded that there is a high chance for the accident to have occurred.

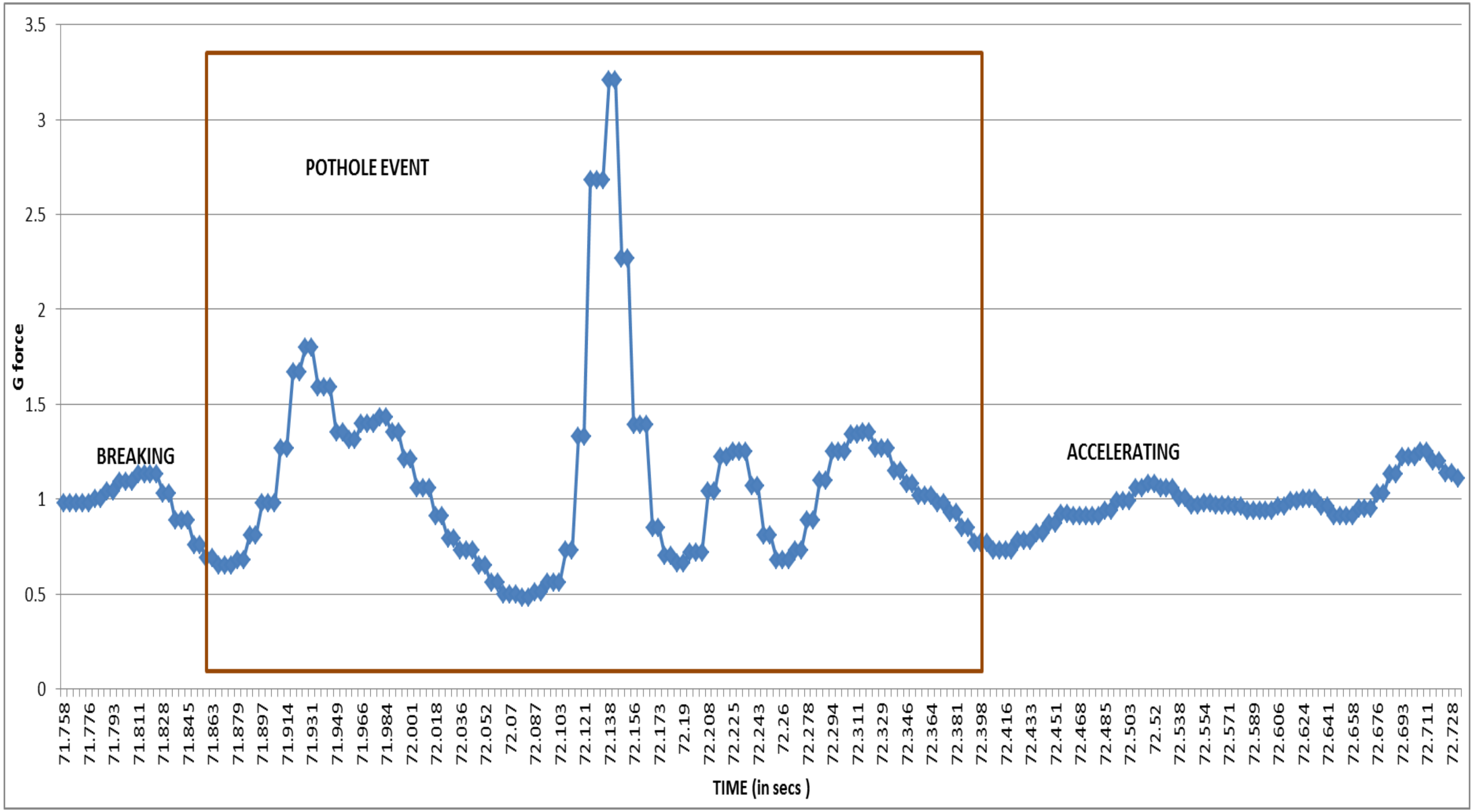


Fig. 5.1 Analysis Result of Pothole

The fig 5.1 shows the analysis results of pothole event. The first peak occurs during the braking action and the next one is for the front wheel entering pot hole. The lower peak is due to the saturation of the force and the highest peak is due to the back wheel entering the pothole where the accelerometer experiences the maximum turbulence. It is evident that the peak does not cross a maximum of 3.5g. Then force recedes to normal after acceleration.

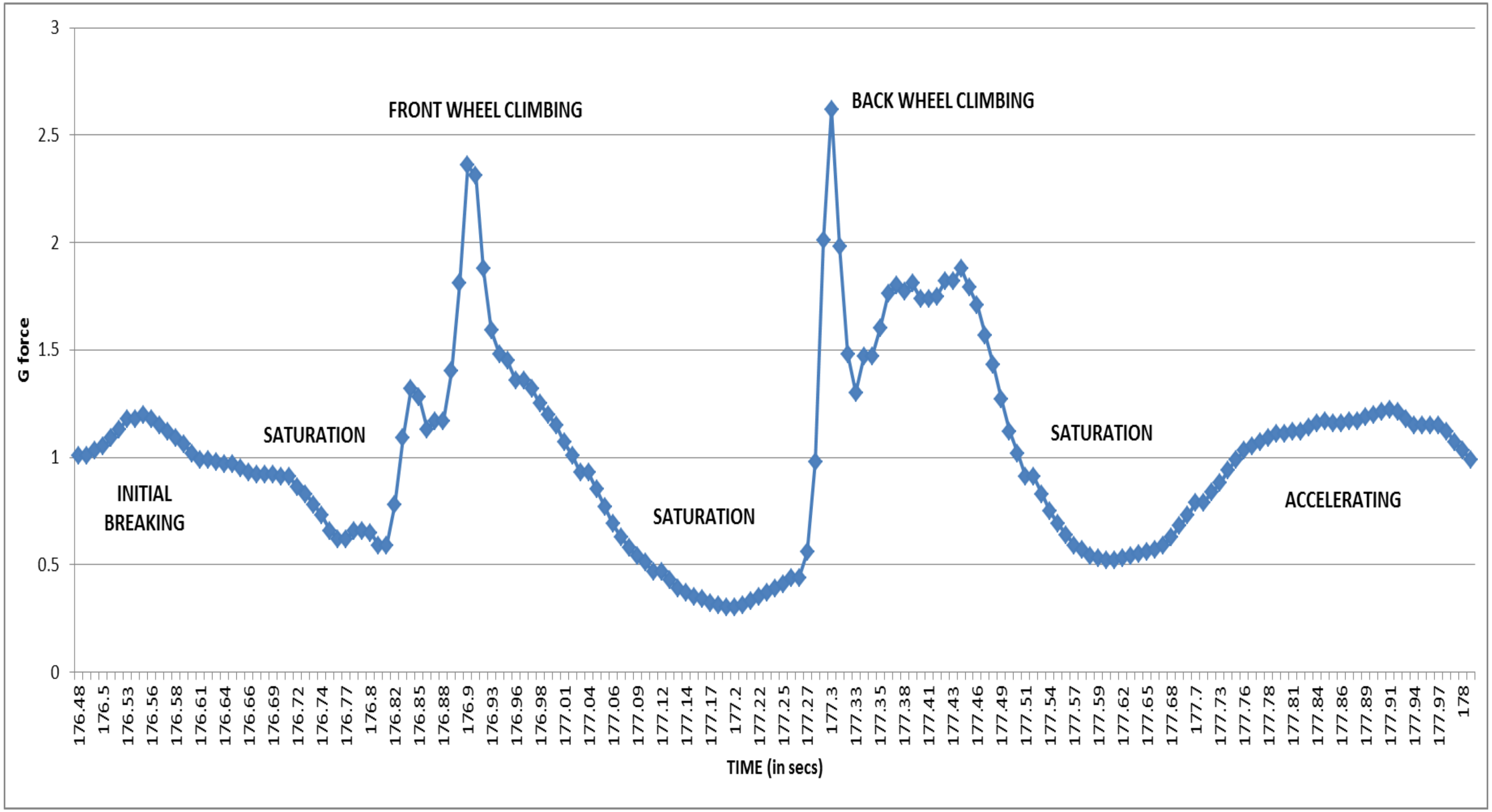


Fig. 5.2 Analysis Result of Speed Breaker

The fig 52 shows results of analysis os speedbreaker event. The first peak occurs during the braking action and the next one is for the front wheel entering pot hole. The lower peak is due to the saturation of the force and the highest peak is due to the back wheel entering the pothole where the accelerometer experiences the maximum turbulence. It is evident that the peak does not cross a maximum of 2.5g. Then force recedes to normal after

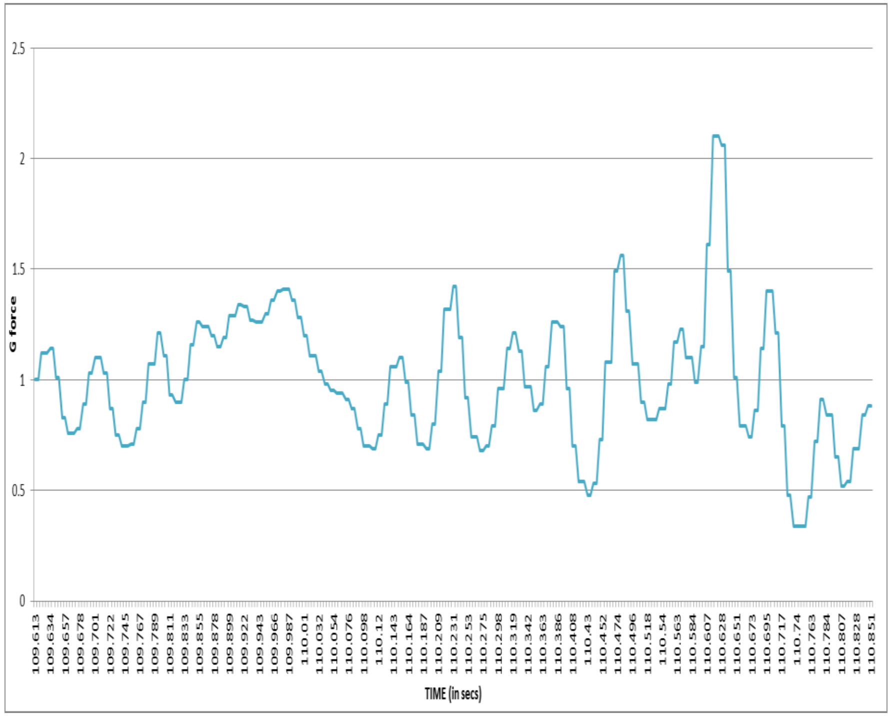


Fig.5.3 Analysis Result Sudden Braking At 90 Kmph

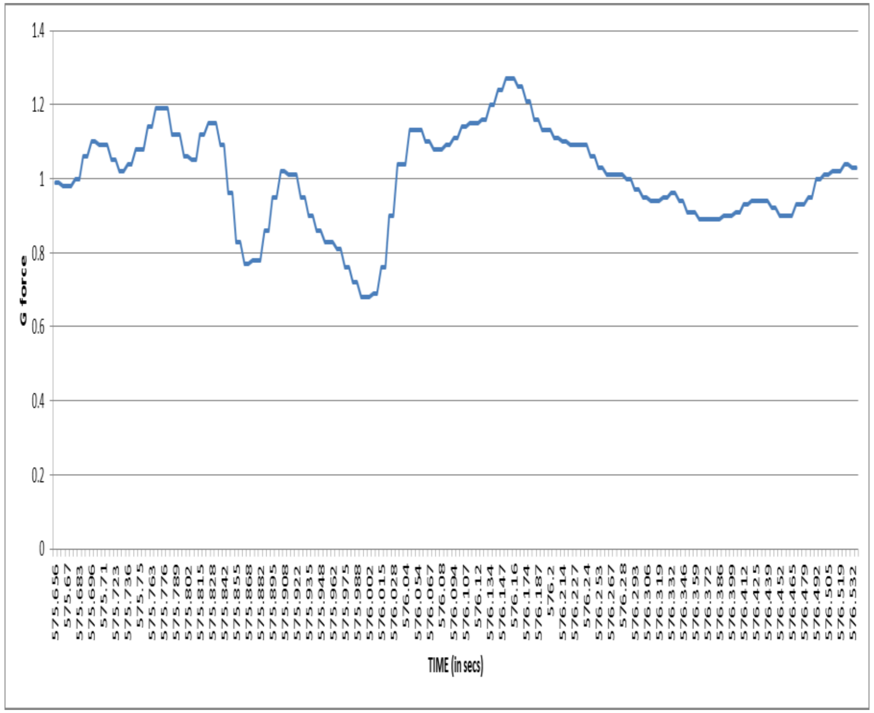


Fig.5.34analysis Result Sudden Braking At 40 Kmph

The fig 5.3 & 5.4 depicts the analysis results of sudden braking at 90 KMPH & 40 KMPH respectively. The plots show that there is a sudden rise in the values at the instant of braking. It is evident that the force experienced at 90 KMPH is greater than force at 40 KMPH and the force not exceeding 1.25 g in both the cases.

CHAPTER 6

CONCLUSION

Though road accidents are not entirely in one's hand, the trauma that it leads to, can be confined. It is arguably true that the fatality of an road accident can be reduced by providing medical assistance to the victim within the golden hour. Thus the project, smart helmet takes a step forward to save one's life by reducing the delay in providing medical help to the victim. Further the project is also modelled in such a manner that it will not send a falsie distress signal to the medical helpline thus making it a reliable accident detector.

The project can be made as a user-friendly product by incorporating the electronic module into any helmet converting them to a Smart Helmet. Thus the project SMART HELMET takes us a step closer in creating a safe and secure roadrides.

APPENDIX 1

ANALOG DEVICES

3-Axis, ±2 *g*/±4 *g*/±8 *g*/±16 *g* Digital Accelerometer

Data Sheet **ADXL345**

FEATURES

Ultralow power: as low as 23 µA in measurement mode and 0.1 µA in standby mode at V_S = 2.5 V (typical)
Power consumption scales automatically with bandwidth
User-selectable resolution
- **Fixed 10-bit resolution**
- **Full resolution, where resolution increases with *g* range, up to 13-bit resolution at ±16 *g* (maintaining 4 m*g*/LSB scale factor in all *g* ranges)**

Patent pending, embedded memory management system with FIFO technology minimizes host processor load
Single tap/double tap detection
Activity/inactivity monitoring
Free-fall detection
Supply voltage range: 2.0 V to 3.6 V
I/O voltage range: 1.7 V to V_S
SPI (3- and 4-wire) and I²C digital interfaces
Flexible interrupt modes mappable to either interrupt pin
Measurement ranges selectable via serial command
Bandwidth selectable via serial command
Wide temperature range (−40°C to +85°C)
10,000 *g* shock survival
Pb free/RoHS compliant
Small and thin: 3 mm × 5 mm × 1 mm LGA package

APPLICATIONS

Handsets
Medical instrumentation
Gaming and pointing devices
Industrial instrumentation
Personal navigation devices
Hard disk drive (HDD) protection

GENERAL DESCRIPTION

The ADXL345 is a small, thin, ultralow power, 3-axis accelerometer with high resolution (13-bit) measurement at up to ±16 *g*. Digital output data is formatted as 16-bit twos complement and is accessible through either a SPI (3- or 4-wire) or I²C digital interface.

The ADXL345 is well suited for mobile device applications. It measures the static acceleration of gravity in tilt-sensing applications, as well as dynamic acceleration resulting from motion or shock. Its high resolution (3.9 m*g*/LSB) enables measurement of inclination changes less than 1.0°.

Several special sensing functions are provided. Activity and inactivity sensing detect the presence or lack of motion by comparing the acceleration on any axis with user-set thresholds. Tap sensing detects single and double taps in any direction. Free-fall sensing detects if the device is falling. These functions can be mapped individually to either of two interrupt output pins. An integrated, patent pending memory management system with a 32-level first in, first out (FIFO) buffer can be used to store data to minimize host processor activity and lower overall system power consumption.

Low power modes enable intelligent motion-based power management with threshold sensing and active acceleration measurement at extremely low power dissipation.

The ADXL345 is supplied in a small, thin, 3 mm × 5 mm × 1 mm, 14-lead, plastic package.

FUNCTIONAL BLOCK DIAGRAM

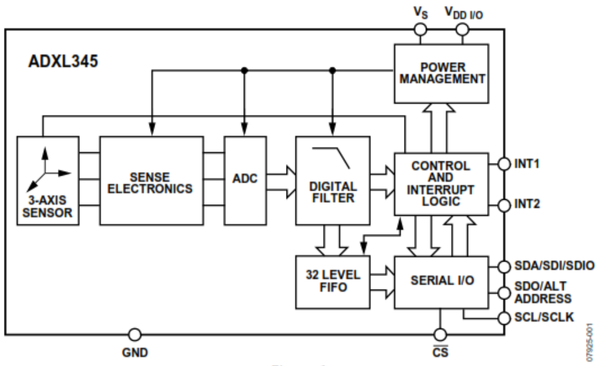


Figure 1.

Rev. D **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

SPECIFICATIONS

T_A = 25°C, V_S = 2.5 V, $V_{DD I/O}$ = 1.8 V, acceleration = 0 *g*, C_S = 10 μF tantalum, $C_{I/O}$ = 0.1 μF, output data rate (ODR) = 800 Hz, unless otherwise noted. All minimum and maximum specifications are guaranteed. Typical specifications are not guaranteed.

Table 1.

Parameter	Test Conditions	Min	Typ[1]	Max	Unit
SENSOR INPUT	Each axis				
Measurement Range	User selectable		±2, ±4, ±8, ±16		*g*
Nonlinearity	Percentage of full scale		±0.5		%
Inter-Axis Alignment Error			±0.1		Degrees
Cross-Axis Sensitivity[2]			±1		%
OUTPUT RESOLUTION	Each axis				
All *g* Ranges	10-bit resolution		10		Bits
±2 *g* Range	Full resolution		10		Bits
±4 *g* Range	Full resolution		11		Bits
±8 *g* Range	Full resolution		12		Bits
±16 *g* Range	Full resolution		13		Bits
SENSITIVITY	Each axis				
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	All *g*-ranges, full resolution	230	256	282	LSB/*g*
	±2 *g*, 10-bit resolution	230	256	282	LSB/*g*
	±4 *g*, 10-bit resolution	115	128	141	LSB/*g*
	±8 *g*, 10-bit resolution	57	64	71	LSB/*g*
	±16 *g*, 10-bit resolution	29	32	35	LSB/*g*
Sensitivity Deviation from Ideal	All *g*-ranges		±1.0		%
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}	All *g*-ranges, full resolution	3.5	3.9	4.3	m*g*/LSB
	±2 *g*, 10-bit resolution	3.5	3.9	4.3	m*g*/LSB
	±4 *g*, 10-bit resolution	7.1	7.8	8.7	m*g*/LSB
	±8 *g*, 10-bit resolution	14.1	15.6	17.5	m*g*/LSB
	±16 *g*, 10-bit resolution	28.6	31.2	34.5	m*g*/LSB
Sensitivity Change Due to Temperature			±0.01		%/°C
0 *g* OFFSET	Each axis				
0 *g* Output for X_{OUT}, Y_{OUT}		−150	0	+150	m*g*
0 *g* Output for Z_{OUT}		−250	0	+250	m*g*
0 *g* Output Deviation from Ideal, X_{OUT}, Y_{OUT}			±35		m*g*
0 *g* Output Deviation from Ideal, Z_{OUT}			±40		m*g*
0 *g* Offset vs. Temperature for X-, Y-Axes			±0.4		m*g*/°C
0 *g* Offset vs. Temperature for Z-Axis			±1.2		m*g*/°C
NOISE					
X-, Y-Axes	ODR = 100 Hz for ±2 *g*, 10-bit resolution or all *g*-ranges, full resolution		0.75		LSB rms
Z-Axis	ODR = 100 Hz for ±2 *g*, 10-bit resolution or all *g*-ranges, full resolution		1.1		LSB rms
OUTPUT DATA RATE AND BANDWIDTH	User selectable				
Output Data Rate (ODR)[3, 4, 5]		0.1		3200	Hz
SELF-TEST[6]					
Output Change in X-Axis		0.20		2.10	*g*
Output Change in Y-Axis		−2.10		−0.20	*g*
Output Change in Z-Axis		0.30		3.40	*g*
POWER SUPPLY					
Operating Voltage Range (V_S)		2.0	2.5	3.6	V
Interface Voltage Range ($V_{DD I/O}$)		1.7	1.8	V_S	V
Supply Current	ODR ≥ 100 Hz		140		μA
	ODR < 10 Hz		30		μA
Standby Mode Leakage Current			0.1		μA
Turn-On and Wake-Up Time[7]	ODR = 3200 Hz		1.4		ms

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

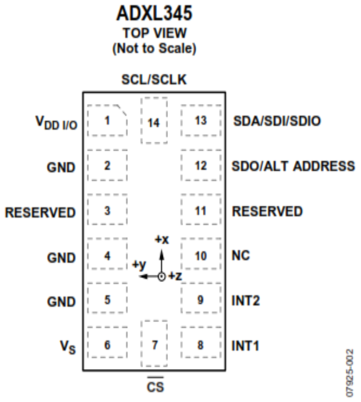


Figure 3. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{DD\ I/O}$	Digital Interface Supply Voltage.
2	GND	This pin must be connected to ground.
3	RESERVED	Reserved. This pin must be connected to V_S or left open.
4	GND	This pin must be connected to ground.
5	GND	This pin must be connected to ground.
6	V_S	Supply Voltage.
7	$\overline{CS}$	Chip Select.
8	INT1	Interrupt 1 Output.
9	INT2	Interrupt 2 Output.
10	NC	Not Internally Connected.
11	RESERVED	Reserved. This pin must be connected to ground or left open.
12	SDO/ALT ADDRESS	Serial Data Output (SPI 4-Wire)/Alternate I^2C Address Select (I^2C).
13	SDA/SDI/SDIO	Serial Data (I^2C)/Serial Data Input (SPI 4-Wire)/Serial Data Input and Output (SPI 3-Wire).
14	SCL/SCLK	Serial Communications Clock. SCL is the clock for I^2C, and SCLK is the clock for SPI.

THEORY OF OPERATION

The ADXL345 is a complete 3-axis acceleration measurement system with a selectable measurement range of ±2 *g*, ±4 *g*, ±8 *g*, or ±16 *g*. It measures both dynamic acceleration resulting from motion or shock and static acceleration, such as gravity, that allows the device to be used as a tilt sensor.

The sensor is a polysilicon surface-micromachined structure built on top of a silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide a resistance against forces due to applied acceleration.

Deflection of the structure is measured using differential capacitors that consist of independent fixed plates and plates attached to the moving mass. Acceleration deflects the proof mass and unbalances the differential capacitor, resulting in a sensor output whose amplitude is proportional to acceleration. Phase-sensitive demodulation is used to determine the magnitude and polarity of the acceleration.

POWER SEQUENCING

Power can be applied to V_S or $V_{DD\,I/O}$ in any sequence without damaging the ADXL345. All possible power-on modes are summarized in Table 6. The interface voltage level is set with the interface supply voltage, $V_{DD\,I/O}$, which must be present to ensure that the ADXL345 does not create a conflict on the communication bus. For single-supply operation, $V_{DD\,I/O}$ can be the same as the main supply, V_S. In a dual-supply application, however, $V_{DD\,I/O}$ can differ from V_S to accommodate the desired interface voltage, as long as V_S is greater than or equal to $V_{DD\,I/O}$.

After V_S is applied, the device enters standby mode, where power consumption is minimized and the device waits for $V_{DD\,I/O}$ to be applied and for the command to enter measurement mode to be received. (This command can be initiated by setting the measure bit (Bit D3) in the POWER_CTL register (Address 0x2D).) In addition, while the device is in standby mode, any register can be written to or read from to configure the part. It is recommended to configure the device in standby mode and then to enable measurement mode. Clearing the measure bit returns the device to the standby mode.

Table 6. Power Sequencing

Condition	V_S	$V_{DD\,I/O}$	Description
Power Off	Off	Off	The device is completely off, but there is a potential for a communication bus conflict.
Bus Disabled	On	Off	The device is on in standby mode, but communication is unavailable and creates a conflict on the communication bus. The duration of this state should be minimized during power-up to prevent a conflict.
Bus Enabled	Off	On	No functions are available, but the device does not create a conflict on the communication bus.
Standby or Measurement	On	On	At power-up, the device is in standby mode, awaiting a command to enter measurement mode, and all sensor functions are off. After the device is instructed to enter measurement mode, all sensor functions are available.

POWER SAVINGS

Power Modes

The ADXL345 automatically modulates its power consumption in proportion to its output data rate, as outlined in Table 7. If additional power savings is desired, a lower power mode is available. In this mode, the internal sampling rate is reduced, allowing for power savings in the 12.5 Hz to 400 Hz data rate range at the expense of slightly greater noise. To enter low power mode, set the LOW_POWER bit (Bit 4) in the BW_RATE register (Address 0x2C). The current consumption in low power mode is shown in Table 8 for cases where there is an advantage to using low power mode. Use of low power mode for a data rate not shown in Table 8 does not provide any advantage over the same data rate in normal power mode. Therefore, it is recommended that only data rates shown in Table 8 are used in low power mode. The current consumption values shown in Table 7 and Table 8 are for a V_S of 2.5 V.

Table 7. Typical Current Consumption vs. Data Rate (T_A = 25°C, V_S = 2.5 V, $V_{DD\ I/O}$ = 1.8 V)

Output Data Rate (Hz)	Bandwidth (Hz)	Rate Code	I_{DD} (µA)
3200	1600	1111	140
1600	800	1110	90
800	400	1101	140
400	200	1100	140
200	100	1011	140
100	50	1010	140
50	25	1001	90
25	12.5	1000	60
12.5	6.25	0111	50
6.25	3.13	0110	45
3.13	1.56	0101	40
1.56	0.78	0100	34
0.78	0.39	0011	23
0.39	0.20	0010	23
0.20	0.10	0001	23
0.10	0.05	0000	23

Table 8. Typical Current Consumption vs. Data Rate, Low Power Mode (T_A = 25°C, V_S = 2.5 V, $V_{DD\ I/O}$ = 1.8 V)

Output Data Rate (Hz)	Bandwidth (Hz)	Rate Code	I_{DD} (µA)
400	200	1100	90
200	100	1011	60
100	50	1010	50
50	25	1001	45
25	12.5	1000	40
12.5	6.25	0111	34

Auto Sleep Mode

Additional power can be saved if the ADXL345 automatically switches to sleep mode during periods of inactivity. To enable this feature, set the THRESH_INACT register (Address 0x25) and the TIME_INACT register (Address 0x26) each to a value that signifies inactivity (the appropriate value depends on the application), and then set the AUTO_SLEEP bit (Bit D4) and the link bit (Bit D5) in the POWER_CTL register (Address 0x2D). Current consumption at the sub-12.5 Hz data rates that are used in this mode is typically 23 µA for a V_S of 2.5 V.

Standby Mode

For even lower power operation, standby mode can be used. In standby mode, current consumption is reduced to 0.1 µA (typical). In this mode, no measurements are made. Standby mode is entered by clearing the measure bit (Bit D3) in the POWER_CTL register (Address 0x2D). Placing the device into standby mode preserves the contents of FIFO.

I²C

With $\overline{CS}$ tied high to $V_{DD\ I/O}$, the ADXL345 is in I²C mode, requiring a simple 2-wire connection, as shown in Figure 40. The ADXL345 conforms to the *UM10204 I²C-Bus Specification and User Manual*, Rev. 03—19 June 2007, available from NXP Semiconductor. It supports standard (100 kHz) and fast (400 kHz) data transfer modes if the bus parameters given in Table 11 and Table 12 are met. Single- or multiple-byte reads/writes are supported, as shown in Figure 41. With the ALT ADDRESS pin high, the 7-bit I²C address for the device is 0x1D, followed by the R/$\overline{W}$ bit. This translates to 0x3A for a write and 0x3B for a read. An alternate I²C address of 0x53 (followed by the R/$\overline{W}$ bit) can be chosen by grounding the ALT ADDRESS pin (Pin 12). This translates to 0xA6 for a write and 0xA7 for a read.

There are no internal pull-up or pull-down resistors for any unused pins; therefore, there is no known state or default state for the $\overline{CS}$ or ALT ADDRESS pin if left floating or unconnected. It is required that the $\overline{CS}$ pin be connected to $V_{DD\ I/O}$ and that the ALT ADDRESS pin be connected to either $V_{DD\ I/O}$ or GND when using I²C.

Due to communication speed limitations, the maximum output data rate when using 400 kHz I²C is 800 Hz and scales linearly with a change in the I²C communication speed. For example, using I²C at 100 kHz would limit the maximum ODR to 200 Hz. Operation at an output data rate above the recommended maximum may result in undesirable effect on the acceleration data, including missing samples or additional noise.

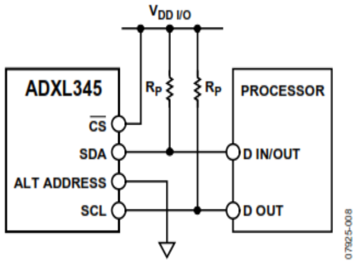


Figure 40. I²C Connection Diagram (Address 0x53)

If other devices are connected to the same I²C bus, the nominal operating voltage level of these other devices cannot exceed $V_{DD\ I/O}$ by more than 0.3 V. External pull-up resistors, R_P, are necessary for proper I²C operation. Refer to the *UM10204 I²C-Bus Specification and User Manual*, Rev. 03—19 June 2007, when selecting pull-up resistor values to ensure proper operation.

Table 11. I²C Digital Input/Output

Parameter	Test Conditions	Limit[1] Min	Limit[1] Max	Unit
Digital Input				
Low Level Input Voltage (V_{IL})			$0.3 \times V_{DD\ I/O}$	V
High Level Input Voltage (V_{IH})		$0.7 \times V_{DD\ I/O}$		V
Low Level Input Current (I_{IL})	$V_{IN} = V_{DD\ I/O}$		0.1	µA
High Level Input Current (I_{IH})	$V_{IN} = 0$ V	−0.1		µA
Digital Output				
Low Level Output Voltage (V_{OL})	$V_{DD\ I/O} < 2$ V, $I_{OL} = 3$ mA		$0.2 \times V_{DD\ I/O}$	V
	$V_{DD\ I/O} \geq 2$ V, $I_{OL} = 3$ mA		400	mV
Low Level Output Current (I_{OL})	$V_{OL} = V_{OL,\ max}$	3		mA
Pin Capacitance	$f_{IN} = 1$ MHz, $V_{IN} = 2.5$ V		8	pF

[1] Limits based on characterization results; not production tested.

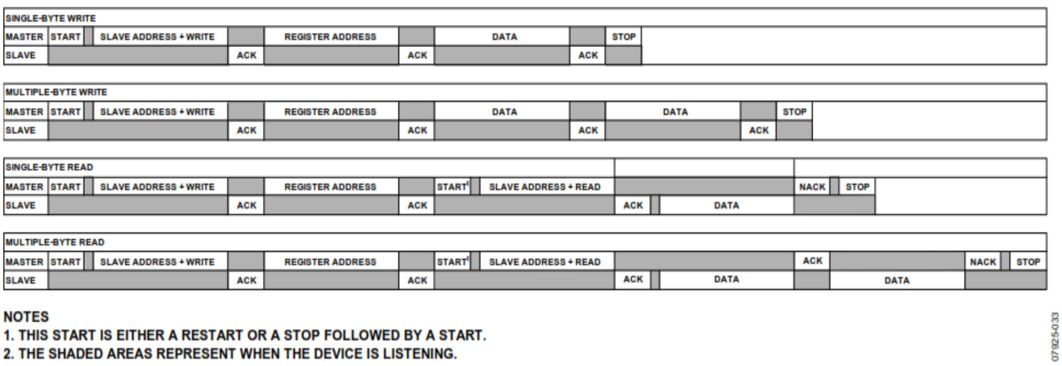


Figure 41. I²C Device Addressing

Table 12. I²C Timing ($T_A = 25°C$, $V_S = 2.5$ V, $V_{DD\ I/O} = 1.8$ V)

Parameter	Limit[1, 2] Min	Max	Unit	Description
f_{SCL}		400	kHz	SCL clock frequency
t_1	2.5		µs	SCL cycle time
t_2	0.6		µs	t_{HIGH}, SCL high time
t_3	1.3		µs	t_{LOW}, SCL low time
t_4	0.6		µs	$t_{HD, STA}$, start/repeated start condition hold time
t_5	100		ns	$t_{SU, DAT}$, data setup time
t_6[3, 4, 5, 6]	0	0.9	µs	$t_{HD, DAT}$, data hold time
t_7	0.6		µs	$t_{SU, STA}$, setup time for repeated start
t_8	0.6		µs	$t_{SU, STO}$, stop condition setup time
t_9	1.3		µs	t_{BUF}, bus-free time between a stop condition and a start condition
t_{10}		300	ns	t_R, rise time of both SCL and SDA when receiving
	0		ns	t_R, rise time of both SCL and SDA when receiving or transmitting
t_{11}		300	ns	t_F, fall time of SDA when receiving
		250	ns	t_F, fall time of both SCL and SDA when transmitting
C_b		400	pF	Capacitive load for each bus line

[1] Limits based on characterization results, with f_{SCL} = 400 kHz and a 3 mA sink current; not production tested.
[2] All values referred to the V_{IH} and the V_{IL} levels given in Table 11.
[3] t_6 is the data hold time that is measured from the falling edge of SCL. It applies to data in transmission and acknowledge.
[4] A transmitting device must internally provide an output hold time of at least 300 ns for the SDA signal (with respect to $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
[5] The maximum t_6 value must be met only if the device does not stretch the low period (t_3) of the SCL signal.
[6] The maximum value for t_6 is a function of the clock low time (t_3), the clock rise time (t_{10}), and the minimum data setup time ($t_{5(min)}$). This value is calculated as $t_{6(max)} = t_3 - t_{10} - t_{5(min)}$.

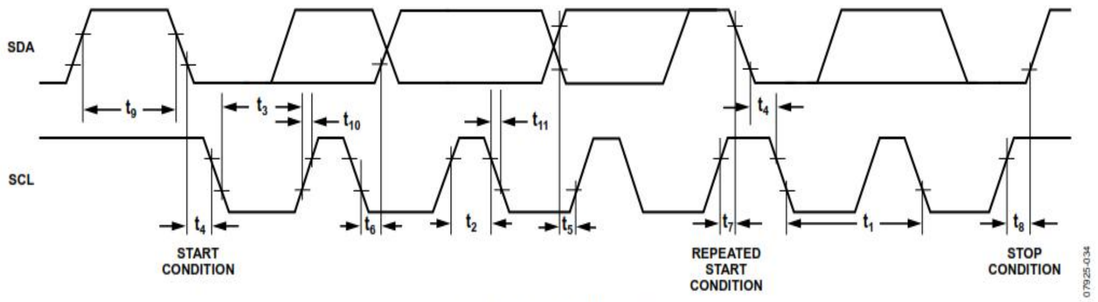


Figure 42. I²C Timing Diagram

REGISTER MAP

Table 19.

Address					
Hex	Dec	Name	Type	Reset Value	Description
0x00	0	DEVID	R	11100101	Device ID
0x01 to 0x1C	1 to 28	Reserved			Reserved; do not access
0x1D	29	THRESH_TAP	R/$\overline{W}$	00000000	Tap threshold
0x1E	30	OFSX	R/$\overline{W}$	00000000	X-axis offset
0x1F	31	OFSY	R/$\overline{W}$	00000000	Y-axis offset
0x20	32	OFSZ	R/$\overline{W}$	00000000	Z-axis offset
0x21	33	DUR	R/$\overline{W}$	00000000	Tap duration
0x22	34	Latent	R/$\overline{W}$	00000000	Tap latency
0x23	35	Window	R/$\overline{W}$	00000000	Tap window
0x24	36	THRESH_ACT	R/$\overline{W}$	00000000	Activity threshold
0x25	37	THRESH_INACT	R/$\overline{W}$	00000000	Inactivity threshold
0x26	38	TIME_INACT	R/$\overline{W}$	00000000	Inactivity time
0x27	39	ACT_INACT_CTL	R/$\overline{W}$	00000000	Axis enable control for activity and inactivity detection
0x28	40	THRESH_FF	R/$\overline{W}$	00000000	Free-fall threshold
0x29	41	TIME_FF	R/$\overline{W}$	00000000	Free-fall time
0x2A	42	TAP_AXES	R/$\overline{W}$	00000000	Axis control for single tap/double tap
0x2B	43	ACT_TAP_STATUS	R	00000000	Source of single tap/double tap
0x2C	44	BW_RATE	R/$\overline{W}$	00001010	Data rate and power mode control
0x2D	45	POWER_CTL	R/$\overline{W}$	00000000	Power-saving features control
0x2E	46	INT_ENABLE	R/$\overline{W}$	00000000	Interrupt enable control
0x2F	47	INT_MAP	R/$\overline{W}$	00000000	Interrupt mapping control
0x30	48	INT_SOURCE	R	00000010	Source of interrupts
0x31	49	DATA_FORMAT	R/$\overline{W}$	00000000	Data format control
0x32	50	DATAX0	R	00000000	X-Axis Data 0
0x33	51	DATAX1	R	00000000	X-Axis Data 1
0x34	52	DATAY0	R	00000000	Y-Axis Data 0
0x35	53	DATAY1	R	00000000	Y-Axis Data 1
0x36	54	DATAZ0	R	00000000	Z-Axis Data 0
0x37	55	DATAZ1	R	00000000	Z-Axis Data 1
0x38	56	FIFO_CTL	R/$\overline{W}$	00000000	FIFO control
0x39	57	FIFO_STATUS	R	00000000	FIFO status

REGISTER DEFINITIONS

Register 0x00—DEVID (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	0	1	0	1

The DEVID register holds a fixed device ID code of 0xE5 (345 octal).

Register 0x1D—THRESH_TAP (Read/Write)

The THRESH_TAP register is eight bits and holds the threshold value for tap interrupts. The data format is unsigned, therefore, the magnitude of the tap event is compared with the value in THRESH_TAP for normal tap detection. The scale factor is 62.5 m*g*/LSB (that is, 0xFF = 16 *g*). A value of 0 may result in undesirable behavior if single tap/double tap interrupts are enabled.

Register 0x1E, Register 0x1F, Register 0x20—OFSX, OFSY, OFSZ (Read/Write)

The OFSX, OFSY, and OFSZ registers are each eight bits and offer user-set offset adjustments in twos complement format with a scale factor of 15.6 m*g*/LSB (that is, 0x7F = 2 *g*). The value stored in the offset registers is automatically added to the acceleration data, and the resulting value is stored in the output data registers. For additional information regarding offset calibration and the use of the offset registers, refer to the Offset Calibration section.

Register 0x21—DUR (Read/Write)

The DUR register is eight bits and contains an unsigned time value representing the maximum time that an event must be above the THRESH_TAP threshold to qualify as a tap event. The scale factor is 625 µs/LSB. A value of 0 disables the single tap/ double tap functions.

Register 0x22—Latent (Read/Write)

The latent register is eight bits and contains an unsigned time value representing the wait time from the detection of a tap event to the start of the time window (defined by the window register) during which a possible second tap event can be detected. The scale factor is 1.25 ms/LSB. A value of 0 disables the double tap function.

Register 0x23—Window (Read/Write)

The window register is eight bits and contains an unsigned time value representing the amount of time after the expiration of the latency time (determined by the latent register) during which a second valid tap can begin. The scale factor is 1.25 ms/LSB. A value of 0 disables the double tap function.

Register 0x24—THRESH_ACT (Read/Write)

The THRESH_ACT register is eight bits and holds the threshold value for detecting activity. The data format is unsigned, so the magnitude of the activity event is compared with the value in the THRESH_ACT register. The scale factor is 62.5 m*g*/LSB. A value of 0 may result in undesirable behavior if the activity interrupt is enabled.

Register 0x25—THRESH_INACT (Read/Write)

The THRESH_INACT register is eight bits and holds the threshold value for detecting inactivity. The data format is unsigned, so the magnitude of the inactivity event is compared with the value in the THRESH_INACT register. The scale factor is 62.5 m*g*/LSB. A value of 0 may result in undesirable behavior if the inactivity interrupt is enabled.

Register 0x26—TIME_INACT (Read/Write)

The TIME_INACT register is eight bits and contains an unsigned time value representing the amount of time that acceleration must be less than the value in the THRESH_INACT register for inactivity to be declared. The scale factor is 1 sec/LSB. Unlike the other interrupt functions, which use unfiltered data (see the Threshold section), the inactivity function uses filtered output data. At least one output sample must be generated for the inactivity interrupt to be triggered. This results in the function appearing unresponsive if the TIME_INACT register is set to a value less than the time constant of the output data rate. A value of 0 results in an interrupt when the output data is less than the value in the THRESH_INACT register.

Register 0x27—ACT_INACT_CTL (Read/Write)

D7	D6	D5	D4
ACT ac/dc	ACT_X enable	ACT_Y enable	ACT_Z enable
D3	**D2**	**D1**	**D0**
INACT ac/dc	INACT_X enable	INACT_Y enable	INACT_Z enable

ACT AC/DC and INACT AC/DC Bits

A setting of 0 selects dc-coupled operation, and a setting of 1 enables ac-coupled operation. In dc-coupled operation, the current acceleration magnitude is compared directly with THRESH_ACT and THRESH_INACT to determine whether activity or inactivity is detected.

In ac-coupled operation for activity detection, the acceleration value at the start of activity detection is taken as a reference value. New samples of acceleration are then compared to this reference value, and if the magnitude of the difference exceeds the THRESH_ACT value, the device triggers an activity interrupt.

Similarly, in ac-coupled operation for inactivity detection, a reference value is used for comparison and is updated whenever the device exceeds the inactivity threshold. After the reference value is selected, the device compares the magnitude of the difference between the reference value and the current acceleration with THRESH_INACT. If the difference is less than the value in THRESH_INACT for the time in TIME_INACT, the device is considered inactive and the inactivity interrupt is triggered.

ACT_x Enable Bits and INACT_x Enable Bits

A setting of 1 enables x-, y-, or z-axis participation in detecting activity or inactivity. A setting of 0 excludes the selected axis from participation. If all axes are excluded, the function is disabled. For activity detection, all participating axes are logically OR'ed, causing the activity function to trigger when any of the participating axes exceeds the threshold. For inactivity detection, all participating axes are logically AND'ed, causing the inactivity function to trigger only if all participating axes are below the threshold for the specified time.

Register 0x28—THRESH_FF (Read/Write)

The THRESH_FF register is eight bits and holds the threshold value, in unsigned format, for free-fall detection. The acceleration on all axes is compared with the value in THRESH_FF to determine if a free-fall event occurred. The scale factor is 62.5 m*g*/LSB. Note that a value of 0 m*g* may result in undesirable behavior if the free-fall interrupt is enabled. Values between 300 m*g* and 600 m*g* (0x05 to 0x09) are recommended.

Register 0x29—TIME_FF (Read/Write)

The TIME_FF register is eight bits and stores an unsigned time value representing the minimum time that the value of all axes must be less than THRESH_FF to generate a free-fall interrupt. The scale factor is 5 ms/LSB. A value of 0 may result in undesirable behavior if the free-fall interrupt is enabled. Values between 100 ms and 350 ms (0x14 to 0x46) are recommended.

Register 0x2A—TAP_AXES (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	Suppress	TAP_X enable	TAP_Y enable	TAP_Z enable

Suppress Bit

Setting the suppress bit suppresses double tap detection if acceleration greater than the value in THRESH_TAP is present between taps. See the Tap Detection section for more details.

TAP_x Enable Bits

A setting of 1 in the TAP_X enable, TAP_Y enable, or TAP_Z enable bit enables x-, y-, or z-axis participation in tap detection. A setting of 0 excludes the selected axis from participation in tap detection.

Register 0x2B—ACT_TAP_STATUS (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
0	ACT_X source	ACT_Y source	ACT_Z source	Asleep	TAP_X source	TAP_Y source	TAP_Z source

ACT_x Source and TAP_x Source Bits

These bits indicate the first axis involved in a tap or activity event. A setting of 1 corresponds to involvement in the event, and a setting of 0 corresponds to no involvement. When new data is available, these bits are not cleared but are overwritten by the new data. The ACT_TAP_STATUS register should be read before clearing the interrupt. Disabling an axis from participation clears the corresponding source bit when the next activity or single tap/double tap event occurs.

Asleep Bit

A setting of 1 in the asleep bit indicates that the part is asleep, and a setting of 0 indicates that the part is not asleep. This bit toggles only if the device is configured for auto sleep. See the AUTO_SLEEP Bit section for more information on autosleep mode.

Register 0x2C—BW_RATE (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	LOW_POWER	Rate			

LOW_POWER Bit

A setting of 0 in the LOW_POWER bit selects normal operation, and a setting of 1 selects reduced power operation, which has somewhat higher noise (see the Power Modes section for details).

Rate Bits

These bits select the device bandwidth and output data rate (see Table 7 and Table 8 for details). The default value is 0x0A, which translates to a 100 Hz output data rate. An output data rate should be selected that is appropriate for the communication protocol and frequency selected. Selecting too high of an output data rate with a low communication speed results in samples being discarded.

Register 0x2D—POWER_CTL (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	Link	AUTO_SLEEP	Measure	Sleep	Wakeup	

Link Bit

A setting of 1 in the link bit with both the activity and inactivity functions enabled delays the start of the activity function until inactivity is detected. After activity is detected, inactivity detection begins, preventing the detection of activity. This bit serially links the activity and inactivity functions. When this bit is set to 0, the inactivity and activity functions are concurrent. Additional information can be found in the Link Mode section.

When clearing the link bit, it is recommended that the part be placed into standby mode and then set back to measurement mode with a subsequent write. This is done to ensure that the device is properly biased if sleep mode is manually disabled; otherwise, the first few samples of data after the link bit is cleared may have additional noise, especially if the device was asleep when the bit was cleared.

AUTO_SLEEP Bit

If the link bit is set, a setting of 1 in the AUTO_SLEEP bit enables the auto-sleep functionality. In this mode, the ADXL345 automatically switches to sleep mode if the inactivity function is enabled and inactivity is detected (that is, when acceleration is below the THRESH_INACT value for at least the time indicated by TIME_INACT). If activity is also enabled, the ADXL345 automatically wakes up from sleep after detecting activity and returns to operation at the output data rate set in the BW_RATE register. A setting of 0 in the AUTO_SLEEP bit disables automatic switching to sleep mode. See the description of the Sleep Bit in this section for more information on sleep mode.

If the link bit is not set, the AUTO_SLEEP feature is disabled and setting the AUTO_SLEEP bit does not have an impact on device operation. Refer to the Link Bit section or the Link Mode section for more information on utilization of the link feature.

When clearing the AUTO_SLEEP bit, it is recommended that the part be placed into standby mode and then set back to measurement mode with a subsequent write. This is done to ensure that the device is properly biased if sleep mode is manually disabled; otherwise, the first few samples of data after the AUTO_SLEEP bit is cleared may have additional noise, especially if the device was asleep when the bit was cleared.

Measure Bit

A setting of 0 in the measure bit places the part into standby mode, and a setting of 1 places the part into measurement mode. The ADXL345 powers up in standby mode with minimum power consumption.

Sleep Bit

A setting of 0 in the sleep bit puts the part into the normal mode of operation, and a setting of 1 places the part into sleep mode. Sleep mode suppresses DATA_READY, stops transmission of data to FIFO, and switches the sampling rate to one specified by the wakeup bits. In sleep mode, only the activity function can be used. When the DATA_READY interrupt is suppressed, the output data registers (Register 0x32 to Register 0x37) are still updated at the sampling rate set by the wakeup bits (D1:D0).

When clearing the sleep bit, it is recommended that the part be placed into standby mode and then set back to measurement mode with a subsequent write. This is done to ensure that the device is properly biased if sleep mode is manually disabled; otherwise, the first few samples of data after the sleep bit is cleared may have additional noise, especially if the device was asleep when the bit was cleared.

Wakeup Bits

These bits control the frequency of readings in sleep mode as described in Table 20.

Table 20. Frequency of Readings in Sleep Mode

Setting		
D1	D0	Frequency (Hz)
0	0	8
0	1	4
1	0	2
1	1	1

Register 0x2E—INT_ENABLE (Read/Write)

D7	D6	D5	D4
DATA_READY	SINGLE_TAP	DOUBLE_TAP	Activity
D3	**D2**	**D1**	**D0**
Inactivity	FREE_FALL	Watermark	Overrun

Setting bits in this register to a value of 1 enables their respective functions to generate interrupts, whereas a value of 0 prevents the functions from generating interrupts. The DATA_READY, watermark, and overrun bits enable only the interrupt output; the functions are always enabled. It is recommended that interrupts be configured before enabling their outputs.

Register 0x2F—INT_MAP (R/$\overline{W}$)

D7	D6	D5	D4
DATA_READY	SINGLE_TAP	DOUBLE_TAP	Activity
D3	**D2**	**D1**	**D0**
Inactivity	FREE_FALL	Watermark	Overrun

Any bits set to 0 in this register send their respective interrupts to the INT1 pin, whereas bits set to 1 send their respective interrupts to the INT2 pin. All selected interrupts for a given pin are OR'ed.

Register 0x30—INT_SOURCE (Read Only)

D7	D6	D5	D4
DATA_READY	SINGLE_TAP	DOUBLE_TAP	Activity
D3	**D2**	**D1**	**D0**
Inactivity	FREE_FALL	Watermark	Overrun

Bits set to 1 in this register indicate that their respective functions have triggered an event, whereas a value of 0 indicates that the corresponding event has not occurred. The DATA_READY, watermark, and overrun bits are always set if the corresponding events occur, regardless of the INT_ENABLE register settings, and are cleared by reading data from the DATAX, DATAY, and DATAZ registers. The DATA_READY and watermark bits may require multiple reads, as indicated in the FIFO mode descriptions in the FIFO section. Other bits, and the corresponding interrupts, are cleared by reading the INT_SOURCE register.

Register 0x31—DATA_FORMAT (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
SELF_TEST	SPI	INT_INVERT	0	FULL_RES	Justify	Range	

The DATA_FORMAT register controls the presentation of data to Register 0x32 through Register 0x37. All data, except that for the ±16 *g* range, must be clipped to avoid rollover.

SELF_TEST Bit

A setting of 1 in the SELF_TEST bit applies a self-test force to the sensor, causing a shift in the output data. A value of 0 disables the self-test force.

SPI Bit

A value of 1 in the SPI bit sets the device to 3-wire SPI mode, and a value of 0 sets the device to 4-wire SPI mode.

INT_INVERT Bit

A value of 0 in the INT_INVERT bit sets the interrupts to active high, and a value of 1 sets the interrupts to active low.

FULL_RES Bit

When this bit is set to a value of 1, the device is in full resolution mode, where the output resolution increases with the *g* range set by the range bits to maintain a 4 mg/LSB scale factor. When the FULL_RES bit is set to 0, the device is in 10-bit mode, and the range bits determine the maximum *g* range and scale factor.

Justify Bit

A setting of 1 in the justify bit selects left-justified (MSB) mode, and a setting of 0 selects right-justified mode with sign extension.

Range Bits

These bits set the *g* range as described in Table 21.

Table 21. *g* Range Setting

Setting		
D1	D0	*g* Range
0	0	±2 *g*
0	1	±4 *g*
1	0	±8 *g*
1	1	±16 *g*

Register 0x32 to Register 0x37—DATAX0, DATAX1, DATAY0, DATAY1, DATAZ0, DATAZ1 (Read Only)

These six bytes (Register 0x32 to Register 0x37) are eight bits each and hold the output data for each axis. Register 0x32 and Register 0x33 hold the output data for the x-axis, Register 0x34 and Register 0x35 hold the output data for the y-axis, and Register 0x36 and Register 0x37 hold the output data for the z-axis. The output data is twos complement, with DATAx0 as the least significant byte and DATAx1 as the most significant byte, where x represent X, Y, or Z. The DATA_FORMAT register (Address 0x31) controls the format of the data. It is recommended that a multiple-byte read of all registers be performed to prevent a change in data between reads of sequential registers.

Register 0x38—FIFO_CTL (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
FIFO_MODE		Trigger	Samples				

FIFO_MODE Bits

These bits set the FIFO mode, as described in Table 22.

Table 22. FIFO Modes

Setting			
D7	D6	Mode	Function
0	0	Bypass	FIFO is bypassed.
0	1	FIFO	FIFO collects up to 32 values and then stops collecting data, collecting new data only when FIFO is not full.
1	0	Stream	FIFO holds the last 32 data values. When FIFO is full, the oldest data is overwritten with newer data.
1	1	Trigger	When triggered by the trigger bit, FIFO holds the last data samples before the trigger event and then continues to collect data until full. New data is collected only when FIFO is not full.

Trigger Bit

A value of 0 in the trigger bit links the trigger event of trigger mode to INT1, and a value of 1 links the trigger event to INT2.

Samples Bits

The function of these bits depends on the FIFO mode selected (see Table 23). Entering a value of 0 in the samples bits immediately sets the watermark status bit in the INT_SOURCE register, regardless of which FIFO mode is selected. Undesirable operation may occur if a value of 0 is used for the samples bits when trigger mode is used.

Table 23. Samples Bits Functions

FIFO Mode	Samples Bits Function
Bypass	None.
FIFO	Specifies how many FIFO entries are needed to trigger a watermark interrupt.
Stream	Specifies how many FIFO entries are needed to trigger a watermark interrupt.
Trigger	Specifies how many FIFO samples are retained in the FIFO buffer before a trigger event.

0x39—FIFO_STATUS (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
FIFO_TRIG	0	Entries					

FIFO_TRIG Bit

A 1 in the FIFO_TRIG bit corresponds to a trigger event occurring, and a 0 means that a FIFO trigger event has not occurred.

Entries Bits

These bits report how many data values are stored in FIFO. Access to collect the data from FIFO is provided through the DATAX, DATAY, and DATAZ registers. FIFO reads must be done in burst or multiple-byte mode because each FIFO level is cleared after any read (single- or multiple-byte) of FIFO. FIFO stores a maximum of 32 entries, which equates to a maximum of 33 entries available at any given time because an additional entry is available at the output filter of the device.

AXES OF ACCELERATION SENSITIVITY

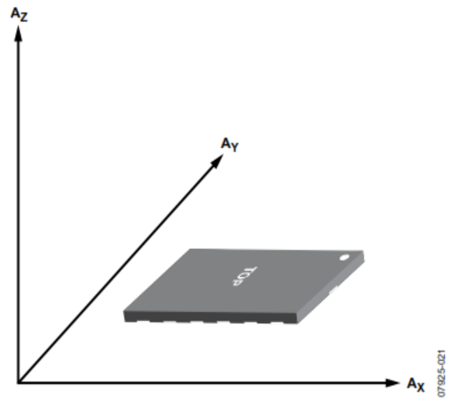


Figure 57. Axes of Acceleration Sensitivity (Corresponding Output Voltage Increases When Accelerated Along the Sensitive Axis)

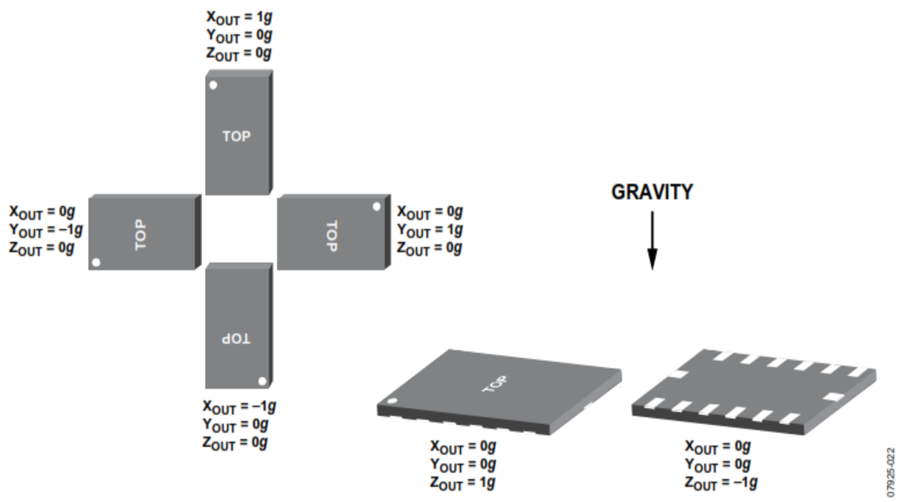


Figure 58. Output Response vs. Orientation to Gravity

APPENDIX 2

2 SIM900A Overview

Designed for global market, SIM900A is a dual-band GSM/GPRS engine that works on frequencies EGSM 900MHz and DCS 1800MHz. SIM900A features GPRS multi-slot class 10/ class 8 (optional) and supports the GPRS coding schemes CS-1, CS-2, CS-3 and CS-4.

With a tiny configuration of 24mm x 24mm x 3mm, SIM900A can meet almost all the space requirements in your applications, such as M2M, smart phone, PDA and other mobile devices.

The physical interface to the mobile application is a 68-pin SMT pad, which provides all hardware interfaces between the module and customers' boards.

- The keypad and SPI display interface will give you the flexibility to develop customized applications.
- Serial port and Debug port can help you easily develop your applications.
- One audio channel includes a microphone input and a speaker output.
- Programmable General Purpose Input & Output.

The SIM900A is designed with power saving technique so that the current consumption is as low as 1.5mA in SLEEP mode.

The SIM900A is integrated with the TCP/IP protocol; extended TCP/IP AT commands are developed for customers to use the TCP/IP protocol easily, which is very useful for those data transfer applications.

2.1 SIM900A Key Features

Table 3: SIM900A key features

Feature	Implementation
Power supply	Single supply voltage 3.4V – 4.5V
Power saving	Typical power consumption in SLEEP mode is 1.5mA (BS-PA-MFRMS=5)
Frequency Bands	● SIM900A Dual-band: EGSM900, DCS1800. The SIM900A can search the 2 frequency bands automatically. The frequency bands also can be set by AT command. ● Compliant to GSM Phase 2/2+
GSM class	Small MS
Transmitting power	● Class 4 (2W) at EGSM 900 ● Class 1 (1W) at DCS 1800
GPRS connectivity	● GPRS multi-slot class 10 （default） ● GPRS multi-slot class 8 (option) ● GPRS mobile station class B

Temperature range	● Normal operation: -30°C to +80°C ● Restricted operation: -40°C to -30°C and +80 °C to +85°C[1] ● Storage temperature -45°C to +90°C
DATA *GPRS:* *CSD:*	● GPRS data downlink transfer: max. 85.6 kbps ● GPRS data uplink transfer: max. 42.8 kbps ● Coding scheme: CS-1, CS-2, CS-3 and CS-4 ● Supports the protocols PAP (Password Authentication Protocol) usually used for PPP connections. ● Integrates the TCP/IP protocol. ● Support Packet Switched Broadcast Control Channel (PBCCH) ● CSD transmission rates: 2.4, 4.8, 9.6, 14.4 kbps, non-transparent ● Unstructured Supplementary Services Data (USSD) support
SMS	● MT, MO, CB, Text and PDU mode ● SMS storage: SIM card
FAX	Group 3 Class 1
SIM interface	Support SIM card: 1.8V, 3V
External antenna	Antenna pad
Audio features	Speech codec modes: ● Half Rate (ETS 06.20) ● Full Rate (ETS 06.10) ● Enhanced Full Rate (ETS 06.50 / 06.60 / 06.80) ● Adaptive multi rate (AMR) ● Echo Cancellation ● Noise Suppression
Serial port and Debug port	Serial Port: ● 8-wire modem interface with status and control lines, unbalanced, asynchronous. ● 1.2kbps to 115.2kbps. ● Serial Port can be used for AT commands or data stream. ● Supports RTS/CTS hardware handshake and software ON/OFF flow control. ● Multiplex ability according to GSM 07.10 Multiplexer Protocol. ● Autobauding supports baud rate from 1200 bps to 115200bps. Debug port: ● 2-wire null modem interface DBG_TXD and DBG_RXD. ● Can be used for debugging and upgrading firmware.
Phonebook management	Support phonebook types: SM, FD, LD, RC, ON, MC.
SIM Application Toolkit	Support SAT class 3, GSM 11.14 Release 99
Real time clock	Implemented
Timer function	Programmable via AT command
Physical characteristics	Size: 24mm x 24mm x 3mm Weight: 3.4g
Firmware upgrade	Firmware upgrade by debug port.

(1) The SIM900A does work, but deviations from the GSM specification may occur.

Table 4: Coding schemes and maximum net data rates over air interface

Coding scheme	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	9.05kbps	18.1kbps	36.2kbps
CS-2:	13.4kbps	26.8kbps	53.6kbps
CS-3:	15.6kbps	31.2kbps	62.4kbps
CS-4:	21.4kbps	42.8kbps	85.6kbps

2.2 SIM900A Functional Diagram

The following figure shows a functional diagram of the SIM900A and illustrates the mainly functional part:

- The GSM baseband engine
- Flash and SRAM
- The GSM radio frequency part
- The antenna interface
- The Other interfaces

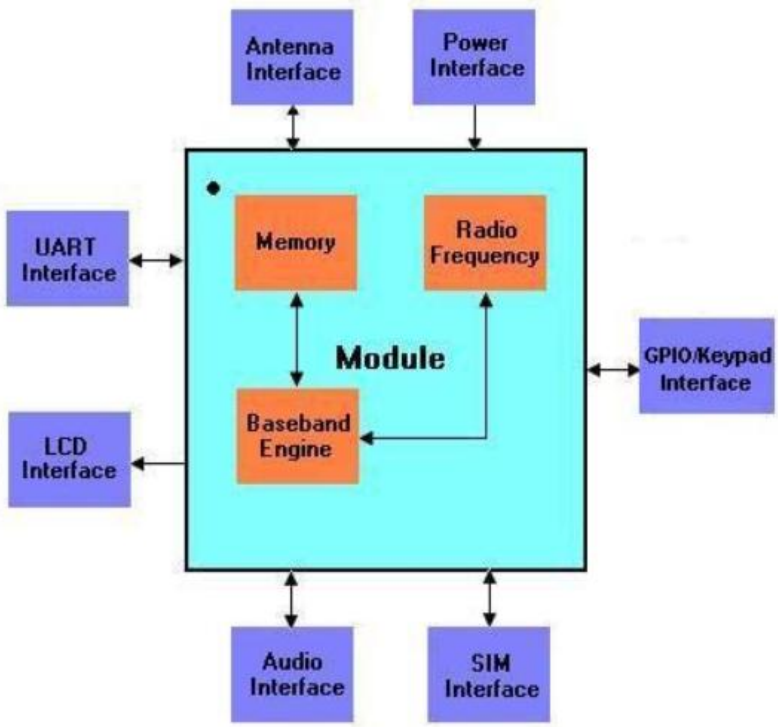


Figure 1: SIM900A functional diagram

3.8 Serial Interfaces

Table 7: Pin definition of the serial interfaces

	Name	Pin	Function
Serial port	DTR	3	Data terminal ready
	RI	4	Ring indicator
	DCD	5	Data carrier detection
	DSR	6	Date set ready
	CTS	7	Clear to send
	RTS	8	Request to send
	TXD	9	Transmit data
	RXD	10	Receive data
Debug port	DBG_RXD	28	Receive data
	DBG_TXD	27	Transmit data

SIM900A provides two unbalanced asynchronous serial ports. One is the serial port and the other is the debug port. The GSM module is designed as a DCE (Data Communication Equipment), following the traditional DCE-DTE (Data Terminal Equipment) connection. The module and the client (DTE) are connected through the following signal (as following figure shows). Autobauding supports baud rate from 1200bps to 115200bps.

Serial port

- TXD: Send data to the RXD signal line of the DTE
- RXD: Receive data from the TXD signal line of the DTE

Debug port

- DBG_TXD: Send data to the RXD signal line of the DTE
- DBG_RXD: Receive data from the TXD signal line of the DTE

The logic levels are described in following table.

Table 8: Logic levels of the serial port and debug port

Parameter	Min	Max	Unit
V_{IL}	0	0.15*VDD_EXT	V
V_{IH}	0.85 *VDD_EXT	VDD_EXT	V
V_{OL}	0	0.1	V
V_{OH}	VDD_EXT -0.1	VDD_EXT	V

6.3 PIN Assignment of SIM900A

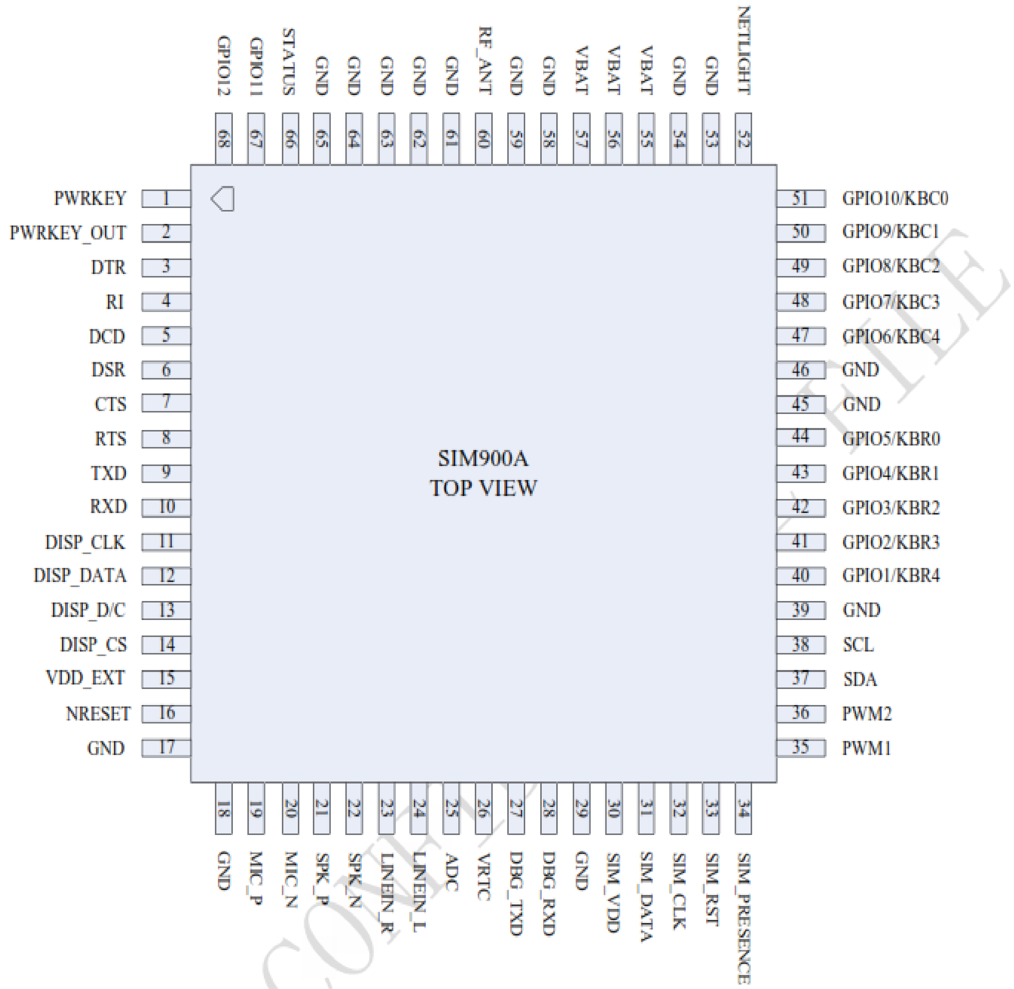


Figure 41: SIM900A pin out diagram (Top View)

Table 31: PIN assignment

Pin Number	Pin Name	Pin Number	Pin Name
1	PWRKEY	**35**	PMW1
2	PWRKEY_OUT	**36**	PWM2
3	DTR	**37**	SDA
4	RI	**38**	SCL
5	DCD	**39**	GND
6	DSR	**40**	GPIO1/KBR4
7	CTS	**41**	GPIO2/KBR3
8	RTS	**42**	GPIO3/KBR2
9	TXD	**43**	GPIO4/KBR1

10	RXD	**44**	GPIO5/KBR0
11	DISP_CLK	**45**	GND
12	DISP_DATA	**46**	GND
13	DISP_D/C	**47**	GPIO6/KBC4
14	DISP_CS	**48**	GPIO7/KBC3
15	VDD_EXT	**49**	GPIO8/KBC2
16	NRESET	**50**	GPIO9/KBC1
17	GND	**51**	GPIO10/KBC0
18	GND	**52**	NETLIGHT
19	MIC_P	**53**	GND
20	MIC_N	**54**	GND
21	SPK_P	**55**	VBAT
22	SPK_N	**56**	VBAT
23	LINEIN_R	**57**	VBAT
24	LINEIN_L	**58**	GND
25	ADC	**59**	GND
26	VRTC	**60**	RF_ANT
27	DBG_TXD	**61**	GND
28	DBG_RXD	**62**	GND
29	GND	**63**	GND
30	SIM_VDD	**64**	GND
31	SIM_DATA	**65**	GND
32	SIM_CLK	**66**	STATUS
33	SIM_RST	**67**	GPIO11
34	SIM_PRESENCE	**68**	GPIO12

APPENDIX 3

1 Functional description

1.1 Overview

The u-blox PAM-7Q patch antenna module has the exceptional performance of the u-blox 7 engine and delivers high sensitivity and minimal acquisition times in an industry proven form factor.

Incorporating the PAM-7Q into customer designs is simple and straightforward, thanks to the embedded antenna, low power consumption, simple interface, and sophisticated interference suppression that ensures maximum performance even in GPS hostile environments.

The 18 x 18 mm patch antenna of PAM-7Q provides RHCP polarization, which is not achievable with smaller patch antenna elements. The simple design and easy interfacing keeps installation costs to a minimum.

PAM-7Q targets industrial and consumer applications that require small and cost efficient smart antenna solutions. It is form-factor compatible with the UP501 module, allowing the upgrade of existing designs with minimal effort.

PAM-7Q modules use u-blox 7 GPS chips qualified according to AEC-Q100 and are manufactured in ISO/TS 16949 certified sites. Qualification tests are performed as stipulated in the ISO16750 standard: "Road vehicles – Environmental conditions and testing for electrical and electronic equipment". PAM-7Q complies with green / halogen-free standards.

1.2 Product features

Model	Type								Supply		Interfaces				Features											Grade		
	GPS / QZSS	GLONASS	Galileo	BeiDou	Timing	Dead Reckoning	Precise Point Positioning	Raw Data	2.7 V – 3.6 V	Lowest power (DC/DC)	UART	USB	SPI	DDC (I²C compliant)	Programmable (Flash)	Data logger	Additional SAW	Additional LNA	RTC crystal	Internal oscillator	Active antenna / LNA supply	Active antenna / LNA control	Antenna short circuit detection / protection pin	Antenna open circuit detection pin	Frequency output	Standard	Professional	Automotive
PAM-7Q	•								•	•	•			•			•	•	•	T							■	

T = TCXO

1.3 GPS performance

Parameter	Specification	
Receiver type	56 Channels GPS L1C/A SBAS L1C/A QZSS L1C/A	
Time-To-First-Fix[1]		
	Cold Start	29 s
	Warm Start	28 s
	Hot Start	1 s
	Aided Starts[2]	5 s
Sensitivity[3]		
	Tracking & Navigation	–161 dBm
	Reacquisition	–159 dBm
	Cold Start	–147 dBm
	Warm Start	–147 dBm
	Hot Start	–155 dBm
Horizontal position accuracy[4]	Autonomous	2.5 m
	SBAS	2.0 m
Accuracy of time pulse signal	RMS 99%	30 ns 60 ns
Frequency of time pulse signal		0.25 Hz … 1 kHz (configurable)
Max navigation update rate		10 Hz
Velocity accuracy[5]		0.1 m/s
Heading accuracy[5]		0.5 degrees
Operational limits[6]	Dynamics Altitude Velocity	≤ 4 g 50,000 m 500 m/s

Table 1: GPS performance of PAM-7Q

[1] All satellites at -130 dBm
[2] Dependent on aiding data connection speed and latency
[3] Measured conducted without antenna
[4] CEP, 50%, 24 hours static, -130 dBm, > 6 SVs
[5] 50% @ 30 m/s
[6] Assuming Airborne < 4 g platform

1.9.1 UART

PAM-7Q modules include one UART interface, which can be used for communication to a host. It supports configurable baud rates. For supported baud rates see the *u-blox 7 Receiver Description Including Protocol Specification* [1].

1.9.2 Display Data Channel (DDC)

An I^2C compliant DDC interface is available for communication with an external host CPU. The interface can be operated in slave mode only. The DDC protocol and electrical interface are fully compatible with the Fast-Mode of the I^2C industry standard. Since the maximum SCL clock frequency is 400 kHz, the maximum transfer rate is 400 kb/s.

The DDC interface is I^2C Fast Mode compliant. For timing parameters consult the I^2C standard.

☞ The maximum bit rate is 400 kb/s. The interface stretches the clock when slowed down while serving interrupts, so real bit rates may be slightly lower.

1.10 Clock generation

1.10.1 Oscillators

PAM-7Q GPS modules are available in TCXO version. TCXO option allows accelerated weak signal acquisition, enabling faster start and reacquisition times.

1.10.2 Real-Time Clock (RTC)

The RTC is driven by a 32 kHz oscillator, which makes use of an external RTC crystal. If the main supply voltage fails and a battery is connected to V_BCKP, parts of the receiver switch off, but the RTC still runs providing a timing reference for the receiver. This operating mode is called Hardware Backup Mode, which enables all relevant data to be saved in the backup RAM to allow a hot or warm start later.

1.11 Power management

u-blox PAM-7Q technology offers a power optimized architecture with built-in autonomous power saving functions to minimize power consumption at any given time. Furthermore, the receiver can be used in two operating modes: Continuous mode for best performance or Power Save Mode for optimized power consumption respectively. In addition a high efficiency DC/DC converter is integrated to allow low power consumption even for higher main supply voltages.

1.11.1 DC/DC converter

PAM-7Q modules integrate a DC/DC converter, allowing reduced power consumption by up to 50% especially when using a main supply voltage above 2.5 V.

☞ For more information see the *PAM-7Q Hardware Integration Manual* [2].

1.11.2 Operating modes

PAM-7Q modules have two operating modes:

- Continuous Mode for best GPS performance
- Power Save Mode to optimize power consumption

1.11.2.1 Continuous Mode

Continuous Mode uses the acquisition engine at full performance resulting in the shortest possible TTFF and the highest sensitivity. It searches for all possible satellites until the almanac is completely downloaded. The receiver then switches to the tracking engine to lower power consumption.

Thus, a lower tracking current consumption level will be achieved when:

- A valid GPS position is obtained
- The entire almanac has been downloaded
- The ephemeris for each satellite in view is valid

1.11.2.2 Power Save Mode

For power sensitive applications u-blox PAM-7Q receivers provide a Power Save Mode for reduced power consumption.

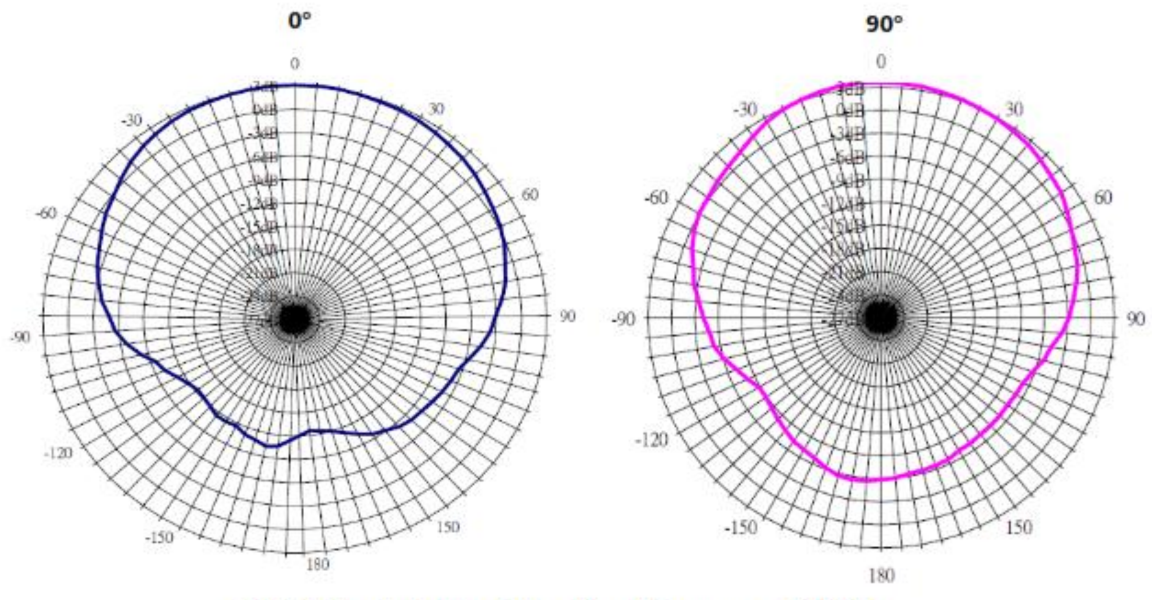
Power Save Mode provides two dedicated methods called ON/OFF and Cyclic tracking, that reduce average current consumption in different ways to match the needs of the specific application. These options can be set by using a specific UBX message.

☞ For more information about power management strategies, see the *u-blox 7 Receiver Description Including Protocol Specification* [1].

1.12 Antenna

PAM-7Q modules are designed with integrated 18 x 18 mm patch antenna provides RHCP polarization. PAM-7Q antenna modules are relatively wideband and tuned a few MHz above L1, customer housing (plastic) usually will de-tune center frequency back to L1.

Figure 2 illustrates the normalized patch antenna gain for PAM-7Q.



TX: Right hand circular polarized signal Frequency = 1580MHz

Radiation Pattern (with 50mm square ground plane)

Figure 2: The Normalized Antenna Gain Chart (For Example: 1580MHz)

☞ In order to maintain good performance for the on-board patch antenna of the PAM-7Q, some design rules should be followed. For more information see the *PAM-7Q Hardware Integration Manual* [2].

2 Pin Definition

2.1 Pin assignment

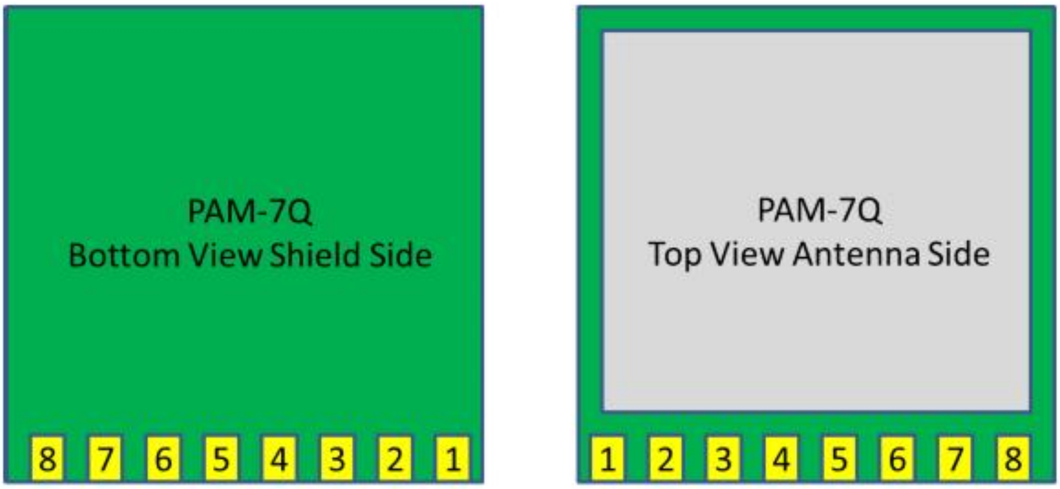


Figure 3: Pin Assignment of PAM-7Q

No	Name	I/O	Description
1	RXD	I	Serial Port
2	TXD	O	Serial Port
3	GND		Ground
4	VCC		Supply voltage
5	V_BCKP		Backup voltage supply
6	TIMEPULSE	O	Time pulse (1PPS)
7	SDA	I/O	DDC Data
8	SCL	I/O	DDC Clock

Table 3: Pinout for PAM-7Q

For more information about Pinouts see the *PAM-7Q Hardware Integration Manual* [2].

4 Electrical specification

The limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to these limits for extended periods may affect device reliability.

Where application information is given, it is advisory only and does not form part of the specification. For more information see the *PAM-7Q Hardware Integration Manual* [2].

4.1 Absolute maximum rating

Parameter	Symbol	Module	Condition	Min	Max	Units
Power supply voltage	VCC	All		–0.5	3.6	V
Backup battery voltage	V_BCKP	All		–0.5	3.6	V
Input pin voltage	Vin	All		–0.5	3.6	V
DC current trough any digital I/O pin (except supplies)	Ipin				10	mA
Input power at RF_IN	Prfin	All	source impedance = 50 Ω, continuous wave[7]		13	dBm
Storage temperature	Tstg	All		–40	85	°C

Table 4: Absolute maximum ratings of PAM-7Q

Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection diodes.

[7] Measured conducted

4.2 Operating conditions

All specifications are at an ambient temperature of 25°C. Extreme operating temperatures can significantly impact specification values. Applications operating near the temperature limits should be tested to ensure the specification.

Parameter	Symbol	Min	Typ	Max	Units	Condition
Power supply voltage	VCC	+2.7	+3.0	+3.6	V	
Backup battery voltage	V_BCKP	+1.4		+3.6	V	
Backup battery current	I_BCKP		15		µA	V_BCKP = 3.0 V VCC = 0 V
SW backup current	I_SWBCKP		35		µA	VCC = 3.0 V
Input pin voltage range	Vin	0		VCC	V	
Digital IO Pin Low level input voltage	Vil	0		0.2*VCC	V	
Digital IO Pin High level input voltage	Vih	0.7*VCC		VCC+0.5V	V	
Digital IO Pin Low level output voltage	Vol			0.4	V	Iol = 4 mA
Digital IO Pin High level output voltage	Voh	VCC–0.4			V	Ioh = 4 mA
Receiver Chain Noise Figure	NFtot		2.0		dB	
Operating temperature	Topr	-40		+85	°C	

Table 5: Operating conditions

Operation beyond the specified operating conditions can affect device reliability.

4.3 Indicative power requirements

Table 6 lists examples of the total system supply current for a possible application.

Values in Table 6 are provided for customer information only, as an example of typical power requirements. Values are characterized on samples; actual power requirements can vary depending on FW version used, external circuitry, number of SVs tracked, signal strength, type of start as well as time, duration and conditions of test.

Parameter	Symbol	Min	Typ	Max	Units
Max. supply current[8]	Iccp			71	mA
Average supply current[9, 10]	Icc Acquisition[11]		26.0		mA
	Icc Tracking (Continuous mode)		21.5		mA
	Icc Tracking (Power Save mode / 1 Hz)		6.0		mA

Table 6: Indicative power requirements at 3.0 V

For more information about power requirements, see the *PAM-7Q Hardware Integration Manual* [2].

[8] Use this figure to dimension maximum current capability of power supply. Measurement of this parameter with 1 Hz bandwidth.
[9] Use this figure to determine required battery capacity.
[10] Simulated constellation of 8 satellites is used. All signals are at −130 dBm.
[11] Average current from start-up until the first fix.

APPENDIX 4

Atmel

ATmega48A/PA/88A/PA/168A/PA/328/P

ATMEL 8-BIT MICROCONTROLLER WITH 4/8/16/32KBYTES IN-SYSTEM PROGRAMMABLE FLASH

DATASHEET

Features

- High Performance, Low Power Atmel®AVR® 8-Bit Microcontroller Family
- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Throughput at 20MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory Segments
  - 4/8/16/32KBytes of In-System Self-Programmable Flash program memory
  - 256/512/512/1KBytes EEPROM
  - 512/1K/1K/2KBytes Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C[(1)]
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True Read-While-Write Operation
  - Programming Lock for Software Security
- Atmel® QTouch® library support
  - Capacitive touch buttons, sliders and wheels
  - QTouch and QMatrix® acquisition
  - Up to 64 sense channels
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Six PWM Channels
  - 8-channel 10-bit ADC in TQFP and QFN/MLF package
    - Temperature Measurement
  - 6-channel 10-bit ADC in PDIP Package
    - Temperature Measurement
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Byte-oriented 2-wire Serial Interface (Philips I^2C compatible)
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change

- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
- I/O and Packages
  - 23 Programmable I/O Lines
  - 28-pin PDIP, 32-lead TQFP, 28-pad QFN/MLF and 32-pad QFN/MLF
- Operating Voltage:
  - 1.8 - 5.5V
- Temperature Range:
  - -40°C to 85°C
- Speed Grade:
  - 0 - 4MHz@1.8 - 5.5V, 0 - 10MHz@2.7 - 5.5.V, 0 - 20MHz @ 4.5 - 5.5V
- Power Consumption at 1MHz, 1.8V, 25°C
  - Active Mode: 0.2mA
  - Power-down Mode: 0.1µA
  - Power-save Mode: 0.75µA (Including 32kHz RTC)

1. Pin Configurations

Figure 1-1. Pinout ATmega48A/PA/88A/PA/168A/PA/328/P

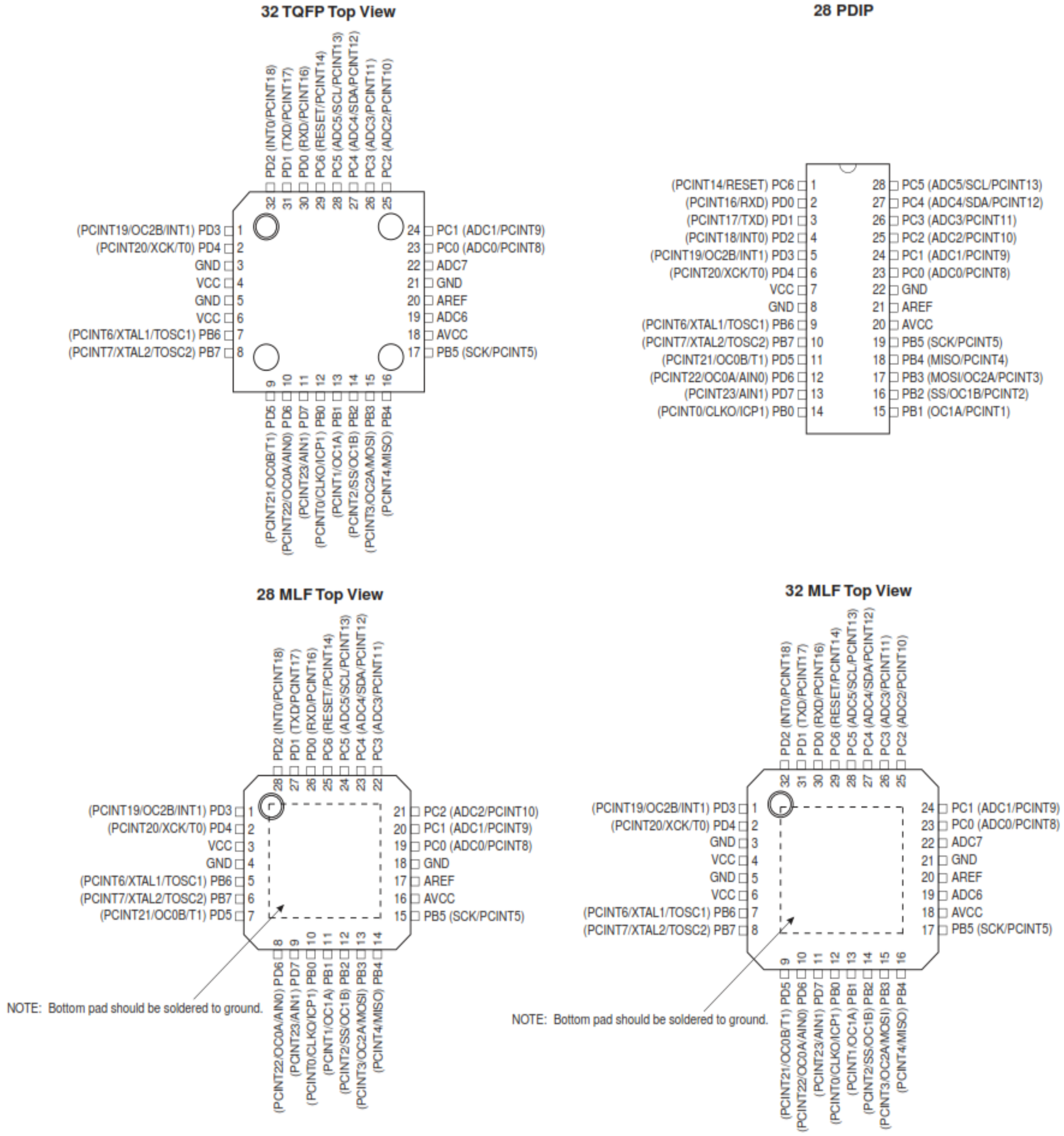


Table 1-1. 32UFBGA - Pinout ATmega48A/48PA/88A/88PA/168A/168PA

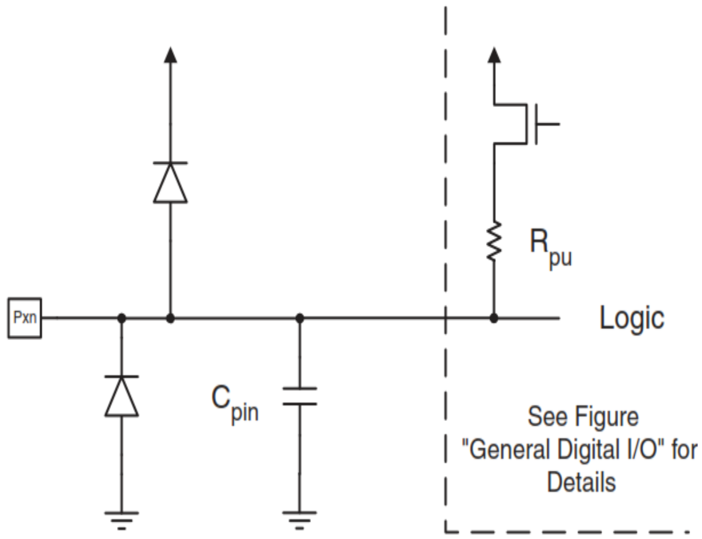
	1	2	3	4	5	6
A	PD2	PD1	PC6	PC4	PC2	PC1
B	PD3	PD4	PD0	PC5	PC3	PC0
C	GND	GND			ADC7	GND
D	VDD	VDD			AREF	ADC6
E	PB6	PD6	PB0	PB2	AVDD	PB5
F	PB7	PD5	PD7	PB1	PB3	PB4

14. I/O-Ports

14.1 Overview

All AVR ports have true Read-Modify-Write functionality when used as general digital I/O ports. This means that the direction of one port pin can be changed without unintentionally changing the direction of any other pin with the SBI and CBI instructions. The same applies when changing drive value (if configured as output) or enabling/disabling of pull-up resistors (if configured as input). Each output buffer has symmetrical drive characteristics with both high sink and source capability. The pin driver is strong enough to drive LED displays directly. All port pins have individually selectable pull-up resistors with a supply-voltage invariant resistance. All I/O pins have protection diodes to both V_{CC} and Ground as indicated in Figure 14-1. Refer to "Electrical Characteristics – (TA = -40°C to 85°C)" on page 299 for a complete list of parameters.

Figure 14-1. I/O Pin Equivalent Schematic



All registers and bit references in this section are written in general form. A lower case "x" represents the numbering letter for the port, and a lower case "n" represents the bit number. However, when using the register or bit defines in a program, the precise form must be used. For example, PORTB3 for bit no. 3 in Port B, here documented generally as PORTxn. The physical I/O Registers and bit locations are listed in "Register Description" on page 91.

Three I/O memory address locations are allocated for each port, one each for the Data Register – PORTx, Data Direction Register – DDRx, and the Port Input Pins – PINx. The Port Input Pins I/O location is read only, while the Data Register and the Data Direction Register are read/write. However, writing a logic one to a bit in the PINx Register, will result in a toggle in the corresponding bit in the Data Register. In addition, the Pull-up Disable – PUD bit in MCUCR disables the pull-up function for all pins in all ports when set.

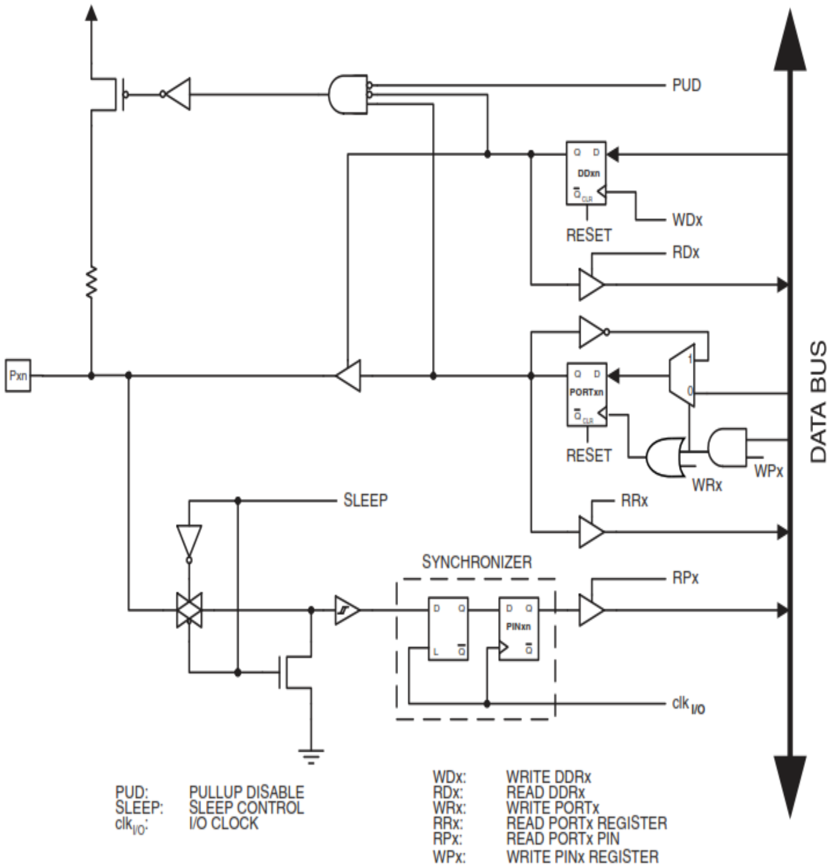
Using the I/O port as General Digital I/O is described in "Ports as General Digital I/O" on page 76. Most port pins are multiplexed with alternate functions for the peripheral features on the device. How each alternate function interferes with the port pin is described in "Alternate Port Functions" on page 80. Refer to the individual module sections for a full description of the alternate functions.

Note that enabling the alternate function of some of the port pins does not affect the use of the other pins in the port as general digital I/O.

14.2 Ports as General Digital I/O

The ports are bi-directional I/O ports with optional internal pull-ups. Figure 14-2 shows a functional description of one I/O-port pin, here generically called Pxn.

Figure 14-2. General Digital I/O[(1)]



Note: 1. WRx, WPx, WDx, RRx, RPx, and RDx are common to all pins within the same port. $clk_{I/O}$, SLEEP, and PUD are common to all ports.

14.2.1 Configuring the Pin

Each port pin consists of three register bits: DDxn, PORTxn, and PINxn. As shown in "Register Description" on page 91, the DDxn bits are accessed at the DDRx I/O address, the PORTxn bits at the PORTx I/O address, and the PINxn bits at the PINx I/O address.

The DDxn bit in the DDRx Register selects the direction of this pin. If DDxn is written logic one, Pxn is configured as an output pin. If DDxn is written logic zero, Pxn is configured as an input pin.

If PORTxn is written logic one when the pin is configured as an input pin, the pull-up resistor is activated. To switch the pull-up resistor off, PORTxn has to be written logic zero or the pin has to be configured as an output pin. The port pins are tri-stated when reset condition becomes active, even if no clocks are running.

If PORTxn is written logic one when the pin is configured as an output pin, the port pin is driven high (one). If PORTxn is written logic zero when the pin is configured as an output pin, the port pin is driven low (zero).

14.2.2 Toggling the Pin

Writing a logic one to PINxn toggles the value of PORTxn, independent on the value of DDRxn. Note that the SBI instruction can be used to toggle one single bit in a port.

20. USART0

20.1 Features

- **Full Duplex Operation (Independent Serial Receive and Transmit Registers)**
- **Asynchronous or Synchronous Operation**
- **Master or Slave Clocked Synchronous Operation**
- **High Resolution Baud Rate Generator**
- **Supports Serial Frames with 5, 6, 7, 8, or 9 Data Bits and 1 or 2 Stop Bits**
- **Odd or Even Parity Generation and Parity Check Supported by Hardware**
- **Data OverRun Detection**
- **Framing Error Detection**
- **Noise Filtering Includes False Start Bit Detection and Digital Low Pass Filter**
- **Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete**
- **Multi-processor Communication Mode**
- **Double Speed Asynchronous Communication Mode**

20.2 Overview

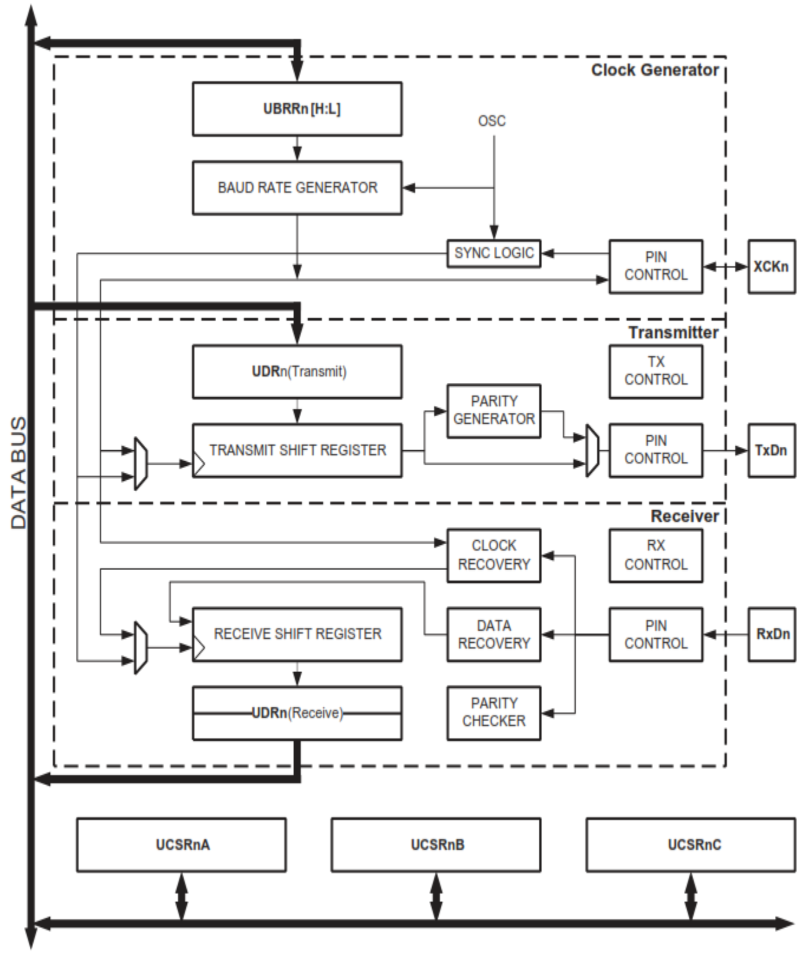
The Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device.

The USART0 can also be used in Master SPI mode, see "USART in SPI Mode" on page 196. The Power Reduction USART bit, PRUSART0, in "Minimizing Power Consumption" on page 42 must be disabled by writing a logical zero to it.

A simplified block diagram of the USART Transmitter is shown in Figure 20-1 on page 171. CPU accessible I/O Registers and I/O pins are shown in bold.

The dashed boxes in the block diagram separate the three main parts of the USART (listed from the top): Clock Generator, Transmitter and Receiver. Control Registers are shared by all units. The Clock Generation logic consists of synchronization logic for external clock input used by synchronous slave operation, and the baud rate generator. The XCKn (Transfer Clock) pin is only used by synchronous transfer mode. The Transmitter consists of a single write buffer, a serial Shift Register, Parity Generator and Control logic for handling different serial frame formats. The write buffer allows a continuous transfer of data without any delay between frames. The Receiver is the most complex part of the USART module due to its clock and data recovery units. The recovery units are used for asynchronous data reception. In addition to the recovery units, the Receiver includes a Parity Checker, Control logic, a Shift Register and a two level receive buffer (UDRn). The Receiver supports the same frame formats as the Transmitter, and can detect Frame Error, Data OverRun and Parity Errors.

Figure 20-1. USART Block Diagram[(1)]



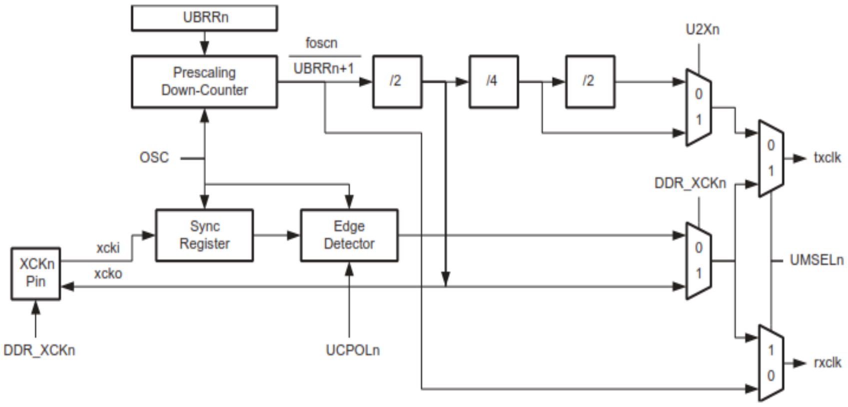
Note: 1. Refer to Figure 1-1 on page 3 and Table 14-9 on page 88 for USART0 pin placement.

20.3 Clock Generation

The Clock Generation logic generates the base clock for the Transmitter and Receiver. The USART supports four modes of clock operation: Normal asynchronous, Double Speed asynchronous, Master synchronous and Slave synchronous mode. The UMSELn bit in USART Control and Status Register C (UCSRnC) selects between asynchronous and synchronous operation. Double Speed (asynchronous mode only) is controlled by the U2Xn found in the UCSRnA Register. When using synchronous mode (UMSELn = 1), the Data Direction Register for the XCKn pin (DDR_XCKn) controls whether the clock source is internal (Master mode) or external (Slave mode). The XCKn pin is only active when using synchronous mode.

Figure 20-2 shows a block diagram of the clock generation logic.

Figure 20-2. Clock Generation Logic, Block Diagram



Signal description:

txclk	Transmitter clock (Internal Signal).
rxclk	Receiver base clock (Internal Signal).
xcki	Input from XCK pin (internal Signal). Used for synchronous slave operation.
xcko	Clock output to XCK pin (Internal Signal). Used for synchronous master operation.
fosc	System clock frequency.

20.3.1 Internal Clock Generation – The Baud Rate Generator

Internal clock generation is used for the asynchronous and the synchronous master modes of operation. The description in this section refers to Figure 20-2.

The USART Baud Rate Register (UBRRn) and the down-counter connected to it function as a programmable prescaler or baud rate generator. The down-counter, running at system clock (f_{osc}), is loaded with the UBRRn value each time the counter has counted down to zero or when the UBRRnL Register is written. A clock is generated each time the counter reaches zero. This clock is the baud rate generator clock output (= f_{osc}/(UBRRn+1)). The Transmitter divides the baud rate generator clock output by 2, 8 or 16 depending on mode. The baud rate generator output is used directly by the Receiver's clock and data recovery units. However, the recovery units use a state machine that uses 2, 8 or 16 states depending on mode set by the state of the UMSELn, U2Xn and DDR_XCKn bits.

27. Boot Loader Support – Read-While-Write Self-Programming

The Boot Loader Support applies to ATmega88A/88PA/168A/168PA/328/328P

27.1 Features

- **Read-While-Write Self-Programming**
- **Flexible Boot Memory Size**
- **High Security (Separate Boot Lock Bits for a Flexible Protection)**
- **Separate Fuse to Select Reset Vector**
- **Optimized Page[(1)] Size**
- **Code Efficient Algorithm**
- **Efficient Read-Modify-Write Support**

Note: 1. A page is a section in the Flash consisting of several bytes (see Table 28-11 on page 285) used during programming. The page organization does not affect normal operation.

27.2 Overview

In ATmega88A/88PA/168A/168PA/328/328P the Boot Loader Support provides a real Read-While-Write Self-Programming mechanism for downloading and uploading program code by the MCU itself. This feature allows flexible application software updates controlled by the MCU using a Flash-resident Boot Loader program. The Boot Loader program can use any available data interface and associated protocol to read code and write (program) that code into the Flash memory, or read the code from the program memory. The program code within the Boot Loader section has the capability to write into the entire Flash, including the Boot Loader memory. The Boot Loader can thus even modify itself, and it can also erase itself from the code if the feature is not needed anymore. The size of the Boot Loader memory is configurable with fuses and the Boot Loader has two separate sets of Boot Lock bits which can be set independently. This gives the user a unique flexibility to select different levels of protection.

27.3 Application and Boot Loader Flash Sections

The Flash memory is organized in two main sections, the Application section and the Boot Loader section (see Figure 27-2). The size of the different sections is configured by the BOOTSZ Fuses as shown in Table 27-7 on page 275 and Figure 27-2. These two sections can have different level of protection since they have different sets of Lock bits.

27.3.1 Application Section

The Application section is the section of the Flash that is used for storing the application code. The protection level for the Application section can be selected by the application Boot Lock bits (Boot Lock bits 0), see Table 27-2 on page 267. The Application section can never store any Boot Loader code since the SPM instruction is disabled when executed from the Application section.

27.3.2 BLS – Boot Loader Section

While the Application section is used for storing the application code, the The Boot Loader software must be located in the BLS since the SPM instruction can initiate a programming when executing from the BLS only. The SPM instruction can access the entire Flash, including the BLS itself. The protection level for the Boot Loader section can be selected by the Boot Loader Lock bits (Boot Lock bits 1), see Table 27-3 on page 267.

27.4 Read-While-Write and No Read-While-Write Flash Sections

Whether the CPU supports Read-While-Write or if the CPU is halted during a Boot Loader software update is dependent on which address that is being programmed. In addition to the two sections that are configurable by the BOOTSZ Fuses as described above, the Flash is also divided into two fixed sections, the Read-While-Write (RWW) section and the No Read-While-Write (NRWW) section. The limit between the RWW- and NRWW sections is given in Table 27-8 on page 275 and Figure 27-2 on page 266. The main difference between the two sections is:

- When erasing or writing a page located inside the RWW section, the NRWW section can be read during the operation.
- When erasing or writing a page located inside the NRWW section, the CPU is halted during the entire operation.

Note that the user software can never read any code that is located inside the RWW section during a Boot Loader software operation. The syntax "Read-While-Write section" refers to which section that is being programmed (erased or written), not which section that actually is being read during a Boot Loader software update.

27.4.1 RWW – Read-While-Write Section

If a Boot Loader software update is programming a page inside the RWW section, it is possible to read code from the Flash, but only code that is located in the NRWW section. During an on-going programming, the software must ensure that the RWW section never is being read. If the user software is trying to read code that is located inside the RWW section (i.e., by a call/jmp/lpm or an interrupt) during programming, the software might end up in an unknown state. To avoid this, the interrupts should either be disabled or moved to the Boot Loader section. The Boot Loader section is always located in the NRWW section. The RWW Section Busy bit (RWWSB) in the Store Program Memory Control and Status Register (SPMCSR) will be read as logical one as long as the RWW section is blocked for reading. After a programming is completed, the RWWSB must be cleared by software before reading code located in the RWW section. See Section "27.9.1" on page 278. for details on how to clear RWWSB.

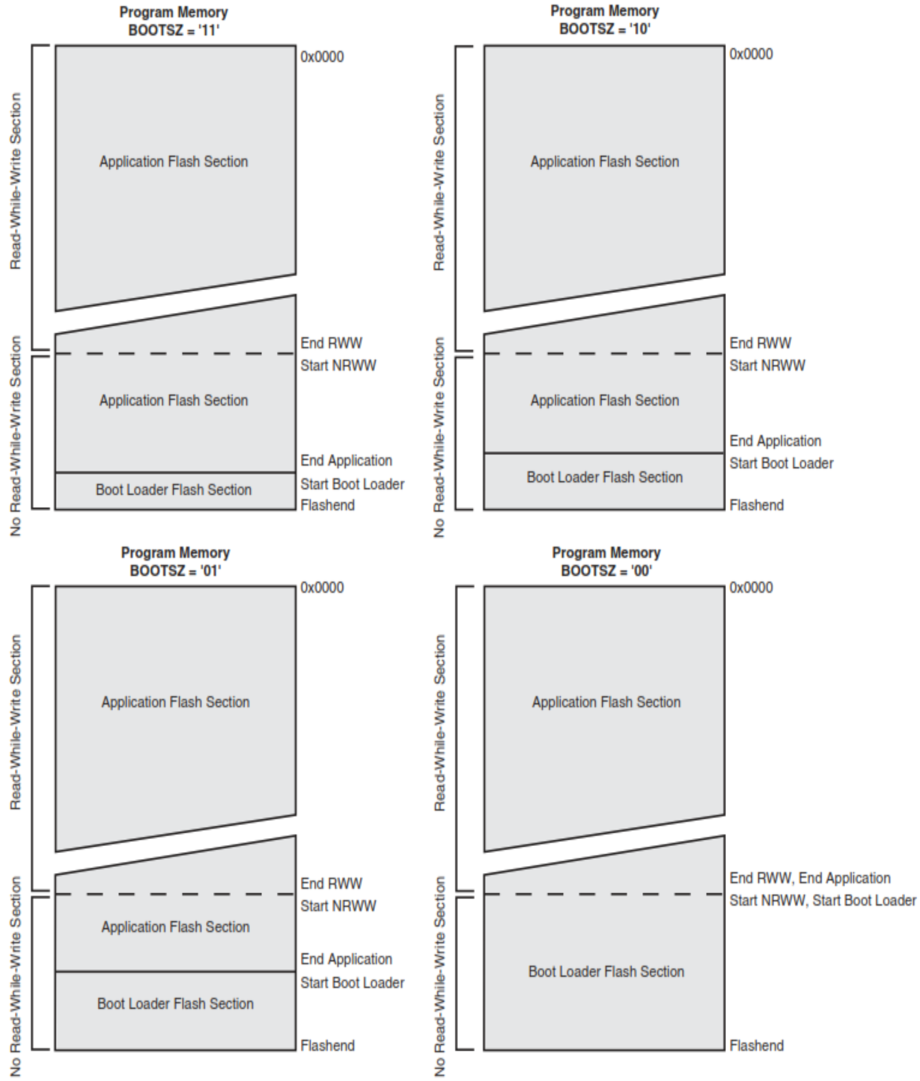
27.4.2 NRWW – No Read-While-Write Section

The code located in the NRWW section can be read when the Boot Loader software is updating a page in the RWW section. When the Boot Loader code updates the NRWW section, the CPU is halted during the entire Page Erase or Page Write operation.

Table 27-1. Read-While-Write Features

Which Section does the Z-pointer Address during the Programming?	Which Section can be read during Programming?	CPU Halted?	Read-While-Write Supported?
RWW Section	NRWW Section	No	Yes
NRWW Section	None	Yes	No

Figure 27-2. Memory Sections



Note: 1. The parameters in the figure above are given in Table 27-7 on page 275.

27.5 Boot Loader Lock Bits

If no Boot Loader capability is needed, the entire Flash is available for application code. The Boot Loader has two separate sets of Boot Lock bits which can be set independently. This gives the user a unique flexibility to select different levels of protection.

The user can select:

- To protect the entire Flash from a software update by the MCU.
- To protect only the Boot Loader Flash section from a software update by the MCU.
- To protect only the Application Flash section from a software update by the MCU.
- Allow software update in the entire Flash.

See Table 27-2 and Table 27-3 for further details. The Boot Lock bits can be set in software and in Serial or Parallel Programming mode, but they can be cleared by a Chip Erase command only. The general Write Lock (Lock Bit mode 2) does not control the programming of the Flash memory by SPM instruction. Similarly, the general Read/Write Lock (Lock Bit mode 1) does not control reading nor writing by LPM/SPM, if it is attempted.

36. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xFF)	Reserved	–	–	–	–	–	–	–	–	
(0xFE)	Reserved	–	–	–	–	–	–	–	–	
(0xFD)	Reserved	–	–	–	–	–	–	–	–	
(0xFC)	Reserved	–	–	–	–	–	–	–	–	
(0xFB)	Reserved	–	–	–	–	–	–	–	–	
(0xFA)	Reserved	–	–	–	–	–	–	–	–	
(0xF9)	Reserved	–	–	–	–	–	–	–	–	
(0xF8)	Reserved	–	–	–	–	–	–	–	–	
(0xF7)	Reserved	–	–	–	–	–	–	–	–	
(0xF6)	Reserved	–	–	–	–	–	–	–	–	
(0xF5)	Reserved	–	–	–	–	–	–	–	–	
(0xF4)	Reserved	–	–	–	–	–	–	–	–	
(0xF3)	Reserved	–	–	–	–	–	–	–	–	
(0xF2)	Reserved	–	–	–	–	–	–	–	–	
(0xF1)	Reserved	–	–	–	–	–	–	–	–	
(0xF0)	Reserved	–	–	–	–	–	–	–	–	
(0xEF)	Reserved	–	–	–	–	–	–	–	–	
(0xEE)	Reserved	–	–	–	–	–	–	–	–	
(0xED)	Reserved	–	–	–	–	–	–	–	–	
(0xEC)	Reserved	–	–	–	–	–	–	–	–	
(0xEB)	Reserved	–	–	–	–	–	–	–	–	
(0xEA)	Reserved	–	–	–	–	–	–	–	–	
(0xE9)	Reserved	–	–	–	–	–	–	–	–	
(0xE8)	Reserved	–	–	–	–	–	–	–	–	
(0xE7)	Reserved	–	–	–	–	–	–	–	–	
(0xE6)	Reserved	–	–	–	–	–	–	–	–	
(0xE5)	Reserved	–	–	–	–	–	–	–	–	
(0xE4)	Reserved	–	–	–	–	–	–	–	–	
(0xE3)	Reserved	–	–	–	–	–	–	–	–	
(0xE2)	Reserved	–	–	–	–	–	–	–	–	
(0xE1)	Reserved	–	–	–	–	–	–	–	–	
(0xE0)	Reserved	–	–	–	–	–	–	–	–	
(0xDF)	Reserved	–	–	–	–	–	–	–	–	
(0xDE)	Reserved	–	–	–	–	–	–	–	–	
(0xDD)	Reserved	–	–	–	–	–	–	–	–	
(0xDC)	Reserved	–	–	–	–	–	–	–	–	
(0xDB)	Reserved	–	–	–	–	–	–	–	–	
(0xDA)	Reserved	–	–	–	–	–	–	–	–	
(0xD9)	Reserved	–	–	–	–	–	–	–	–	
(0xD8)	Reserved	–	–	–	–	–	–	–	–	
(0xD7)	Reserved	–	–	–	–	–	–	–	–	
(0xD6)	Reserved	–	–	–	–	–	–	–	–	
(0xD5)	Reserved	–	–	–	–	–	–	–	–	
(0xD4)	Reserved	–	–	–	–	–	–	–	–	
(0xD3)	Reserved	–	–	–	–	–	–	–	–	
(0xD2)	Reserved	–	–	–	–	–	–	–	–	
(0xD1)	Reserved	–	–	–	–	–	–	–	–	
(0xD0)	Reserved	–	–	–	–	–	–	–	–	
(0xCF)	Reserved	–	–	–	–	–	–	–	–	
(0xCE)	Reserved	–	–	–	–	–	–	–	–	
(0xCD)	Reserved	–	–	–	–	–	–	–	–	
(0xCC)	Reserved	–	–	–	–	–	–	–	–	
(0xCB)	Reserved	–	–	–	–	–	–	–	–	
(0xCA)	Reserved	–	–	–	–	–	–	–	–	
(0xC9)	Reserved	–	–	–	–	–	–	–	–	
(0xC8)	Reserved	–	–	–	–	–	–	–	–	
(0xC7)	Reserved	–	–	–	–	–	–	–	–	
(0xC6)	UDR0	USART I/O Data Register								191
(0xC5)	UBRR0H					USART Baud Rate Register High				195
(0xC4)	UBRR0L	USART Baud Rate Register Low								195
(0xC3)	Reserved	–	–	–	–	–	–	–	–	
(0xC2)	UCSR0C	UMSEL01	UMSEL00	UPM01	UPM00	USBS0	UCSZ01 /UDORD0	UCSZ00 / UCPHA0	UCPOL0	193/204
(0xC1)	UCSR0B	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	UCSZ02	RXB80	TXB80	192
(0xC0)	UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0	191
(0xBF)	Reserved	–	–	–	–	–	–	–	–	
(0xBE)	Reserved	–	–	–	–	–	–	–	–	

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xBD)	TWAMR	TWAM6	TWAM5	TWAM4	TWAM3	TWAM2	TWAM1	TWAM0	–	233
(0xBC)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	230
(0xBB)	TWDR	2-wire Serial Interface Data Register								232
(0xBA)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	232
(0xB9)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0	231
(0xB8)	TWBR	2-wire Serial Interface Bit Rate Register								230
(0xB7)	Reserved	–		–	–	–	–	–	–	
(0xB6)	ASSR	–	EXCLK	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB	158
(0xB5)	Reserved	–	–	–	–	–	–	–	–	
(0xB4)	OCR2B	Timer/Counter2 Output Compare Register B								157
(0xB3)	OCR2A	Timer/Counter2 Output Compare Register A								157
(0xB2)	TCNT2	Timer/Counter2 (8-bit)								157
(0xB1)	TCCR2B	FOC2A	FOC2B	–	–	WGM22	CS22	CS21	CS20	156
(0xB0)	TCCR2A	COM2A1	COM2A0	COM2B1	COM2B0	–	–	WGM21	WGM20	153
(0xAF)	Reserved	–	–	–	–	–	–	–	–	
(0xAE)	Reserved	–	–	–	–	–	–	–	–	
(0xAD)	Reserved	–	–	–	–	–	–	–	–	
(0xAC)	Reserved	–	–	–	–	–	–	–	–	
(0xAB)	Reserved	–	–	–	–	–	–	–	–	
(0xAA)	Reserved	–	–	–	–	–	–	–	–	
(0xA9)	Reserved	–	–	–	–	–	–	–	–	
(0xA8)	Reserved	–	–	–	–	–	–	–	–	
(0xA7)	Reserved	–	–	–	–	–	–	–	–	
(0xA6)	Reserved	–	–	–	–	–	–	–	–	
(0xA5)	Reserved	–	–	–	–	–	–	–	–	
(0xA4)	Reserved	–	–	–	–	–	–	–	–	
(0xA3)	Reserved	–	–	–	–	–	–	–	–	
(0xA2)	Reserved	–	–	–	–	–	–	–	–	
(0xA1)	Reserved	–	–	–	–	–	–	–	–	
(0xA0)	Reserved	–	–	–	–	–	–	–	–	
(0x9F)	Reserved	–	–	–	–	–	–	–	–	
(0x9E)	Reserved	–	–	–	–	–	–	–	–	
(0x9D)	Reserved	–	–	–	–	–	–	–	–	
(0x9C)	Reserved	–	–	–	–	–	–	–	–	
(0x9B)	Reserved	–	–	–	–	–	–	–	–	
(0x9A)	Reserved	–	–	–	–	–	–	–	–	
(0x99)	Reserved	–	–	–	–	–	–	–	–	
(0x98)	Reserved	–	–	–	–	–	–	–	–	
(0x97)	Reserved	–	–	–	–	–	–	–	–	
(0x96)	Reserved	–	–	–	–	–	–	–	–	
(0x95)	Reserved	–	–	–	–	–	–	–	–	
(0x94)	Reserved	–	–	–	–	–	–	–	–	
(0x93)	Reserved	–	–	–	–	–	–	–	–	
(0x92)	Reserved	–	–	–	–	–	–	–	–	
(0x91)	Reserved	–	–	–	–	–	–	–	–	
(0x90)	Reserved	–	–	–	–	–	–	–	–	
(0x8F)	Reserved	–	–	–	–	–	–	–	–	
(0x8E)	Reserved	–	–	–	–	–	–	–	–	
(0x8D)	Reserved	–	–	–	–	–	–	–	–	
(0x8C)	Reserved	–	–	–	–	–	–	–	–	
(0x8B)	OCR1BH	Timer/Counter1 - Output Compare Register B High Byte								135
(0x8A)	OCR1BL	Timer/Counter1 - Output Compare Register B Low Byte								135
(0x89)	OCR1AH	Timer/Counter1 - Output Compare Register A High Byte								135
(0x88)	OCR1AL	Timer/Counter1 - Output Compare Register A Low Byte								135
(0x87)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								135
(0x86)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								135
(0x85)	TCNT1H	Timer/Counter1 - Counter Register High Byte								134
(0x84)	TCNT1L	Timer/Counter1 - Counter Register Low Byte								134
(0x83)	Reserved	–	–	–	–	–	–	–	–	
(0x82)	TCCR1C	FOC1A	FOC1B	–	–	–	–	–	–	134
(0x81)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	133
(0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	–	–	WGM11	WGM10	131
(0x7F)	DIDR1	–	–	–	–	–	–	AIN1D	AIN0D	236
(0x7E)	DIDR0	–	–	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	251
(0x7D)	Reserved	–	–	–	–	–	–	–	–	
(0x7C)	ADMUX	REFS1	REFS0	ADLAR	–	MUX3	MUX2	MUX1	MUX0	248
(0x7B)	ADCSRB	–	ACME	–	–	–	ADTS2	ADTS1	ADTS0	251
(0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	249

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x79)	ADCH	ADC Data Register High byte								250
(0x78)	ADCL	ADC Data Register Low byte								250
(0x77)	Reserved	–	–	–	–	–	–	–	–	
(0x76)	Reserved	–	–	–	–	–	–	–	–	
(0x75)	Reserved	–	–	–	–	–	–	–	–	
(0x74)	Reserved	–	–	–	–	–	–	–	–	
(0x73)	Reserved	–	–	–	–	–	–	–	–	
(0x72)	Reserved	–	–	–	–	–	–	–	–	
(0x71)	Reserved	–	–	–	–	–	–	–	–	
(0x70)	TIMSK2	–	–	–	–	–	OCIE2B	OCIE2A	TOIE2	157
(0x6F)	TIMSK1	–	–	ICIE1	–	–	OCIE1B	OCIE1A	TOIE1	135
(0x6E)	TIMSK0	–	–	–	–	–	OCIE0B	OCIE0A	TOIE0	109
(0x6D)	PCMSK2	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16	74
(0x6C)	PCMSK1	–	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	74
(0x6B)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	74
(0x6A)	Reserved	–	–	–	–	–	–	–	–	
(0x69)	EICRA	–	–	–	–	ISC11	ISC10	ISC01	ISC00	71
(0x68)	PCICR	–	–	–	–	–	PCIE2	PCIE1	PCIE0	
(0x67)	Reserved	–	–	–	–	–	–	–	–	
(0x66)	OSCCAL	Oscillator Calibration Register								37
(0x65)	Reserved	–	–	–	–	–	–	–	–	
(0x64)	PRR	PRTWI	PRTIM2	PRTIM0	–	PRTIM1	PRSPI	PRUSART0	PRADC	42
(0x63)	Reserved	–	–	–	–	–	–	–	–	
(0x62)	Reserved	–	–	–	–	–	–	–	–	
(0x61)	CLKPR	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	37
(0x60)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	54
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	10
0x3E (0x5E)	SPH	–	–	–	–	–	(SP10) [5.]	SP9	SP8	13
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	13
0x3C (0x5C)	Reserved	–	–	–	–	–	–	–	–	
0x3B (0x5B)	Reserved	–	–	–	–	–	–	–	–	
0x3A (0x5A)	Reserved	–	–	–	–	–	–	–	–	
0x39 (0x59)	Reserved	–	–	–	–	–	–	–	–	
0x38 (0x58)	Reserved	–	–	–	–	–	–	–	–	
0x37 (0x57)	SPMCSR	SPMIE	(RWWSB)[5.]	SIGRD	(RWWSRE)[5.]	BLBSET	PGWRT	PGERS	SPMEN	278
0x36 (0x56)	Reserved	–	–	–	–	–	–	–	–	
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0x34 (0x54)	MCUSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	54
0x33 (0x53)	SMCR	–	–	–	–	SM2	SM1	SM0	SE	40
0x32 (0x52)	Reserved	–	–	–	–	–	–	–	–	
0x31 (0x51)	Reserved	–	–	–	–	–	–	–	–	
0x30 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	235
0x2F (0x4F)	Reserved	–	–	–	–	–	–	–	–	
0x2E (0x4E)	SPDR	SPI Data Register								169
0x2D (0x4D)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	168
0x2C (0x4C)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	167
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0x2A (0x4A)	GPIOR1	General Purpose I/O Register 1								26
0x29 (0x49)	Reserved	–	–	–	–	–	–	–	–	
0x28 (0x48)	OCR0B	Timer/Counter0 Output Compare Register B								
0x27 (0x47)	OCR0A	Timer/Counter0 Output Compare Register A								
0x26 (0x46)	TCNT0	Timer/Counter0 (8-bit)								
0x25 (0x45)	TCCR0B	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	
0x24 (0x44)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00	
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0x1B (0x3B)	PCIFR	–	–	–	–	–	PCIF2	PCIF1	PCIF0	
0x1A (0x3A)	Reserved	–	–	–	–	–	–	–	–	
0x19 (0x39)	Reserved	–	–	–	–	–	–	–	–	
0x18 (0x38)	Reserved	–	–	–	–	–	–	–	–	
0x17 (0x37)	TIFR2	–	–	–	–	–	OCF2B	OCF2A	TOV2	158
0x16 (0x36)	TIFR1	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1	136

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x15 (0x35)	TIFR0	–	–	–	–	–	OCF0B	OCF0A	TOV0	
0x14 (0x34)	Reserved	–	–	–	–	–	–	–	–	
0x13 (0x33)	Reserved	–	–	–	–	–	–	–	–	
0x12 (0x32)	Reserved	–	–	–	–	–	–	–	–	
0x11 (0x31)	Reserved	–	–	–	–	–	–	–	–	
0x10 (0x30)	Reserved	–	–	–	–	–	–	–	–	
0x0F (0x2F)	Reserved	–	–	–	–	–	–	–	–	
0x0E (0x2E)	Reserved	–	–	–	–	–	–	–	–	
0x0D (0x2D)	Reserved	–	–	–	–	–	–	–	–	
0x0C (0x2C)	Reserved	–	–	–	–	–	–	–	–	
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	92
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	92
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	92
0x08 (0x28)	PORTC	–	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	91
0x07 (0x27)	DDRC	–	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	91
0x06 (0x26)	PINC	–	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	92
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	91
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	91
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	91
0x02 (0x22)	Reserved	–	–	–	–	–	–	–	–	
0x01 (0x21)	Reserved	–	–	–	–	–	–	–	–	
0x0 (0x20)	Reserved	–	–	–	–	–	–	–	–	

Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The ATmega48A/PA/88A/PA/168A/PA/328/P is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 - 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.
5. Only valid for ATmega88A/88PA/168A/168PA/328/328P.
6. BODS and BODSE only available for picoPower devices ATmega48PA/88PA/168PA/328P

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