DESIGN OF SAR ADCs WITH IMPROVED COMPARATOR STRUCTURE

PROJECT REPORT
PHASE II

Submitted by

JANANI.G
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KUMARAGURU COLLEGE OF TECHNOLOGY
(An Autonomous Institution Affiliated to Anna University, Chennai)
COIMBATORE – 641 049

ANNA UNIVERSITY, CHENNAI 600 025

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BONAFIDE CERTIFICATE

Certified that this project report titled **"DESIGN OF SAR ADCs WITH IMPROVED COMPARATOR STRUCTURE"** is the bonafide work of **JANANI.G [Reg. No. 15MAE005]** who carried out the research under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other project or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

SIGNATURE

Ms.S.Nagarathinam

Project Supervisor

Department of ECE

Kumaraguru College of Technology

Coimbatore-641 049

SIGNATURE

Mr.K.Ramprakash

Head of PG Programmes

Department of ECE

Kumaraguru College of Technology

Coimbatore-641 049

The candidtae with University **Register No.15MAE005** was examined by us in the project viva-voice examination held on .....

INTERNAL EXAMINER **EXTERNAL EXAMINER**

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ABSTRACT

Analog to Digital converters (ADC) focused for use in medical implant devices serve a critical part as the interface between analog signal and digital processing system. Normally, low power utilization is required for a long battery lifetime. In such application which requires low power utilization and moderate speed and resolution, a standout amongst the most commonly utilized ADC models is the successive approximation register (SAR) ADC.The other popular ADC architectures are Pipeline ADC, Flash ADC , Integrating ADC, Sigma Delta ADC. ADCs are selected according to specific application within the consideration of resolution, power, size, sampling frequency, performance and etc. A SAR ADC is usually first considered for its low power and small size with medium resolution applications. The basic architecture of SAR ADC consist of sample and hold circuit, successive approximation register, digital-to-analog converter and an analog voltage comparator.This project deals with the design of an improved double tail dynamic latch comparator which is placed in the comparator block of SAR ADCs and various parameters Measurements such as Power Consumption,Signal to Noise distortion ratio,Effective Number of bits are taken and compared with the SAR ADC designed with conventional comparator.The schematics are designed and processed in Tanner v13 software tool.

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

ADC	Analog-To-Digital Converters
SAR	Successive Approximation Register
DAC	Digital-To-Analog Converters
CMOS	Complementary Metal Oxide Semiconductor
FOM	Figure Of Merit
EDA	Electronic Design Automation
MSB	Most Significant Bit
LSB	Least Significant Bit
SAR ADC	Successive Approximation Register Analog To Digital Converter
DNL	Differential Nonlinearity
INL	Integral Nonlinearity
SFDR	Spurious-Free Dynamic Range
SINAD	Signal To Noise Distortion Ratio
ENOB	Effective Number Of Bits
EOC	End Of Conversion

CHAPTER 1

INTRODUCTION

1.1 OVERVIEW OF THE PROJECT

Analog-to-digital converters (ADC) targeted for use in applications such as portable/battery-powered instruments,pen digitizers industrial controls,and data/signal ,and medical implant devices which serves an important role as the interface between analog signal and digital processing system. Usually, low power consumption is required for a long battery lifetime. In such application which requires low power consumption and moderate speed and resolution, one of the most prevalently used ADC architectures is the successive approximation register (SAR) ADC. Successive-approximation-register (SAR) analog-to-digital converters (ADCs) represent the majority of the ADC market for medium- to high-resolution ADCs.

SAR ADCs provide up to 5Msps sampling rates with resolutions from 8 to 18 bits. The SAR architecture allows for high-performance, low-power ADCs to be packaged in small form factors for today's demanding applications. The SAR ADC architecture includes sample and hold circuit, successive Approximation Register, digital-to-analog converter and an analog voltage comparator . Comparators are basic building blocks in most ADCs since they are responsible for decision-making when digital information needs to be recovered from analog signals. Mismatches due to feature scaling, process variation and input-referred supply noise cause offset that directly affects the resolution of a comparator and thus has a crucial influence on the overall performance of the ADCs. Implementation of single comparator always requires full resolution quantization for all bits, which in turn slows down the SAR loop and consumes more power.

To resolve these issues, SAR ADC is designed by replacing conventional comparator with the improved double tail dynamic latch comparator since double tail structure incorporates input-output isolation which reduces kickback noise, strong positive feedback provides fast decisions during decision-making phase and avoid too many stacking of transistors which minimize area and latch delay time.

1.2 NEED FOR THE PROJECT

The two critical components of a SAR ADC are the comparator and the DAC.Hence ,The speed of SAR ADCs is limited by the settling time of the DAC, which must settle to within the resolution of the overall converter, for example, ½ LSB and the Comparator,which is one of the major blocks in A/D converters since they used to represent analog signal in digital domain [1-6]. With the supply voltage scaling in CMOS technologies and the increasing demand for low power and high speed, the channel length of the transistors are minimized at the expense of an increased level of mismatch [7-8]. Mismatches in the pre-amplifier and regenerative stages due to process variations, and input-referred supply noise cause offset that directly affects the resolution of a comparator and thus has a crucial influence on the overall performance in those applications [9-11]. Effective and simple method for offset cancel by applying additional circuits without scarifying the power, speed and area is always challenging.

Furthermore, based on the double-tail structure proposed in [10], a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. On the other hand, SAR ADC can benefit from the advancement of scaled CMOS technology since, it occupies less area.The comparator, which must resolve small differences in V_{IN} and V_{DAC} within the specified time and the logic overhead.

The requirements of the comparator are speed and accuracy. Comparator offset does not affect overall linearity as it appears as an offset in the overall transfer characteristic. In addition, offset-cancellation techniques are usually applied to reduce the comparator offset. Noise, however, is a concern, and the comparator is usually designed to have input-referred noise less than 1 LSB. Additionally, the comparator needs to resolve voltages within the accuracy of the overall system. Here, This project concerns for the design of improved comparator circuit to be placed in the comparator block in such a way it resolves the small differences in V_{IN} and V_{DAC} within the prior time,thus improving the efficiency of the Successive Approximation Register Analog to Digital converter.Hence,The need for this project in future helps the various demanding applications with more accuracy and efficiency.

1.3 OBJECTIVE

Many ADC architectures and integrated circuit technologies have been proposed and implemented to push back performance limits. Although different metrics and interpretations of ADC performances may be used in different research work, an overall trend is not affected in a significant way. The trend that cuts across nearly all resolutions and sampling rates is low power utilization. The average Figure of Merit (FOM) becomes smaller and smaller, indicating lower energy consumed in each effective conversion step.

ADCs with medium resolution (8-bit to 16-bit) and moderate sampling rate (several tens to hundred of MHz) are required for applications such as such as portable/battery-powered instruments, pen digitizers, industrial controls, and data/signal acquisition. Therefore, energy efficient and area efficient ADCs with high performance are in great demand. In this work a 8 bit SAR ADCs is designed with the replacement of conventional comparator with proposed comparator in such a way that the power consumption is reduced to 50micro watts, and comparison works of various parameters are done.

1.4 SOFTWARE USED

The following Software were used in the Project

- Tanner EDA V13.0 (Electronic Design Automation)
  - S-edit
  - T-Spice
  - L-edit

1.5 ORGANIZATION OF THE REPORT

- Chapter 2 is about the literature survey done on various comparator designs.
- Chapter 3 deals about different ADC structures and performance metrics.
- Chapter 4 illustrates design of SAR ADC and various blocks.
- Chapter 5 describes the results and analysis.
- Chapter 6 gives the conclusion of the project

CHAPTER 2
LITERATURE REVIEW ON COMPARATORS

2.1 OPEN-LOOP COMPARATOR

Open-loop comparator is in fact a high gain amplifier with differential input and single ended output with large swing. A two stage op-amp without compensation is an excellent realization of open-loop comparator which is illustrated in Figure 2.1. Since precise gain in not required in comparator,hence, no compensation technique is needed

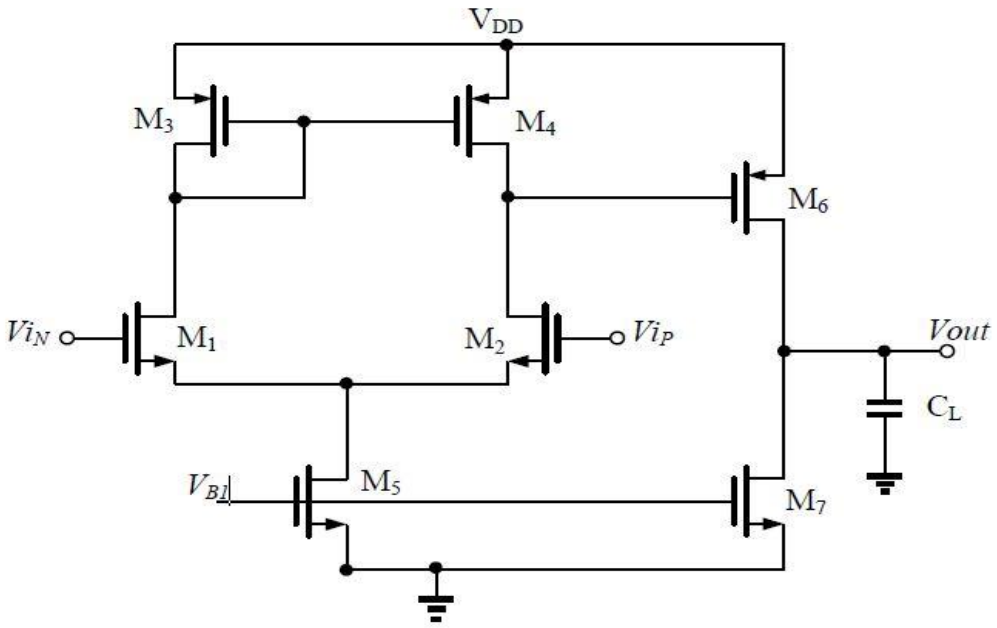


Figure 2.1 Open Loop Comparator

This comparator has two poles which compared to the one-pole implementation of the open loop comparator achieves higher speed. In one stage amplifier which has one pole, increasing the gain and simultaneously maintaining the large bandwidth, f_u, poses limitation on the gain bandwidth, f_c, which results in speed reduction of the comparator. In order to mitigate this problem two stage comparator has been proposed. Cascading two stages with lower gain in each stage leads to higher speed however it introduces more input-referred offset voltage. Furthermore, this configuration consumes more power; therefore this type of comparator is not suited for high speed A/D converters as well as low power ADCs.

2.2 LATCH-ONLY COMPARATOR

Different from open-loop comparators, latched comparators make use of the combination of amplification and positive feedback. They operate in discrete-time domain rather than continuous-time domain. According to the latch signal, they operate in two phases. Shown in Figure 2.2 a,2.2 b. In the reset phase (*Latch* low), the comparator tracks the inputs; In the regeneration phase (*Latch* high), the positive feedback starts work and the comparator generates a digital output based on the sign of the input difference.

Figure 2.2 a Reset Phase

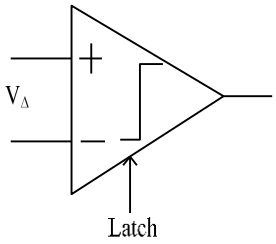
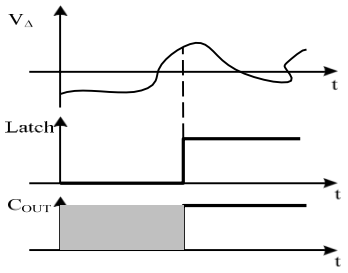


Figure 2.2 b Regeneration Phase



In Figure 2.3, the circuit schematic of a latch comparator is shown [12,13]. During the reset phase (*RST* low), nodes V_O+ and V_O- are pre-charged to VDD by M5/M6. When *RST* goes high, the comparison starts. V_O+ and V_O- discharge the output capacitance with unequal rates due to the different input voltages. When one of the nodes is lower than VDD-VTHP, the cross-coupled PMOS transistors M3/M4 are activated, allowing VDD to fully charge one of the output capacitances. The output inverters are for signal level recovery [13].

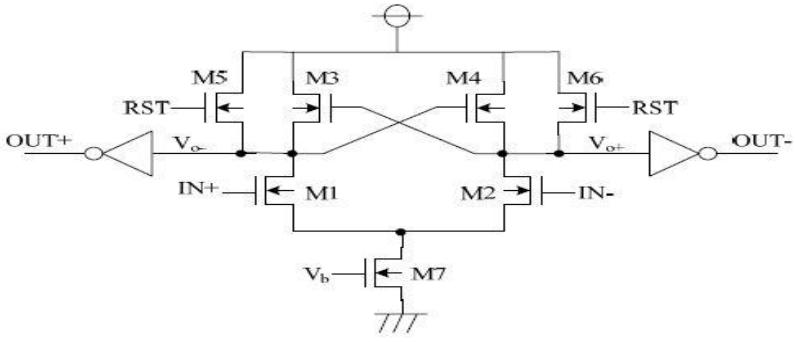


Figure 2.3 Latch-only Comparator

It is important to note that M7 works as a bias transistor. It consumes power during the whole comparison. There is a trade-off between choosing a small bias current for low power consumption and a large value for speed maximization and noise minimization [13]. Moreover, due to the mismatch of the transistors, high input-referred offset voltage directly adds to the total ADC offset. Offset cancellation techniques is required if necessary.

2.3 LATCHED COMPARATOR FOLLOWING PRE-AMPLIFIER

It was described above that there is a trade-off between comparator's speed, power and resolution. Though latch-only comparators provide fast speed and low power, they suffer from high input offset error which makes them unattractive to designs requiring small input differences. An optimal solution combining a pre-amplifier and a latch, shown in Figure 2.4, is employed to compromise the situation [14,15].

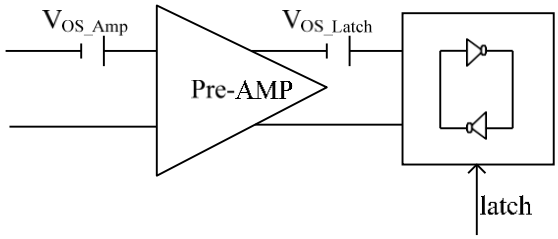


Figure 2.4 Latch Comparator following Pre-Amplifier

Figure 2.5 shows a detailed implementation presented in [15]. The preamplifier is a conventional one-stage differential amplifier with NMOS input pair and PMOS resistive load. It provides sufficient gain to attenuate the error. The design of latch comparator is quite similar to the circuit shown in Figure 2.3, which employs differential technique with a cross-coupled inverter as a positive feedback

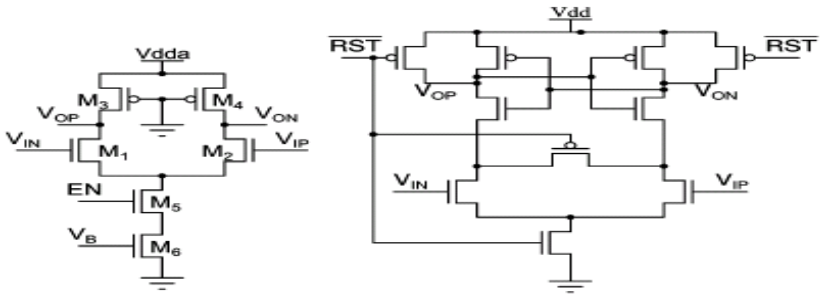


Figure 2.5 Detailed implementation of fig 2.4

2.4 DYNAMIC LATCH COMPARATOR

A more power efficient approach is to design a dynamic latched comparator, which only consumes the power during regeneration phase. Figure 2.6 shows an example, presented in [16]. Unlike the comparator presented in [13], a switch M9 instead of a bias transistor is employed. During the reset phase (Comp low), M5/M6 and M7/M8 switch on to pull the internal nodes down to ground. M9 is cut off and no supply current exists. When Comp goes high, M9 is switched on and current flows in it. The reset switches are cut off. The cross-coupled inverters start to make the regeneration. After the regeneration, one of the outputs is V_{DD} and the other is GND. Therefore, no supply current flows and the power efficiency is maximized. However, the problem of the offset voltage happens again. In [16], a programmable capacitor array is used to calibrate the offset error.

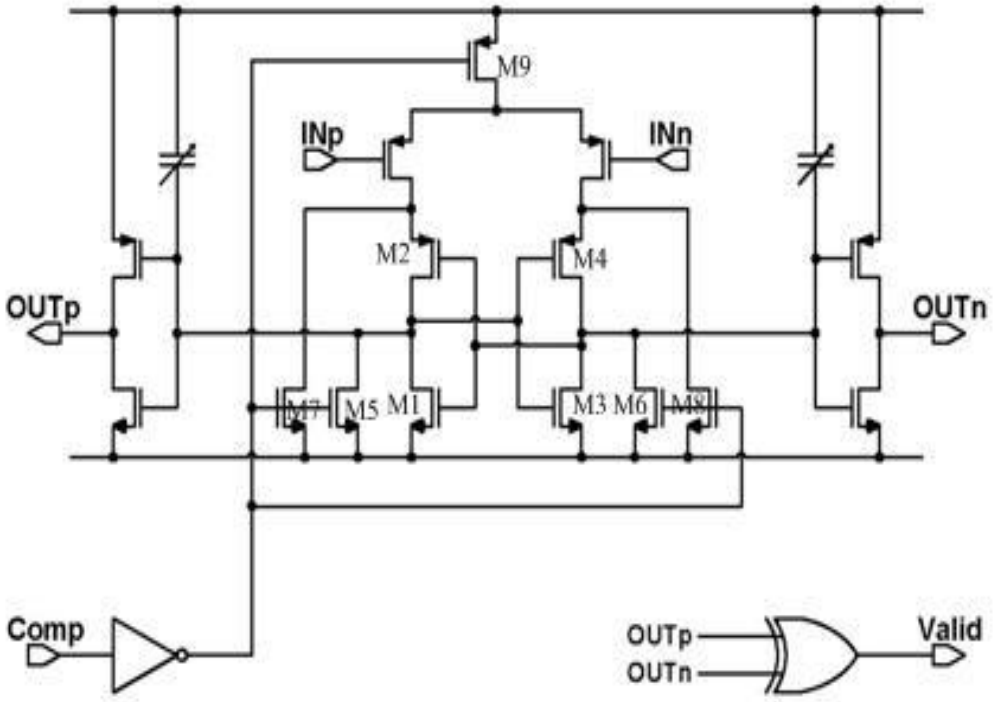


Figure 2.6 Dynamic Latch Comparator

Dynamic latched architecture is the most power efficient comparator, however, it introduces large input referred offset which makes it unappealing for high resolution ADCs. This effect can be reduced by increasing the width of input transistors in differential pair. Employing offset cancelation techniques in the comparator implementation is also an effective approach to mitigate this problem. Furthermore, the offset voltage can be reduced by using a pre-amplifier which is

previously described as a latched comparator with preamplifier. However, in all the mentioned methods, offset reduction is achieved at the cost of more power consumption.

2.4.1 CONVENTIONAL DYNAMIC LATCH COMPARATOR

The widely used A/D converter is conventional dynamic comparator due to high input impedance, rail-to-rail output swing, and no static power consumption which is shown in Fig. 2.7 .The operation of the comparator is as follows.when clk = 0 that is during reset phase when Mtail is off, The output nodes Outn and Outp have been pulled to VDD by the reset transistors to start the initial condition and to have a valid logical level during reset. when CLK = VDD, that is during the comparison phase transistors M7 and M8 are off, and Mtail is on. Output voltages (Outp, Outn), which had been pre-charged to VDD, begin to emit with different discharging rates depending on the appropriate input voltage (INN/INP).

Assuming the case where VINP > VINN, Output at p node emits faster than Output at node n, hence when Output at node p falls down to VDD–|Vthp| before Output at node n will turn on initiating the regeneration of latch caused by back-to-back inverters (M3, M5 and M4, M6). Thus, Output at node n pulls to supply and Output at node p discharges to ground. If VINP < VINN, the circuits works vice versa.

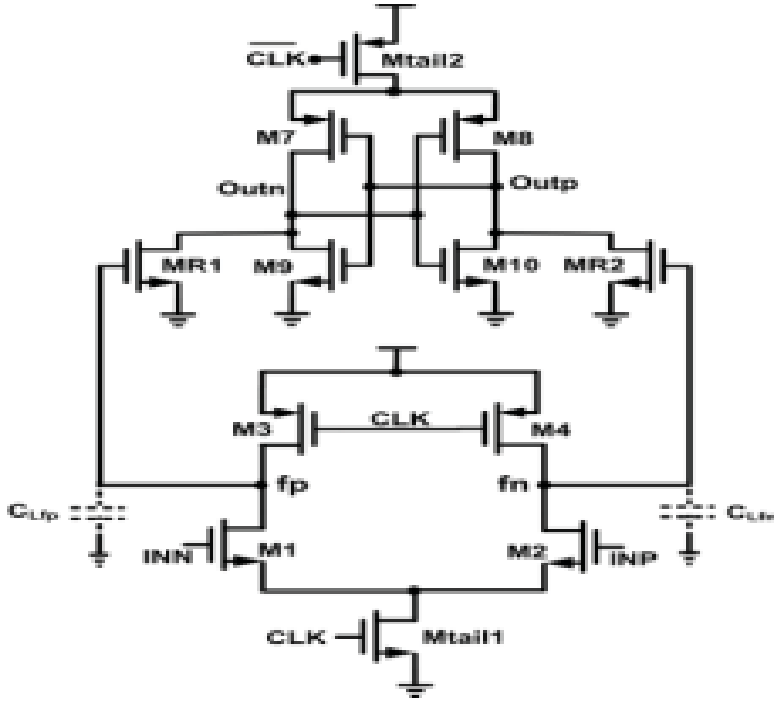


Figure 2.7 Conventional Dynamic Latch Comparator

2.4.2 DOUBLE TAIL DYNAMIC LATCH COMPARATOR

The comparator operation is as follows which is shown in Fig. 2.8 ,At reset phase when clk is 0 and Mtail 1 & 2 are off, pre-charge of fn and fp nodes to VDD by the transistors M3 and M4 takes place which discharges output nodes to gnd by MR1 and MR2.when CLK = VDD, Mtail1 and Mtail2 is on, which is also called decision phase in which M3-M4 turn off and node voltage of fn and fp start to discharge with the rate given by IMtail1/C fn(p) and an input-dependent differential voltage Vfn(p) will build up on top. The MR1 and MR2 which forms an intermediate stage passes Vfn(p) to the inverters which is cross coupled and also gives a good protection between input and output, which also results in the reduction of kickback noise. once the latch of the first n-channel transistor turns on (for instance, M9), the corresponding output (e.g., Outn) will be discharged to the ground, making front p-channel transistor (e.g., M8) to turn on, charging another output (Outp) to the supply voltage (VDD).

Both intermediate stage transistors of this comparator will be finally cut-off, (since fn and fp nodes both discharge to the ground), hence it does not take part in the improvement of effective trans conductance of the latch. Besides, during reset phase, charging of nodes have to be done from ground to VDD, which means power utilization. A high speed analog to digital converter such as Flash ADC are implemented using offset cancellation technique[17]. Comparator structure is added with offset cancellation network which inturn increases the transistor count. The suitable technique for very low power clocked and continuous time circuits is Supply boosting technique.

To ensure correct detection on each comparison, the analog input must have sufficient magnitude to overcome deterministic errors such as offset and hysteresis, as well as random errors due to device thermal noise and flicker noise. In present time everything has to be operated with less power consumption. Delay also a function of power consumption. In low power comparator power consumption is low because of low supply voltage. Low power comparator also having reduced area so chip size is reduced and power consumption also reduced. This structure has the boon of input impedance being high , output swing which is of rail-to-rail ,power consumption being not static, and robustness being good against noise and mismatch. The offset can be minimized by the possible design of large input transistors since the switching speed of the node at the output is not directly affected by the parasitic capacitances of the input transistors. Important drawback of this structure is the Mtail which is the only one current path, that defines the current

for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to make the differential pair in the region of weak inversion and get a interval of long integration and a better Gm/I ratio, a tail current would be able to make fast regeneration in the latch if the tail current is large enough, Besides, as long as Mtail operates in the region of triode, input common-mode voltage affects the tail current, inturn makes it unfavorable for regeneration.

In many devices of fully supplied current the problem related to power is automatically related to cost. However power problem for the devices which is of low powered is not only economical issue but also becomes very necessary in terms of functionality. Availability of inconsiderable amount of energy or unstable energy makes engineer tempt to find a solution is a key point in this area. In today's scenario every appliances should have the quality of low power consumption.

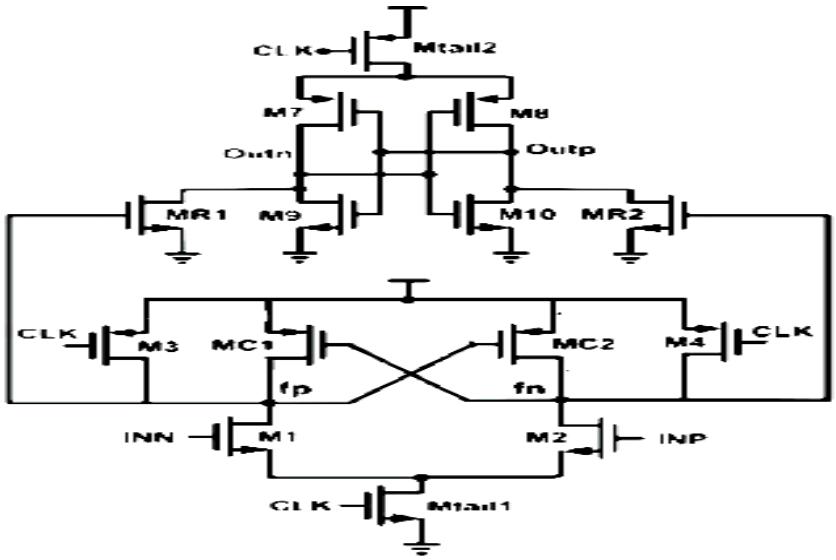


Figure 2.8 Double Tail Dynamic Latch Comparator

2.4.3 PROPOSED DOUBLE TAIL DYNAMIC LATCH COMPARATOR

The better performance of dual tail architecture in low-voltage applications made to design the proposed comparator in dual tail structure. The idea of the proposed comparator is to increase Vfn/fp in order to increase the latch regeneration speed. For this progress, the control transistors which are named Mc1 and Mc2 have been connected in parallel to M3/M4 transistors in a criss cross manner in the first stage [Fig. 2.9]. The operation of the proposed comparator is as follows. When CLK = 0, Mtail1 and Mtail2 are off, that is in reset phase, avoiding power which is static ,transistor M3 and M4 drops both node voltage at input and output to supply, hence cut off region

exists in transistor Mc1 and Mc2. The Intermediate stage transistors which are named MR1 and MR2, reset output of both latches to ground. At decision-making phase when CLK is at VDD, Mtail1, and Mtail2 are in on state, transistors M3 and M4 gets turned off. Furthermore, at the starting of this phase, the transistors which involve in control are still in off State. Thus, node voltages fn and fp start to fall with different rates prior to the input voltages. Suppose input voltage at node p is greater than the voltage at node n VINP > VINN, thus node voltage fn falls quicker than fp, (since M2 provides more current than M1).

Whenever fn falls the appropriate pMOS control transistor (Mc1 in this case) begins to turn on, draining fp node back to the supply; so another transistor which involves as a controlling factor (Mc2) remains off, facilitating fn to be drained completely. In other words, conventional dual tail dynamic comparator, in which Vfn/fp is a function of input transistor, trans conductance and input voltage difference, whereas In the proposed structure as soon as the comparator finds that for instance node fn drains faster, a pMOS transistor (Mc1) turns on, dropping the other node fp back to the supply. Therefore by the time passing, the difference between fn and fp (_Vfn/ fp) increases in an exponential manner, leading to the lowering of latch regeneration time. inspite the effectiveness of the proposed idea, one of the points which should be noted is that in this circuit, when one of the control transistors turns on, supply current is given to the ground through input and tail transistor achieving in static power consumption.

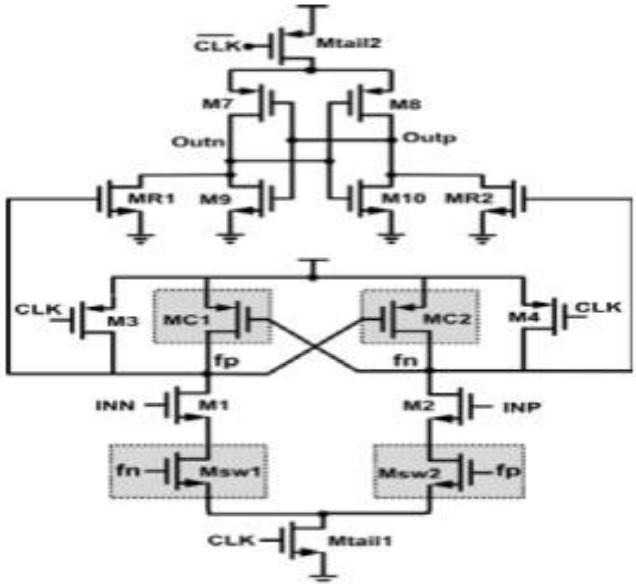


Figure 2.9 Proposed Double Tail Dynmaic Latch Comparator

CHAPTER 3
ADC ARCHITECTURES AND PERFORMANCE METRICS

3.1 ADC ARCHITECTURES

The five popular ADC architectures were described in the below sections. ADCs are selected according to specific application within the consideration of resolution, power, size, sampling frequency, performance and etc. For some applications, almost all the architectures may work well; for others, there may be a better choice to achieve the best performance. For example, a Flash ADC is most popular for applications requiring ultra-high speed when power consumption is not primary concern. A Sigma-Delta ADC is always the best choice when high resolution is demanded. A SAR ADC is usually first considered coming to low power and small size with medium resolution[18],[19].

3.1.1 FLASH ADC

Flash ADC is known for its fast speed. As depicted in Figure 3.1, it has 2^N-1 comparators corresponding to 2^N-1 quantization steps. The total 2^N resistors generate all the voltage references. The comparator outputs one if the input voltage is larger than the related reference voltage, and zero vice versa. There is a decoder followed at the last stage to translate the thermometer code produced by comparators to N-bit binary digital output. Though Flash ADC has a high speed, the great numbers of comparators consume huge power and area. Taking a 9-bit Flash ADC as an example, there will be 511 comparators in the circuit. This disadvantage limits the resolution of Flash ADC up to 6 bits.

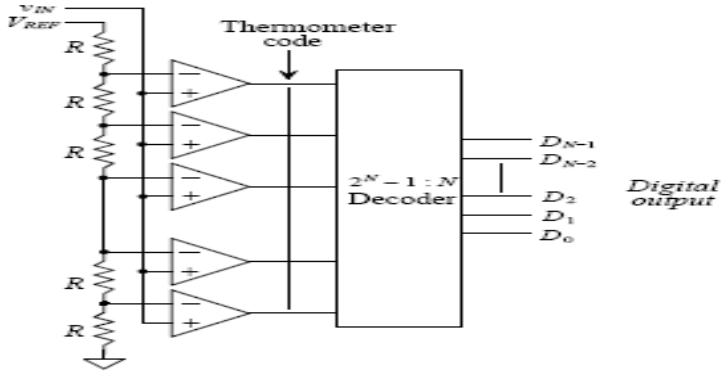


Figure 3.1 Flash ADC

3.1.2 PIPELINE ADC

Pipeline ADC, shown in Figure 3.2 , consists of N steps conversion shown in Figure. Each stage (except the LSB's) is composed of a sample and hold circuit, a comparator, a differential amplifier and an amplifier with a gain of 2. The input voltage (V_{IN}) is sampled and firstly compared to half of the reference voltage (V_{REF}). If V_{IN} is larger, the comparator outputs one. Then V_{IN} is subtracted by Vref/2 and input to the gain 2 amplifier.

If V_{IN} is smaller, the comparator outputs zero, and the original signal is directly passed to the amplifier. MSB is decided by the comparator result. Same as the operation of the first stage, the amplified residue is again sampled and compared with Vref/2. The above operation continues until the LSB is decided. Pipeline ADC needs N clock cycles to complete the first conversion, but afterwards it can make each conversion per clock cycle due to its property of pipelining. Despite the initial N-clock cycles, Pipeline ADC is frequently used for its high speed and resolution.

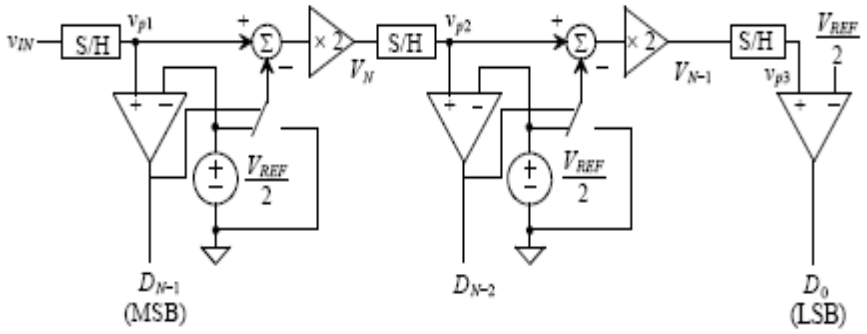


Figure 3.2 Pipeline ADC

3.1.3 INTEGRATING ADC

Integrating ADC,as the name indicates,integrates the input signal and counts the integration time. The counted time converts to N-bit digital information. A famous type of converter based on this concept is the dual slope converter (shown in Figure 3.4). Before the explanation of the dual slope converter, a single slope converter, which is the simplest type of integrating ADC, is first explained here (shown in Figure 3.3). The single slope converter consists of an integrator,a comparator and a counter. Before the integration starts, the input voltage is sampled (V_{IN}) and the

integrator is reset by closing the switch. Then V_{IN} is hold and sent to the comparator. At the same time the integrator starts producing the ramp function and the counter begins countering clock pulses. The moment the integrated voltage (V_C) is larger than V_{IN}, the counter stops. An equation below shows the relation between the input signal and the integrating time:

$$V_{IN} = V_{REF} \frac{T_2}{T_1}$$

Based on the equation,it is concluded that the accuracy of conversion is tightly related with the RC constant, the reference voltage and the clock generator.

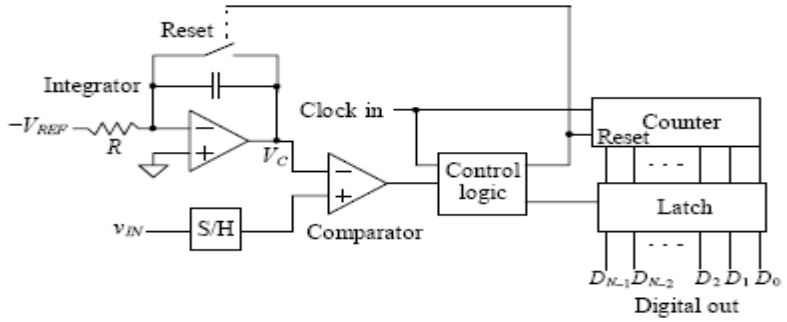


Figure 3.3 Single Slope converter

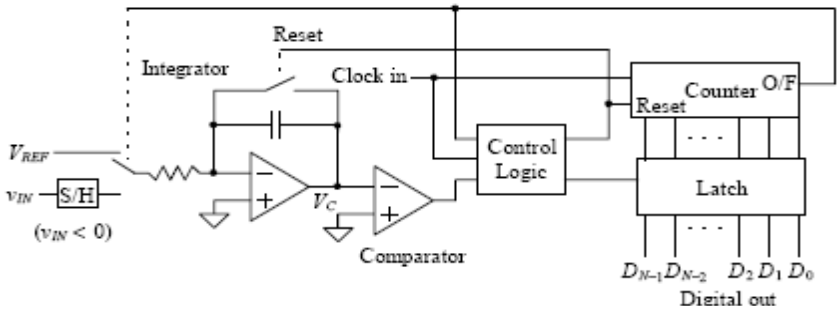


Figure 3.4 Dual Slope Converter

To eliminate the accuracy problems of single slope ADC, the dual slope ADC is designed (shown in Figure 2.16). It has two integration steps. First, V_{IN} is integrated with a constant time and then V_{REF} is integrated until the discharged voltage is arriving at zero which detected by the comparator. Figure 3.5 shows the time diagram of these two integrations. An equation shows the relationship:

$$V_{IN} = V_{REF} \frac{T_2}{T_1}$$

As V_{IN} is decided by the ratio between the charge and discharge time, the accuracy problem of clock itself is suppressed. However, a drawback of this design is that it needs more integration time than that of the single slope.

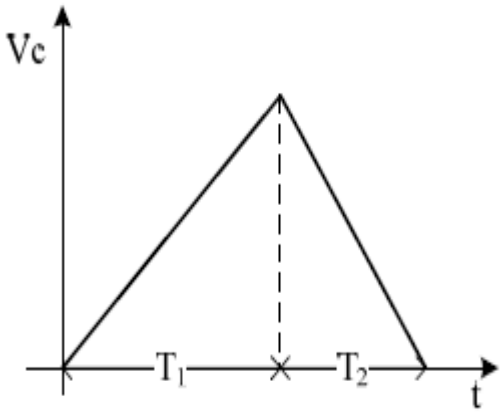


Figure 3.5 Timing Diagram of two integrations

3.1.4 SUCCESSIVE APPROXIMATION ADC

Successive approximation register (SAR) ADC is designed based on a binary search algorithm. It consists of a successive approximation register (SAR), a digital-to-analog converter, a comparator and a sample and hold circuit, which is illustrated in Figure 3.6 . First, input voltage (V_{IN}) is sampled and the registers are reset to zero. Secondly, the conversion starts through an approximation of MSB (set MSB as one) by SAR; DAC converts the digital information to a voltage V_{OUT} (half of the reference voltage V_{REF}); Comparator compares V_{OUT} with V_{IN}. If V_{IN} is larger than V_{OUT}, it outputs *one*, otherwise, it outputs zero; SAR loads the comparator result, registers the value of MSB and generates its next approximation; the conversion continues until the LSB is decided. Therefore, an N-bit SAR ADC needs N clock cycles per conversion. SAR ADC is known for its simple structure, thus consuming less power and saving more die size. However, with increase of its resolution, the linearity problem of DAC becomes more severe, which directly causes non linearity of ADC. Therefore, SAR ADC is not suitable for high resolution.

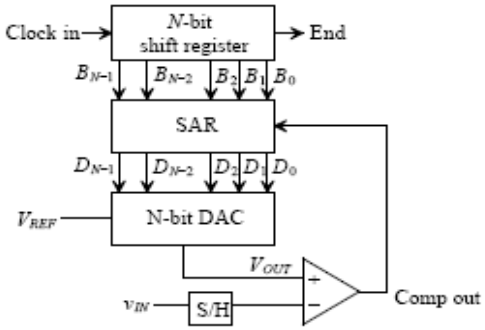


Figure 3.6 Basic Block diagram of SAR ADC

3.1.5 SIGMA DELTA ADC

Up till now, all the architectures explained here could be categorized into Nyquist-rate ADCs because the sampling frequency is two times of the input signal frequency. In order to obey the Nyquist rule, anti-aliasing filters are always used between analog input and Nyquist-rate ADCs. While, to design such kind of a filter is not an easy task due to the sharp transition band.

To overcome this problem, another category of ADC whose sampling frequency is much higher than the signal bandwidth, named oversampling ADC, has been designed [19], [20]. Sigma-Delta ADC is referred to as oversampling ADC. The block diagram of a first-order sigma-delta ADC is shown in Figure 3.7. It consists of a differential amplifier, an integrator and a 1-bit ADC with feedback loop contains a 1-bit DAC. The 1-bit ADC is simply a comparator, which outputs ones or zeros.

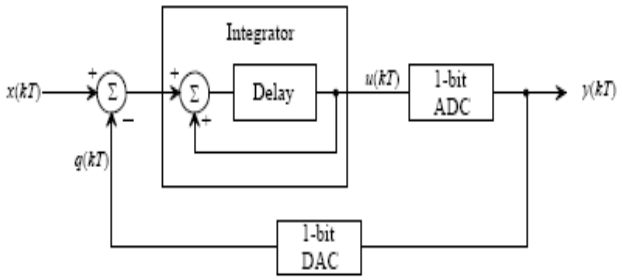


Figure 3.7 First-order Sigma-Delta ADC

The purpose of DAC is to keep the average output of the integrator near the comparator's reference level [21]. When the input increases, the comparator outputs more ones, otherwise it generates less ones. The density of positive pulses is proportional to the input signal. The integrator

serves as a low-pass filter to the input and a high-pass filter to the quantization noise. Therefore, oversampling has improved converter's SNR by changing the distribution of noise power [21].

3.2 PERFORMANCE METRICS OF ADCs

3.2.1 RESOLUTION

The resolution of an ADC is the number of its output words, which indicates the minimum input voltage that an ADC can generate a code transition. Figure 3.8 shows a simplified block diagram of an ADC. The smallest step is defined as the least-significant-bit (LSB) by equation $V_{LSB} = V_{REF}/2^{N}$, where V_{REF} is the reference voltage of the converter. The N-bit binary codes $D_0D_1\ldots D_{N-1}$ represents the input voltage with a value of $(D_0 2^{-N} + D_1 2^{-N+1} + \ldots + D_{N-1} 2^{-1}) * V_{REF}$.

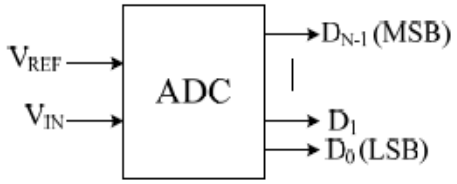


Figure 3.8 Simplified block diagram of ADC

3.2.2 DIFFERENTIAL NONLINEARITY (DNL)

Deviation of the code transition width from the ideal one (1 LSB) is called differential nonlinearity (DNL). For narrow code width, DNL is negative while for the wide one DNL is positive. In an ideal ADC the code width is always one, thus, DNL is zero.

3.2.3 INTEGRAL NONLINEARITY (INL)

Integral nonlinearity (INL) is the difference between the code centers from the ideal line. INL can also be specified as the sum of DNLs [22]. Additionally, INL can be defined as the distance of the code centers with the best fit line. Figure 3.9 depicts the maximum INL which is measured with the ideal one.

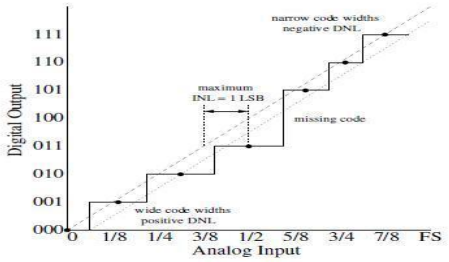


Figure 3.9 DNL and maximum INL

3.2.4 SPURIOUS-FREE DYNAMIC RANGE (SFDR)

Spurious-Free Dynamic Range (SFDR) is defined as the ratio of the input signal to the largest peak of spur or harmonic distortion tone. Spurious-free dynamic range (SFDR) is the strength ratio of the fundamental signal to the strongest spurious signal in the output. It is also defined as a measure used to specify ADCs and DACs, respectively and radio receivers.SFDR is presented mathematically in Equation ,SFDR = 20 $\log_{10}$ (Vsignal/(V_{noise}+V_{HD})).

3.2.5 SIGNAL TO NOISE DISTORTION RATIO (SINAD)

Signal-to-noise and distortion ratio (SINAD) is a measure of the quality of a signal from a communications device, often defined as

$$\mathrm{SINAD} = \frac{P_{\mathrm{signal}} + P_{\mathrm{noise}} + P_{\mathrm{distortion}}}{P_{\mathrm{noise}} + P_{\mathrm{distortion}}}$$

where P_{signal} ,P_{noise} and $P_{distortion}$ is the average power of the signal, noise and distortion components. SINAD is usually expressed in dB and is quoted alongside the receiver RF sensitivity, to give a quantitative evaluation of the receiver sensitivity. Note that with this definition, unlike SNR, a SINAD reading can never be less than 1 (i.e. it is always positive when quoted in dB).

3.2.6 EFFECTIVE NUMBER OF BITS (ENOB)

Effective number of bits (ENOB) is a measure of the dynamic range of an Analog-to-Digital converter (ADC) and its associated circuitry.

$$\mathrm{ENOB} = \frac{\mathrm{SINAD} - 1.76}{6.02}$$

CHAPTER 4

SUCCESSIVE APPROXIMATION REGISTER ADC

4.1 INTRODUCTION

Basic understanding of ADCs with different types and literature study on various comparators which is part od ADC is described in previous chapters.Hence,In this project,An improved double tail dynamic latch comparator for 8 bit SAR ADC is designed in 130nm technology in tanner tool with the power consumption of 326.9 μW.

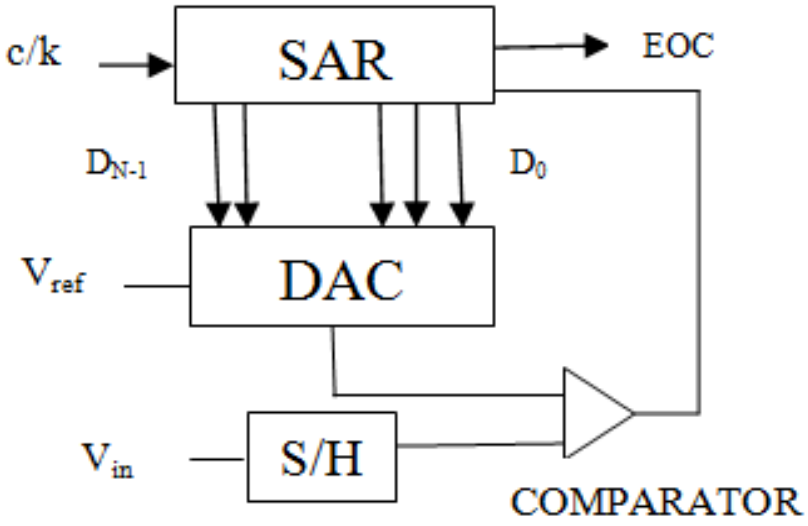


Figure 4.1 Basic Block of SAR ADC

The basic block diagram of SAR ADC is shown in Figure4.1 .The block includes sample and hold circuit, successive approximation register, digital-to-analog converter and an analog voltage comparator. The successive approximation register is begun with the most significant bit (MSB) is equal to a digital 1. This code is sent into the DAC, which then supplies the analog equivalent of this digital code ($V_{ref}/2$) into the comparator circuit for comparison with the input sampled voltage. If this analog voltage exceeds V_{in} the SAR resets this bit; otherwise, the bit is left as 1. Then the next bit is set to 1 and the same progress is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital code of the sampled input voltage and is

finally drawn as output from the SAR at the end of the conversion (EOC).

4.2 R-2R LADDER DAC

R/2R ladder networks provide a simple means to convert digital information to an analog output. Although simple in design and function, applying an R/2R resistor network to a real application requires attention to how the device is specified. Output errors due to resistor tolerances are often overlooked in the design of the digital to analog conversion (DAC) circuit and in the selection of the R/2R ladder itself. This application note identifies these issues, provides methods for calculating R/2R resolution and accuracy and a means to better specify R/2R ladder networks.Hence R-2R ladder structure is uesd dor DAC.

Resistor ladder networks provide a simple, inexpensive way to perform digital to analog conversion (DAC). The most popular networks are the binary weighted ladder and the R/2R ladder. Both devices will convert digital voltage information to analog, but the R/2R ladder has become the most popular due to the network's inherent accuracy superiority and ease of manufacture. Figure 4.2 is a diagram of the basic R/2R ladder network with N bits. The "ladder" portrayal comes from the ladder-like topology of the network. Note that the network consists of only two resistor values; R and 2R (twice the value of R) no matter how many bits make up the ladder. The particular value of R is not critical to the function of the R/2R ladder.

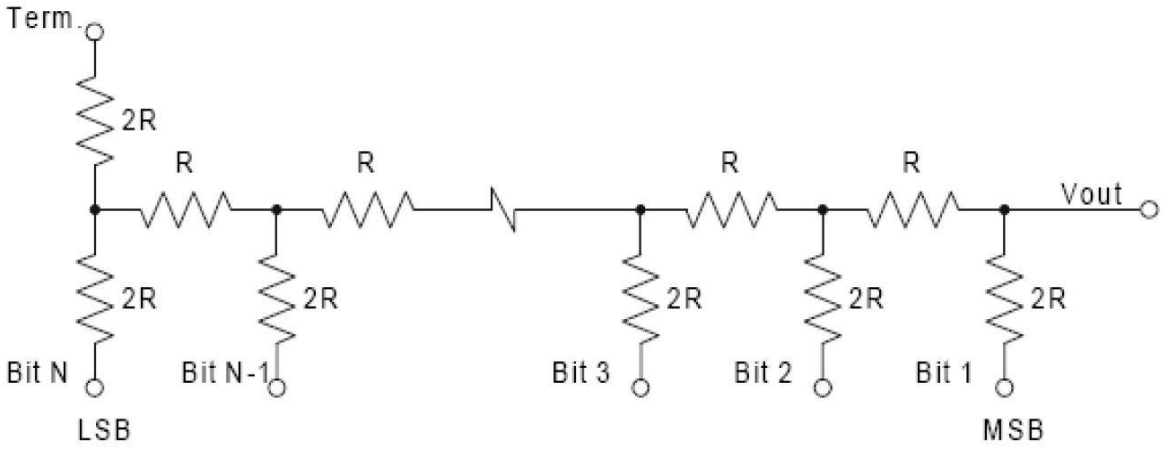


Figure 4.2 Basic Structure of R-2R ladder DAC

The R/2R ladder works as follows. The expression "Term" in Figure 4.2 is the termination resistor and is connected to ground. The termination resistor assures that the Thevenin resistance of the network as measured to ground looking toward the LSB (with all bits grounded) is R as shown

in Figure 4.3. The Thevenin resistance of an R/2R ladder is always R regardless of the number of bits in the ladder.

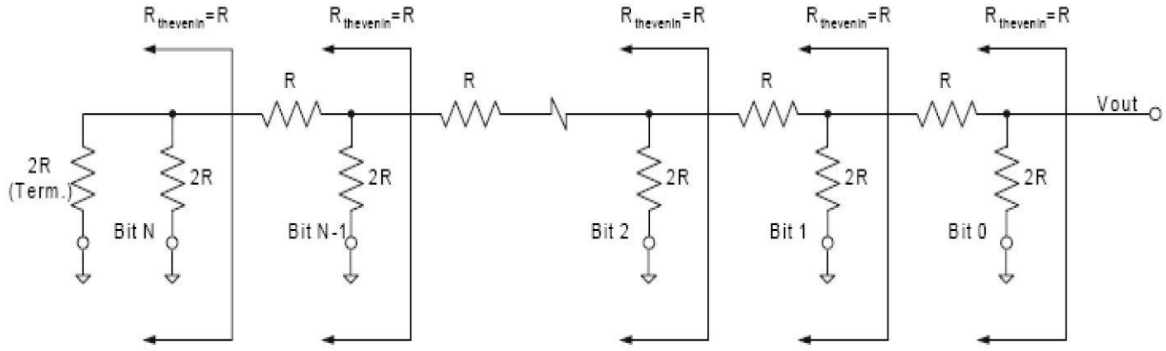


Figure 4.3 Thevenin's Resistance of Ladder Structure

Digital information is presented to the ladder as individual bits of a digital word switched between a reference voltage (Vr) and ground (Figure 4). Depending on the number and location of the bits switched to Vr or ground, Vout will vary between 0 volts and Vr. If all inputs are connected to ground, 0 volts is produced at the output, if all inputs are connected to Vr, the output voltage approaches Vr, and if some inputs are connected to ground and some to Vr then an output voltage between 0 volts and Vr occurs.

These inputs (also called bits in the digital lingo) range from the Most Significant Bit to the Least Significant Bit. As the names indicate, the MSB, when activated, causes the greatest change in the output voltage and the LSB, when activated, will cause the smallest change in the output voltage. If we label the bits (or inputs) bit 1 to bit N the output voltage caused by connecting a particular bit to Vr with all other bits grounded is: Vout = Vr/2N where N is the bit number. For bit 1, Vout =Vr/2, for bit 2, Vout = Vr/4 etc.

4.2.1 RESOLUTION AND ACCURACY

The number of inputs or bits determines the resolution of an R/2R ladder. Since there are two possible states at each input, ground or Vr, (also designated as “0” or “1” in digital lingo for positive logic) there are 2N combinations of Vr and ground to the inputs of an R/2R ladder. The resolution of the ladder is the smallest possible output change for any input change to the ladder and is given by 1/2N where N is the number of bits. This is the output change that would occur for a change in the least significant bit. For a 10bit R/2R there are 2N or or 1024 possible binary

combinations at the inputs. The resolution of the network is 1/1024 or 0.0009766. A change in state at the LSB input should change the output of the ladder by .09766% of the full scale output voltage.The output accuracy of the R/2R ladder is typically specified in terms of full-scale output ± some number of least significant bits. R/2R ladders are usually specified with output accuracies of ±1 LSB or ±1/2 LSB. For example, a ±1/2 LSB specification on a 10 bit ladder is exactly the same as ±0.04883% full-scale accuracy.

4.3 SUCCESSIVE APPROXIMATION REGISTER

Figure 4.4 shows a simplified SAR logic which is proposed by Anderson. It is based on a ring counter and shift registers. In this work, a binary search SAR is implemented based on this approach. The detailed operation of this circuit will be explained as follows

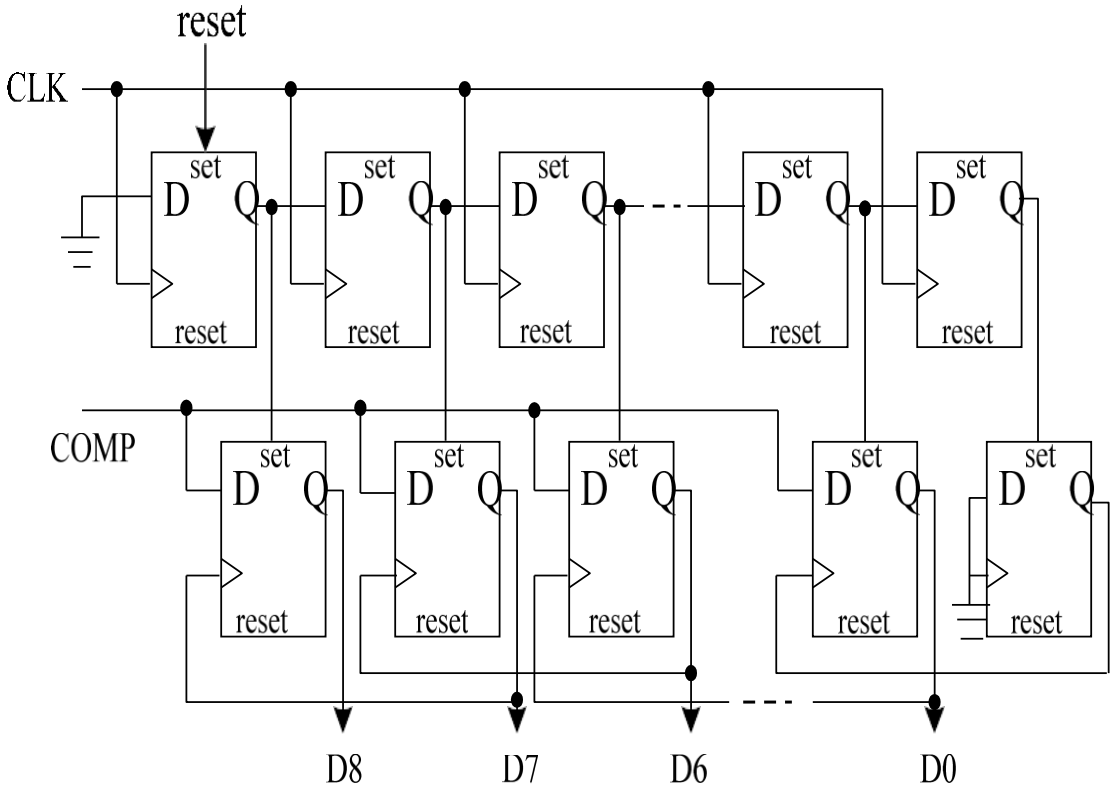


Figure 4.4 Simplified SAR Logic

SAR supports three main operations: First, it shifts the initial guess “one” to the right by one bit; secondly, it loads the result from the comparator by the positive triggering of next nearest bit; thirdly, it holds the determined bits. After 9 clocks, SAR outputs a pulse, which means that one

whole conversion is completed. The signal eoc in the above figure is generated to indicate the start of the next sampling. Table 4.1 gives the detailed explanation of Successive approximation algorithm. In step 0, all the data outputs are reset to zero and EOC is set to one. In step 1, SAR outputs a guess 'one' of D8 and EOC returns to zero. Meanwhile, the comparator decides the real value of D8. In step 2, SAR loads the result of D8 and again makes a guess 'one' of D7. Following this sequence, SAR completes one conversion through 9 clocks in total.

Step	DAC								EOC	COMP
0	0	0	0	0	0	0	0	0	1	-
1	1	0	0	0	0	0	0	0	0	D8
2	D8	1	0	0	0	0	0	0	0	D7
3	D8	D7	1	0	0	0	0	0	0	D6
4	D8	D7	D6	1	0	0	0	0	0	D5
5	D8	D7	D6	D5	1	0	0	0	0	D4
6	D8	D7	D6	D5	D4	1	0	0	0	D3
7	D8	D7	D6	D5	D4	D3	1	0	0	D2
8	D8	D7	D6	D5	D4	D3	D2	1	0	D1

Table 4.1 SAR Algorithm for 8 bit ADC

4.3.1 D FLIP FLOP WITH SET AND RESET

There are several types of D Flip-Flops (DFF). The transmission-gate based (TGMS) Flip-flop shown in Figure 4.5 has reduced delay measure in 130 nm CMOS process. The logic of the set and reset is: if Reset= High, q outputs 0; if Reset= Low and Set= High, q outputs 1; if Reset= Low and Set= Low, q remains its initial value. The sizing of the DFF, same as the above digital design, is kept minimum size and appropriate P/N ratio.

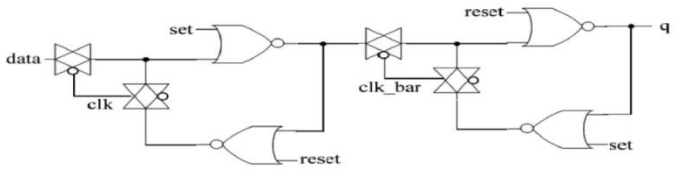


Figure 4.5 Transmission -gate based Flip-flop

4.3.2 SR OUTPUT LATCH

Two cross coupled NOR gate constitutes a SR latch shown in figure 4.6.The SR latch

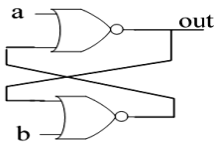


Figure 4.6 SR Latch

helps to keep the comparator result constant for the whole period of clock cycle. otherwise, The comparator output is always precharged to VDD at the reset mode.

4.4 SAMPLE AND HOLD CIRCUIT

In general, Sample and hold circuit (SHC) contains a switch and a capacitor. In the tracking mode, when the sampling signal is high and the switch is connected, it tracks the analog input signal. Then, it holds the value when the sampling signal turns to low in the hold mode. In this case, sample and hold provides a constant voltage at the input of the ADC during conversion. Regardless of the type of S/H (inherent or separate S/H), sampling operation has a great impact on the dynamic performance of the ADC such as SNDR.The sample and hold circuit is shown in fig 4.7

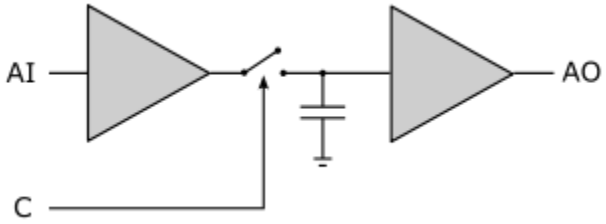


Figure 4.7 Sample and Hold Circuit

4.5 COMPARATOR

Comparator is a basic device for ADC. So, the requirement of better comparator is increasing. Some comparators are clocked and only provide an output after the transition of the clock. The value of the input to a clocked comparator is only of concern in a short time interval around the clock transition. The speed of clocked comparators can be very high and the power dissipation of clocked comparators can be very low. Clocked comparators are often called dynamic Comparators. Dynamic comparators are widely used in the design of high-speed ADC

Regenerative feedback is often used in dynamic comparators and occasionally in non-clocked comparators. Delay of signals should be reduced in ADC processing for faster conversion. New comparator is designed based upon the double tail structure as it consumes low voltage and it has better performance. In this external transistors are added to the double tail dynamic comparator for the positive feedback generation. The latch generation speed is increased in double tail comparator.The basic symbol of comparator is shown below in fig 4.8.

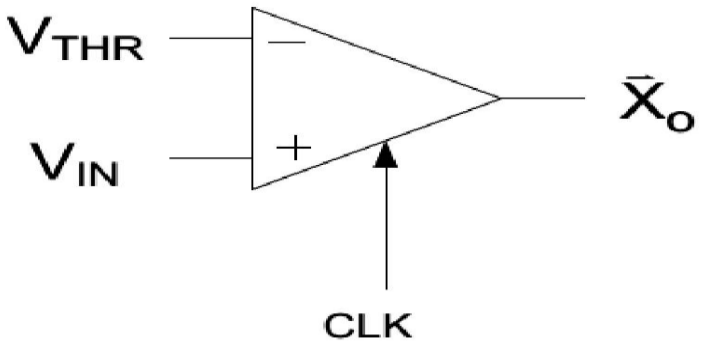


Figure 4.8 Basic Comparator Symbol

4.5.1 IMPORTANCE OF DUAL TAIL STRUCUTURE

High speed devices such as ADC, operational amplifier are of great importance and for this high speed application a major thrust is given towards low power methodologies. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and widerM_{tail2}, for fast latching independent of the input common-mode voltage (V_{cm}), and a small current in the input stage (small M_{tail1}), for low offset.

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise, offset, random decision errors and kick-back noise. The main idea of the new dynamic comparator is to increase $\Delta V_{fn/fp}$ in order to improve the latch regeneration. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but connected in a cross-coupled manner.

4.5.2 DESCRIPTION OF PROPOSED DOUBLE TAIL DYNAMIC LATCH COMPARATOR

The double-tail dynamic comparator due to the better performance of double-tail architecture in low-voltage applications, the comparator is designed based on the double-tail structure. The main idea of the comparator is to increase ΔVfn/fpin order to increase the latch regeneration speed. The operation of the comparator is during reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground.

During decisionmaking phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of the phase, the control transistors are still off (since fn and fp are aboutVDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding p MOS control transistor (Mc1 in the case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely.

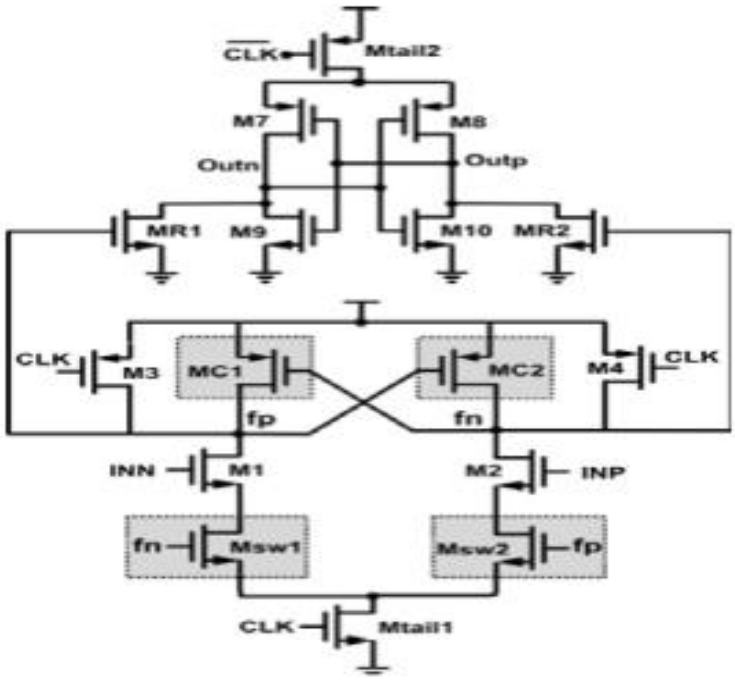


Figure 4.9 Proposed Double Tail Dynamic Latch Comparator

In other words, unlike conventional double-tail dynamic comparator, in which ΔVfn/fp is just a function of inpu ttransistor trans conductance and input voltage difference, in the structure as soon as the comparator detects that for instance node fn discharges faster, a PMOS transistor (Mc1) turns on, pulling the other node fp back to the VDD. Therefore by the time passing, the difference between fn and fp (ΔVfn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the idea, one of the points which should be considered is that in the circuit, when one of the control transistors (e.g., Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, and Mtail1), To overcome the issue two nMOS switches are used below the input transistors [Msw1 and Msw2]as shown in figure 4.9.

At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been precharged to VDD (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the VDD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from VDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

4.6 IMPLEMENTATION OF SAR ADC

SAR ADCs are frequently used architecture which is a choice for medium-to-high-resolution applications with sample rates under few mega samples per second (Msps). Resolution for SAR ADCs most commonly ranges from 8 to 16 bits, and they provide low power consumption as well as a small form factor. This combination of features makes these ADCs ideal for a wide variety of applications, such as portable/battery-powered instruments, pen digitizers, industrial controls, and data/signal acquisition. As the name implies, the SAR ADC basically implements a binary search algorithm. Therefore, while the internal circuitry may be running at several megahertz (MHz), the ADC sample rate is a fraction of that number due to the successive-approximation algorithm

4.6.1 CONVERSION MODE

A conversion mode determines how the ADC processes the input and performs the conversion operation. A standard ADC has basically two types of conversion modes.

- Single ended conversion mode.
- Differential conversion mode.

4.6.1.1 SINGLE ENDED CONVERSION MODE

In single ended conversion, only one analog input is taken and the ADC sampling and conversion is done on that input. In single ended conversion ADC can be configured to operate in unsigned or signed mode. The analog is connected to ADC has non-inverting (+) input and inverting (-) input which should be differently connected under signed or unsigned mode. For example in signed mode of operation, the single-ended input may be given to the non-inverting input of the ADC and the inverting input of the ADC is grounded shown in Figure 4.10. In this case the reference voltage is from – VREF to + VREF, which means it, allows negative input voltages.

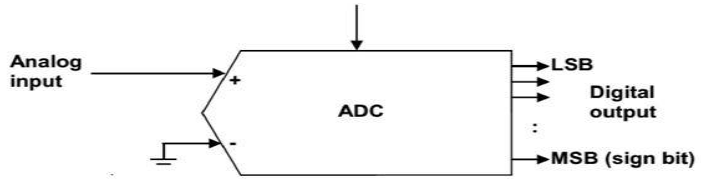


Figure 4.10 Signed Mode of Operation

In unsigned single-ended mode, the single-ended input is given to the non-inverting input of the ADC as before and the inverting input of the ADC is supplied with some fixed voltage value VFIXED which is usually half of the reference voltage minus a fixed offset) as shown in Figure 4.11. In this case the input voltage range is from 0V to VREF, which means it does not allows negative input voltages.

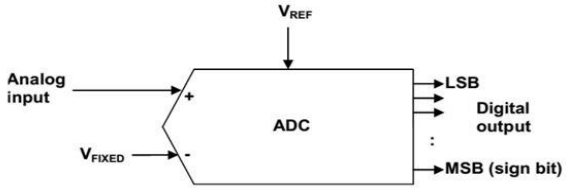


Figure 4.11 Unsigned Mode of Operation

4.6.1.2 DIFFERENTIAL CONVERSION MODE

In differential conversion mode, two analog inputs are taken and applied to the inverting and non-inverting inputs of the ADC, either directly or after doing some amplification by selecting some programmable amplification stages such as gain amplifier stage. Differential conversions are usually operated in signed mode, where the MSB of the output code acts as the sign bit. Also the reference voltage is from -VREF to +VREF for signed mode.The figure 4.12 below illustrates the differential conversion mode.

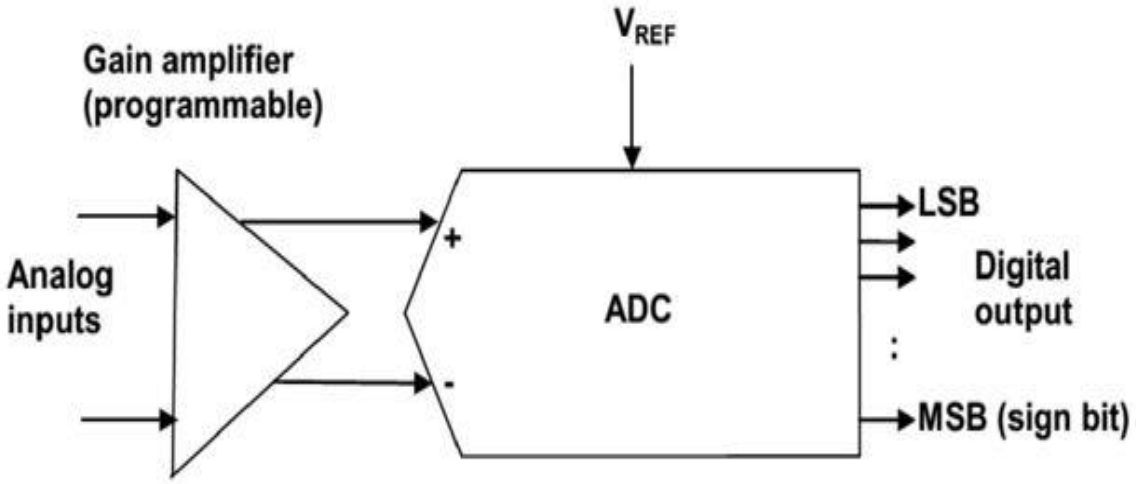


Figure 4.12 Differential Conversion Mode

Proposed ADC is designed in unsigned single-ended mode, where single-ended input is given to the non-inverting input of the ADC as before and the inverting input of the ADC is supplied with some fixed voltage value which is usually half of the reference voltage shown in Figure 4.11. An ideal ADC is just a theoretical concept, and cannot be implemented in real life. It has infinite resolution, where every possible analog input value gives a unique digital output from the ADC within the specified conversion range. An ideal ADC can be described mathematically by a linear transfer function as shown in below Figure 4.13.Eventhough SAR ADC can be implemented in two conversion modes,The practically implementable design is Unsigned single

ended mode which is described above along with the signed architecture also.

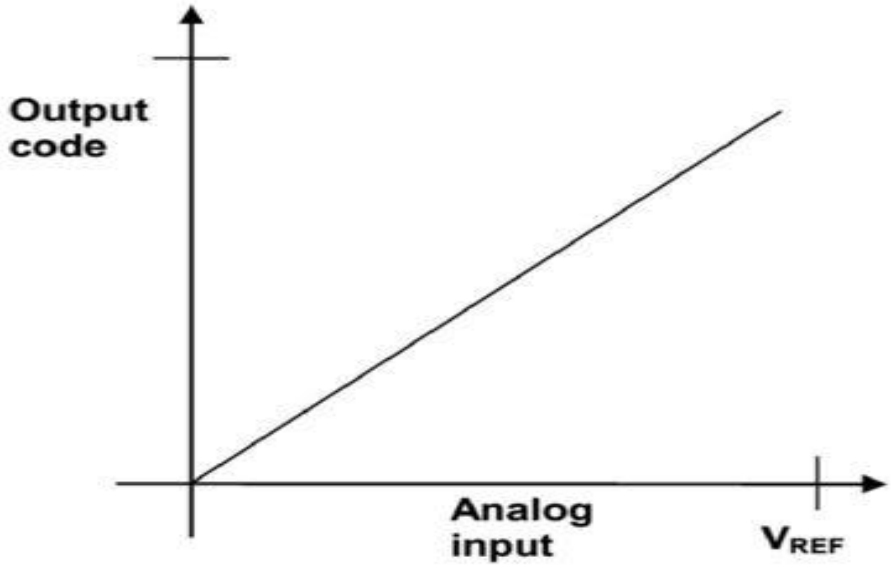


Figure 4.13 Linear Transfer Function of Ideal ADC

Hence,The Various Blocks of SAR ADCs with its proposed improved comparator structure have been described in detail in this chapter,therefore all the blocks are combined,simulated in the software tools and the corresponding parameters which measure the performance of the structure have been analysed and compared for various structures of SAR ADC with the conventional comparator and the proposed comparators in the next chapters. The power consumption and delay timings form the major parameters which determine the efficiency of the structure.

The software tool used here is Tanner electronic Design Automation of version 13.0.The tool has a lots of advanced feature inorder to process the schematic structures and retrieve the parameters such as power factor,Noise factors etc to compare the various structures.The detailed description of the Software Tool Tanner is described below with its stages of Simulation flow and various schematic structures and Simulation Results have been Screenshoted and shown in next coming chapters with the tabulation and comparison of parameters of both conventional dynamic latch comparator and proposed dual tail dynamic latch comparator.The relevant technology adopted for the above said software is 130nm technology.hence The nm can be decreased by using various other softwares such as microwind,cadence virtuoso etc

CHAPTER 5

SIMULATION RESULTS

5.1 INTRODUCTION TO SPICE MODELING

Simulating a circuit design before committing it to silicon is always the wise thing to do, since problems can be caught before they become costly mistakes. Analog designers mostly prefer spice models of analog-to-digital converters (ADCs). An SAR ADC compares an analog input signal to a reference voltage and produces a digital representation of that comparison. Conversion accuracy depends primarily on how accurately the signal is captured. If the signal has perfectly settled, the results of the conversion will accurately represent that signal (minus the inherent error of the ADC).

If the input drive circuitry does not permit the analog input signal to settle to the correct value, the conversion will be incorrect. Tanner V13.0 EDA tool is used for backend design and simulation work in this project. Tanner's schematic and simulation tools are fully integrated to allow AC, DC, or transient analysis of design, with interactive setup, simulation, and post-processing. The three components of this process are S-Edit, T-Spice, and W-Edit, and there are three primary stages to the simulation flow:

- In the setup stage, entered commands and information which describe the type of simulation (DC, AC, transient, etc.), and establish the simulator options and outputs.

- S-Edit is a fully hierarchical computer-aided schematic capture application for the logical design of integrated circuits. In the design export and simulation stage, S-Edit generates a SPICE file (a netlist) from the design. Then, T-Spice simulates the SPICE file to create a probing data file with voltage and current value for each node and device in the design, and for each analysis specified in the SPICE file.

- In the probing stage, W-Edit displays traces from the probe data file corresponding to an analysis type and a specific net or device selected in S-Edit. S-Edit can also annotate schematic with node voltages and device terminal currents and charges.

5.2 BACK END DESIGNS AND RESULTS

Design and simulation results of SAR ADC and comparators are shown in following figures with power and delay measurements

5.2.1 R-2R LADDER DAC

schematic design of R-2R ladder structure for DAC is drawn in Tanner EDA tool is shown in fig 5.1

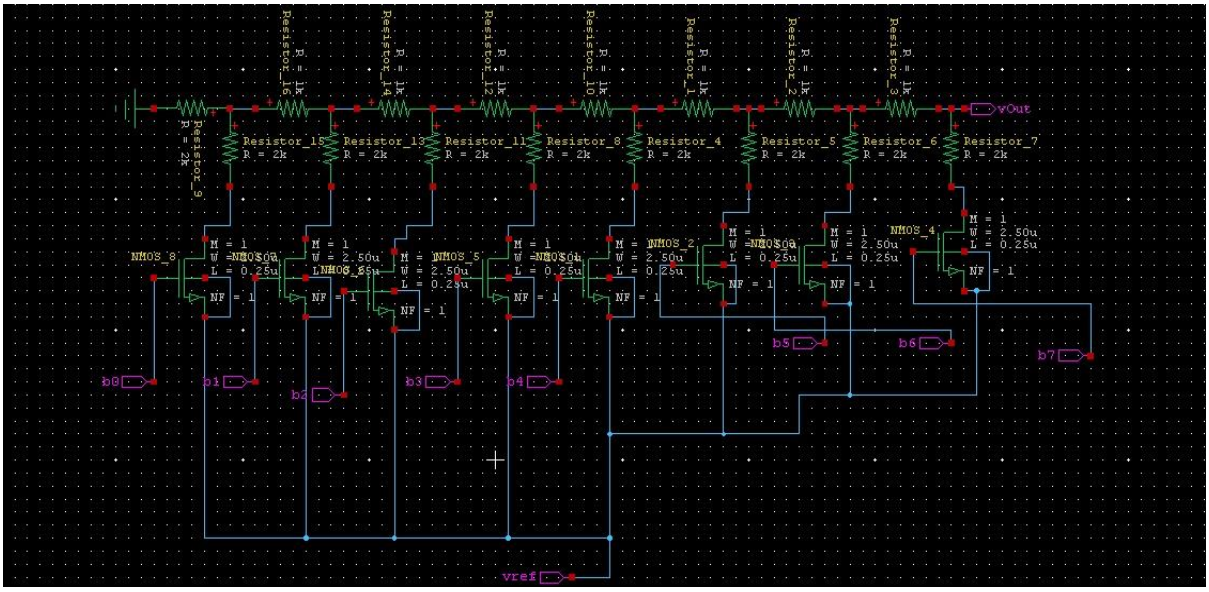


Figure 5.1 R-2R Ladder Structure DAC

5.2.2 SUCCESSIVE APPROXIMATION REGISTER

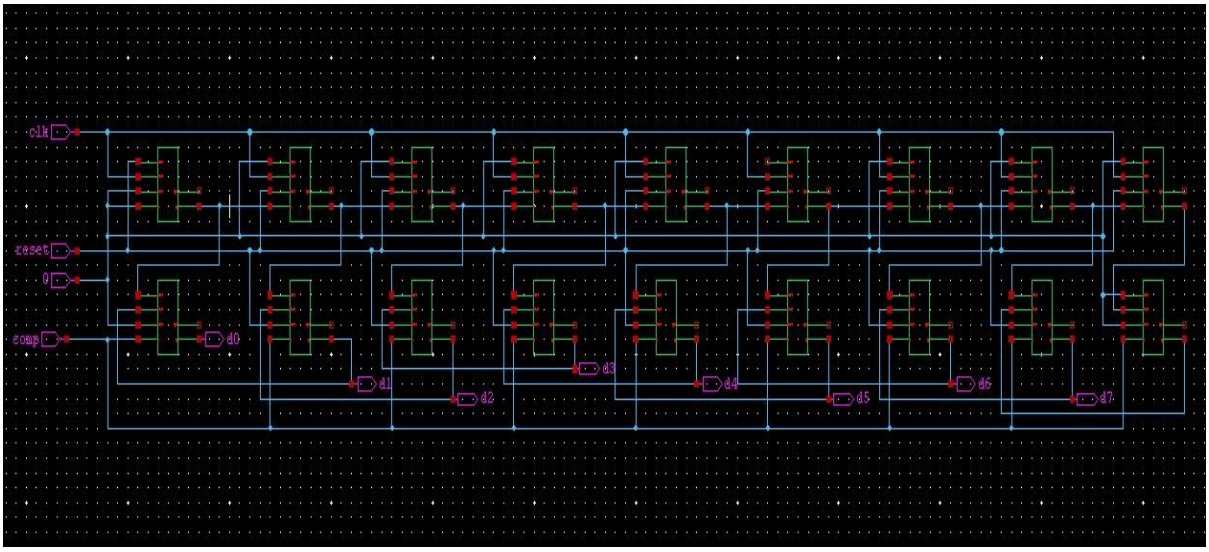


Figure 5.2 Successive Approximation Register

schematic design of successive approximation register structure is drawn in Tanner EDA tool is shown in the above fig 5.2.

5.2.3 CONVENTIONAL COMPARATOR

Schematic design of conventional comparator is shown in fig 5.3

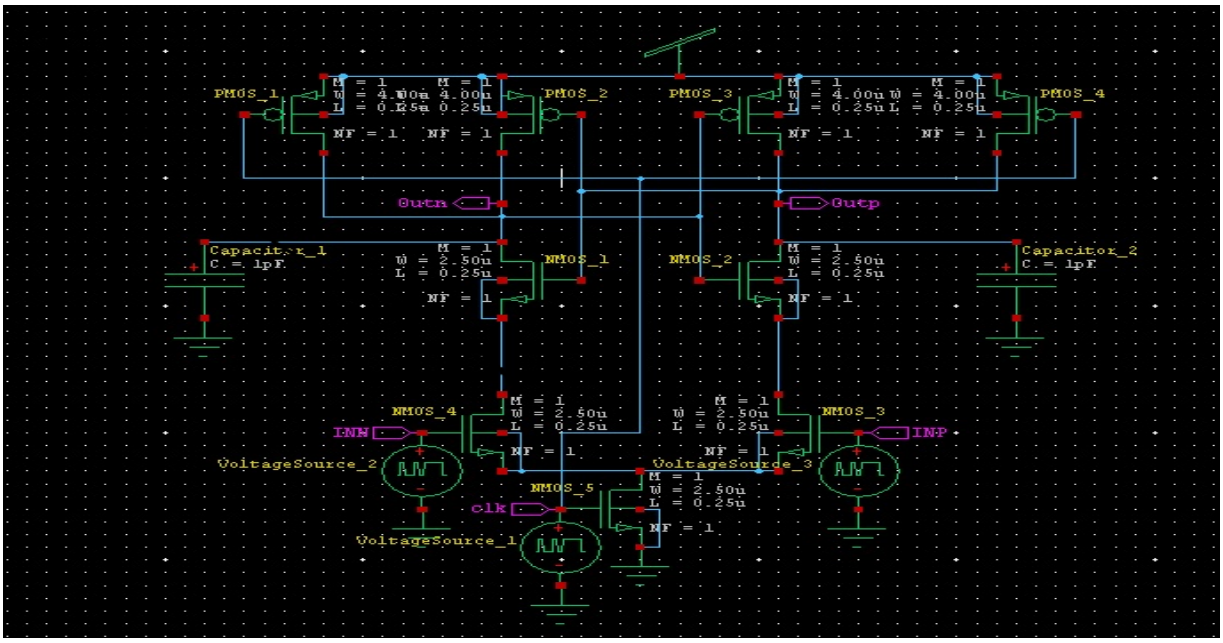


Figure 5.3 Conventional Dynamic Latch Comparator

Simulation result of conventional comparator is shown in figure 5.4 below

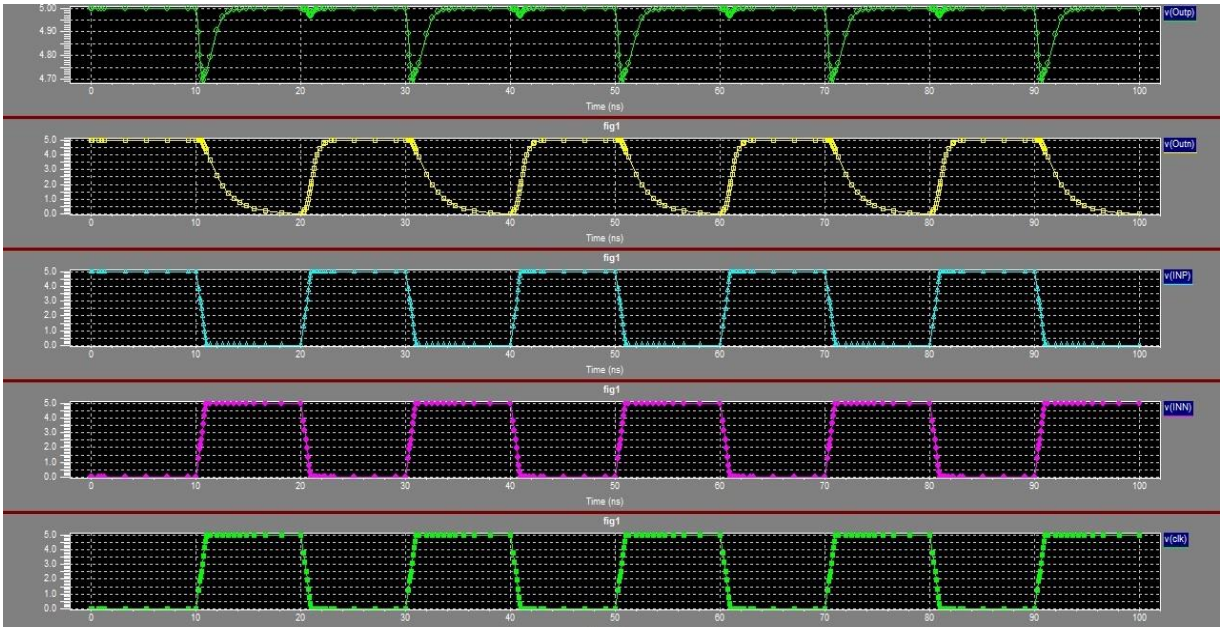


Figure 5.4 Simulation Results of Conventional Comparator

5.2.4 PROPOSED DOUBLE TAIL DYNAMIC LATCH COMPARATOR

Schematic design of proposed comparator is shown in fig5.5.

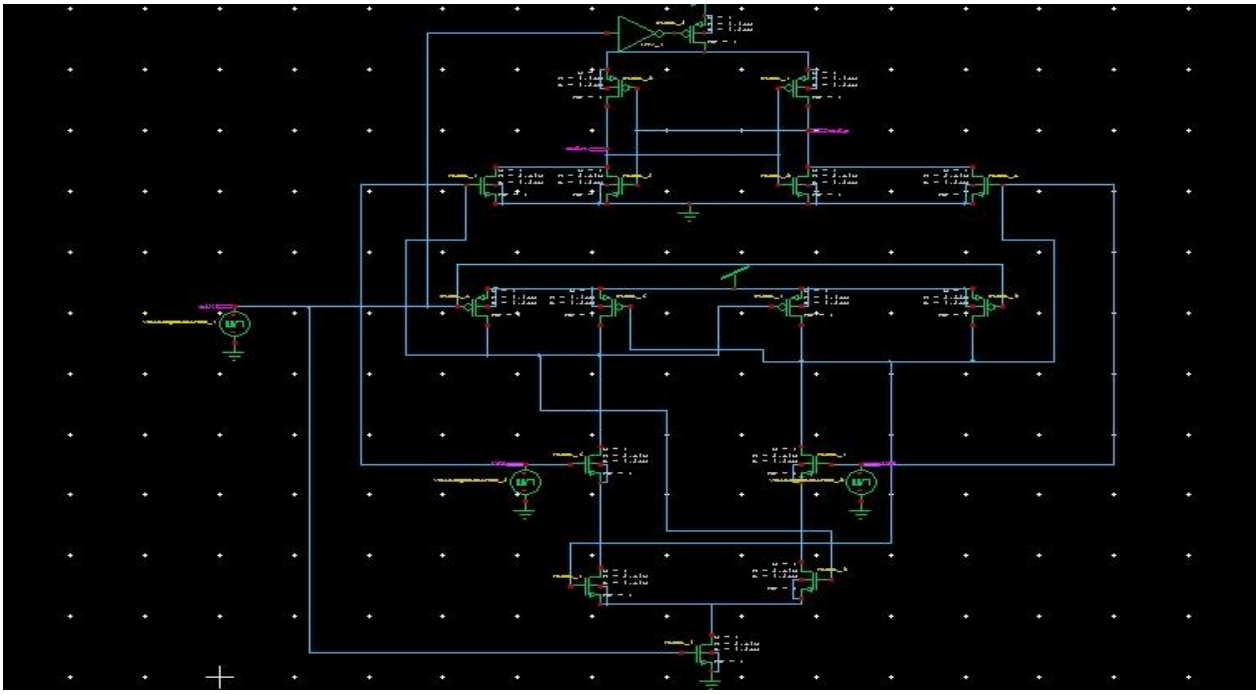


Figure 5.5 Proposed double tail Dynamic Latch Comparator

The corresponding simulation results of proposed comparator is shown in fig 5.6

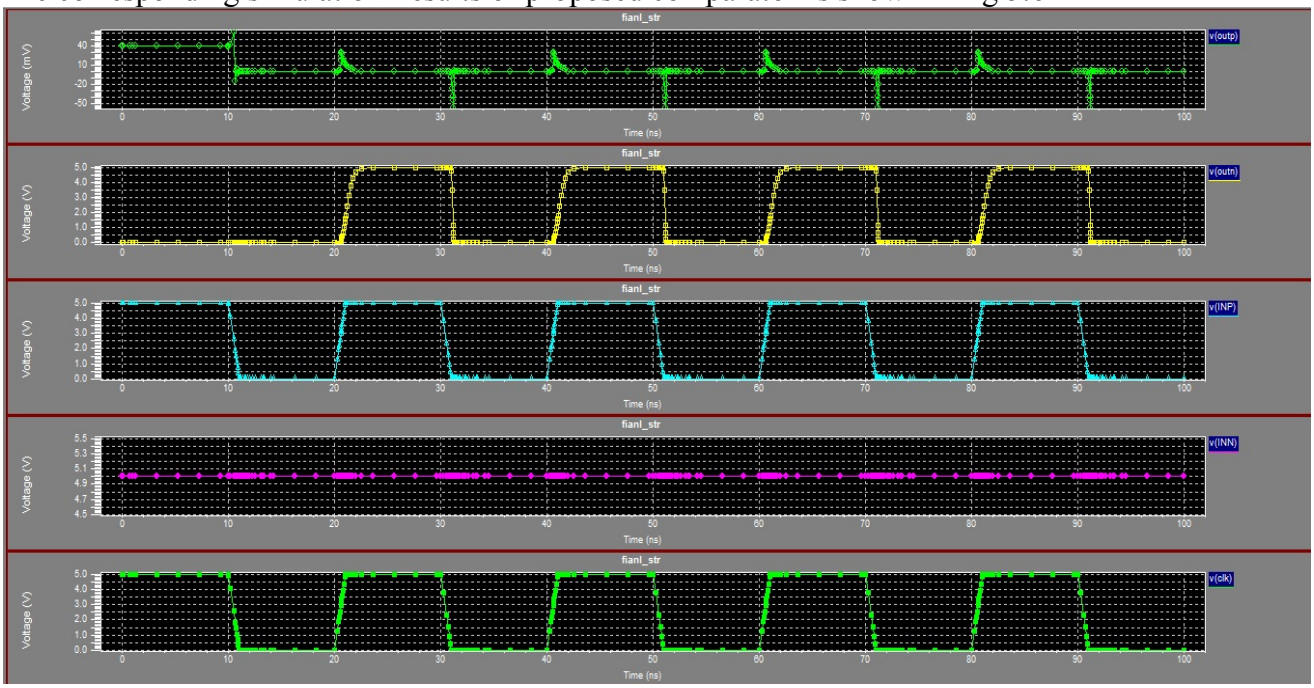


Figure 5.6 Simulation Results of Proposed comparator Structure

5.2.5 8 BIT SAR ADC WITH CONVENTIONAL COMPARATOR

schematic design of SAR ADC with the conventional comparator is shown in fig 5.7

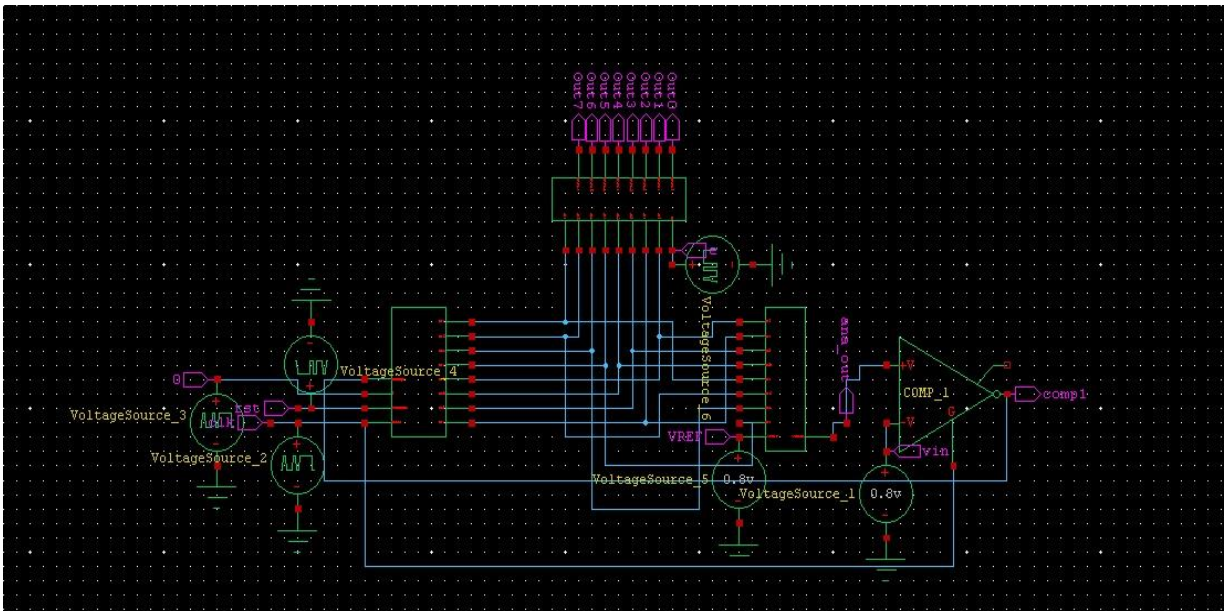


Figure 5.7 SAR ADC Designed with conventional comparator

The respective simulated output of the conventional SAR ADC is shown below in fig 5.8

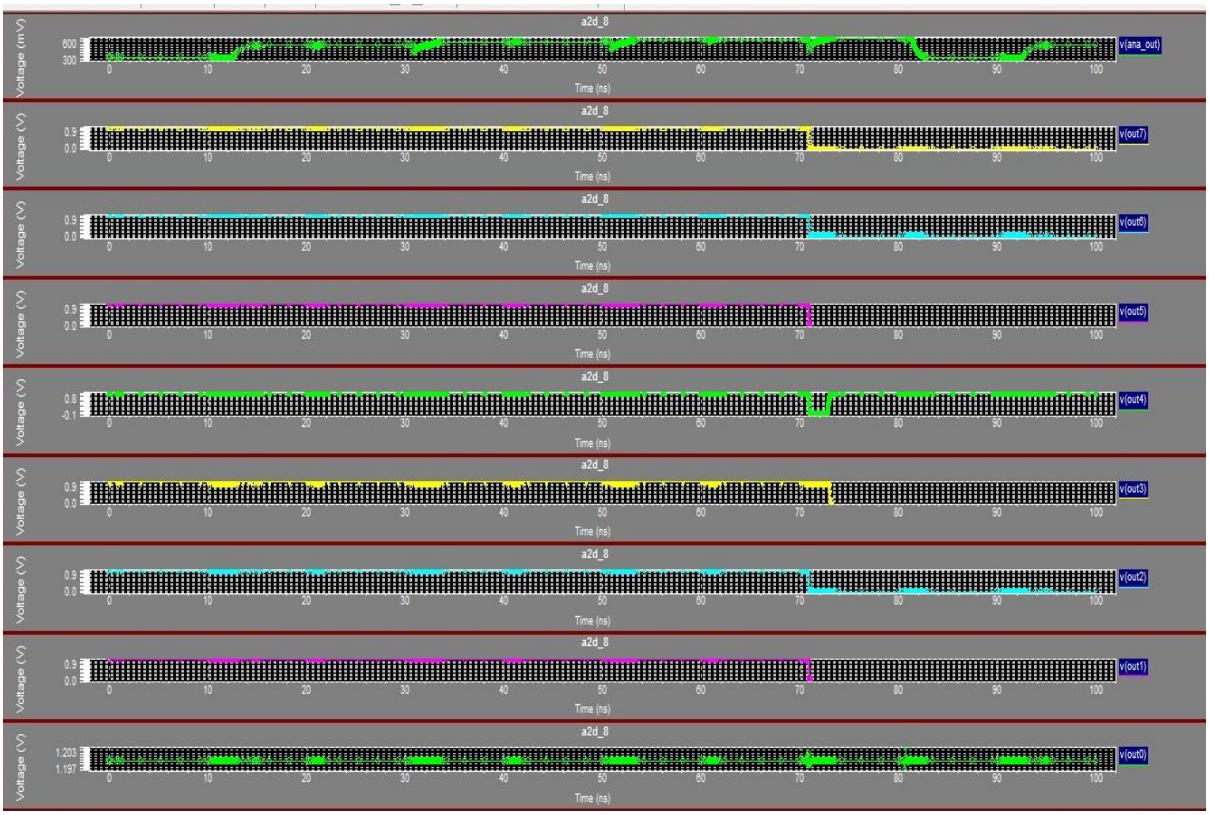


Fig 5.8 Simulated output of SAR ADC designed with conventional comparator

5.2.6 8 BIT SAR ADC WITH PROPOSED DOUBLE TAIL DYNAMIC LATCH COMPARATOR

schematic design of SAR ADC with the proposed comparator is shown in fig 5.9

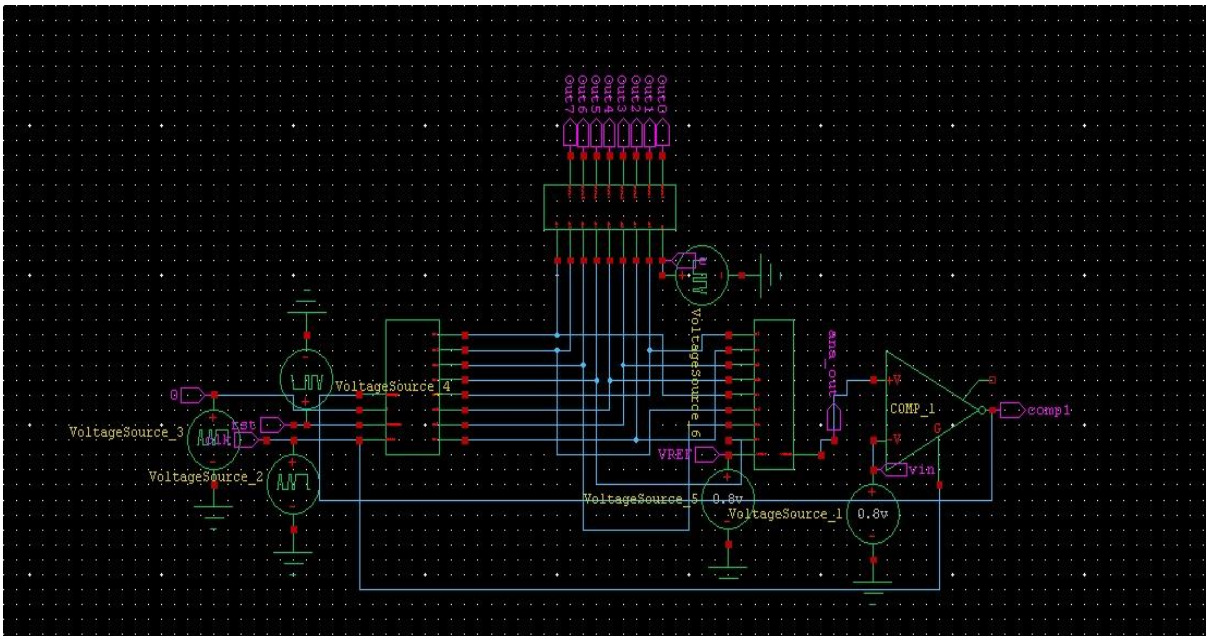


Figure 5.9 SAR ADC designed with Proposed Comparator Structure

The respective simulated output of the SAR ADC with the proposed comparator is shown below in fig 5.10

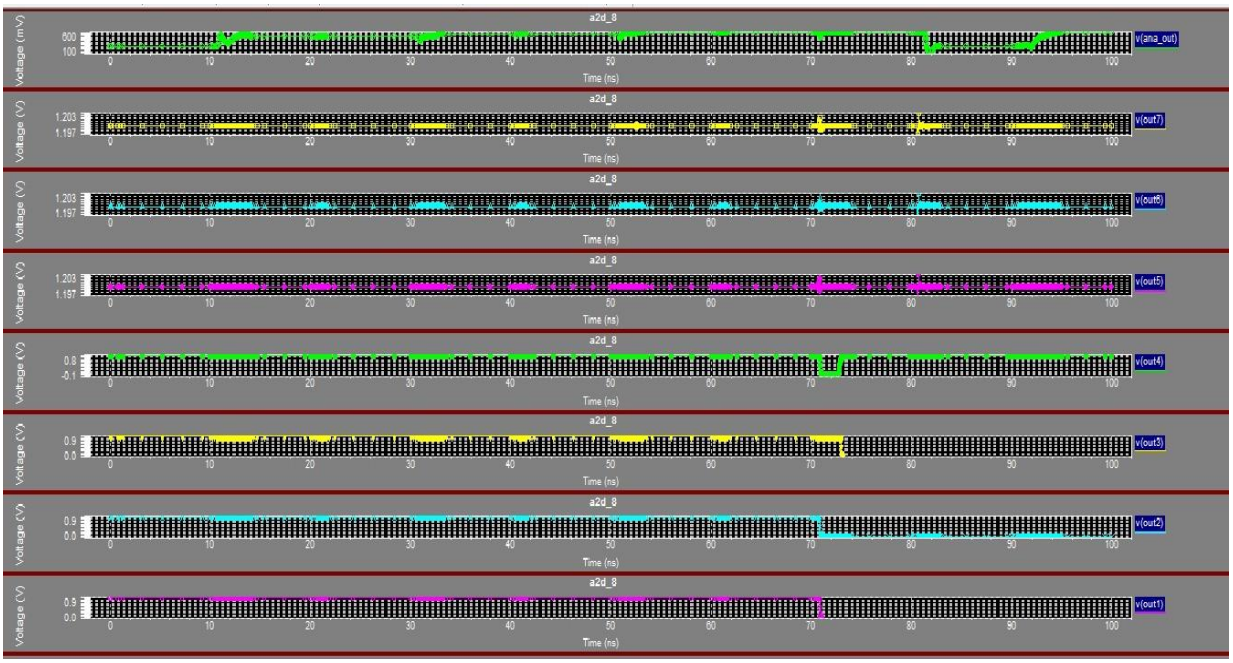


Figure 5.10 Simulated output of SAR ADC designed with Proposed Comparator Structure

5.3 DESIGN SUMMARY

Table 5.1 summarizes the design parameters of 130 nm CMOS technology specifications.

Table 5.1 Features of cmos 130nm technology

CMOS SPECIFICATIONS(130-nm technology)	
Lithography	**130 nm**
Supply voltage	**1.2 V**
Input Range	**0-0.8 V**
Sampling Frequency	**1 KHZ**
Temperature	**25°C(Nominal)**

5.4 PERFORMANCE METRICS OF TWO SAR ADCs

The various parameters which measure the performance of the ADC such as power consumption,Signal to noise distortion ratio ,Spurious free dynamic Range ,Effective number of bits are processed by the software and comparison is made as shown below in table 5.2

Table 5.2 power and noise parameters of SAR ADCs designed with conventional and proposed comparator

Parameters	ADC with Conventional Comparator	ADC with Proposed Dual tail comparator
Power(μW)	**370.86**	**326.9**
SINAD(DB)	**34.5698**	**32.0412**
SFDR(DB)	**65.3256**	**79.7216**
ENOB(bits)	**5.0456**	**5.0301**

5.5 PERFORMANCE METRICS OF TWO COMPARATORS

Table 5.3 provides the design specification and parameters like delay ,rise time ,fall time for the conventional and the proposed comparators so that the comparison can be made easily.

Table 5.3 power and delay parameters of two comparators

Design specification	Conventional Dynamic latch comparator	Proposed double tail dynamic latch comparator
Technology	**130nm**	**130nm**
Supply	**1.2v**	**1.2v**
Rise time	**2.35ns**	**1.34ns**
Fall time	**5.71ns**	**0.67ns**
Delay time	**1.34ns**	**1.18ns**
Power-Delay-product	**1.66**	**0.81**
Power consumption	**1.24mw**	**0.69mw**

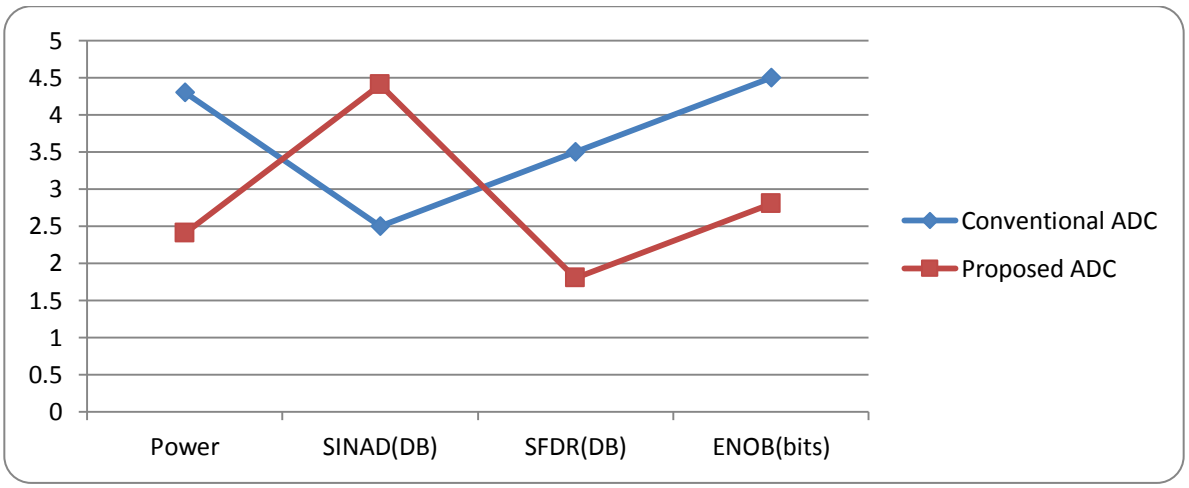


Figure 5.11 comparison plots of two ADC

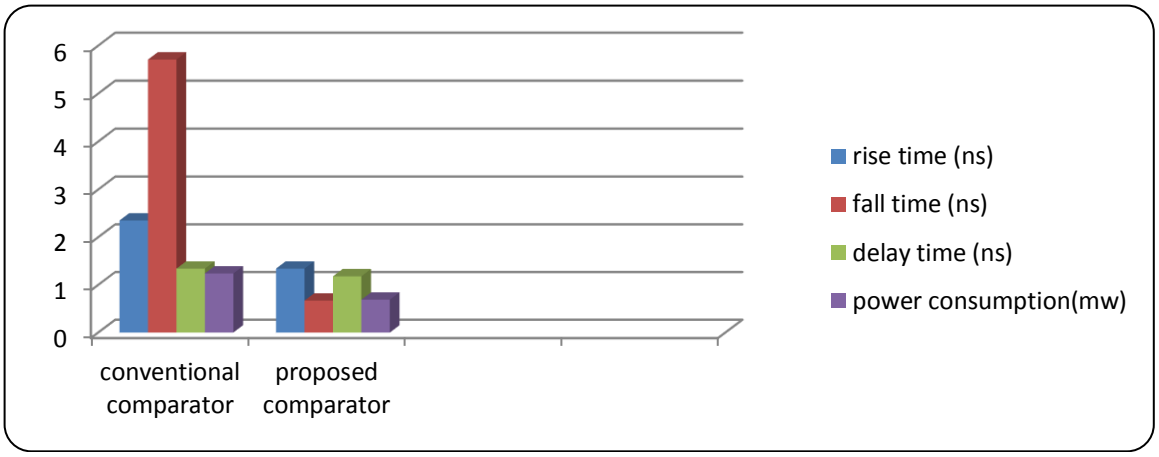


Figure 5.12 comparison plot of two comparators

5.6 COMPARISON RESULTS OF SEVERAL ADCs

Proposed SAR ADC configured with dual tail comparator which provides low power consumption with high speed and optimum resolution. Table 5.4 lists comparison of performance metrics of this work and several ADCs.

Table 5.4 Performance metrics of different ADCs

Sources	This work	Conventional ADC	10	11	23	24
Technology(nm)	130	130	250	180	180	90
Resolution(bit)	8	8	8	9	12	9
Supply Voltage(V)	1.2	1.2	1	1	1	1
Sampling rate(S/s)	12.5M	12.5M	100K	150K	100K	20M
Input Range(V)	0.8	0.8	1	0.5	N/A	N/A
ENOB(bit)	8	8	7.9	8.2	10.55	7.8
Power Consumption(W)	326.9 µ	370.86 µ	3.1µ	30 µ	25 µ	290 µ

CHAPTER 6
CONCLUSION AND FUTURE SCOPE

Modern portable and wireless applications are driving ADC design towards higher resolution and data rates with dramatically low power in scaled CMOS technology. Among the two critical components such as Comparator and DAC in SAR ADC,The speed of the ADC is limited by Comparator since it must resolve small differences in V_{in} and V_{ref} of dac within specified time. So the proposed SAR ADC utilizing the double tail dynamic latch comparator which is a low power consumer correspondingly reduce the power consumption of SAR ADC thereby making it more efficient for Biomedical applications than the conventional one. SAR ADC can benefits from the scaled CMOS because it is opamp less structure and occupies less area. This work explores design of SAR ADC with the proposed dual tail comparator that employs reduced latch delay time and offers low power consumption at small supply voltages. The current work presents implementation of 8-bit SAR ADC operating at 12.5MS/s and supply voltage of 1.2 V in 130nm CMOS technology. The power consumption of xx μw is achieved. The ADC employs an R-2R DAC, a dual tail dynamic latch comparator and a SAR control logic containing a sequencer and a ring counter. The ADC exhibits good performance and achieves ENOB of 8 bit. The priority of the future improvement is to design a more efficient SAR ADC with a lower supply voltage.

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