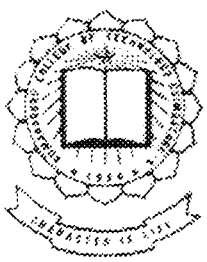
INDUSTRIAL AUTOMATION USING WIRELESS COMMUNICATION



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CERTIFICATE

This is to certify that the Project report entitled

INDUSTRIAL AUTOMATION USING

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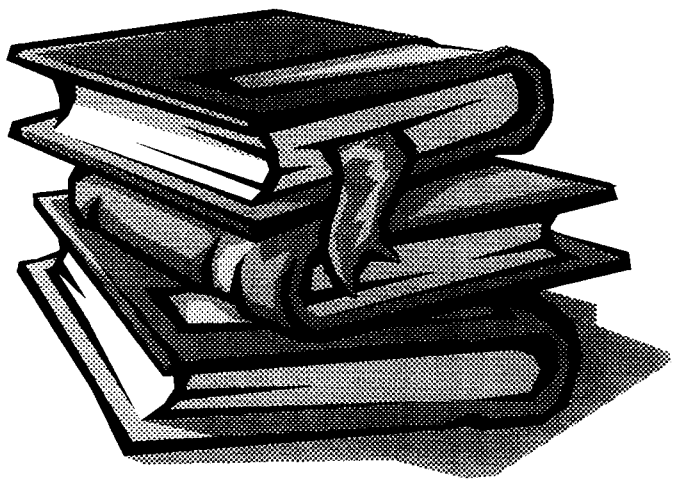

DEDICATED TO OUR BELOVED PARENTS AND FRIENDS

ACKNOWLEDGEMENT

We express our profound gratitude and sincere thanks to our guide **Mr.R.K.Pongiannan, B.E., MISTE, AMIE,** Lecturer, Department of Electrical And Electronics Engineering, Kumaraguru College of Technology, for his able guidance, constant encouragement and kind co-operation. Without his valuable suggestions, constructive criticism and meticulous guidance at every stage, this work would not have attained fruition.

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SYNOPSIS

As the fore coming scenario is AUTOMATION, automating the entire industrial processes is essential. We to be the pre-eminent engineers have made an attempt to do this project titled **"INDUSTRIAL AUTOMATION USING WIRELESS COMMUNICATION"**.

As the drive is used almost in all industrial process, the automation of stepper motor drive has been implemented using microcontrollers. In this system, a set value with wide range of speed including direction is programmed in the microcontroller.

The set value is given through a remote control switch to the FM Transmitter. In the Transmitter section, a DTMF encoder is used. It encodes the signals from the input device (i.e.) remote control switch and the tone signals at a particular frequency are produced. The signal is modulated with a carrier of frequency 97Mhz. The FM Transmitter transmits the modulated signal.

The FM receiver receives the Transmitter signal. The received signal is given to DTMF decoder. The Decoder decodes or senses the particular signal. This signal is given to input port of the 89C51 microcontroller, which is programmed to control the stepper motor. The output from microcontroller is fed to drive circuit, which drives the stepper motor.

CONTENTS

INTRODUCTION

Over the years, the problem of quality in industrial production has come to occupy the center stage in terms of priority. Stringent control of product quality has become the need of the hour. The manual methods of monitoring and controlling of industrial processes is time consuming and inaccurate. To overcome the inherent inadequancies of the manual technologies, an automation technique was conceived as a faster and more accurate alternative.

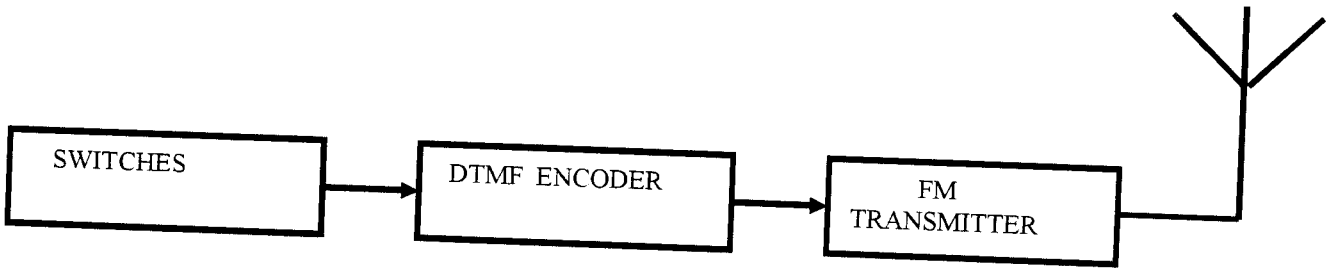
The automation system employs monitoring systems and modern control devices like microcontrollers, PLC's and wireless communication.

1.1 System Architecture

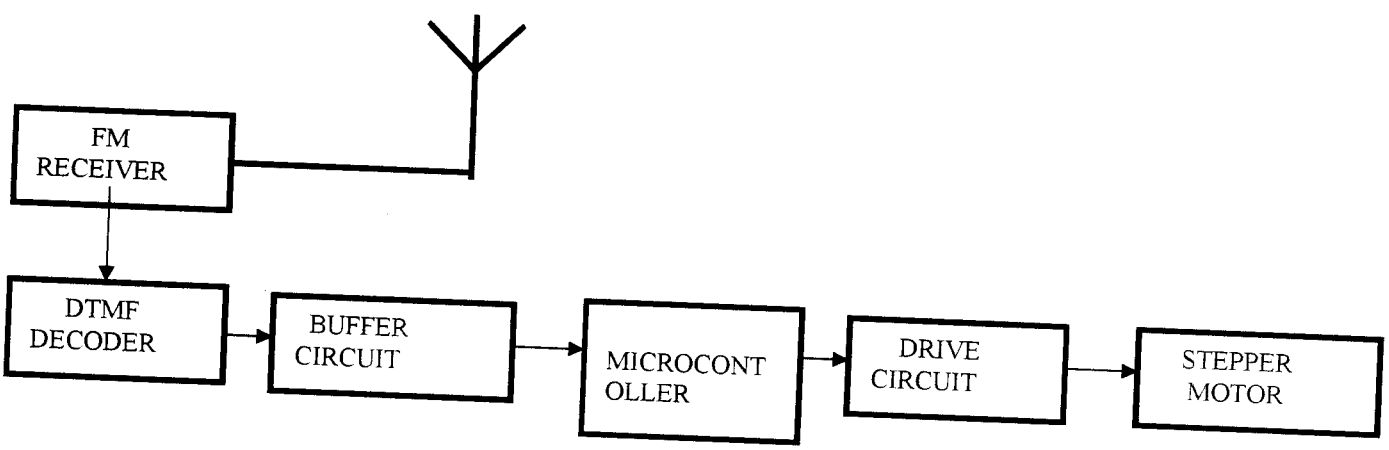
The automation system consists of the following functional units

- Transmitter
- Receiver
- Micro controller
- Stepper Motor

TRANSMITTER SECTION:



RECEIVER SECTION:



2 . HARDWARE DESCRIPTION

2.1 POWER SUPPLY

The figure shows the rectifier unit. This unit rectifies the input A.C and also regulates it .The power circuit consists of the following units.

2.1.1 Transformer:

In our project the secondary voltage of the step-down transformer is designed to be 9v . It's current rating is 0.75amps. The transformer is of shell type. The output of the secondary is given to rectifier.

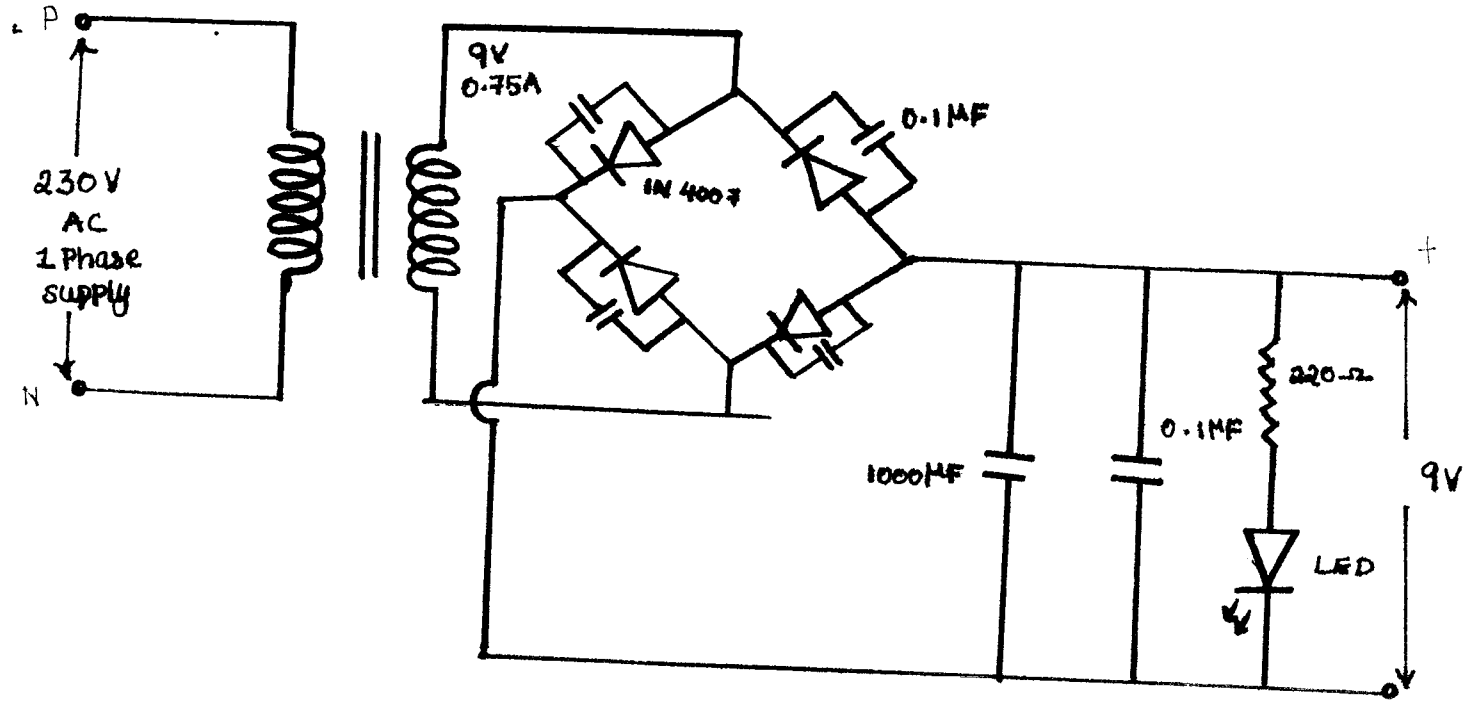
2.1.2 Rectifier:

The rectifier used in our project is full wave-bridge rectifier . The 9v output voltage from the transformer is given to the full wave bridge rectifier.

2.1.3 Full wave bridge rectifier:

In a full wave bridge rectifier four diodes are used. During the positive half cycle, diodes D1 and D3 conduct and during the negative half cycle, diodes D2 and D4 conduct. So we get the rectified D.C output. The voltage drop across the diode is 0.6v. The

POWER SUPPLY AND RECTIFIER CIRCUIT



rectified D.C voltage consists of A.C ripple components that should be filtered.

2.1.4 Filter circuit:

The output D.C voltage from the rectifier may contain A.C ripple components. We can filter or smooth out A.C variation from the rectifier voltage shunt capacitor and is normally used as a filter. A large capacitor shorted with a load resistor causes only a small part of A.C to pass through load, producing a small ripple voltage.

2.1.5 Voltage Regulator:

The function of voltage regulator is to provide a stable D.C voltage for powering other electronic circuits , independent of the load current , temperature and A.C line voltage variations. IC voltage regulators are used for the low cost , high reliability, and reduction in size and excellent performance . Examples of monolithic regulators are 78xx series and 723 general-purpose regulators , 78xx are three terminal , positive , fixed voltage regulators . The last two numbers indicates the output voltage. The ICs used in our circuits are 7805.

2.1.6 Transformer Design:

The transformer steps down the high voltage A.C signal to a suitable value for rectification .The most important factor to be considered while selecting the step –down transformer is the output load current .

INPUT :	=200V
OUTPUT :	= 9V/ 0.75A
RATING IN KA:	= 6.75KA
SAFETY MARGIN	= 0.3
PRIMARY CURRENT	= 0.01875A
TURNS (N)	= 10turns/volt
PRIMARY TURNS	= 2000 turns
SECONDARY TURNS	= 90 turns
PRIMARY CONDUCTOR SIZE	= 40swg
SECONDARY CONDUCTOR SIZE	= 24swg

2.1.7 Rectifier Selection:

The power supplies uses a full wave bridge rectifier circuit to rectify the A.C input signal .The diode selection is based on the diode rating.

Diode current, Id = 2 to 3 times the load current

$$Id = 3 * 750 \text{ mA}$$

$$Id = 2.5 \text{ A}$$

So, we have chosen a diode of current rating of 2.5 A for the full wave bridge rectifier circuit

2.2 DTMF ENCODER

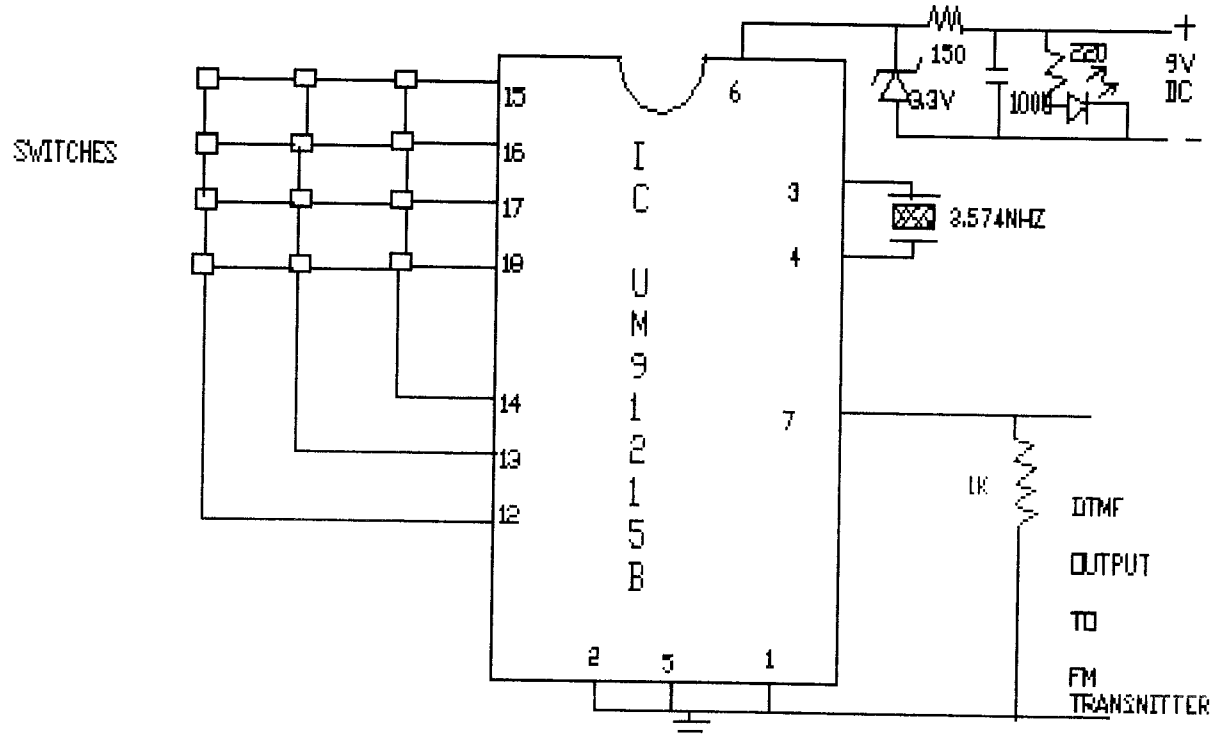
DTMF (Dual Tone Multiple Frequency) :

DTMF is generic name for push button telephone signaling equivalent to bell systems touch-tone. DTMF signaling is quickly replacing dial pulse signaling in telephone networks worldwide. It is also becoming popular in interactive control applications such as Telephone Banking or Electronic Mail systems in which the user can select options from a menu by sending mails through a telephone.

DTMF (dual tone multiple frequency) encoder IC type number MC912151B. This IC utilizes pairs of low audio frequencies to represent various codes that the designer wishes to transmit . The frequencies are generated from the various modular divisions of a crystal-controlled oscillator with a source frequency of 3.58MHz. This is fed into the keypad scan circuitry for clocking purposes and into the tone generator to provide the required frequencies.

For the control operations of the stepper motor switches are used. The switches are connected such that, pressing each switch the signals are produced at different frequency ranges from the encoder circuit. The carrier

DTMF ENCODER



frequency of the FM Transmitter used here is 97. MHz The signals at a frequency range from the encoder are frequency modulated with the carrier frequency and are transmitted from the FM transmitter.

DTMF Tones:

In DTMF encoder there are 16 distinct tones . Each tone is the sum of two frequencies : one from a low and one from a high frequency group . There are four different frequencies in each group, having four rows (R1, R2, R3 and R4) and 3 columns (C1, C2 and C3). The rows and columns select frequencies from the low and high frequency group respectively. The exact value of the frequencies are listed in Table 3 below:

DTMF row/column frequencies:

LOW-FREQUENCIES	
ROW #	FREQUENCY (HZ)
R1: ROW 0	697
R2: ROW 1	770
R3: ROW 2	852
R4: ROW 3	941
HIGH-FREQUENCIES	
COL #	FREQUENCY (HZ)
C1: COL 0	1209
C2: COL 1	1336
C3: COL 2	1477
C4: COL 3	1633

Thus using the above table, "2" has a frequency of 770 + 1336 = 2106 Hz the "9" is row 2 (R3) and column 2 (C3) and has a frequency of 852 + 1477 = 1329 .

Thus by pressing each switch the signals at different frequency ranges are produced, which are frequency modulated with the carrier wave and transmitted.

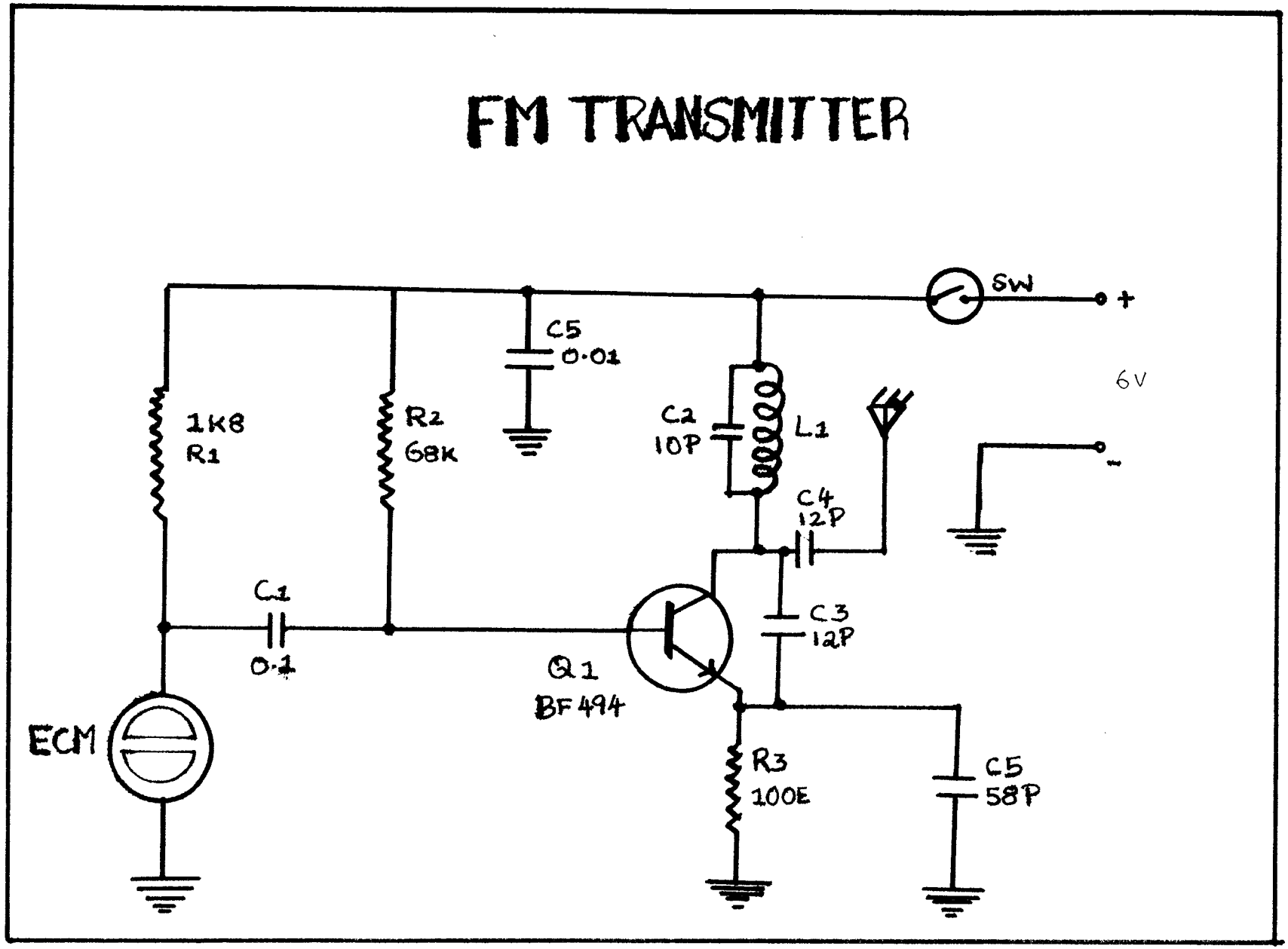
2.3 FM TRANSMITTER

A simple but practical FM transmitter circuit is given in the figure. This circuit can be operated at 6.0V D.C. supply source. The signals are passed from the DTMF encoder circuit to the base of the transistor Q1 (BF494) through the capacitor C1 (0.1) . Q1 is a NPN transistor and its collector is given positive supply through the coil L1 . It's emitter is connected to the ground through the resistance R3 (100E) while its base is given the forward supply through the resistance R2 (68K) .the voltage signals are given to base of the transistor Q1 (BF494) through the capacitor C1 (0.1).

Oscillator circuit:

Giving 5 turns of 24SWG wire on base of 0.5-cm diameter can make the coil L1 connected at its collector. A capacitor C3 (12pf) has also been connected between the collector and the emitter of the transistor Q1. This capacitor triggers the oscillations . As soon as the audio signal is received at the base then the transistor starts to oscillate and is generates FM frequency, which is given to, the antenna through the capacitor and it generates FM frequency , which is given to the antenna through the

FM TRANSMITTER



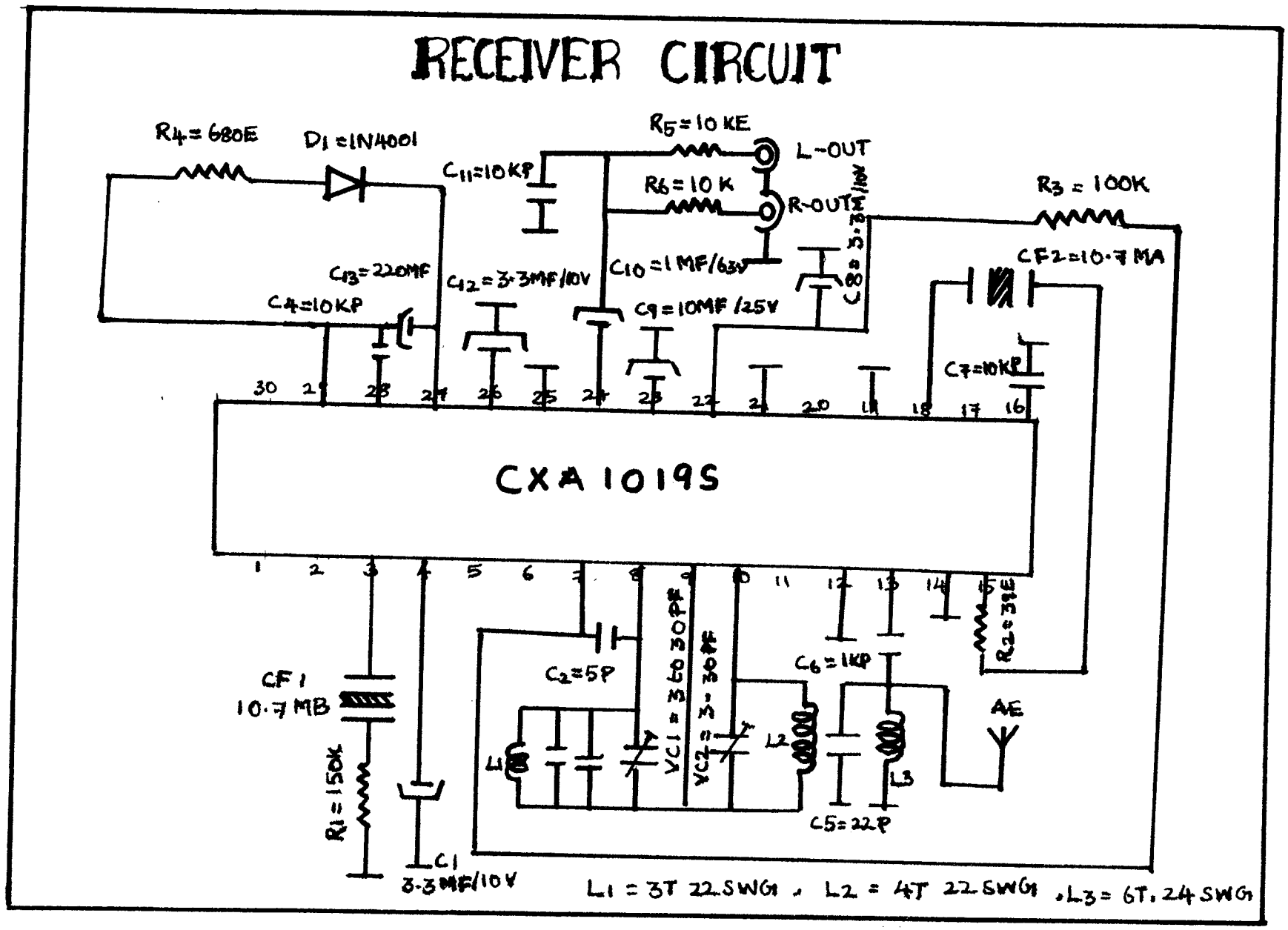
capacitor C4 (1kpf) and transmitted . The range of this transmitter lies between 100 meters to 500 meters . The carrier frequency is selected as 97MHZ.

2.4 FM RECEIVER

IC CXA1019S is a thirty pin DIL IC. Facility to connect a tuning indicator has been provided in this IC apart from the various sections built within the IC.A 10.7 MHz ceramic filter has been used in this circuit in place of the IFTs. An audio output section is also built within the IC apart from all the necessary sections . The audio output section of this IC has not been used in the give circuit. The signal received at the IC pin number 24 is given to the pin 1 of the volume control and the pin 2 of the volume controllers connected to the audio output sections. This section is not shown in the given circuit.

The IC pin no : 27 is the positive supply pin which is given +6 Volt supply through a resistance R4 (56E) . This supply is filtered by the capacitor C1 (1000MF , 16Volt) . IC pin no : 7 and 8 are connected to the oscillator section and a coil L1 is connected at the pin no : 8 . The capacitor C3 (39 pf) and a button trimmer B1 (15pf) are connected parallel to this coil L1. The desired frequency is selected by this trimmer RF coil L2 is connected at the IC pin no : 10 and a capacitor C7 (33pf) and a button trimmer B2 (15pf) are connected in parallel to this coil. IC pin no : 9 is the RF ground pin.

RECEIVER CIRCUIT



RF coils , the oscillator and the related components are all connected at this pin . Antenna coil L3 is connected at the IC pin no : 13 through a capacitor C9 (1kpf) and a capacitor C10 (27 pf) is connected in parallel to this coil . A telescopic antenna is connected from the center point of the capacitor C9 and coil L3 . Tuning indicator LED is connected at the IC pin no:20. The capacitor C8 (0.02) has been connected to it for filtration.Positive supply is given to the anode of the LED through a resistance R3 (920E). The IC pin no:1,2,4,5,12,14,19,21 and 30 are the dc ground pins. IC pin no:9 is the RF ground pin.

Tuning of the circuit:

For the first the supply is given the circuit. Hissing sound should now be received . Now keep the FM Mike near a sound source such as a tape recorder . Next , adjust the button trimmer B1 with the small screw drive called the aligner. When the sound is received clearly from the receiver then stop rotating the trimmer . Now adjust the trimmer B2 to get the maximum clarity in the sound received from receiver . At this point the FM Mike and the receiver circuit are tuned with each other.

2.5 DTMF DECODER

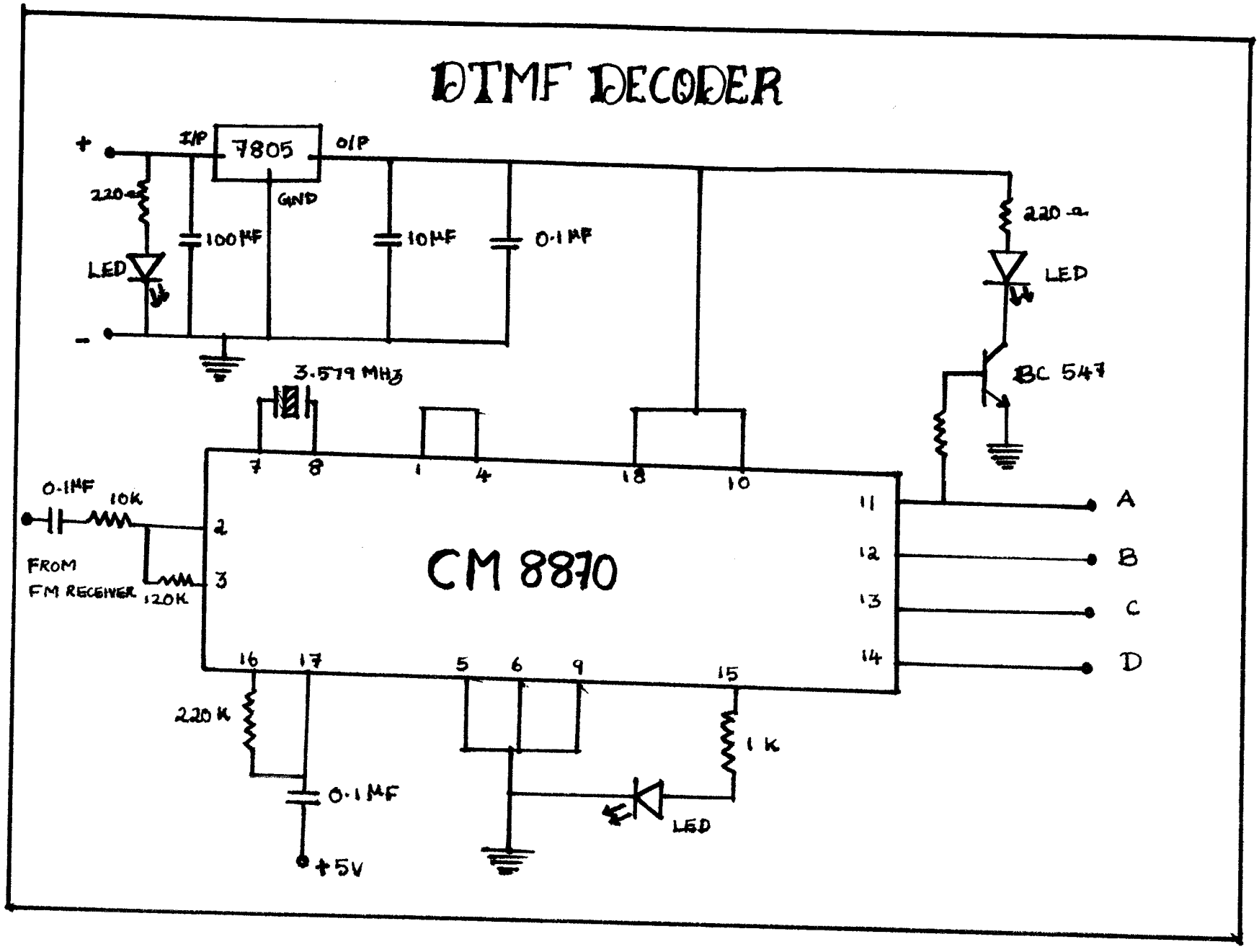
DTMF signals transmitted can be received and decoded using DTMF decoder IC 8870. It includes a band split filter that separates high and Low tones of the received par . digital decoder to verify both the frequency And duration of the received tones before passing the resulting 4 bit code to the output bus.

Features:

1. Low power consumption
2. Adjustable acquisition and release time
3. Central office quality and performance
4. Single 5V power supply
5. Dual tone suppression

DTMF clock circuit:

The internal clock circuit is completed with the addition of a Standard 3.579MHZ television color burst crystal. The crystal can be Connected to a single M-8870 or to a series of M-8870s by coupling the Oscillator output of each M-8870 through a 30pFcapacitor to the oscillator input of the next M-8870.


DTMF DECODER
+
IIP
7805
OIP
GND
220Ω
LED
100MF
10MF
0.1MF
-
220Ω
LED
BC 547
3.579 MHz
7
8
1
4
18
10
0.1MF
10K
FROM
FM RECEIVER
120K
2
3
CM 8870
11
12
13
14
A
B
C
D
16
17
5
6
9
15
220K
0.1MF
+5V
1K
LED

Algorithm:

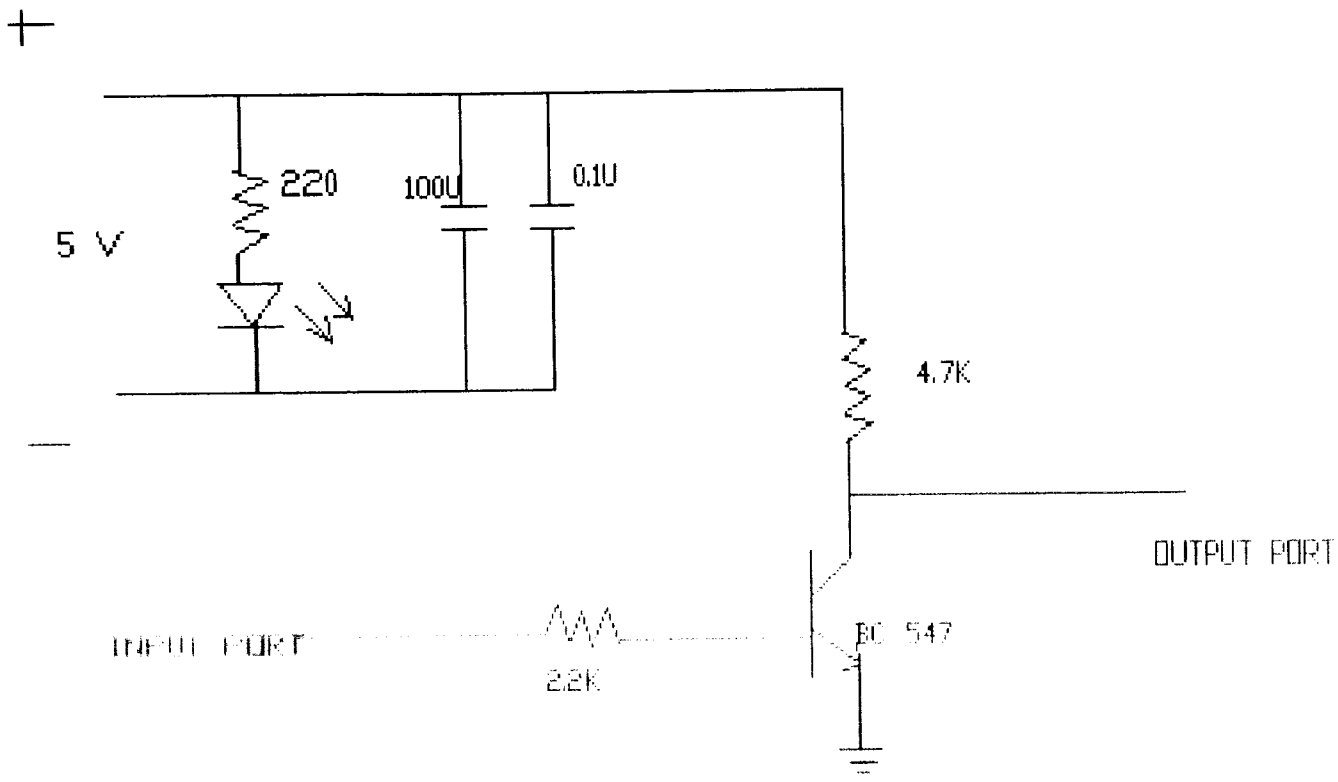
The M-8870 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies . A complex averaging algorithm is used to protect against tone simulation by extraneous signal (voice) while tolerating small frequency variations. The algorithm ensures an optimum combination of immune tonoise, talk-off and tolerance to interfacing signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones, it raises the Early Steering Flag. Any subsequent loss of signal condition will cause EST to fall.

2.6 BUFFER CIRCUIT

The signals that are received from the FM Receiver in the receiver section are weak signals. From these signals the decoder circuits will not be able to drive the microcontroller IC which inturn affects the operations of stepper motor. So it is necessary to incorporate the buffer circuit that boosts up to the value required driving the circuit.

The NPN transistor in the common emitter configuration is employed here. Transistor BC547 is used here. The current in the milliamps after consumed by the supply units , FM Receivers is supplied to the decoder IC that will not drive the microcontroller. So the output of the decoder circuit is given as the input to the buffer circuit, that boosts upped certain milliamps and its output is given to the Microcontroller,which enables it to drive the stepper motor.

BUFFER CIRCUIT



2.7 MICRO CONTROLLER:

A Microcontroller consists of a powerful CPU tightly coupled with memory (RAM, ROM, EPROM) various I/O features like Serial ports, parallel ports, timer/Counters, Interrupt controller, Data Acquisition interfaces - Analog to Digital Converter (ADC), Digital to Analog Converter (DAC), everything is integrated into a single Silicon Chip.

Advantage:

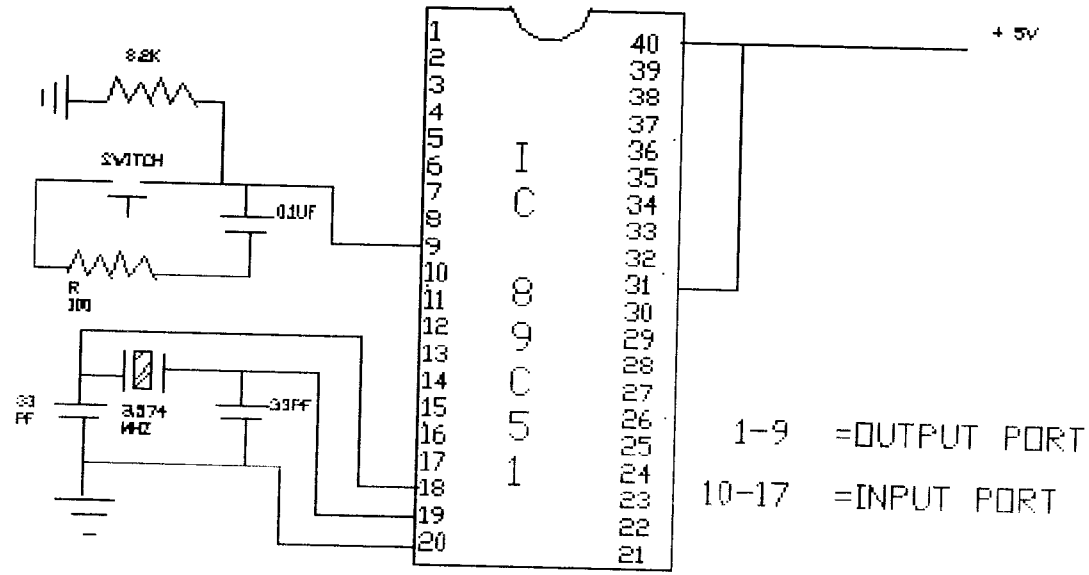
We generally prefer the use of a Microcontroller rather than the microprocessor based on the following advantages that a microcontroller overweighs a microprocessor . Size of the board is decreased since the memory required such as ROM, RAM, EPROM etc... are embedded on a single chip. The data transfer is in bits and not bytes as in real world applications. Hence they can be used for various switching operation.

Special features:

The AT89c51 microcontroller provides the following standard features:

- 8 bit CPU optimized for control applications
- Extensive Boolean processing (Single – bit Logic) Capabilities.
- On-Chip Flash Program Memory

MICRO CONTROLLER CIRCUIT



- On –Chip Data RAM
- Bi-directional and individually addressable I/O Lines
- Multiple 16 bit Timer /Counters
- Full Duplex UART
- Multiple Source/Vector/Priority Interrupt Structure
- On- chip Oscillator and Clock circuitry
- On-Chip EEPROM
- SPI Serial Bus Interface
- Watch Dog Timer

Special function register:

The fig shows the architectural block diagram of AT89c51 Microcontroller.

The functions of various SFRs are outlined below.

1) Accumulator:

ACC is the accumulator register. The mnemonics for accumulator – Specific instructions refer the register simply as A.

2) B Register:

The B Register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

3) Program Status Word:

The PSW register contains program status

information and holds the information about various flags that are set as a result of certain instructions.

4) Stack Pointer:

The 8-bit wide stack pointer is incremented before data is stored during PUSH and CALL executions. The stack may reside anywhere in the internal RAM area but the stack pointer is initialized to 07H after reset and the stack Begins at location 08H.

5) Data Pointer :

The Data pointer consists of a high byte (DPH) and a low byte (DPL). Its Intended function is to hold a 16 - bit address . It may be manipulated as a 16 bit register or as two independent 8 bit registers.

6) Serial data buffer:

The serial data buffer is actually two separate registers, a transmit buffer and a receive buffer register. When data is moved to SBUF, it comes from the receive buffer.

7) Power modes of Atmel 89c51 microcontroller:

To exploit the power savings available in CMOS circuitry, Atmel's Flash Microcontroller have two software-invited reduced

power modes.

Idle mode:

The CPU is turned of while the RAM and other On-Chip peripherals continue operating. In these mode current drawn is reduced to about 15 percent of the current drawn when the device is fully active.

Power down mode:

All On-Chip activities are suspended while the On-chip RAM continues to hold its data. In this mode, the device typically draws less than 15 micro Amps and can be as low as 0.6 Micro Amps.

8) Power on reset:

When power is turned ON, the circuit holds the RST pin high for an amount of time that depends on the capacitor value and the rate at which it charges.

To ensure a valid reset, the RST pin must be held high long enough to allow the oscillator to start up plus two machine cycles. On-power-up, Vcc should rise within approximately 10 ms. The Oscillator start up time depends on the oscillator frequency.

For a 10MHz crystal , The start-up time is typically 1ms.With the given circuit,reducing Vcc quickly to 0 causes the RST pin

voltage to momentarily fall below 0V. However, this voltage is internally limited and willnot harm the device.

9) Memory Organization:

All Atmel Flash Microcontroller have separate address spaces for program and data memory .The logical separation of program and data memory allows the data memory to be accessed by 8 bit addresses, which can be more quickly stored and manipulated by an 8 bit CPU. Nevertheless, 16 Bit data Memory address can also be generated through the DPTR register.

Program memory can only be read. There can be up to 64k bytes of directly addressable program memory. The read strobe for External Program memory is the Program Strobe Enable Signal (SEN). Data memory occupies a separate address space from program memory. Upto 64 Kbytes of External memory can be directly addressed in the external data Memory space.The CPU generates read and write signals, RD' and WR', during external data accesses.

External program memory and external data memory can be combined by applying the RD' and PSEN, signals to the inputs of an AND gate And using the output of the gate as the read strobe to the external program/data Memory.

10) Data Memory:

The Internal Data memory is divided into three blocks namely,

1 The lower 128 Bytes of Internal RAM.

2 The Upper 128 Bytes of Internal Ram.

3 Special Function Register.

Internal Data memory Addresses are always 1 byte wide,Which implies an address space of only 256 bytes. However, the Direct Addresses higher than 7Fh access a different Memory space, and Indirect Addresses higher than 7Fh access a different memory Space. The lowest 32 bytes are grouped into 4 banks of 8 registers.Program instructions call out these registers as R0 through R7.

Two bits in the Program Status Word (PSW) select, Which register bank, is in use. Instructions are shorter than use direct address.

The next 16-byte above the register bank's form a block of bit addressable memory space. The Microcontroller instruction set includes a wide selection of single – bit instructions and these instructions can directly address the 128 bytes in this area. These bit addresses are 00h through 7Fh.

Either direct or indirect addressing can access all of the bytes in lower 128 bytes .The upper 128 can only be accessed by indirect addressing .The upper 128 bytes of RAM are only in the devices with 256 Bytes of RAM.

The Special Function Register includes Port latches, timers, peripherals controls etc Direct addressing can only access these registers .In general ,all Atmel Micro controller have the same SFR's at the same address in SFR space as the At89c51 have additional SFR's .Sixteen addresses in SFR space are both byte and bit addressable .The bit addressable SFR's are those whose address ends in 000BH.

AT89C51 ADDRESSING MODES:

The addressing modes of AT 89c51 flash Microcontroller instruction set are as follows.

Direct addressing : In Direct addressing , an 8- bit address field in the instructions specifies the operand .Only internal data RAM and SFR's can be directly addressed.

1. Indirect addressing:

In direct addressing .the instruction specifies a register that contains the address of the operand. Both internal and external RAM can indirectly addressed. The address register for 8-bit address can be either the stack pointer or R0 or R1 of the selected register Bank .The address register for 16- bit addresses can be only the 16-bit pointer register DPTR.

2. Indexed addressing :

Program memory can only be accessed via indexed addressing.

This addressing mode is intended or reading look-up tables in Program memory . A16 bit base register (Either DPTR or the Program with the table entry number ,Adding the accumulator data to the base pointer forms the address of the table entry in program memory.Another type of indexed addressing is used in the "case jump" instructions. In this case the destination address of a jump instruction is computed as the sum of the base pointer and the Accumulator data.

3. Register Instruction :

The register bank's , which contains registers R0 through R7, can be accessed by instructions whose opcodes carry a3 –bit register specification.Instruction that access the registers this way make the instruction is executed , one of four bank's is selected at execution time by the two bank select bits in PSW.

4. Register –Specific instruction:

Some instruction are specific to a certain register . or example some instruction always operate on the Accumulator .so no address byte is needed to point to it.

Instruction that refer to Accumulator as specific Opcodes.

5. Immediate constants:

The value of a constant can follow the opcode in program memory

For example,

MOV A,#100

Loads the accumulator with the decimal number 100. The same number could be specified in hex digit as 64h.

Oscillator and clock circuit:

All Atmel flash microcontroller have an On-Chip oscillator that can be used as the clock source for the CPU. To use the on-Chip oscillator, connect a crystal between XTAL1 And XTAL2 pins of the Microcontroller and connect capacitors to the ground , the frequency range is in from 1.2MHz to 12 MHz.

To drive the chip with an internal oscillator .one would around XTAL1 and XTAL2 . Since the input to the clock generator is divide by two flip-flop there are no requirement on the duty cycle of the external oscillator signal.

CPU Timing:

A machine cycle consists of 6 States numbering s1 to s6. Each state time lasts for two oscillators periods. Thus a machine Cycle lasts 12

oscillator periods or one microsecond if the oscillator frequency is 12MHz .Each state is divided into a phase 1 half and phase 2 half . Even if the instruction does not require it. If the instruction being and the PC is not incremented, Execution of one cycle instruction begins the instruction register . A second fetch occurs during s4 of the same machine cycle . Execution is complete at the end of state 6 of the same machine cycle.

Interrupts:

The AT89C51 provides 5 interrupt sources : Two external interrupts, two timer interrupts and one serial port The External Interrupts INTO and INTI can each either level activated or transition – activated ,depending on bits ITO and ITI in Register TCON .The Flags that actually generate these interrupts are the IEO and IE1 bits in TCON. When the service routine is vectored to interrupt was transition – activated. if the interrupt was level –activated , then the external requesting source (rather than the on-chip hardware) controls the requested flag. The timer 0 and Timer 1 Interrupt are generated by TFO and TF1, which are set by a rollover in their respective Timer/Counter register (except for Timer in Mode 3). When a timer interrupts is the service routine is vectored to. The logical OR of RI and TI generate the Serial Port Interrupt. Neither of these flag is cleared by hardware when the service routine is vectored to.

In fact, the service routine normally must determine whether RI or TI generated the interrupt an the bit must be cleared in software.

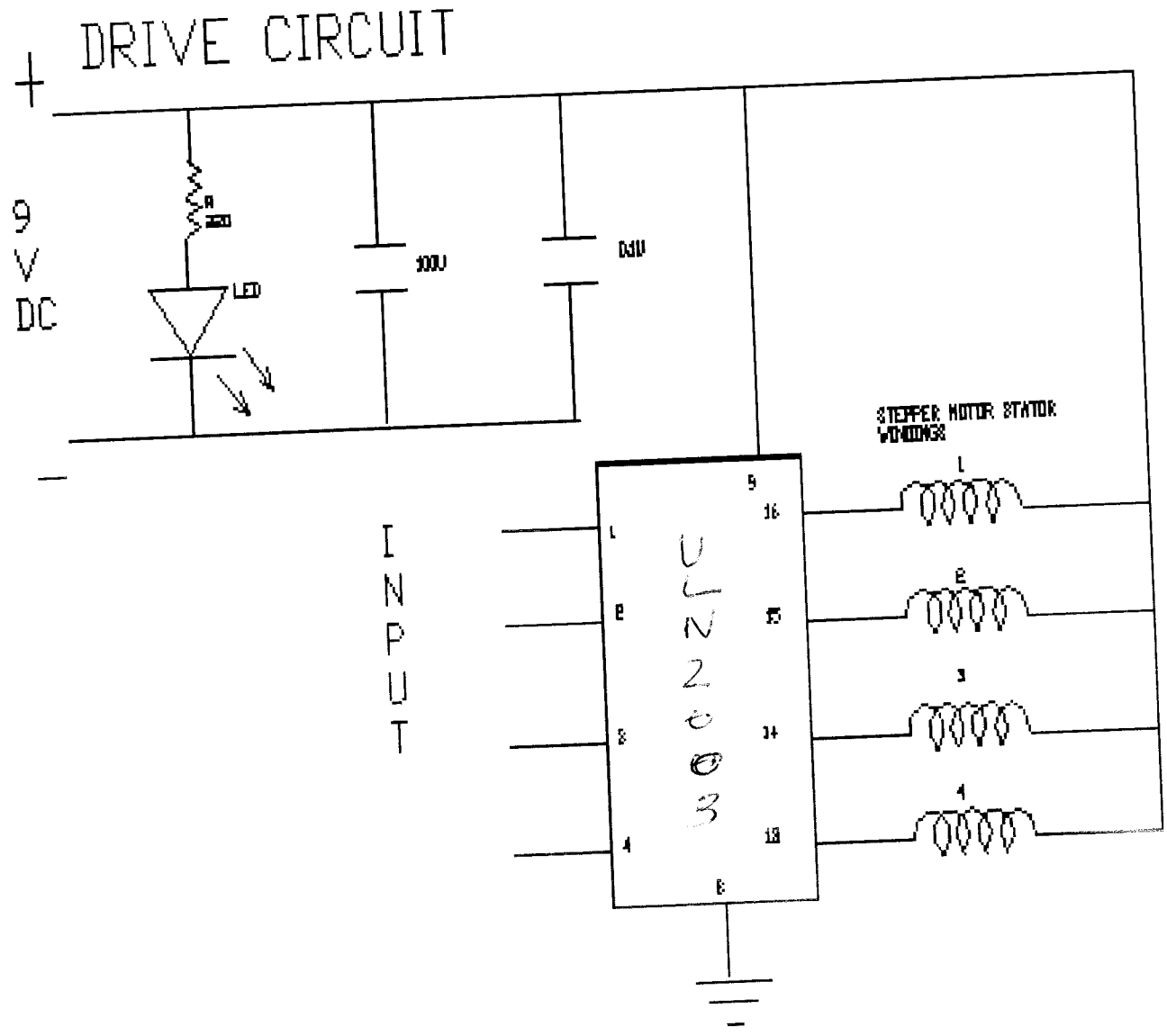
Interrupt Priorities:

Each interrupt source can also be individually programmed to one of two priority levels by setting or clearing the interrupt priority (IP) bit in the SFR. A lower priority interrupt can be interrupted by a high priority interrupt but not by another low priority interrupt cannot be interrupted . On the other hand a high priority interrupt cannot be interrupted by another interrupt source . If interrupt of similar priorities are received an internal polling sequence determines which request is to serviced .

2.8 DRIVE CIRCUIT

The control signals for the stepper motor operation are given to the micro controller input port P3, based on the signals from the decoder circuits that are received from the FM Receiver. With output signals from the port P1 the operation of the stepper motor is possible by using separate drive unit. So we need to incorporate the drive circuit for this purpose.

The driver circuit employed here consists of ULN2003 IC. The signals from the micro controller output port are given to the driver circuit input. The gate circuits incorporated in this ULN2003 IC has the open collector configuration which enables the driver circuits to withstand the voltage up to 28v.The output signals from the ULN2003 IC is given to the coils of the stepper motor. With the operations such as forward, reverse, forward increase and decrease and reverse increase and decrease, the IC receives the signals from the micro controller and energizes the stepper motor coils at its output and the required sequence of operation of the stepper motor is achieved.


DRIVE CIRCUIT
+
9
V
DC
LED
100U
0.1U
STEPPER MOTOR STATOR
WINDINGS
INPUT
ULN2003
5
16
1
2
15
3
14
4
13
8
–

2.9 STEPPER MOTOR

Stepper motors require that their power source be continuously pulsed (ON/OFF voltage cycles) in specific patterns and they do not spin freely as other motors do when power is applied. Positioning remains the same if the coils receive constant dc excitation. Continuously rotating the phases through one electrical cycle after another causes the motor to move a precise number of steps or micro steps. These steps or step angle are the rotational movement of stepper motors in predetermined angles. Stepper motors "step " a little bit at a time and are very useful for direct and very precise computer control. A good stepper motor usually has an accuracy of 3-5 percent of a step. This error is non cumulative from one step to the next.

The stepper motors enable simple and accurate control of angle of rotation and rotational speed, making them suitable for a wide range of applications. Uses of stepper motors in factory automation include X-Y plotters and laser processors. In semiconductor fabrication equipment, stepper motors can be found in wafer processing devices, IC bonders and IC inspection devices.

A stepper motor positions itself without using feedback. Position feedback is used to confine that a stepper motor has arrived at the desired

position. More and more, stepper motor applications are also using position feedback for extra safety. Performance of stepper motor motion systems depends a deal on the drive electronics and control method used. Stepper motor controllers generate high-speed step and direction signals to create continuous motion at a constant or accelerating velocity. The amplifier uses the direction signal to determine the phase sequence. Changing the direction signal reverses the motor direction. Another unique characteristic of stepper motors is their high holding torque, which is most common performance specification for stepper motors. When the windings are energized, the motor is able to hold its position (full torque) firmly when it is standing still. This stop position can be held without relying on a mechanical brake.

When choosing stepper motors, it is important to determine whether the motor characteristics are suited to the required load.

Two main characteristics of stepper motor performance:

1. Static characteristics
2. Dynamic characteristics.

Static characteristics relates to the changes in angle that take place when the stepper motor is stopped or during motor standstill.

Dynamic characteristics relates to speed and torque when the stepper motor starts or during rotation.

As mentioned before, stepper motors are self-positioning. Thus, no external devices like encoders are required to feedback their position. This feature makes stepper motors less expensive as compared to servomotors, which require an encoder to operate in a position mode. Furthermore, a stepper motor does not usually require a permanent magnet in its rotor or stator. Instead, stepper motors can consist mainly of copper wire, which carries the current that creates electromagnetic force, and iron or other "soft" ferromagnetic materials, which focus the magnetic flux.

Stepper motors are brushless. This means that external circuits make no electrical contact with the rotor. This relieves stepper motors of mechanical-Commutator problems like degradation because of wear or arcing. The life of the motor is thus simply dependent on the life of the bearing. Besides, stepper motors produce a relatively high torque for a given package size. A wide range of rotational speeds can also be obtained, as the speed is proportional to the frequency of the input pulses.

DRAWBACKS:

The drawbacks associated with the use of stepper motors include noise, which is often audible and induce vibrations that can disturb the load or affect sensitive parts of the systems. These resonances occur only if the motor is not properly controlled. Some techniques like micro stepping and the use of mechanical dampers can reduce vibration. However, it is almost impossible to completely remove the problem. Another drawback of stepper motors is their relatively low torque speed. Most stepper motor systems are driven at around 5000 rpm or less. Besides, stepper motors also deliver torque that drop significantly at higher velocities. These limitations mean that stepper motors are generally unavailable in power ranges above several hundred watts. Temperature rise characteristics are also an important consideration as stepper motors are operated under constant current with frequent START/STOP.

Trends in stepper technology:

Stepper motor technology has seen great changes and evolution in recent times. Before, the industry believed that with the emergence of more affordable and higher performance servomotors, stepper motor technology would be relegated to lower end applications. However, new developments in stepper motors have made this technology more competitive when competing with other motors in applications in which size, cost, and power are most important.

An increasing number of stepper systems have an option for position feedback to monitor or control position, with or without formal loop closure. Digital Signal Processors (DSPs), which have contributed greatly to the improved closed-loop performance of servo drives, is also now more commonly used in stepper systems. There is a trend in the market towards drives that blend control of servo and stepper motors into one unit, making economic use of common sections and modules along the way. The introduction of DSPs to stepper motors has definitely made the stepper more capable and flexible in handling a wider range of applications. For example, DSPs can be used in place of more costly high frequency-rate indexers in systems that utilize micro stepping. The computational power of the DSP can also be used in the place of encoders for stall detection, stopping the drive and providing a status signal for display by an LED. Other benefits of closed loop stepper control include synchronizing motion with data acquisition boards or cameras from feedback on position or velocity.

Mechatronics is another trend in stepper technology. This is the integration of mechanics, power electronics, controls and communication. Stepper motors are often utilized in machines with numerous motion axes. An integrated motor, drive and control, coupled with networking, can there by simplify implementation of such machine systems. Network communication gateways such as Device Net can reduce parts like wiring. It also allows a

clean interface to main controller, with simple loading of new position/velocity commands from the network scanner. Further more Device Net improves machine diagnostics by enabling system fault information like over voltage.

Other trends include the development of stepper motors with three and five phase windings. Skewed-rotor and flux-control motors have also been made available, both of which can produce smoother, more powerful motion. Major advancements have been made on the control side too. Recent technology breakthroughs in amplifiers include high-efficiency, high current, stepper motor drivers that use special current-modulation techniques to control oscillations and reduce noise.

The development of new generation of trajectory-control chips is yet another important advancement. By implementing encoder feedback, load handling is improved and micro stepping becomes possible. Micro stepping brings higher accuracy and smooth performance, eliminating most cogging and harmonic instabilities. Although these improvements are obtained at a cost, they enable stepper motors to function as smoothly as servo motor systems.

Besides, the implementation of programmable starting velocities, and S-curve profiling on control-chips has also significantly expanded the range of stepper motor applications. Better magnetic structures have let stepper motors produce more torque, rectifying this notorious inefficiency of the past.

3. SOFTWARE DESCRIPTION

3.1 ALGORITHM:

Main Program:

1. Initialise the output port as high.
2. Initialise the input port as low.
3. Compare the input port with data 0eh.
4. If equal, call the subroutine forward.
5. Otherwise, call the subroutine reverse.
6. Go to step 3.

Subroutine 1. Forward:

1. Move the data's 1,2,4,8 to output port so that the stepper motor moves forward.
2. Compare the input port with 07h.
3. If equal, go to subroutine increase.
4. Otherwise, compare the input port to 0bh.
5. If equal, go to subroutine decrease.
6. Otherwise, compare the input port to 0eh.
7. If equal, go to main program.
8. Otherwise, go to step2.

Subroutine 2. Reverse:

1. Move the data's 1,2,4,8 to output port so that the stepper motor moves forward.
2. Compare the input port with 07h.
3. If equal, go to subroutine increase.
4. Otherwise, compare the input port to 0bh.
5. If equal, go to subroutine decrease.
6. Otherwise, compare the input port to 0eh.
7. If equal, go to main program.
8. Otherwise, go to step2.

Subroutine 3. Increase:

This is the delay program so that it decreases the execution period by incrementing the comparing value.

1. Initialise a register as 10h.
2. Compare this data with 20h
3. If equal, return to main program.
4. Otherwise, increment the register

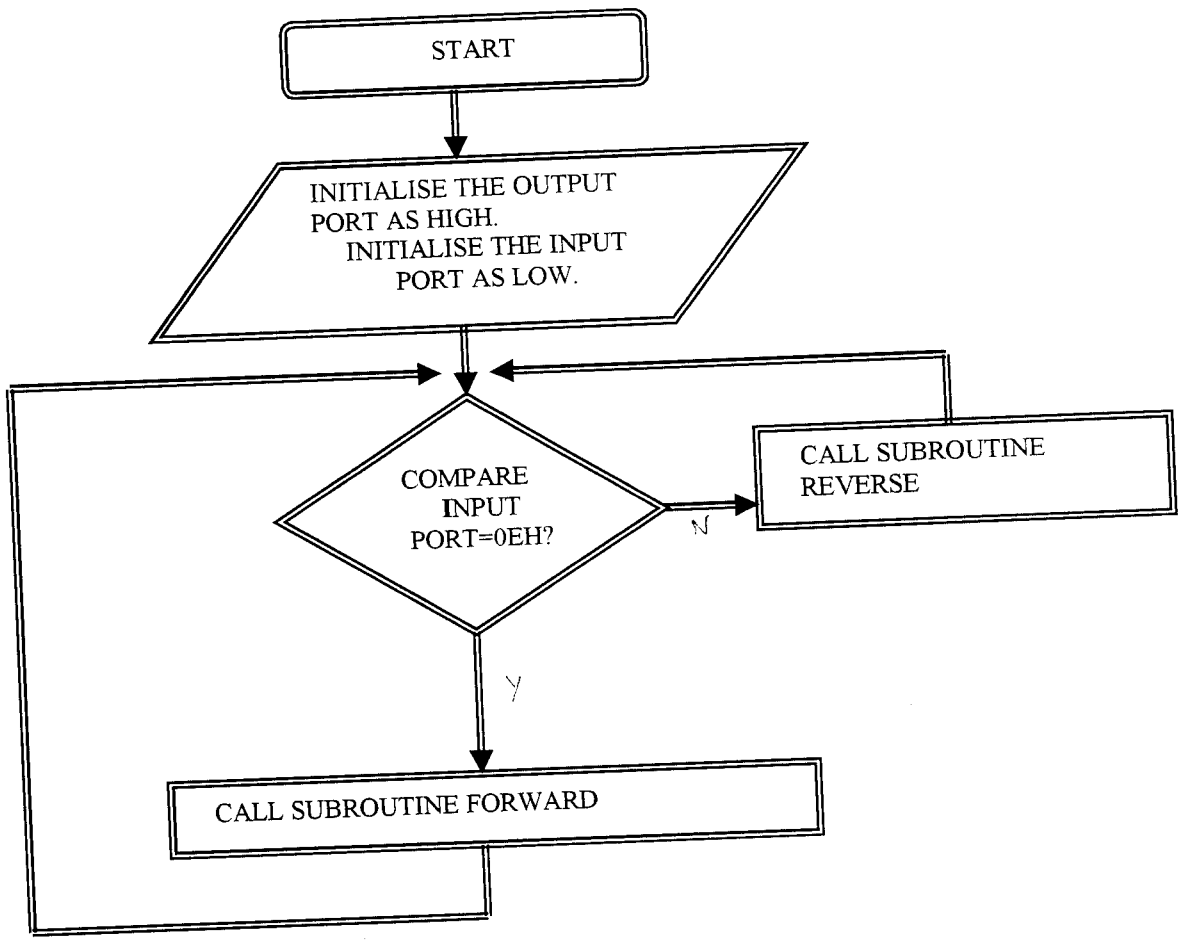
Subroutine 4. Decrease:

This is the delay program so that it increases the execution period by incrementing the comparing value.

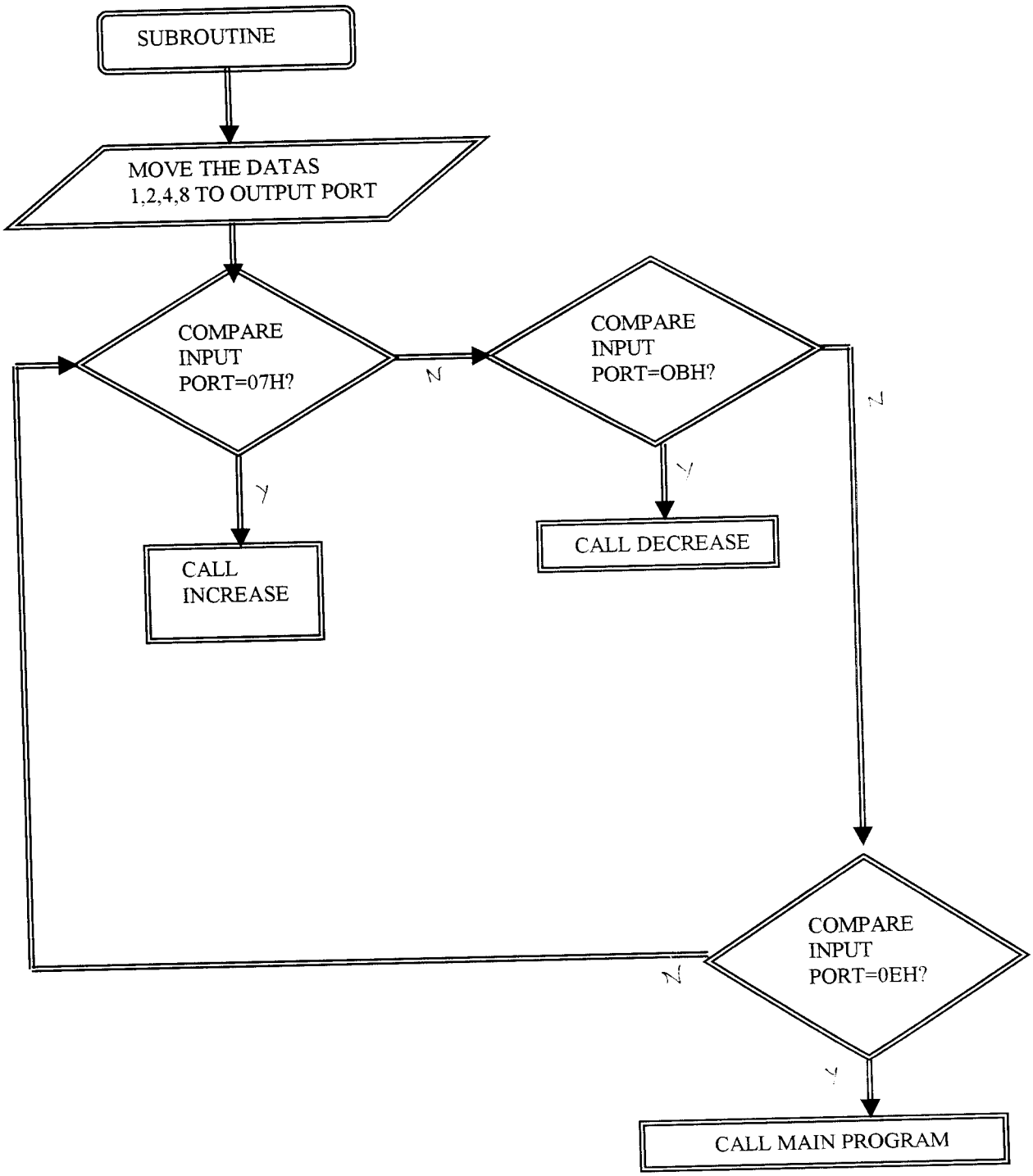
1. Initialise a register as 10h.
2. Compare this data with 01h
3. If equal, return to main program.
4. Otherwise, decrement the register

3.2 FLOWCHART

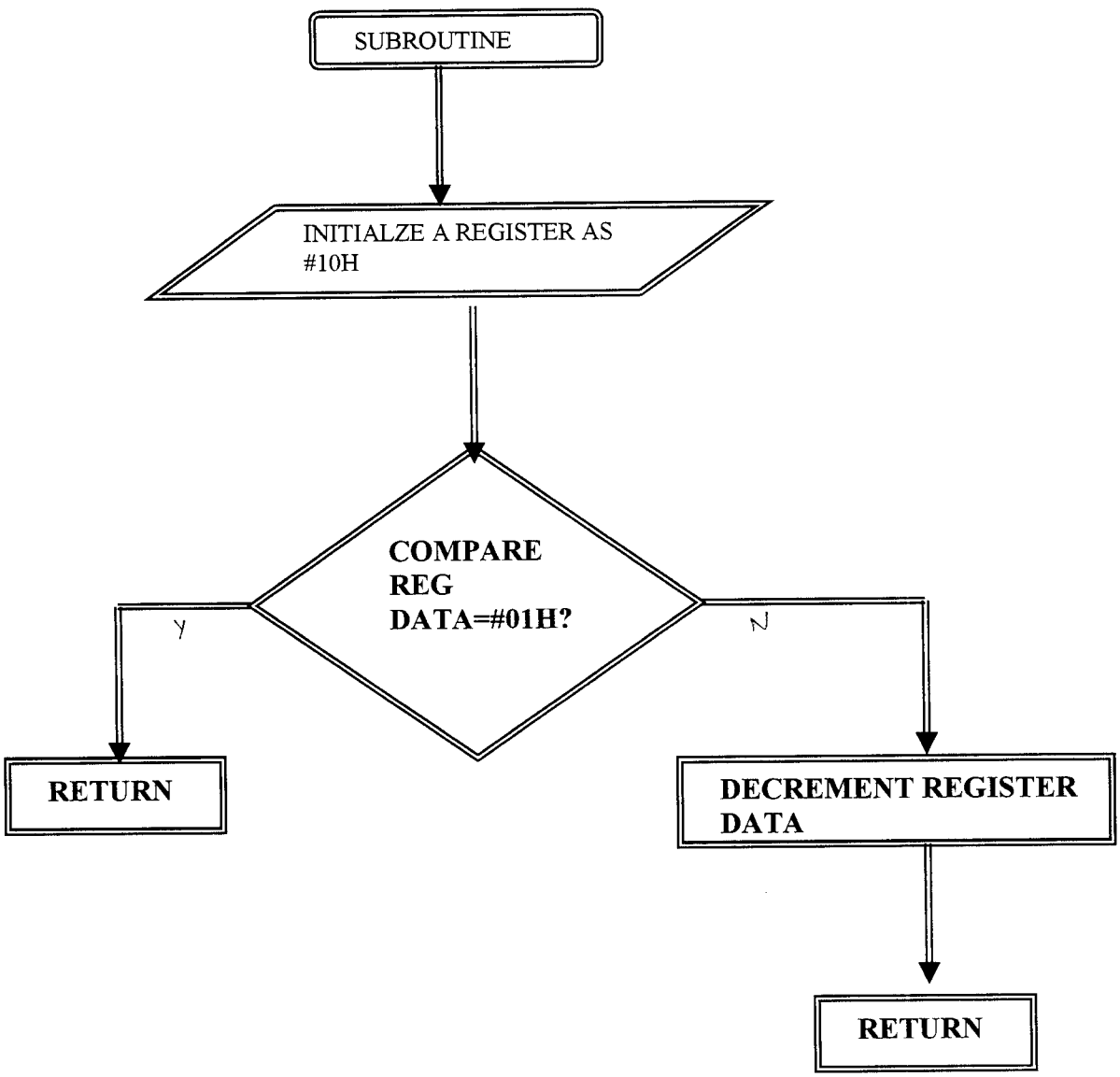
Main Program:



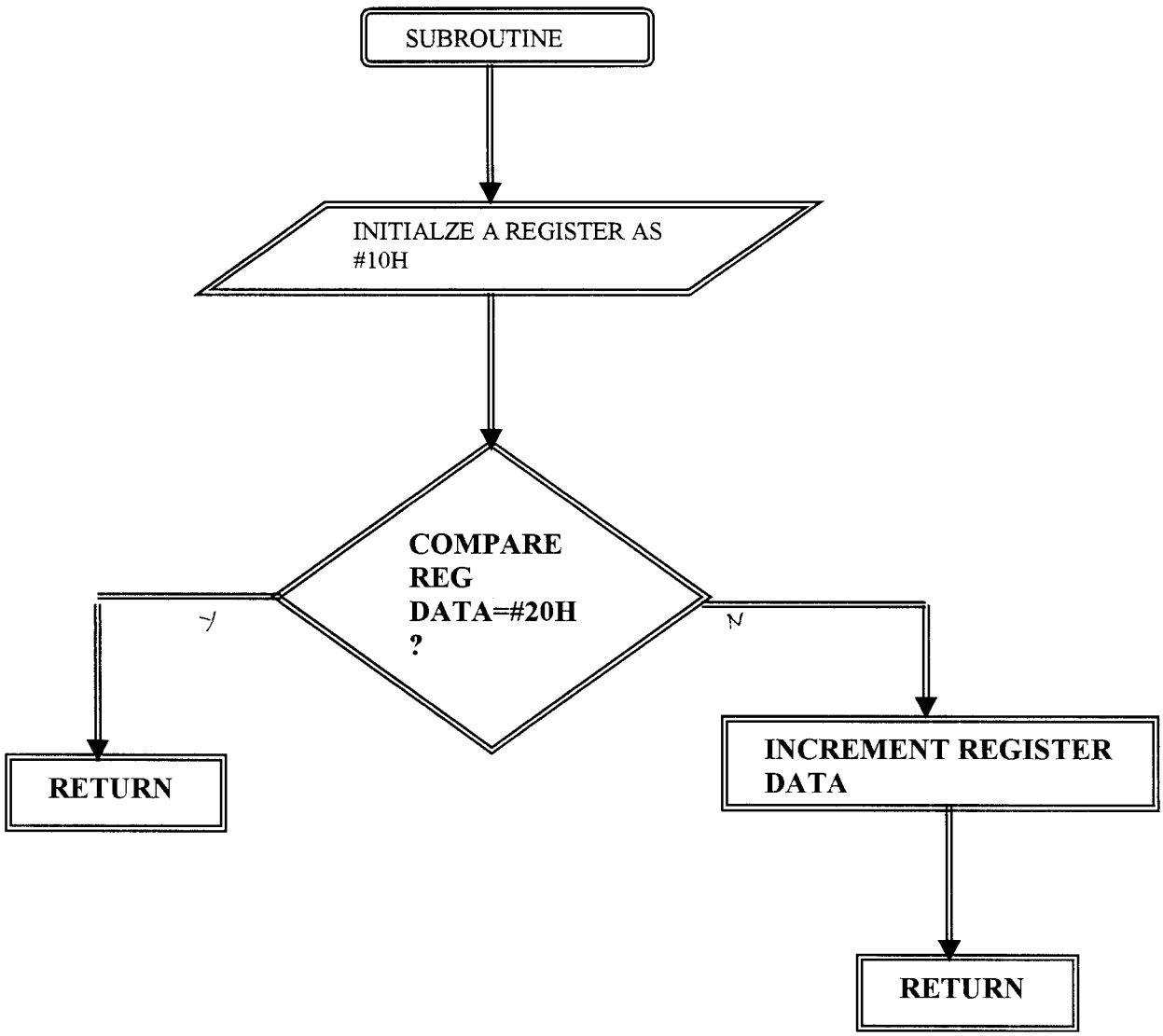
Subroutine Forward:



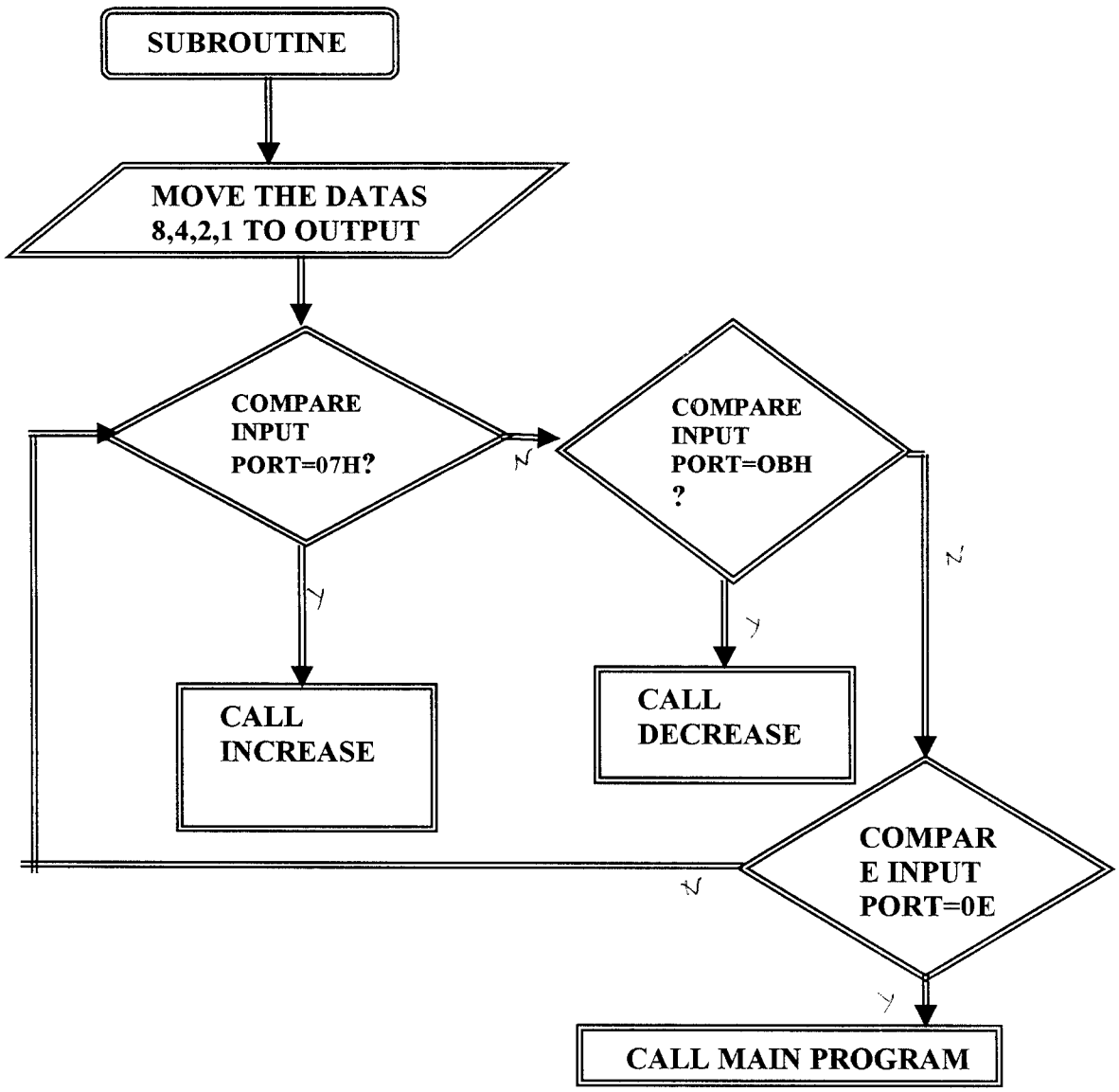
Subroutine decrease:



Subroutine Increase:



Subroutine Reverse:



3.3 ASSEMBLY LANGUAGE PROGRAM

Program for the speed control of stepper motor:

```
                org 0000h
                mov p1,#00h
                mov p3,#0ffh
                mov r4,#00h
                mov r5,#10h

loop            mov 30h,#0ah
x               acall delay1
                djnz 30h,x
                mov 30h,#0ah
                mov r4,p3
                cjne r4,#0eh,l
                sjmp forward
                mov r4,p3
fl              cjne r4,#0dh,loop
                sjmp reverse
                sjmp loop

forward         mov 30h,#0ah        ;forward
forward1        mov p1,#01h
                acall delay
                mov p1,#02h
                acall delay
                mov p1,#04h

                acall delay
                mov p1,#08h
```

```
                acall delay
f               mov r4,p3
                cjne r4,#0ch,f1
                acall increase
f1              mov r4,p3
                cjne r4,#0bh,f2
                acall decrease
f2              djnz 30h,forward1
                mov 30h,#0ah
                mov r4,p3
                cjne r4,#0eh,f
                sjmp loop

                sjmp forward1



reverse         mov 30h,#0ah            ;reverse
reverse1        mov p1,#08h
                acall delay
                mov p1,#04h
                acall delay
                mov p1,#02h
                acall delay
                mov p1,#01h
                acall delay
re              mov r4,p3
                cjne r4,#0ch,re1

                acall increase
re1             mov r4,p3
                cjne r4,#0bh,re2
```

```
                    acall decrease

re2                 djnz 30h,reverse1
                    mov 30h,#0ah
                    cjne r4,#0dh,re
                    sjmp loop
                    sjmp reverse1


increase            cjne r5,#20h,in         ;increase
                    ret
in                  inc r5
                    ret


decrease            cjne r5,#01h,de
                    ret                     ;decrease
de                  dec r5
                    ret


delay                                       ;ret
                    mov r2,05h              ;05h=r5
label2              mov r0,#3fh
label1              mov r1,#3fh
wait                djnz r1,wait
                    djnz r0,label1

                    djnz r2,label2
                    ret

delay1                                      ;ret
```

```
                mov r2,#01h
labe2           mov r0,#00h
labe1           mov r1,#00h
wait1           djnz r1,wait1
                djnz r0,labe1
                djnz r2,labe2
                ret
```

4.CONCLUSION

An automation system using wireless communication to control the bidirectional speed of a stepper motor drive has been designed and implemented. The complete system is more reliable than the existing manual methods in the industrial process. The integration of hardware and software provide efficient operation of the system . Moreover the developed system is quite simple and user friendly. The system has been working satisfactorily with the designed values of speed and the system will fulfill the industrial requirement.

5. FUTURE ENHANCEMENT

"Change is the only changeless phenomenon the world over".

We held this saying right from the inception of this project. New technologies emerge and subside as time goes on, but our project stands against winds of time. Our project can be enhanced in the following ways.

- In automation system, a "PROGRAMMABLE LOGIC CONTROLLERS" can be used as it has many features.
- This automation system can be interfaced to the PC using wireless communication which paves way for effective functioning and monitoring of the system.
- This system can be modified to any kind of process such as Temperature control, Pressure control, Flow control, Position control etc. according to the requirement.

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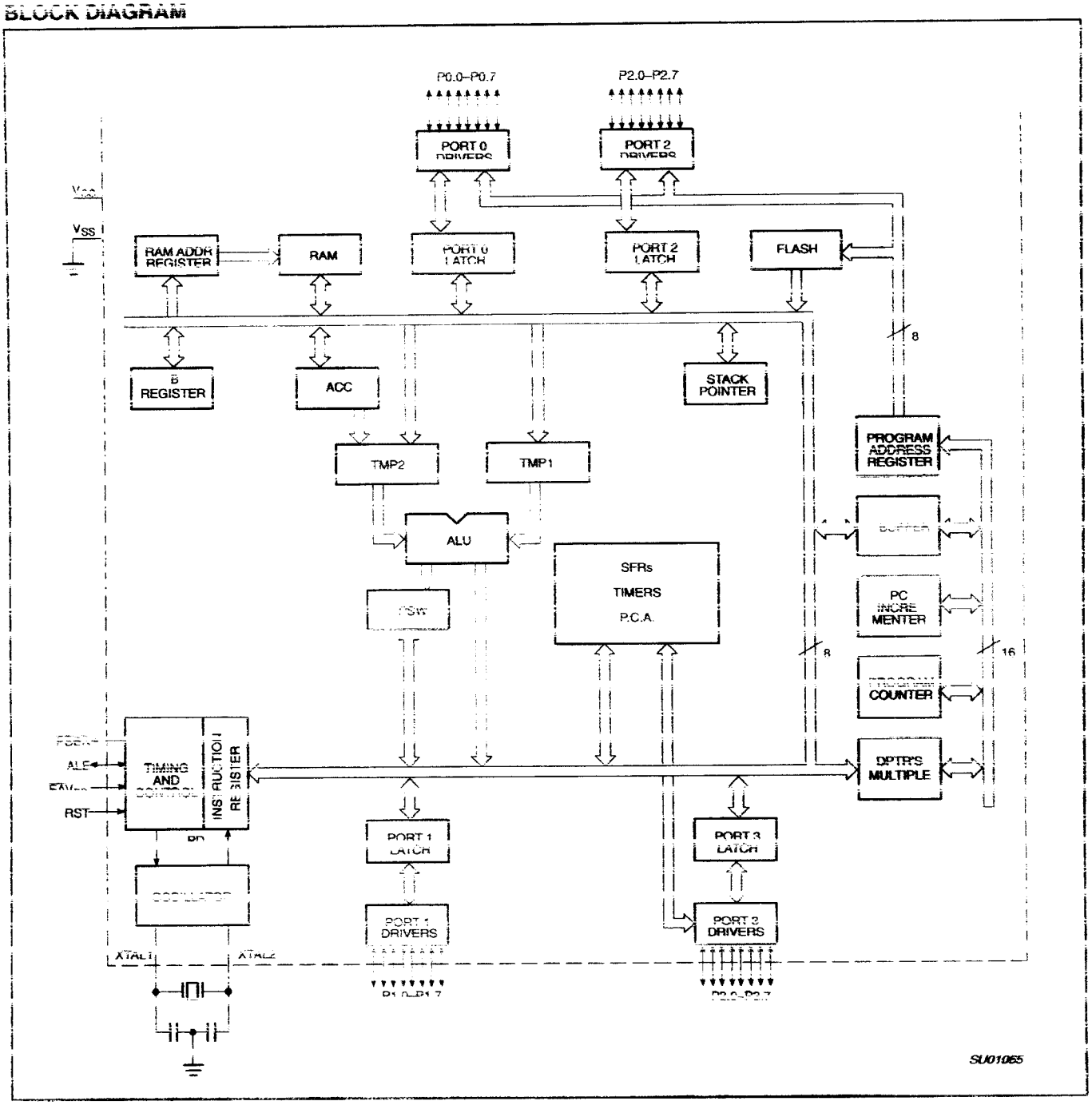
- V.V.Athani and H.N.Vinod,"Linear Current Drive for Stepping Motors", Electronic engg.,Vol.10, No.12,p.28.Dec.1986.

- www.atmel.com - Microcontoller

- www.eio.com/jasstep.html - Stepper Motor

- www.electronicsforu.com - Wireless Communication

BLOCK DIAGRAM



80C51 8-bit Flash microcontroller family 32K/64K ISP FLASH with 512–1K RAM

89C51RC+/RD+

DESCRIPTION

The 89C51RX+ devices contain a non-volatile FLASH program memory (up to 64K bytes in the 89C51RD+) that is both parallel programmable and Serial In-System Programmable. In-System reprogramming allows devices to alter their own program memory, in the actual end product, under software control. This opens up a range of applications that can include the ability to field update the application firmware.

A default serial loader (boot loader) program in ROM allows In-System serial programming of the FLASH memory without the need for a loader in the FLASH code. User programs may erase and reprogram the FLASH memory at will through the use of standard routines contained in ROM.

These devices are Single-Chip 8-Bit Microcontrollers manufactured in advanced CMOS process and are derivatives of the 80C51 microcontroller family. All the devices have the same instruction set as the 80C51.

FLASH/EPROM Memory Size (X by 8)	RAM Size (X by 8)	Programmable Timer Counter (PCA)
89C51RC+		
32K	512	Yes
89C51RD+		
64K	1024	Yes

The devices also have four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source, four-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits. For systems that require extra memory capability up to 64k bytes, each can be expanded using standard TTL-compatible memories and logic.

The added features of the P89C51RX+ Family makes them even more powerful microcontrollers for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities such as motor control.

FEATURES

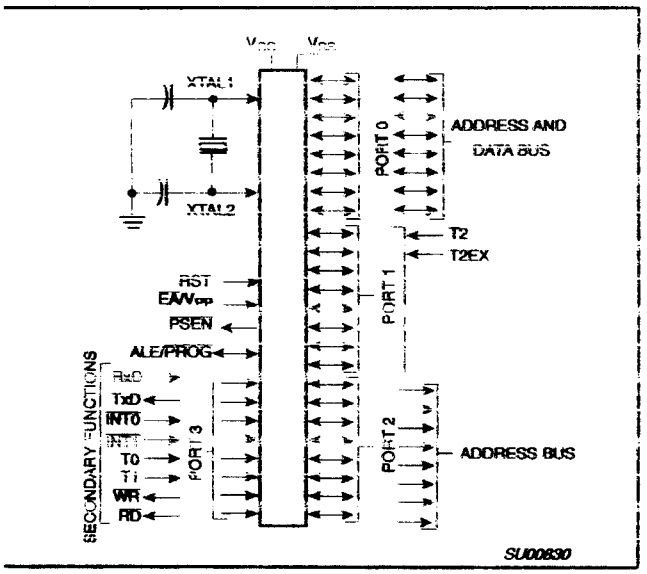
- 80C51 Central Processing Unit
- On-chip FLASH Program Memory with In-System Programming (ISP) capability
- Boot ROM contains low level FLASH programming routines and a default serial loader
- Speed up to 33MHz
- Full static operation
- RAM expandable externally to 64K bytes
- 4 level priority interrupt
- 7 interrupt sources, depending on device
- Four 8 bit I/O ports
- Full-duplex enhanced UART
  - Framing error detection
  - Automatic address recognition
- Power control modes
  - Clock can be stopped and resumed
  - Idle mode
  - Power down mode
- Programmable clock out
- Second DPTR register
- Asynchronous port reset
- Low EMI (inhibit ALE)

ORDERING INFORMATION

MEMORY SIZE 32K × 8	MEMORY SIZE 64K × 8	TEMPERATURE RANGE °C AND PACKAGE	VOLTAGE RANGE	FREQ. (MHz)	DWG. #
P89C51RC+IN	P89C51RD+IN	0 to +70, 40-Pin Plastic Dual In-line Pkg.	5V	0 to 33	SOT129-1
P89C51RC+IA	P89C51RD+IA	0 to +70, 44-Pin Plastic Leaded Chip Carrier	5V	0 to 33	SOT187-2
P89C51RC+IB	P89C51RD+IB	0 to +70, 44-Pin Plastic Quad Flat Pack	5V	0 to 33	SOT307-2
P89C51RC+JN	P89C51RD+JN	–40 to +85, 40-Pin Plastic Dual In-line Pkg.	5V	0 to 33	SOT129-1
P89C51RC+JA	P89C51RD+JA	–40 to +85, 44-Pin Plastic Leaded Chip Carrier	5V	0 to 33	SOT187-2
P89C51RC+JB	P89C51RD+JB	–40 to +85, 44-Pin Plastic Quad Flat Pack	5V	0 to 33	SOT307-2

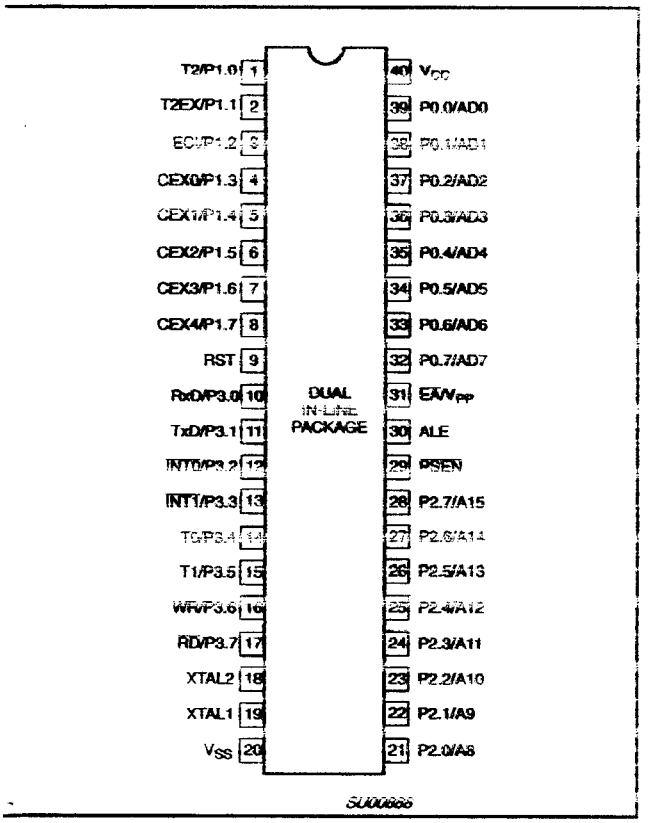
NOTE:
1. The devices (89C51RA+/RB+) are planned for release at a future date. Check with your local Philips Sales office for availability information.
2. See 89C2c/89C54/89C58 will be released without ISP (see separate data sheet). Only 89C51RX+ devices will be offered at this time with ISP capability.
3. Hardware Watchdog removed from datasheet. Watchdog Timer using PCA Module 4 is still available.

LOGIC SYMBOL

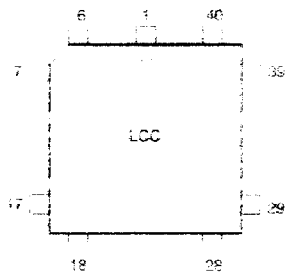


PIN CONFIGURATIONS

DUAL IN-LINE PACKAGE PIN FUNCTIONS



CERAMIC AND PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS

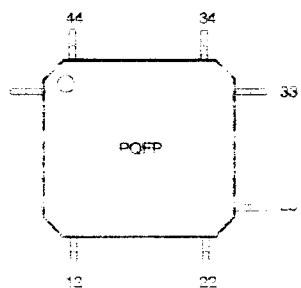


Pin	Function	Pin	Function	Pin	Function
1	NIC*	16	P3.4/T0	31	P2.7/A15
2	P1.0/T2	17	P3.5/T1	32	PSEN
3	P1.1/T2EX	18	P3.6/WR	33	ALE
4	P1.2/ECI	19	P3.7/RD	34	NIC*
5	P1.3/CEX0	20	XTAL2	35	EA/Vpp
6	P1.4/CEX1	21	XTAL1	36	P0.7/AD7
7	P1.5/CEX2	22	VSS	37	P0.6/AD6
8	P1.6/CEX3	23	NIC*	38	P0.5/AD5
9	P1.7/CEX4	24	P2.0/A8	39	P0.4/AD4
10	RST	25	P2.1/A9	40	P0.3/AD3
11	P3.0/RxD	26	P2.2/A10	41	P0.2/AD2
12	NIC*	27	P2.3/A11	42	P0.1/AD1
13	P3.1/TxD	28	P2.4/A12	43	P0.0/AD0
14	P3.2/INT0	29	P2.5/A13	44	VCC
15	P3.3/INT1	30	P2.6/A14		

* NC INTERNAL CONNECTION

SU00690

PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function	Pin	Function
1	P1.5/CEX2	16	VSS	31	P0.6/AD6
2	P1.6/CEX3	17	NIC*	32	P0.5/AD5
3	P1.7/CEX4	18	P2.0/A8	33	P0.4/AD4
4	RST	19	P2.1/A9	34	P0.3/AD3
5	P3.0/RxD	20	P2.2/A10	35	P0.2/AD2
6	NIC*	21	P2.3/A11	36	P0.1/AD1
7	P3.1/TxD	22	P2.4/A12	37	P0.0/AD0
8	P3.2/INT0	23	P2.5/A13	38	VCC
9	P3.3/INT1	24	P2.6/A14	39	NIC*
10	P3.4/T0	25	P2.7/A15	40	P1.0/T2
11	P3.5/T1	26	PSEN	41	P1.1/T2EX
12	P3.6/WR	27	ALE	42	P1.2/ECI
13	P3.7/RD	28	NIC*	43	P1.3/CEX0
14	XTAL2	29	EA/Vpp	44	P1.4/CEX1
15	XTAL1	30	P0.7/AD7		

* NC INTERNAL CONNECTION

SU00691

Table 1. Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	–	–	–	–	–	–	EXTRAM	AO	xxxxxx00B
AUXR1#[2]	Auxiliary 1	A2H	–	–	ENBOOT	–	GF2	0	–	DPS	xxxxxxx0B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
CCAP0H#	Module 0 Capture High	FAH									xxxxxxxxB
CCAP1H#	Module 1 Capture High	FBH									xxxxxxxxB
CCAP2H#	Module 2 Capture High	FCH									xxxxxxxxB
CCAP3H#	Module 3 Capture High	FDH									xxxxxxxxB
CCAP4H#	Module 4 Capture High	FEH									xxxxxxxxB
CCAP0L#	Module 0 Capture Low	EAH									xxxxxxxxB
CCAP1L#	Module 1 Capture Low	EBH									xxxxxxxxB
CCAP2L#	Module 2 Capture Low	ECH									xxxxxxxxB
CCAP3L#	Module 3 Capture Low	EDH									xxxxxxxxB
CCAP4L#	Module 4 Capture Low	EEH									xxxxxxxxB
CCAPM0#	Module 0 Mode	DAH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM1#	Module 1 Mode	DBH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM2#	Module 2 Mode	DCH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM3#	Module 3 Mode	DDH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM4#	Module 4 Mode	DEH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
			DF	DE	DD	DC	DB	DA	D9	D8	
CCON*#	PCA Counter Control	D8H	CF	CR	–	CCF4	CCF3	CCF2	CCF1	CCF0	00x00000B
CH#	PCA Counter High	F9H									00H
CL#	PCA Counter Low	E9H									00H
CMOD#	PCA Counter Mode	D9H	CIDL	WDTE	–	–	–	CPS1	CPS0	ECF	00xxx000B
DPTR:	Data Pointer (2 bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*	Interrupt Enable	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H
			BF	BE	BD	BC	BB	BA	B9	B8	
IP*	Interrupt Priority	B8H	–	PPC	PT2	PS	PT1	PX1	PT0	PX0	x0000000B
			B7	B6	B5	B4	B3	B2	B1	B0	
IPH#	Interrupt Priority High	B7H	–	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x0000000B
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	CEX4	CEX3	CEX2	CEX1	CEX0	ECI	T2EX	T2	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	RD	WR	T1	T0	INT1	INT0	TXD	RXD	FFH
PCON#[1]	Power Control	87H	SMOD1	SMOD0	–	–	GF1	GF0	PD	IDL	00xx0000B

SFRs are bit addressable.
SFRs are modified from or added to the 80C51 SFRs.
Reserved bits.
Reset value depends on reset source.
The state of the ENBOOT bit depends on the status byte and PSEN when reset is exited. See the AUXR1 description on page 20.

PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER DIP	LCC	QFP	TYPE	NAME AND FUNCTION
V_{SS}	20	22	16	I	**Ground:** 0V reference.
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	39–32	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}).
					Alternate functions for 89C51RX+ Port 1 include:
	1	2	40	I/O	**T2 (P1.0):** Timer/Counter 2 external count input/Clockout (see Programmable Clock-Out)
	2	3	41	I	**T2EX (P1.1):** Timer/Counter 2 Reload/Capture/Direction Control
	3	4	42	I	**ECI (P1.2):** External Clock Input to the PCA
	4	5	43	I/O	**CEX0 (P1.3):** Capture/Compare External I/O for PCA module 0
	5	6	44	I/O	**CEX1 (P1.4):** Capture/Compare External I/O for PCA module 1
	6	7	1	I/O	**CEX2 (P1.5):** Capture/Compare External I/O for PCA module 2
	7	8	2	I/O	**CEX3 (P1.6):** Capture/Compare External I/O for PCA module 3
	8	9	3	I/O	**CEX4 (P1.7):** Capture/Compare External I/O for PCA module 4
P2.0–P2.7	21–28	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 89C51RX+ family, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port
	11	13	7	O	**TxD (P3.1):** Serial output port
	12	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt
	13	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE	30	33	27	O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. ALE can be disabled by setting SFR auxiliary.0. With this bit set, ALE will be active only during a MOVX instruction.

Voltage regulator data

Fixed voltage regulators

Device	*Output voltage (V)*	*Output current (A)*	*Pinout ref.*
7805	+5	1	a (Fig 6.15)
7905	−5	1	b
7809	+9	1	a
7909	−9	1	b
7812	+12	1	a
7912	−12	1	b
7815	+15	1	a
7915	−15	1	b
7824	+24	1	a
7924	−24	1	b
78L05	+5	0.1	c
79L05	−5	0.1	d
78L12	+12	0.1	c
79L12	−12	0.1	d
78L15	+15	0.1	c
79L15	−15	0.1	d
78S05	+5	2	a
78S12	+12	2	a
78S15	+15	2	a
78S24	+24	2	a
78T05	+5	3	a
78T12	+12	3	a
78T15	+15	5	a
78H05	+5	5	e
78H12	+12	5	e

Variable voltage regulators

Device	*Output voltage*		*Output current (A)*	*Pinout ref.*
	min. (V)	*max. (V)*		
L200	2.9	36	2	
LM317LZ	1.2	37	0.1	
LM317T	1.2	37	1.5	f
LM317K	1.2	37	1.5	g
LM338K	1.2	32	5	g
LM396K	1.2	15	10	h