P-909

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
KUMARAGURU COLLEGE OF TECHNOLOGY
COIMBATORE – 641 006.

Estd. 1984

ISO 9001:2000

CERTIFICATE

This is to certify that the Project Report entitled

"DESIGN OF THREE PHASE CYCLOCONVERTER USING MICROCONTROLLER"

has been submitted by

M.DURAIRAJ	99EEE13
J.J.MAHESH	99EEE25
A.SAJEETH RAJA	99EEE44
S.SENGOTTUVELU	99EEE49

in partial fulfillment of the requirements for the award of the degree of Bachelor of Engineering in Electrical and Electronics branch of Bharathiar University, Coimbatore during the academic year 2002 - 2003

R. Mehalakshmi
Project Guide

Head of Department

Certified that the candidate with University Register No. _____
was examined in project work Viva – Voce Examination on _____

Internal Examiner

External Examiner

DEDICATED
TO
OUR BELOVED PARENTS
AND LOVABLE FRIENDS

ACKNOWLEDGEMENT

ACKNOWLEDGEMENT

We are highly privileged to thank **Dr.K.K.PADMANABHAN B.Sc.,(Engg).,M.Tech.,Ph.D.,** Principal, Kumaraguru college of Technology for allowing us to do this project.

We are highly indebted to **Dr.T.M.KAMESWARAN B.E., M.Sc.,(ENGG)Ph.d.,MISTE.,Sr.M.I.E.E.E.,FIE,** Professor and Head, who encouraged us and kindly agreed to our request for using the various college facilities.

With deep sense of gratitude, we thank our project guide and our Lecturer **Mrs.R.MAHALAKSHMI M.E.,** whose valuable guidance and enthusiastic encouragement for the successful completion of this project.

We shall be failing in our duty if we do not thank all the department staffs, lab technicians and our friends for having encouraged us and supported us morally while doing the project.

Finally, we thank one and all who co-operated with us in bringing out this project successfully.

CONTENTS

CONTENTS

1. SYNOPSIS

2. INTRODUCTION 1

3. THYRISTOR

a. Introduction 2

b. Characteristics 3

c. Thyristors Turn-on and Turn-off 6

4. CYCLOCONVERTER

a. Introduction 8

b. Types 9

c. Applications 15

5. HARDWARE DETAILS

a. Block diagram 16

b. Thyristor triggering circuit 20

c. Isolation of gate circuit 21

d. Zero crossing detectors 23

e. Power supply module 27

f. Circuit diagram of Three phase cycloconverter..29

6. PIC MICROCONTROLLER

a. Introduction 34

b. Architecture of PIC 16F877 36

c. I/O ports 40

d. Memory organization 47

e. Instruction set summary 50

f. Program Coding 54

7. CONCLUSION 60

8. BIBILIOGRAPHY 62

9. APPENDIX 64

SYNOPSIS

SYNOPSIS

The project "DESIGN OF THREE PHASE CYCLOCONVERTER USING MICROCONTROLLER" deals with the design and fabrication of three phase cycloconverter using PIC microcontroller.

This module is capable of generating frequency controlled three phase AC supply. Cycloconverter plays an important role in college laboratories and industries.

This module is directly applicable in electric traction where we need supply frequency in the range of 15-25 Hz. This scheme can be easily extended for the implementation of AC motor drives.

INTRODUCTION

The frequency conversion of three phase AC supply can be done with the help of controlled rectifier-inverter module or cycloconverter module. The former one has losses in 2 stages (rectifier stage and inverter stage). Compared to this controlled rectifier-inverter system, the cycloconverter has less power loss. So it is more preferable wherever the variable frequency is needed.

Cycloconverter is a power electronic device, which converts AC power of one frequency to AC power of another frequency. The major modules in three phase cycloconverter are listed below.

- ✓ Microcontroller
- ✓ Zero crossing detector
- ✓ Gate drive circuits
- ✓ Three phase cycloconverter module

The microcontroller gets input from the user for frequency control and generates the firing sequence for thyristors. It also gets input from three zero crossing detectors, which senses the zero crossing position of three phases. The microcontroller ON-OFF pulses are given to the driver circuit and thus, the frequency control of three phase AC supply is achieved.

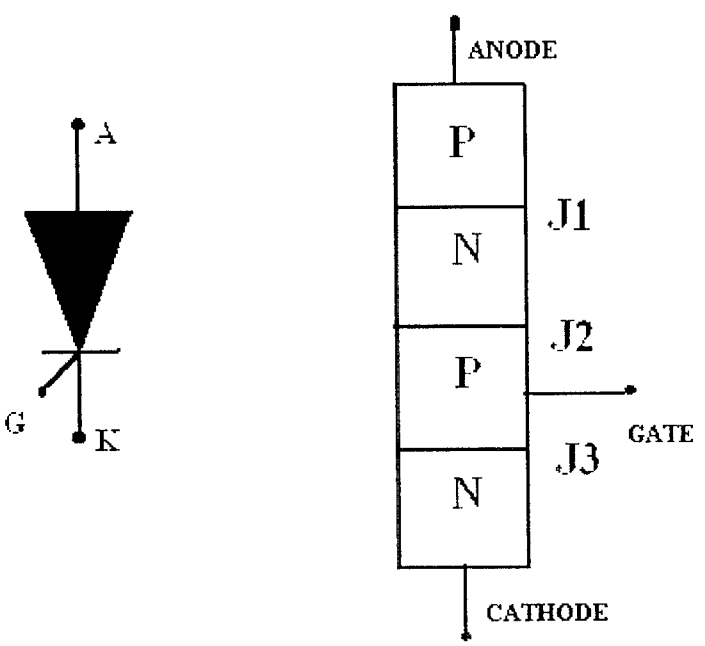
THYRISTOR

3.a INTRODUCTION

A thyristor is one of the most important types of power semiconductor devices. Thyristors are used extensively in power electronics circuits. They are operated as bistable switches, operating from non conducting state to conducting state.

A thyristor, also known as the silicon controlled rectifier (SCR),was the first solid state power semiconductor device to be developed to function as a control static switch with large current ,and voltage capacity.

Figure 3.1 JUNCTION STRUCTURE



The junction structure is shown in above fig.3.1 is a four-layer structure with three internal junctions shown labeled as J1, J2 and J3. The device has three terminals. The anode (A) and cathode (K) are the power

terminals of the switch. Control input is between the gate G and K. The anode metallic contact is on the outer P layer. The cathode contact is on the outer N layer.

The inner P layer is the Gate layer. During the fabrication of the device the regions where the gate electrical contact is to be made are masked before the cathode N layer is formed. Since the gate P layer lies sandwiched between two N layers, it is impossible to make external electrical contact with the entire gate layer area. Actually, the gate electrical is limited to a relatively small fraction of the total wafer area, the rest of it being allocated for the cathode contact. The geometrical pattern of the gate contact area on the surface of the pallet significantly affects the switching characteristics of the device.

When a forward voltage exists across the main terminals of the thyristor, a short current pulse from gate top cathode will fire the thyristor, i.e. trigger it into the ON state. Once the thyristor is fired, the gate has no further control over the current flow through the device. During the subsequent conduction, it behaves like a diode. It cannot be turned OFF by a reverse current pulse on the gate.

3.b THYRISTOR CHARACTERISTICS

When the anode voltage is made positive with respect to the cathode, the junctions J1 and J3 are forward biased. The junction J2 is reverse biased, and only a small leakage current flows from anode to cathode. Then the thyristor is said to be operating in forward blocking or OFF state condition and the leakage current is known as OFF state current Id.

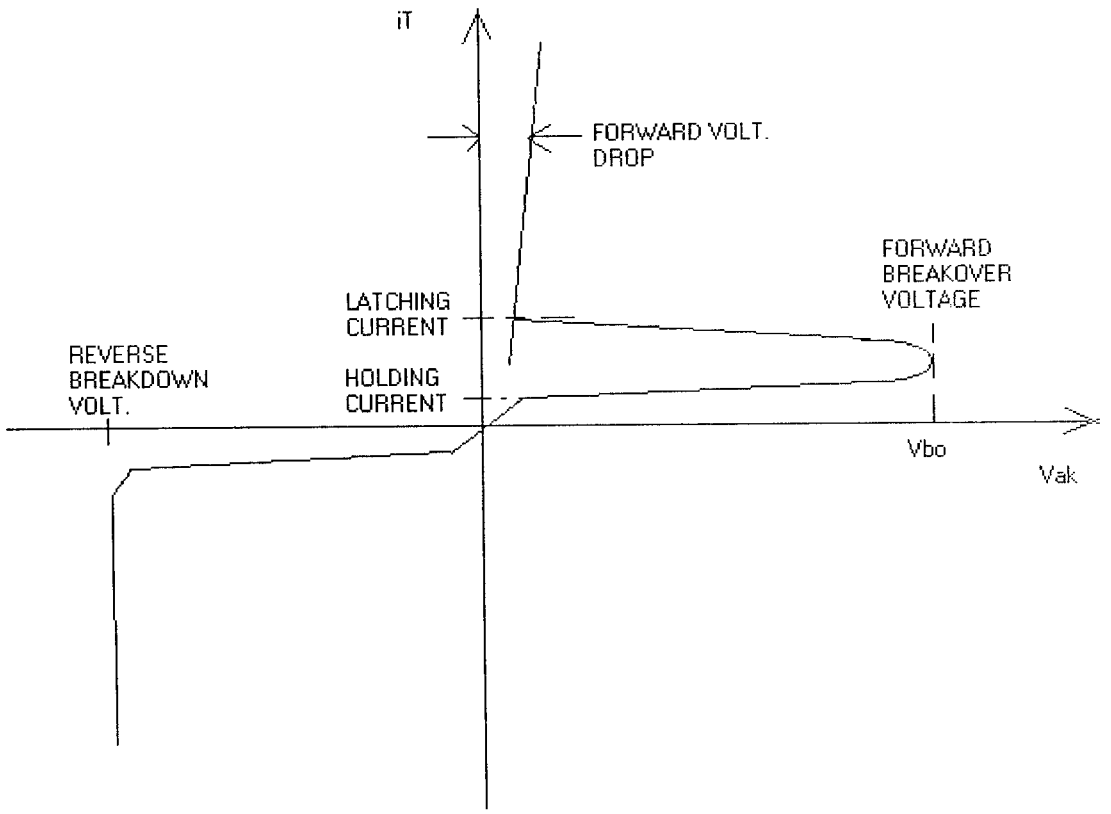


Figure 3.2 V-I Characteristics

If the anode to cathode voltage VAK is increased to a sufficiently large value, the reverse biased junction J2 will break. This is known as avalanche break down and the corresponding voltage is called forward break down voltage VBO. Since the junctions J1 and J3 are already in forward biased condition there will be free movement of carriers across all the junctions, resulting in a large forward anode current. Now the device is said to be in ON state or conducting state.

The anode current must be more than a value known as latching current IL, in order to maintain the required amount of carrier flow across the junction. Otherwise, the device will revert to the blocking condition as the anode to cathode voltage is reduced. Latching current IL is the minimum

anode current required to maintain the thyristor in ON state immediately after the thyristor has been turned ON and the gate signal has been removed. A typical V-I characteristics of a thyristor is shown in the above graph.

Once a thyristor conducts, it behaves like a conducting diode and there is no control over the device. It will continue to conduct because of depletion layer on the junction J2 due to free movements of carriers. However if the forward anode current is reduced to a level known as holding current IH , depletion region will develop around junction J2 due to the reduced number of carriers and the thyristor will be in blocking state. The holding current is in the order of milli amperes and is less than latching current. Holding current is the minimum anode current to maintain the device in the ON state, but the holding current is less than the latching current.

When the cathode voltage is positive with respect to the anode, the junction J2 is forward biased, but the junctions J1 and J3 are reversed biased. This is like two series connected diodes with reverse voltage across them. The thyristor will be in the reversed blocking state and a reverse leakage current known as reverse current IR, would flow through the device.

Thyristor can be turned ON by increasing the forward voltage VAK beyond break over voltage but such a turn ON could be destructive. In practice, the forward voltage is maintained below VBO and the thyristor is turned ON by applying a positive voltage between its gate and cathode.

3.c THYRISTOR TURN ON AND TURN OFF

THYRISTOR TURN ON

A thyristor is turned ON by increasing the anode current. This can be accomplished in any one of the following ways.

- ✓ Thermal turn ON
- ✓ Light turn ON
- ✓ High voltage turn ON
- ✓ Gate current turn ON

In thermal turn ON method the thyristor is turned ON by increasing the temperature which in turn increase the number of electron-hole pairs, which would increase the leakage current.

In Light turn ON method, light is focused on the junctions of a thyristor which increases the electron-hole pairs in the junction and causes the device turn ON.

In high voltage method, the forward anode to cathode voltage is made higher than the break down voltage, which generates the sufficient leakage current flow to initialize the regenerative turn ON.

The most important and commonly used method is the gate current turn ON method. If a thyristor is forward biased, the injection of gate current by applying positive gate voltage between the gate and cathode terminal would turn ON the thyristor.

In our project, we adopt this gate turn ON method, to trigger the SCRs present in the cycloconverter circuit.

The following points should be considered in designing the gate control circuit:

- ✓ The gate signal should be removed after the thyristor is tuned ON. A continuous gating signal would increase the power loss in the gate junction.
- ✓ While the thyristor is reverse biased, there should be no gate signal; otherwise, the thyristor will fail due to an increased leakage current.

THYRISTOR TURN-OFF

Thyristor which is in ON state can be turned OFF by reducing the forward current to a level below the holding current IH.

There are various techniques to turn OFF a thyristor. They are mainly sub divided into two categories as follows:

- ✓ Line commutating TURN OFF method.
- ✓ Forced commutating TURN OFF method.

In forced commutating turn OFF method, a negative gate pulse is applied to the gate terminal of the device and our goal is achieved, whereas in the line commutating turn OFF method, thyristor is turned OFF by the reversal of the anode voltage. Since no negative gate pulse is required in this method, this is the best method commonly adopted by all.

CYCLOCONVERTER

4.a INTRODUCTION

A cycloconverter is a direct frequency changer that converts ac power of one frequency to ac power at another frequency by ac-ac conversion, without an intermediate conversion link.

The main purpose of using cycloconverter is, that it can convert both frequency as well as, voltage of the given ac supply. In general, cycloconverter is used for reducing the supply frequency level.

The ac voltage controllers provide a variable output voltage, but the frequency is fixed and in addition, the harmonics level is very high, especially in low voltage range.

In another method, a variable output voltage at variable frequency can be obtained from two stages; A fixed ac- variable dc conversion and dc to variable ac voltage at variable frequency conversion. The former is done by the controlled rectifier and the latter is done with the help of inverter.

Anyway, this method has losses in two stages (one in rectifier stage and other in the inverter stage).

Thus the cycloconverter is the direct frequency and voltage converter which has minimum loss as compared to other methods. The majority of the cycloconverter are naturally commutated and the maximum output frequency is limited to a value that is only the fraction of the source frequency.

4.b TYPES OF CYCLOCONVERTER

According to the number of phases of the input and output voltage, cycloconverter are mainly categorized into three types, as follows:

- ✓ Single phase cycloconverter.
- ✓ Three phase to single phase cycloconverter.
- ✓ Three phase to three phase cycloconverter.

SINGLE PHASE CYCLOCONVERTER

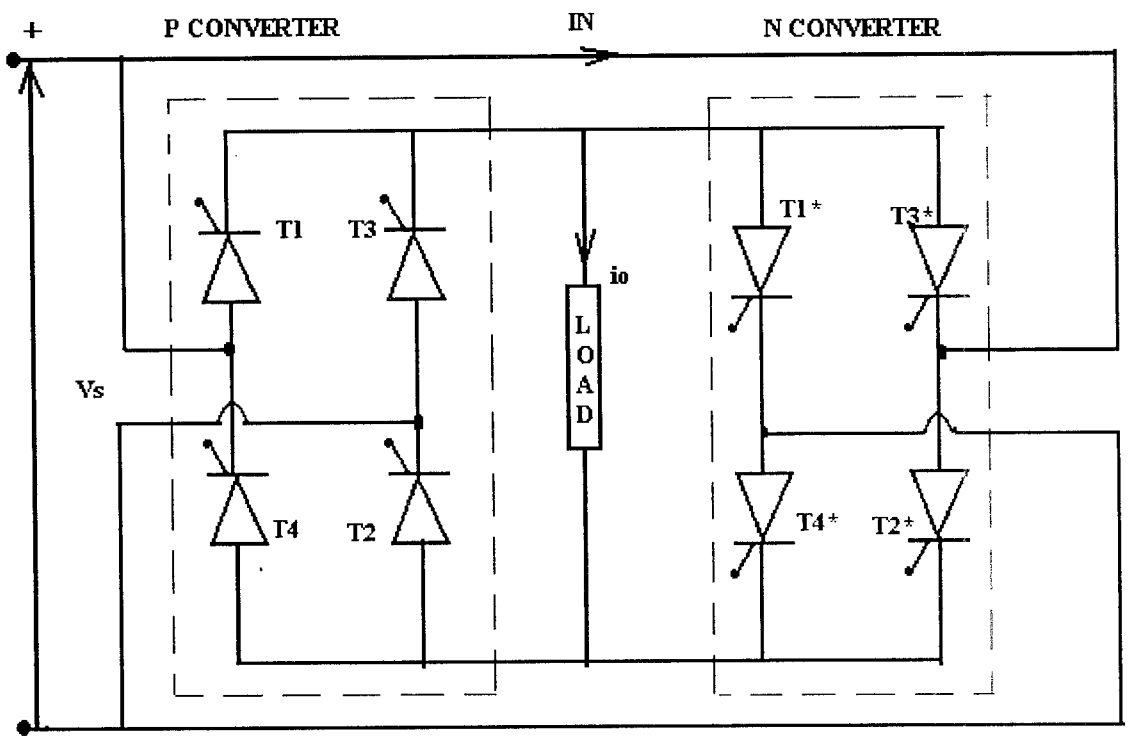


Figure 4.1 circuit diagram

The principle of operation of single phase to single phase cycloconverter can be explained with the help of fig.3. The two single phase controlled converters are operated as bridge rectifiers. However, the delay angles are such that the output voltage of one converter is equal and opposite to that of other converter.

There are two major parts in this cycloconverter circuit .They are P type converter and N type converter. P type stands for positive converters where the positive half cycles of ac supply voltage are triggered. N type are for the negative converter which works during the negative half cycles of the ac input supply.

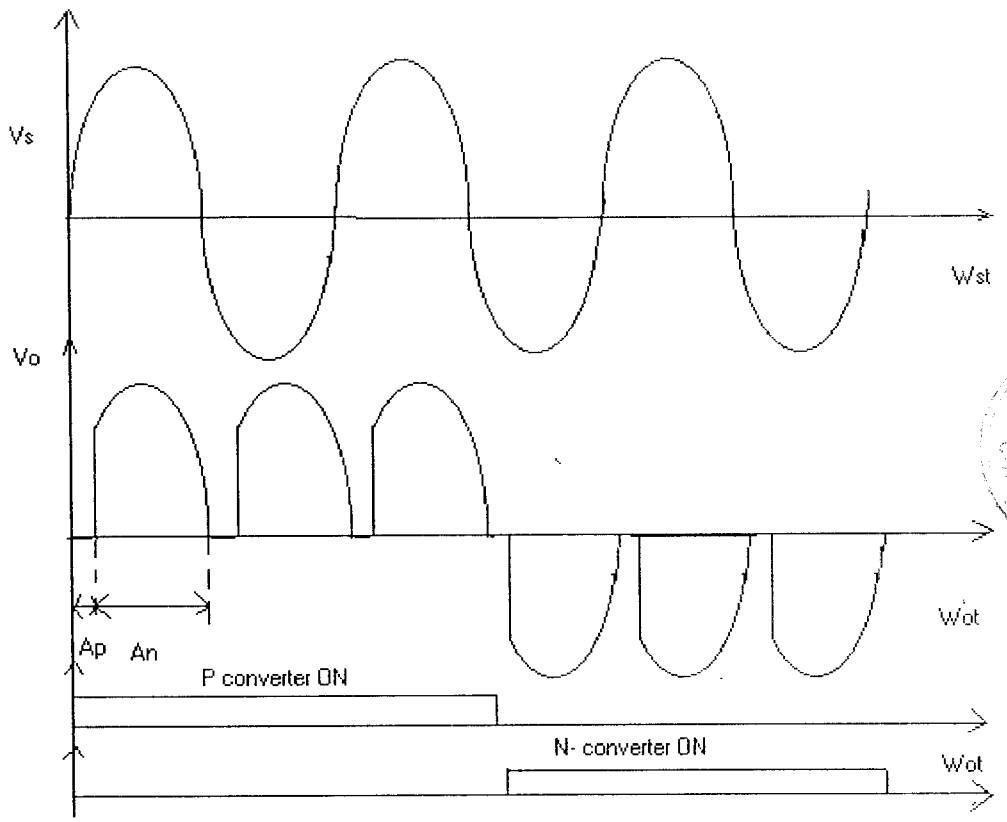


Figure 4.2 SINGLE PHASE TO SINGLE PHASE CONVERTER

If converter P is operating alone, the average output voltage is positive and if converter N is operating, the average output voltage is negative .The frequency of the output voltage is the inverse of the duty cycle (To).

i.e. Fo =1/To;

If the delay angle of positive converter is Ap and the delay angle of negative converter is (π -Ap), then the average output voltage is equal and opposite to that of negative converter.

The circulating current can be eliminated by suppressing the gate pulse to the converter which does not deliver load current at that instant.

WORKING

Referring to Fig 3, the working principle of single phase cycloconverter is quiet obvious. During the positive half cycle of the input ac supply (0-π), Thyristor T1 and T2 are triggered at a delay angle of Ap, which generates (Ap-π) positive cycle at the output waveform. Then T3 and T4 are triggered during the negative cycle of input that generates (π+Ap to 2π) positive cycle of the output waveform.

Likewise, T1*, T2*, T3*and T4* SCRs are triggered for the generation of the negative cycle of the output voltage. Thus, the frequency is reduced by 3 times, and hence the duty cycle is increased by 3 times. By changing the triggering sequence, the supply frequency can be varied accordingly.

The single phase cycloconverter is mainly used in the ac motor drives where the frequency and voltage to the motor is controlled by this circuit and hence the speed of the motor is controlled according to the load current .Thus it finds its main application in electrical drives.

THREE PHASE CYCLOCONVERTER

The cycloconverter which employs three phase supply are called as three phase cycloconverter. According to the number of phases at the output side, these cycloconverter are categorized into two. They are:

- ✓ Three phase to Single phase cycloconverter and,
- ✓ Three phase to three phase cycloconverter.

THREE PHASE TO SINGLE PHASE CYCLOCONVERTER

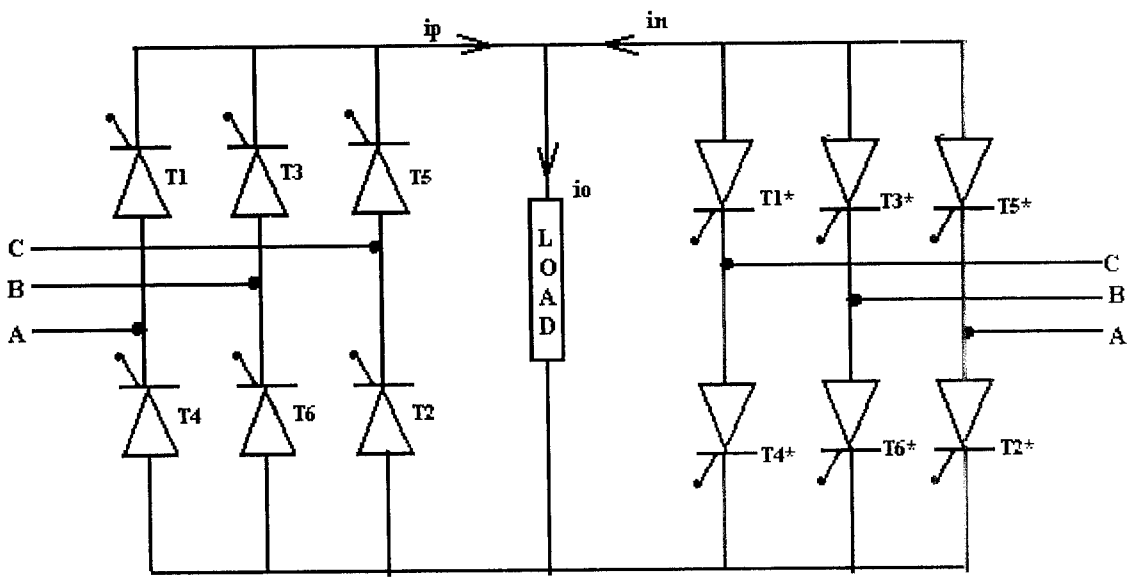


Figure 4.3 Schematic diagram

WORKING

The circuit diagram of three phases to single phase cycloconverter is shown in the Fig 5. The two ac to dc converters are three phase controlled rectifiers. The synthesis of output waveform for an output frequency of one third of the supply frequency.

Twelve SCRs are employed here, in which six for positive cycle and the other six for negative cycle of the output voltage. SCRs T1 and T6 are triggered when V_{ca} phase becomes zero, whereas T3 and T2 are triggered when phase V_{ab} starts its negative half cycle.T5 and T4 has its role when Vbc starts its negative period. In the same manner the other six SCRs are triggered for the generation of negative period of output voltage.

Output frequency value depends on the number of waveforms present in one half cycle at the output voltage. Each waveform has the period of two third of input period. The formula to the output frequency is derived as follows.

To=2/3x (No. of waves present at the one period of output voltage)x Ts

Where,

To: Output time period

Ts: Input time period

Output frequency, Fo = 1/To.

THREE PHASE TO THREE PHASE CYCLOCONVERTER

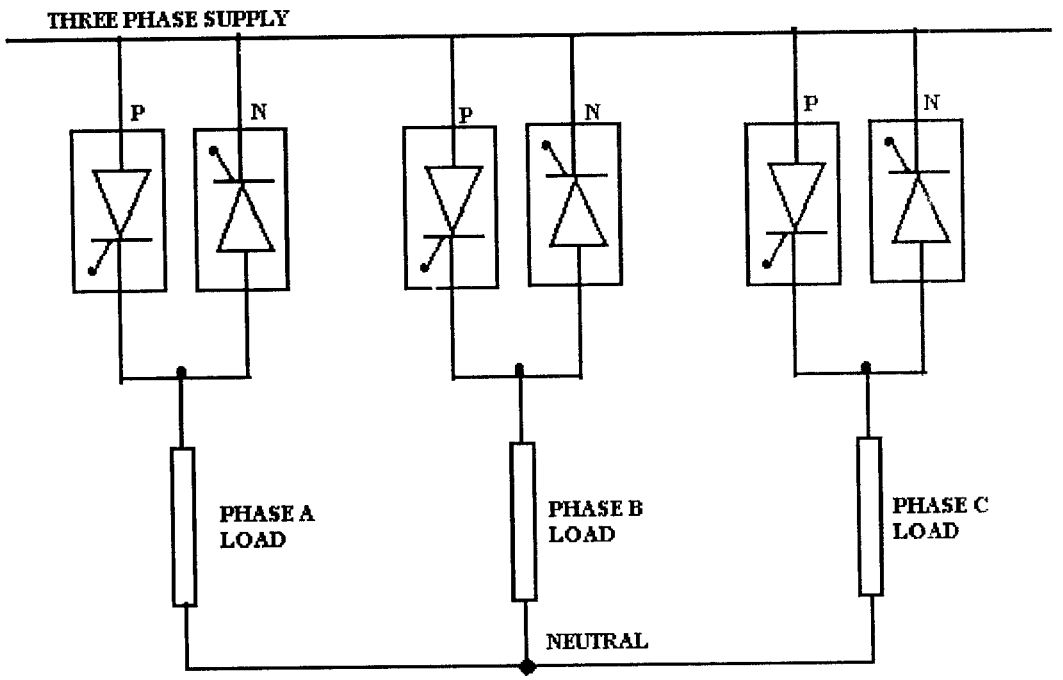


Figure 4.4 Schematic diagram

The schematic diagram of three phase to three phase cycloconverter is shown in the above figure. This circuit consists of 3 positive type converters and 3 negative type converters for each phase of load respectively. Each positive type converter has 3 thyristors connected to the phases R, Y and B respectively. The actual circuit diagram is illustrated in the following chapter.

4.c APPLICATIONS OF CYCLOCONVERTER

The major applications of cycloconverter are low speed, ac motor drives in the range up to 15,000 Kw with frequencies from 0 to20 Hz.

In the induction and synchronous motors, the motor speed is directly proportional to supply frequency.

$$N = (120 * F)/P$$

Where, N: synchronous speed of the motor.

F: supply frequency.

P: number of poles.

Thus, the cycloconverter is more preferable for ac motor drives with low frequency range. The electric traction finds its better operation when the frequency of AC supply is in the range of 15-25 Hz. This low frequency is achieved with the help of cycloconverter.

The next major area of its application is in the high frequency transmission system. Here, the ac voltage of high frequency is generated and is transmitted to the nearby areas. At the receiving side, cycloconverter is employed for the conversion of both voltage and frequency of transmitted ac power to the required level.

The advantages of high frequency transmission system are as follows.

- ✓ The size of the transformers and capacitors in the different stages of the transmission line is considerably minimized.
- ✓ The voltage fluctuations are minimized.

HARDWARE DETAILS

5.a BLOCK DIAGRAM

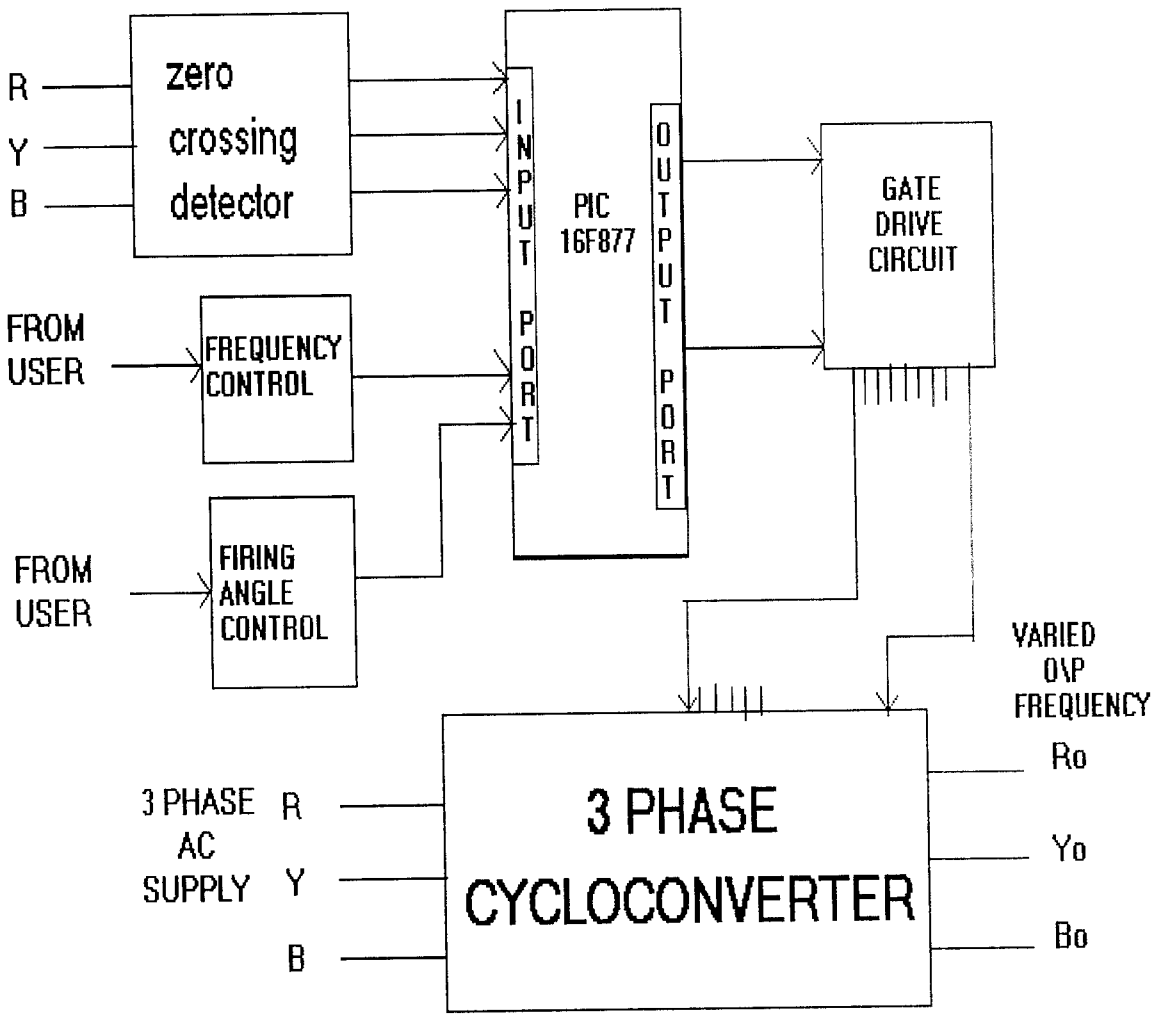


Figure 5.1

The schematic diagram of three phase cycloconverter with frequency control and firing angle control is illustrated in the above Fig.1.

Three phase cycloconverter circuit consists of 18 SCRs which has to be triggered in a proper timing sequence. The timing sequences of the various gate signals to the SCRs are controlled by the PIC microcontroller PIC16F877 type IC. The various blocks are explained below.

ZERO CROSSING DETECTORS

It is a circuit that converts the input line supply into the low voltage square pulses to analyze the zero crossing of the input sine wave. We have designed this circuit with the help of OP-amp (IC741). This detector generates positive state of square pulse during the negative half cycle of the input sine wave and the negative state of the output pulse during the positive half period of sine wave. Thus the zero crossing of the high voltage input supply is successfully analyzed using this zero crossing detector. The output terminal of the zero crossing detectors is connected to the input port of the microcontroller to feed the zero crossing data to the controller.

FREQUENCY CONTROL

The three phase cycloconverter must generate variable frequency output voltage according to the requirement of the user. So the user input is given to the frequency control circuit that generates the corresponding signal to the microcontroller to vary the gate timing signal which in turn, varies the frequency of the cycloconverter output.

VOLTAGE CONTROL

The voltage control in any converter circuit is done by varying the firing angle of SCR triggering. When the firing angle is less the output voltage is somewhat same as the input voltage level. The output voltage can be reduced to a considerable value by increasing the firing angle accordingly. The user feeds his\her data into the firing angle unit which generates the signals for microcontroller to change the output voltage at the required level. So the voltage control unit is connected to the input port pin of the controller.

MICROCONTROLLER

The analog control scheme for the cycloconverter can be implemented by hard wired electronics. An analog control scheme has several disadvantages:

Non linearity of voltage sensor, temperature dependency, drift and offset. Once a control circuit is built to meet certain performance criteria, it may require changes in the hard wire logic circuits to meet other performance requirements. So the microcontroller is selected to control the gate sequence of the SCRs, present in the cycloconverter circuits.

Microcontroller reduces the size and cost of hard wired electronics, improving reliability and control performance. This control scheme is implemented in the software and is flexible to change the control strategy to meet different performance characteristics of the cycloconverter. In our project we have adopted PIC microcontroller due to its easiness, reliability, cost effective and various other features.

GATE DRIVE CIRCUIT

The microcontroller output pins which generate gate signals for the thyristors cannot be directly connected to the gate terminal of the SCR. If it so connected, there is a chance for the back flow of high voltage from the power circuit, that may damage the microcontroller. In addition, the gate signal from the microcontroller is so weak that it cannot trigger a thyristor. So it has to be amplified by a gate drive circuit. Here we have 18 gate drive circuits for the SCRs in the cycloconverter.

THREE PHASE CYCLOCONVERTER

This is the main part of our project which is a power electronic converter circuit to convert three phase AC power at one frequency to AC power at another frequency by AC to AC conversion without an intermediate conversion link. The frequency and voltage of the input AC supply can be varied according to the user input to the frequency control and firing control circuits, with the help of three phase cycloconverter. The three phase cycloconverter finds its major application in low speed AC motor drives with the frequency range of 0-20 Hz, supply circuits for traction and in the receiving system of high frequency transmission line.

5.b TRIGGERING CIRCUIT

DESIGN OF GATE CIRCUIT:

The triggering circuit of the thyristor converter is designed to provide the gate firing pulses to the thyristors at the appropriate instants of time. The switching control unit of a power electronic converter generally has a timing circuit in it. This timing circuit generates the timing pulses at the correct instance of time at which each power device has to be switched. The timing circuit for different switching element normally provides a pulse whose duration is the ON time of the device. In general, such a pulse from the triggering circuit cannot be applied to the gate terminal of the device for the following reasons:

1. Thyristor only needs a pulse of short duration and not for the entire duration of the ON time.
2. It may need further amplification to be able to provide the required current and power to successfully turn ON the device.
3. It is invariably necessary to provide electrical isolation between the triggering circuit and the power circuit of the converter. The power switching elements will generally be working at high and variable potentials, from which the control circuits should have to be isolated.

In this project, the microcontroller is employed to generate the timing and triggering pulses for the SCRs. So, the design of triggering circuit becomes an easy job.

Even though the triggering signals for various SCRs in the converter are generated directly by the microcontroller, the outport pin of the controller cannot be directly connected to the gate terminal of the thyristor. In thyristor converters, different potentials exist at various terminals. The power circuit is subjected to a high voltage, usually greater than 100V and

the gate circuit is held at low voltage, typically 8 to 30V. An isolation circuit is necessary between an individual thyristor and its gate pulse generating circuit.

5.c ISOLATION OF GATE CIRCUIT

Generally, the isolation can be accomplished either by pulse transformers or optocouplers. An optocoupler could be phototransistor as shown in next page.

In pulse transformer isolation, pulse transformer is connected with a diode across its primary winding and the secondary is connected to the gate terminal of the SCR.

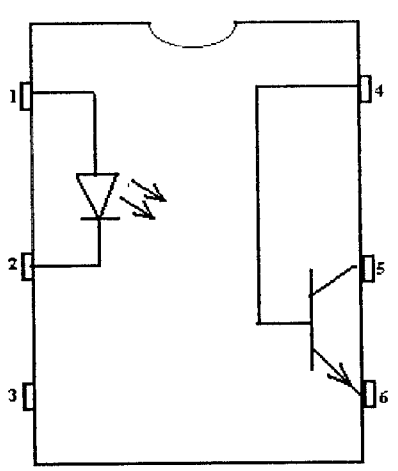
For our circuit, we have adopted optocoupler isolation technique.

OPTOCOUPLER

An optocoupler could be a phototransistor or photo-SCR. A short pulse to the input of the infrared light emitting diode (ILED), the diode turns ON the phototransistor. This type of isolation requires the separate power supply and the cost and weight of the firing circuit is increased.

Optocoupler (MCT2E):

Figure 5.2 Pin diagram



WORKING

The infrared light emitting diode (ILED) is connected to the output port pin of the microcontroller in which the gate signal is generated. The base of the NPN photo transistor is left free. The collector terminal is supplied by the separate source voltage Vcc (8V). The gate of the SCR is connected to the emitter of the photo transistor.

When the output pin of the controller is in HIGH state, the infrared LED glows which activates the base of the photo transistor. After the numbers of free electrons present in the base crosses a particular range, the photo transistor is triggered and the supply Vcc at the collector is connected to the emitter of the transistor. When controller output goes to LOW state, the ILED is turned off and the transistor is triggered OFF. Thus the emitter Is not connected to the collector supply (Vcc).

Since there is no physical contact between the power circuit and the microcontroller circuit, perfect isolation is achieved by this optocoupler triggering circuit.

5.d ZERO CROSSING DETECTORS

This detector circuit is added to analyze the state of three phase input sine wave at each instant. The basic comparator circuit can be modified as zero crossing detector. Here, we have adapted general purpose op-amp (IC741).

Op_ amps have five basic terminals that is, two input terminals, one output terminals, two power supply terminals. The significance of other terminals varies with the type of the op-amp. The general purpose op-amp has eight pins. Pin 2 is called the inverting input terminal and pin 3 is non inverting input terminal, pin 6 is the output terminal and pins 7 and 4 are the

supply terminals labeled as V+ and V- respectively. Terminals 1 and 5 are used for DC offset. The pin 8 marked NC indicates no connection.

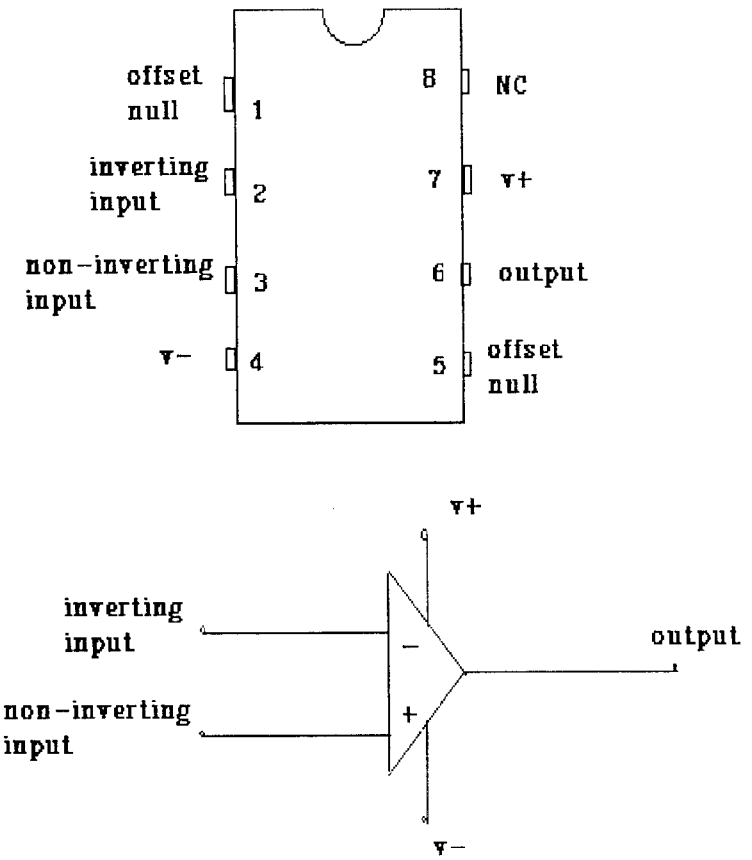


Figure 5.4 Pin diagram of IC741

The V+ and V- power supply terminals are connected to two DC voltage sources. V+ is connected to the positive terminal of one source and V- pin is connected to the negative terminal of the other source. The general op-amp circuit is shown in the above Fig. The power supply voltage range from about 5V to 22V. The common terminal of V+ and V- sources is connected to the reference or ground.

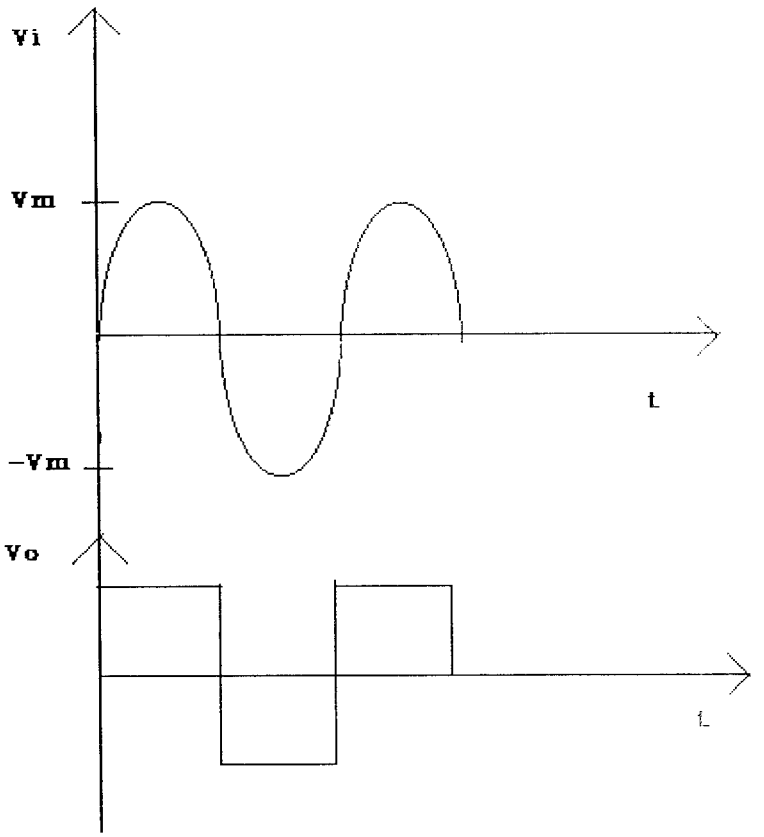


Figure 5.6 Waveforms

When the input sine wave of the inverting terminal crosses 0v from negative to positive cycle, the output waveform of zero crossing detector shifts from +Vsat value to ground state. When the sine wave crosses the zero from +ve to –ve half cycle, the output waveform is suddenly shifted to the HIGH state from ground state. Thus the zero crossing detector generates square wave for the given sine wave. So, this circuit is also called sine to square wave generator.

5.e POWER SUPPLY MODULES

DC REGULATED SUPPLY FOR MICROCONTROLLER

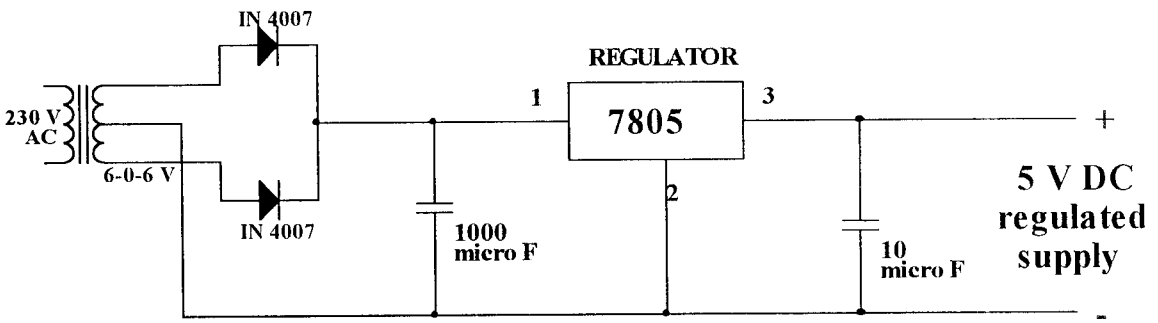


Figure 5.7(a)

DC REGULATED SUPPLY FOR THYRISTOR GATE

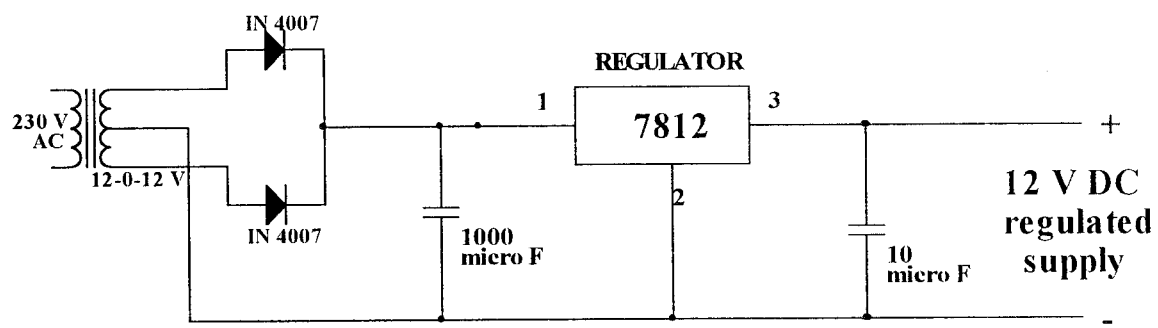
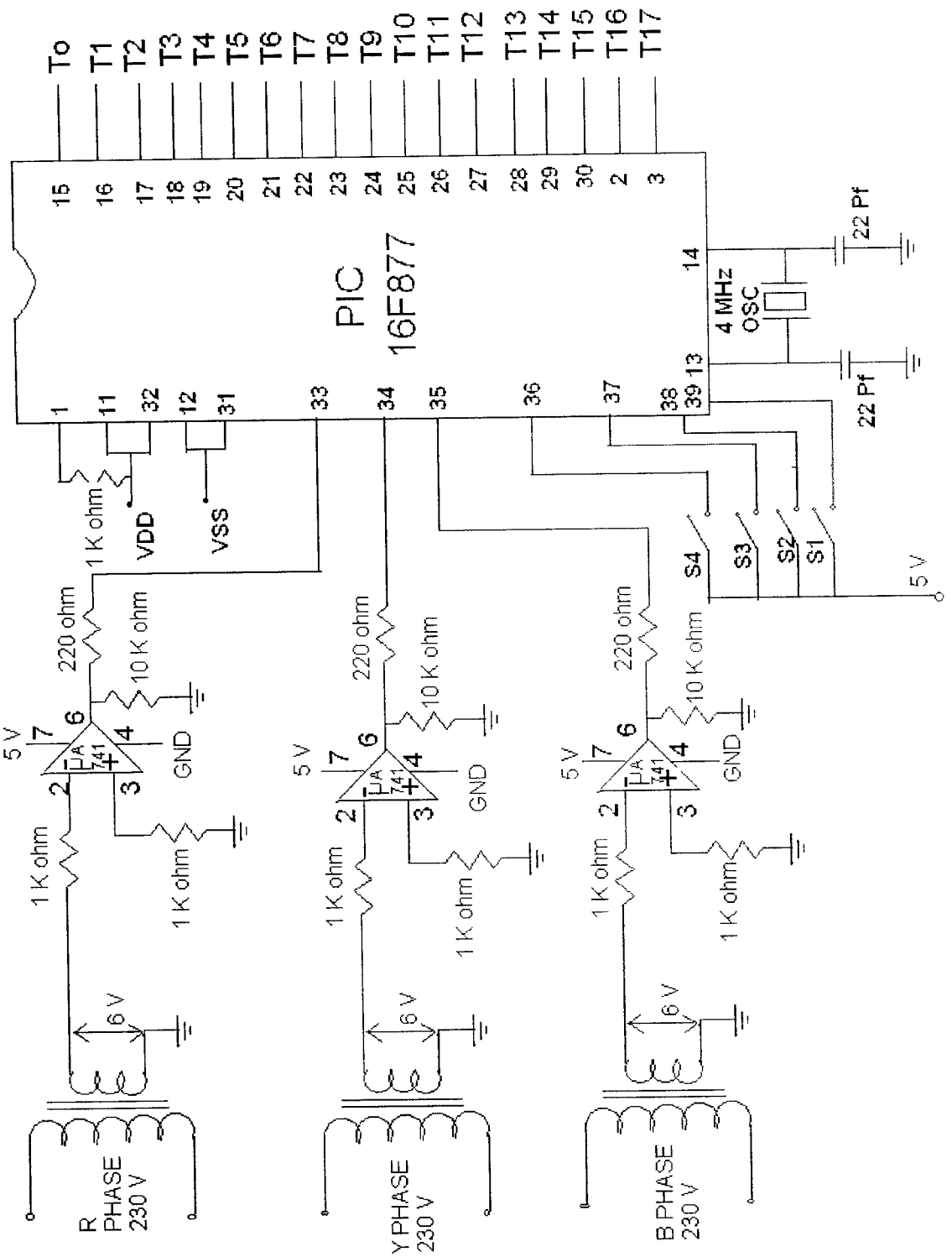


Figure 5.7(b)

The above figures illustrate the power supply modules for microcontroller and thyristor triggering. The microcontroller needs a regulated 5V DC supply whereas the thyristor is triggered by 12V regulated DC supply.

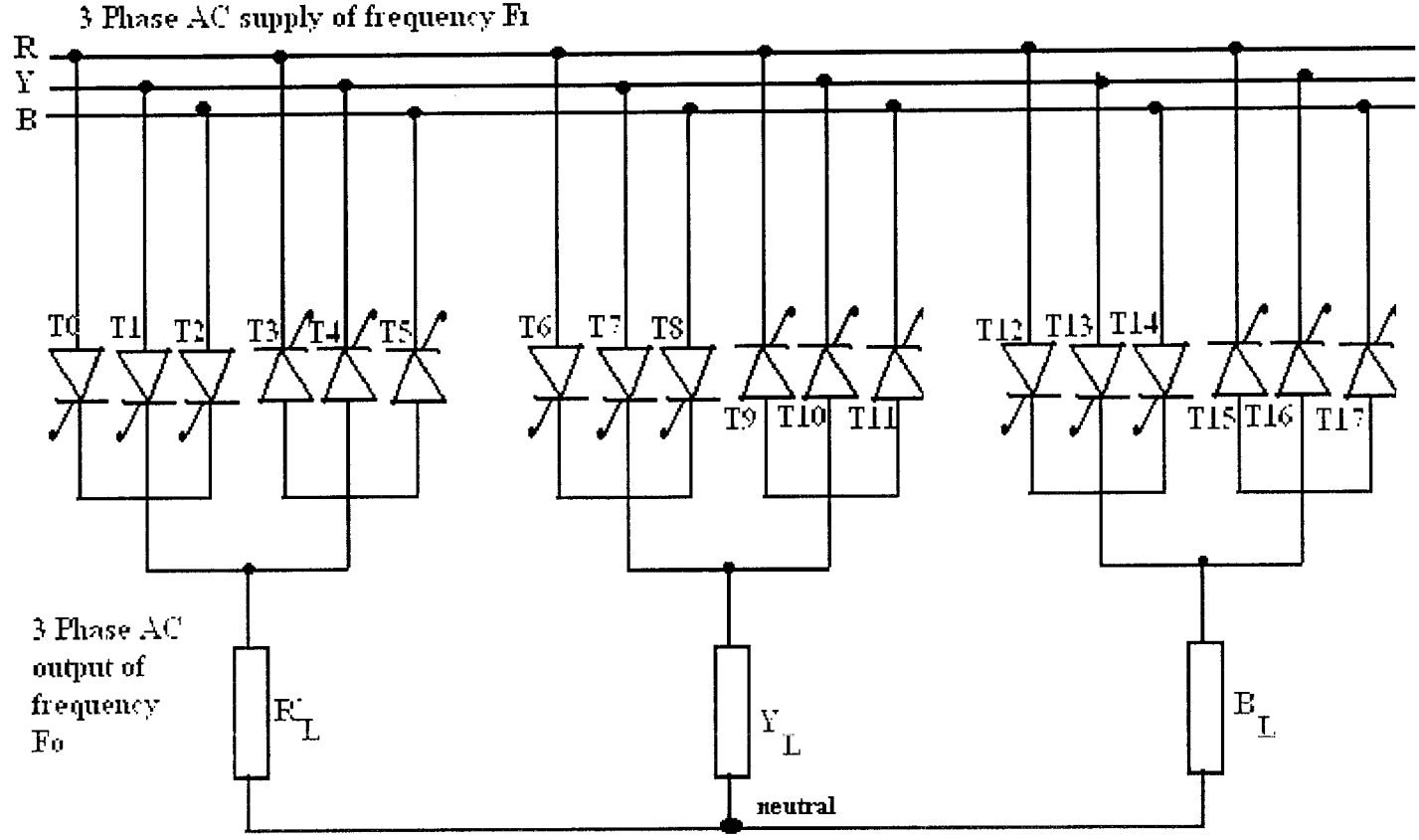
In this circuit, the AC voltage of 230V is stepped down and is full wave rectified by means of two diodes. To get the 5V DC supply, 230/6-0-6 V transformer is used. The IN 4007 diodes have been employed for the rectification purpose. Since the diode output is not a pure DC, the ripples are filtered using a 1000 micro farad capacitor. To get the regulated power supply IC7805 and IC 7812 regulators are employed. Even though the output of regulator is pure regulated DC there may be some ripples which are filtered by means of 10 micro farad capacitor and thus the regulated DC supply is obtained.

In this project, single 5V regulated supply is enough whereas we need six 12V regulated supplies for the thyristors. SCRs which do not have common cathode connection, cannot be fed with common 12 V gate supply. So it is very essential to design separate six 12V regulated DC supplies.



CIRCUIT DIAGRAM 1

THREE PHASE CYCLOCONVERTER



CIRCUIT DIAGRAM 2

TRIGGERING PULSES FOR SCRs

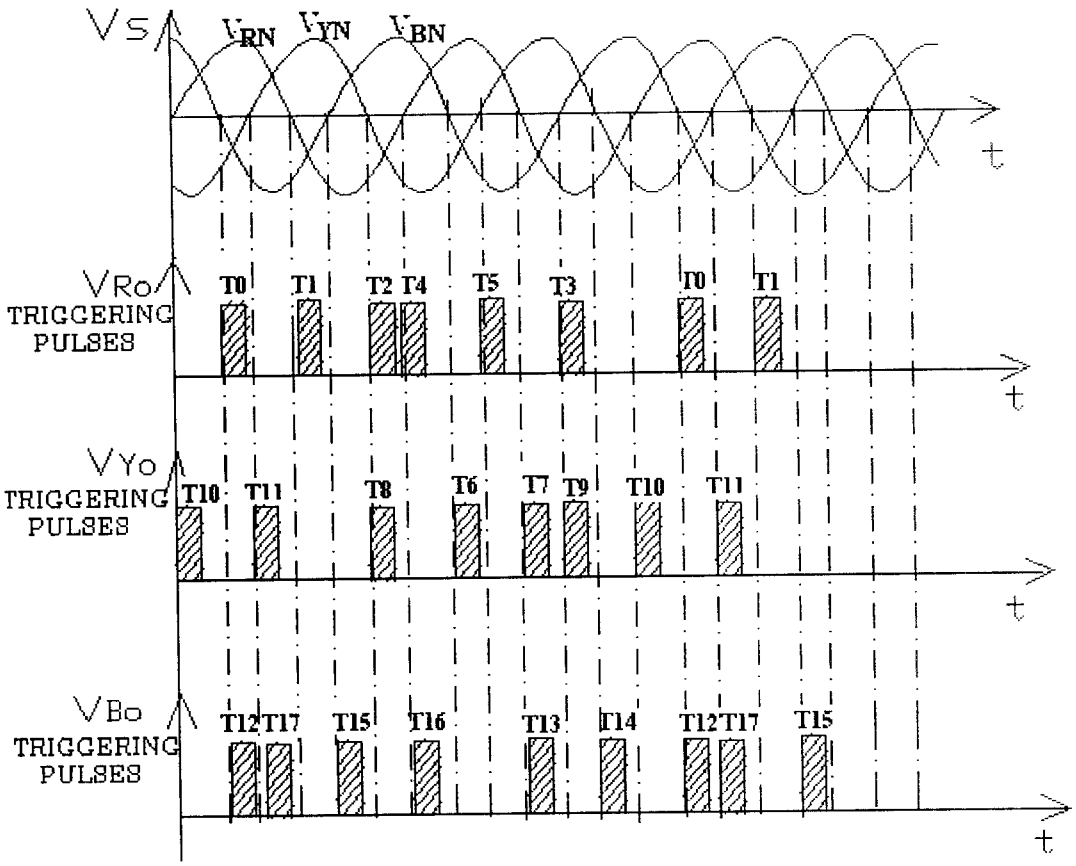


Figure 5.8

WAVEFORMS OF THREE PHASE CYCLOCONVERTER

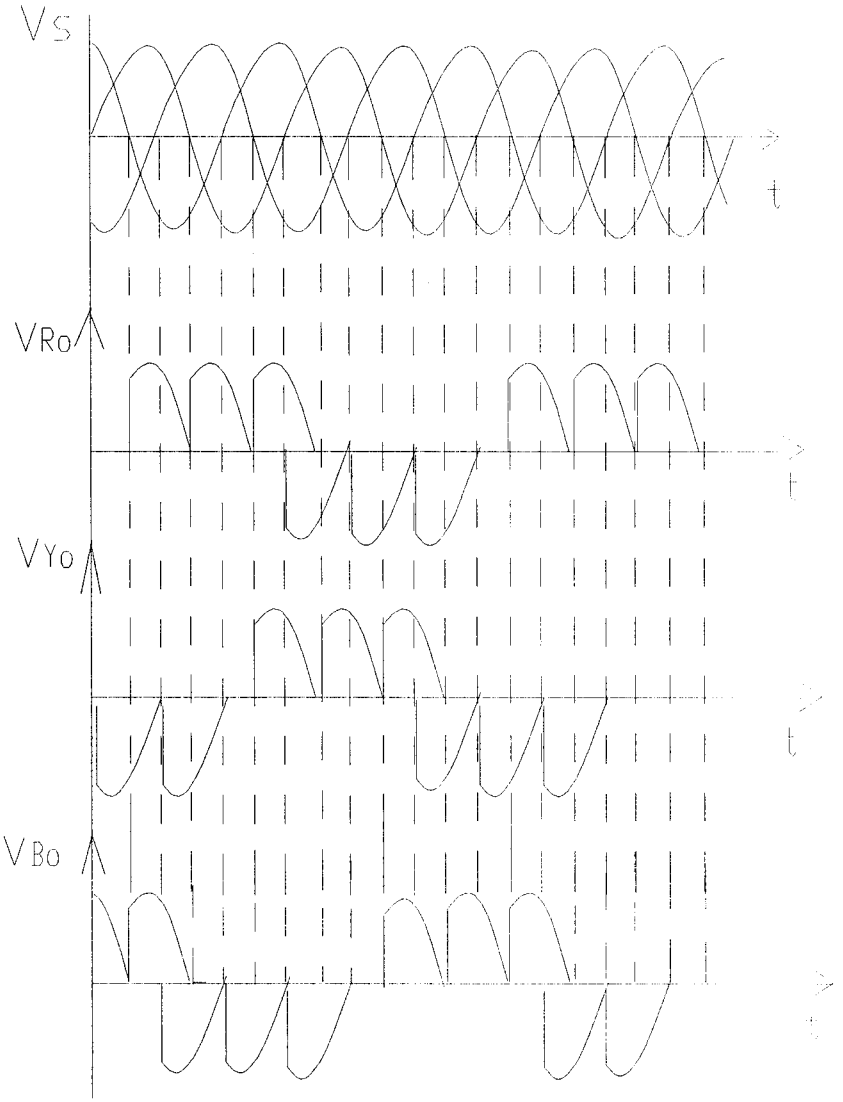


Figure 5.9

The circuit diagram 1 explains the pin connections of the PIC microcontroller. Here port B is treated as input port and other ports (port A, port C and port D) are taken as output port. Three are three zero crossing detectors whose outputs are connected to the port B pins (33, 34 and 35). The user input for firing angle control is given through the four switches S1-S4.

The controller is programmed to sense all these input data and to generate the gate pulses for 18 SCRs present in the three phase cycloconverter circuit. These pulses are fed to the gate drive circuit which is illustrated in the figure 5.3.

The circuit diagram of three phase cycloconverter alone is shown in the diagram 2. The triggering pulses generated by the microcontroller for the zero firing angle is shown in the Figure 5.8. The input and output three phase AC waveforms are shown in the figure 5.9. This is the triggering control logic for getting half frequency three phase output from the cycloconverter circuit. By using this triggering logic, any variable frequency is possibly obtained.

PIC MICROCONTROLLER

6. a INTRODUCTION

The core features of PIC Microcontroller are

- High performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Up to 8K x 14 words of FLASH Program Memory,
  Up to 368 x 8 bytes of Data Memory (RAM)
  Up to 256 x 8 bytes of EEPROM Data Memory
- Pinout compatible to the PIC16C73B/74B/76/77
- Interrupt capability (up to 14 sources)
- Eight level deep hardware stack
- Direct, indirect and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low power, high speed CMOS FLASH/EEPROM technology
- Fully static design
- In-Circuit Serial Programming. (ICSP) via two pins
- Single 5V In-Circuit Serial Programming capability
- In-Circuit Debugging via two pins
- Processor read/write access to program memory
- Wide operating voltage range: 2.0V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial, Industrial and Extended temperature ranges
- Low-power consumption:
  < 0.6 mA typical @ 3V, 4 MHz
  20 μA typical @ 3V, 32 kHz
  < 1 μA typical standby current

Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during SLEEP via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
  - Capture is 16-bit, max. resolution is 12.5 ns
  - Compare is 16-bit, max. resolution is 200 ns
  - PWM max. resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI. (Master mode) and I2C. (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

6.b ARCHITECTURE OF PIC 16F877

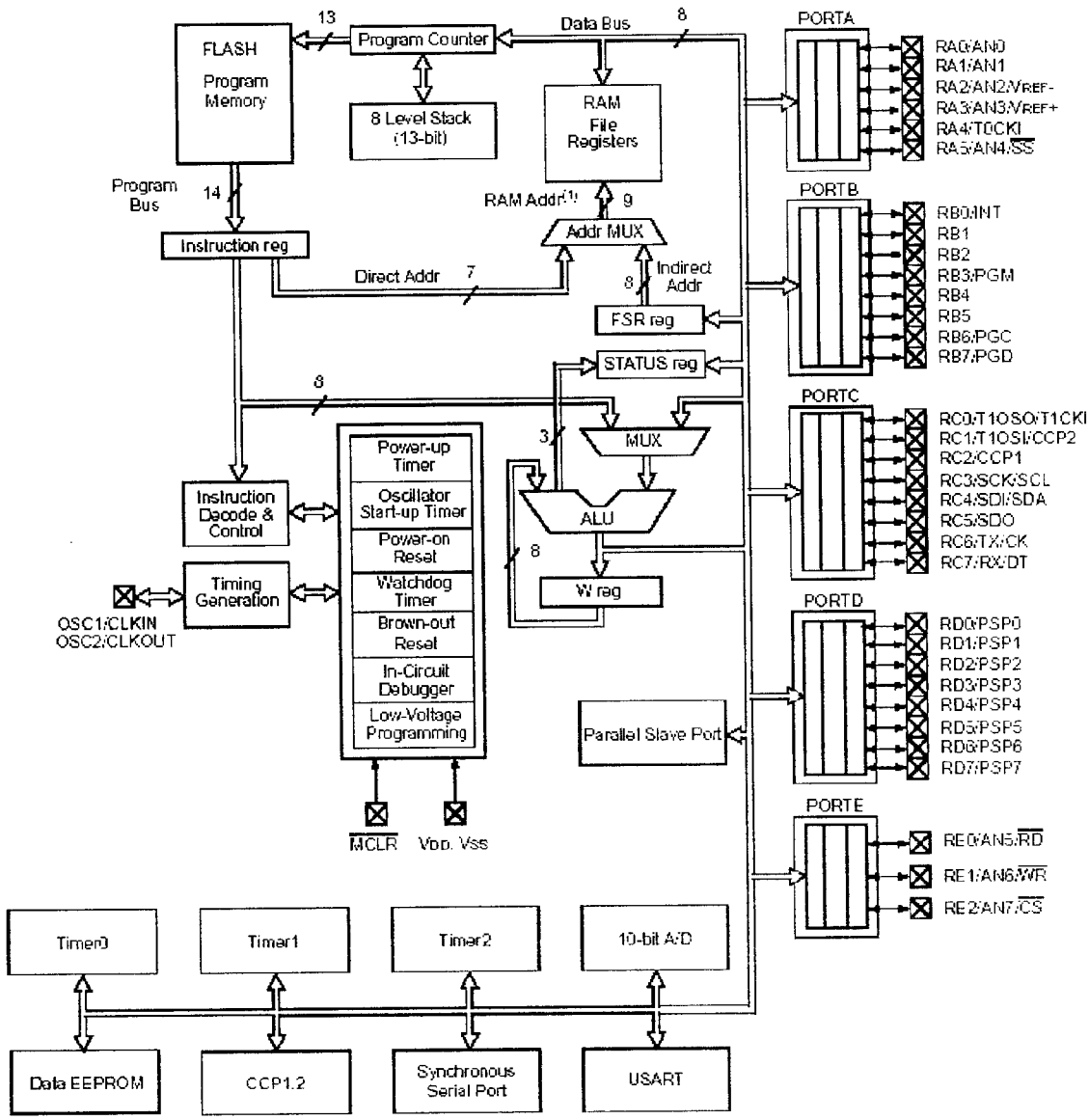


Fig 6.1: ARCHITECTURE OF PIC 16F877

DEVICE	PROGRAM FLASH	DATA MEMORY	DATA EEPROM
PIC 16F877	8K	368 Bytes	256 Bytes

Fig 6.2 16F877-PIN CONFIGURATION

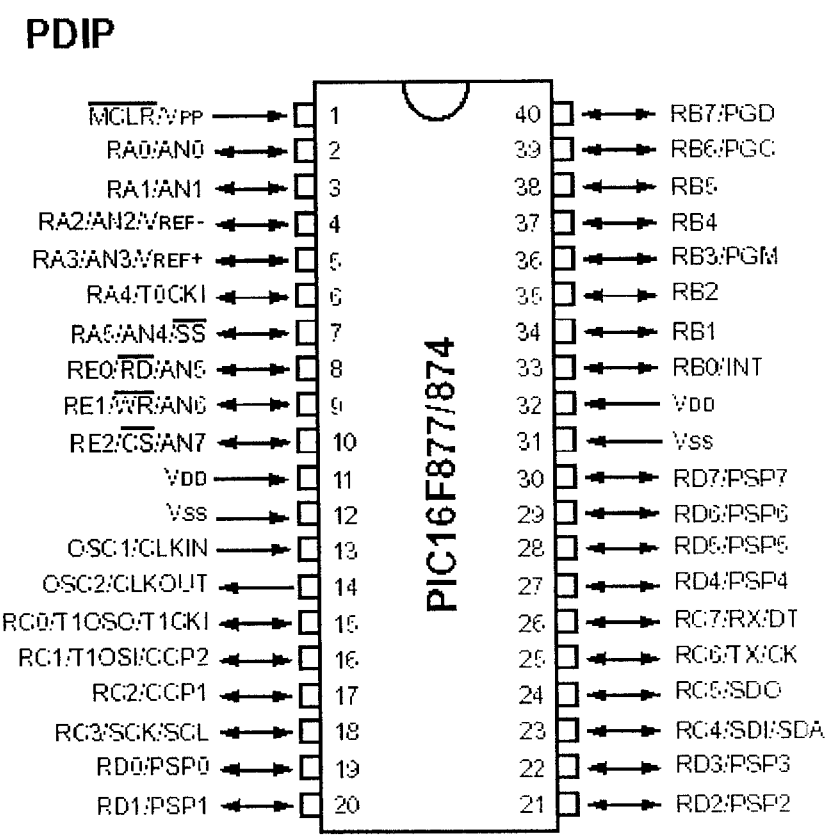


Table 1: PIN OUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	I	ST/CMOS(4)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	2	18	I/P	ST	Master Clear (Reset) input or programming voltage input. This pin is an active low RESET to the device.
						PORTA is a bi-directional I/O port.
RA0/AN0	2	3	19	I/O	TTL	RA0 can also be analog input0.
RA1/AN1	3	4	20	I/O	TTL	RA1 can also be analog input1.
RA2/AN2/VREF-	4	5	21	I/O	TTL	RA2 can also be analog input2 or negative analog reference voltage.
RA3/AN3/VREF+	5	6	22	I/O	TTL	RA3 can also be analog input3 or positive analog reference voltage.
RA4/T0CKI	6	7	23	I/O	ST	RA4 can also be the clock input to the Timer0 timer/ counter. Output is open drain type.
RA5/$\overline{SS}$/AN4	7	8	24	I/O	TTL	RA5 can also be analog input4 or the slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be soft-ware programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST(1)	RB0 can also be the external interrupt pin.
RB1	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3/PGM	36	39	11	I/O	TTL	RB3 can also be the low voltage programming input.
RB4	37	41	14	I/O	TTL	Interrupt-on-change pin.
RB5	38	42	15	I/O	TTL	Interrupt-on-change pin.
RB6/PGC	39	43	16	I/O	TTL/ST(2)	Interrupt-on-change pin or In-Circuit Debugger pin. Serial programming clock.
RB7/PGD	40	44	17	I/O	TTL/ST(2)	Interrupt-on-change pin or In-Circuit Debugger pin. Serial programming data.

Legend: I = input O = output I/O = input/output P = power

— = Not used TTL = TTL input ST = Schmitt Trigger input

Note

1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

4: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
						PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	15	16	32	I/O	ST	RC0 can also be the Timer1 oscillator output or a Timer1 clock input.
RC1/T1OSI/CCP2	16	18	35	I/O	ST	RC1 can also be the Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output.
RC2/CCP1	17	19	36	I/O	ST	RC2 can also be the Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3 can also be the synchronous serial clock input/output for both SPI and I^2C modes.
RC4/SDI/SDA	23	25	42	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	24	26	43	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK	25	27	44	I/O	ST	RC6 can also be the USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	26	29	1	I/O	ST	RC7 can also be the USART Asynchronous Receive or Synchronous Data.
						PORTD is a bi-directional I/O port or parallel slave port when interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	I/O	ST/TTL(3)	
RD1/PSP1	20	22	39	I/O	ST/TTL(3)	
RD2/PSP2	21	23	40	I/O	ST/TTL(3)	
RD3/PSP3	22	24	41	I/O	ST/TTL(3)	
RD4/PSP4	27	30	2	I/O	ST/TTL(3)	
RD5/PSP5	28	31	3	I/O	ST/TTL(3)	
RD6/PSP6	29	32	4	I/O	ST/TTL(3)	
RD7/PSP7	30	33	5	I/O	ST/TTL(3)	
						PORTE is a bi-directional I/O port.
RE0/$\overline{RD}$/AN5	8	9	25	I/O	ST/TTL(3)	RE0 can also be read control for the parallel slave port, or analog input5.
RE1/$\overline{WR}$/AN6	9	10	26	I/O	ST/TTL(3)	RE1 can also be write control for the parallel slave port, or analog input6.
RE2/$\overline{CS}$/AN7	10	11	27	I/O	ST/TTL(3)	RE2 can also be select control for the parallel slave port, or analog input7.
Vss	12,31	13,34	6,29	P	—	Ground reference for logic and I/O pins.
VDD	11,32	12,35	7,28	P	—	Positive supply for logic and I/O pins.
NC	—	1,17,28, 40	12,13, 33,34		—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input O = output I/O = input/output P = power

— = Not used TTL = TTL input ST = Schmitt Trigger input

Note

1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

4: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

6.c I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

PORTA and the TRISA Register

PORTA is a 6-bit wide, bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin). Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, the value is modified and then written to the port data latch. Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other PORTA pins have TTL input levels and full CMOS output drivers. Other PORTA pins are multiplexed with analog inputs and analog VREF input. The operation of each pin is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register1).

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

Table 2: PORT A Functions

Name	Bit#	Buffer	Function
RA0/AN0	bit0	TTL	Input/output or analog input.
RA1/AN1	bit1	TTL	Input/output or analog input.
RA2/AN2	bit2	TTL	Input/output or analog input.
RA3/AN3/VREF	bit3	TTL	Input/output or analog input or VREF.
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0. Output is open drain type.
RA5/SS/AN4	bit5	TTL	Input/output or slave select input for synchronous serial port or analog input.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Table 3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--0x 0000	--0u 0000
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
9Fh	ADCON1	ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0	--0- 0000	--0- 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

PORTB and the TRISB Register

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin). Three pins of PORTB are multiplexed with the Low Voltage Programming function: RB3/PGM, RB6/PGC and RB7/PGD. The alternate functions of these pins are described in the Special Features Section. Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION_REG<7>). The weak pull-up is automatically turned off

when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of the PORTB pins, RB7:RB4, have an interrupt on- change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt on-change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition

b) Clear flag bit RBIF. A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared. The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature. This interrupt-on-mismatch feature, together with software configurable pull-ups on these four pins, allow easy interface to a keypad and make it possible for wake-up on key depression.

Table 4: PORT B FUNCTIONS

Name	Bit#	Buffer	Function
RB0/INT	bit0	TTL/ST[1]	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3/PGM[3]	bit3	TTL	Input/output pin or programming pin in LVP mode. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6/PGC	bit6	TTL/ST[2]	Input/output pin (with interrupt-on-change) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming clock.
RB7/PGD	bit7	TTL/ST[2]	Input/output pin (with interrupt-on-change) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input
Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: Low Voltage ICSP Programming (LVP) is enabled by default, which disables the RB3 I/O function. LVP must be disabled to enable RB3 as an I/O pin and allow maximum compatibility to the other 28-pin and 40-pin mid-range devices.

Table 5: SUMMARY OF REGISTERS ASSOCIATED WITH PORT B

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h, 186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
81h, 181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

PORTC and the TRISC Register

PORTC is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISC. Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin).

PORTC is multiplexed with several peripheral functions (Table 3-5). PORTC pins have Schmitt Trigger input buffers.

When the I2C module is enabled, the PORTC<4:3> pins can be configured with normal I2C levels or with SM Bus levels by using the CKE bit (SSPSTAT<6>).

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify write instructions (BSF, BCF, XORWF) with TRISC as destination, should be avoided.

Table 6: PORT C FUNCTIONS

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input.
RC1/T1OSI/CCP2	bit1	ST	Input/output port pin or Timer1 oscillator input or Capture2 input/ Compare2 output/PWM2 output.
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/ PWM1 output.
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I^2C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	bit5	ST	Input/output port pin or Synchronous Serial Port data output.
RC6/TX/CK	bit6	ST	Input/output port pin or USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	bit7	ST	Input/output port pin or USART Asynchronous Receive or Synchronous Data.

Legend: ST = Schmitt Trigger input

Table 7: SUMMARY OF REGISTERS ASSOCIATED WITH PORT C

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged

PORTD and TRISD Register

PORTD and TRISD are not implemented on the PIC16F873 or PIC16F876.

PORTD is an 8-bit port with Schmitt Trigger input buffers.
Each pin is individually configurable as an input or output.

PORTD can be configured as an 8-bit wide microprocessor port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers
are TTL.

Table 8: PORT D FUNCTIONS

Name	Bit#	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL[1]	Input/output port pin or parallel slave port bit0.
RD1/PSP1	bit1	ST/TTL[1]	Input/output port pin or parallel slave port bit1.
RD2/PSP2	bit2	ST/TTL[1]	Input/output port pin or parallel slave port bit2.
RD3/PSP3	bit3	ST/TTL[1]	Input/output port pin or parallel slave port bit3.
RD4/PSP4	bit4	ST/TTL[1]	Input/output port pin or parallel slave port bit4.
RD5/PSP5	bit5	ST/TTL[1]	Input/output port pin or parallel slave port bit5.
RD6/PSP6	bit6	ST/TTL[1]	Input/output port pin or parallel slave port bit6.
RD7/PSP7	bit7	ST/TTL[1]	Input/output port pin or parallel slave port bit7.

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note

1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port mode.

Table 9: SUMMARY OF REGISTERS ASSOCIATED WITH PORT D

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
08h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
88h	TRISD	PORTD Data Direction Register								1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTD.

PORTE and TRISE Register

PORTE and TRISE are not implemented on the PIC16F873 or PIC16F876.

PORTE has three pins (RE0/RD/AN5, RE1/WR/AN6, and RE2/CS/AN7) which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers.

The PORTE pins become the I/O control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make certain that the TRISE<2:0> bits are set, and that the pins are configured as digital inputs. Also ensure that ADCON1 is configured for digital I/O. In this mode, the input buffers are TTL.

PORTE pins are multiplexed with analog inputs. When selected for analog input, these pins will read as '0's. TRISE controls the direction of the RE pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.

Table 10: PORT E FUNCTIONS

Name	Bit#	Buffer Type	Function
RE0/$\overline{RD}$/AN5	bit0	ST/TTL(1)	I/O port pin or read control input in Parallel Slave Port mode or analog input: $\overline{RD}$ 1 = Idle 0 = Read operation. Contents of PORTD register are output to PORTD I/O pins (if chip selected)
RE1/$\overline{WR}$/AN6	bit1	ST/TTL(1)	I/O port pin or write control input in Parallel Slave Port mode or analog input: $\overline{WR}$ 1 = Idle 0 = Write operation. Value of PORTD I/O pins is latched into PORTD register (if chip selected)
RE2/$\overline{CS}$/AN7	bit2	ST/TTL(1)	I/O port pin or chip select control input in Parallel Slave Port mode or analog input: $\overline{CS}$ 1 = Device is not selected 0 = Device is selected

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note

1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port mode.

Table 10: SUMMARY OF REGISTERS ASSOCIATED WITH PORT E

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
09h	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	---- -uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111	0000 -111
9Fh	ADCON1	ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0	--0- 0000	--0- 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTE.

6. d MEMORY ORGANISATION

There are three memory blocks in each of the PIC16F877 MCUs. The Program Memory and Data Memory have separate buses so that concurrent access can occur.

PROGRAM MEMORY ORGANISATION

The PIC16F87X devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. The PIC16F877 devices have 8K x 14 words of FLASH program memory. Accessing a location above the physically implemented address will cause a wraparound.

The RESET vector is at 0000h and the interrupt vector is at 0004h.

DATA MEMORY ORGANISATION

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 (STATUS<6>) and RP0 (STATUS<5>) are the bank select bits.

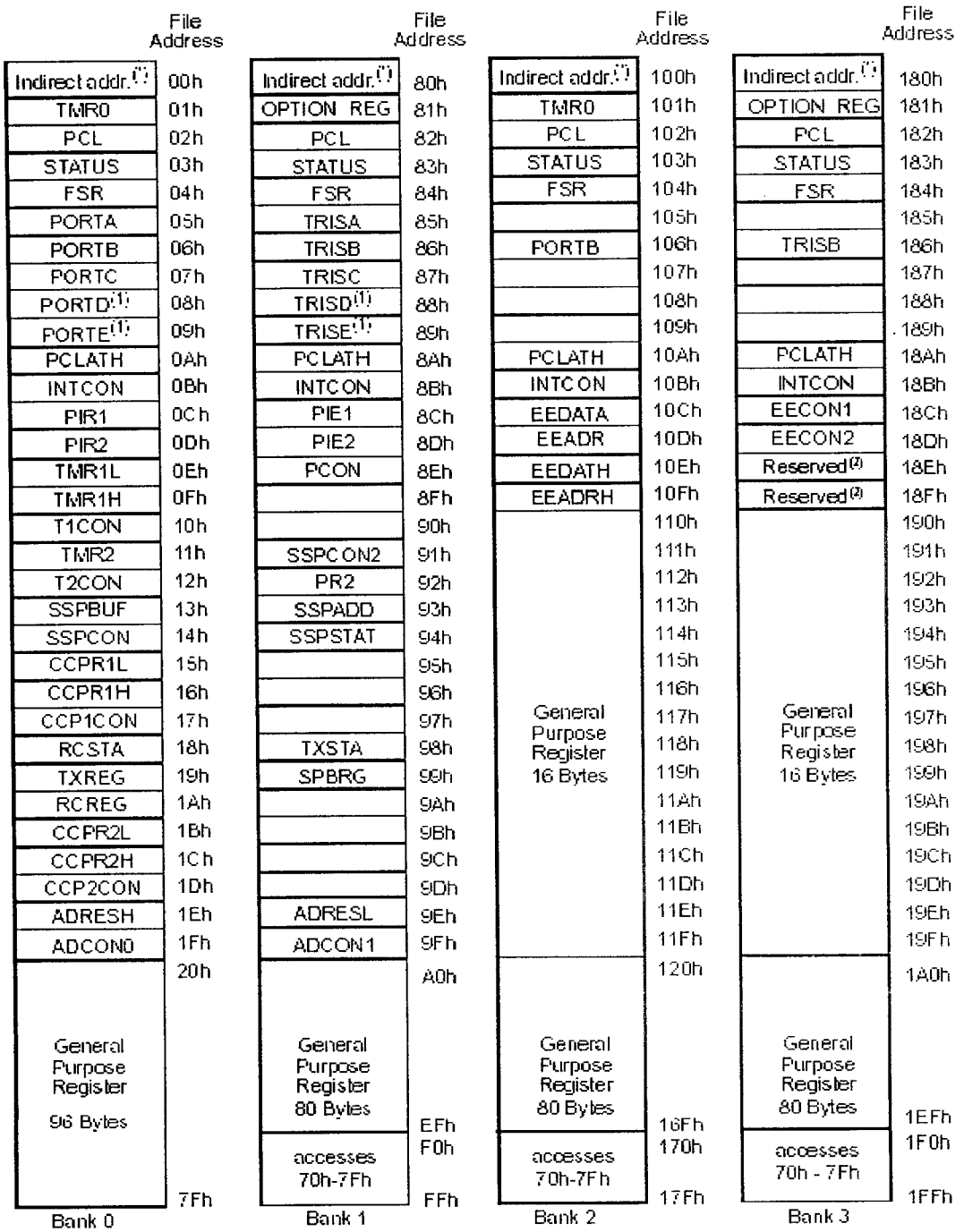
RP1:RP0	Bank
00	0
01	1
10	2
11	3

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank may be mirrored in another bank for code reduction and quicker access.

GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly through the File Select Register (FSR).

Figure 6.3 PIC 16F877 REGISTER FILE MAP



☐ Unimplemented data memory locations, read as '0'.
* Not a physical register.

Note 1: These registers are not implemented on the PIC16F876.
2: These registers are reserved, maintain these registers clear.

6.e INSTRUCTION SET SUMMARY

Each PIC16F87X instruction is a 14-bit word, divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16F87X instruction set summary in Table 12 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 11 shows the Opcode Field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction. The destination designator specifies where the result of the operation is to be placed. If'd' is zero, the result is placed in the W register. If'd' is one, the result is placed in the file register specified in the Instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

Table 11: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W. d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

The instruction set is highly orthogonal and is grouped into three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true, or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs. Table 12 lists the instructions recognized by the MPASMTM assembler. Figure 4 shows the general formats that the instructions can have.

Figure 6.4 GENERAL FORMAT FOR INSTRUCTIONS

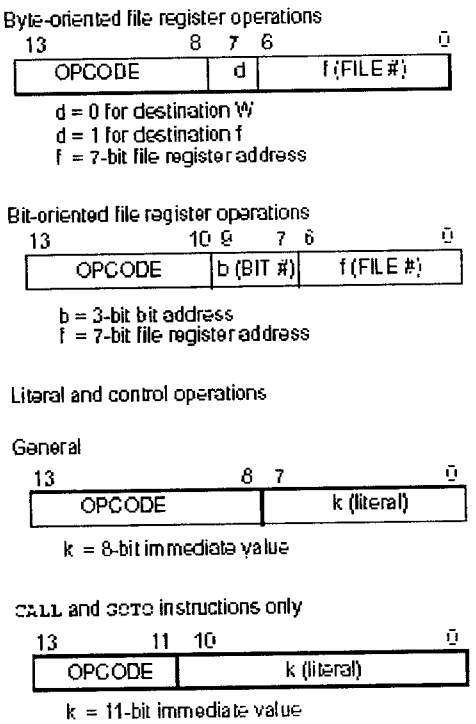


Table 12: 16F877 INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS						
ADDWF	f, d	Add W and f	1	00 0111 dfff ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00 0101 dfff ffff	Z	1,2
CLRF	f	Clear f	1	00 0001 lfff ffff	Z	2
CLRW	-	Clear W	1	00 0001 0xxx xxxx	Z	
COMF	f, d	Complement f	1	00 1001 dfff ffff	Z	1,2
DECF	f, d	Decrement f	1	00 0011 dfff ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00 1011 dfff ffff		1,2,3
INCF	f, d	Increment f	1	00 1010 dfff ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00 1111 dfff ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00 0100 dfff ffff	Z	1,2
MOVF	f, d	Move f	1	00 1000 dfff ffff	Z	1,2
MOVWF	f	Move W to f	1	00 0000 lfff ffff		
NOP	-	No Operation	1	00 0000 0xx0 0000		
RLF	f, d	Rotate Left f through Carry	1	00 1101 dfff ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00 1100 dfff ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00 0010 dfff ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00 1110 dfff ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00 0110 dfff ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS						
BCF	f, b	Bit Clear f	1	01 00bb bfff ffff		1,2
BSF	f, b	Bit Set f	1	01 01bb bfff ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01 10bb bfff ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01 11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS						
ADDLW	k	Add literal and W	1	11 111x kkkk kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11 1001 kkkk kkkk	Z	
CALL	k	Call subroutine	2	10 0kkk kkkk kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00 0000 0110 0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10 1kkk kkkk kkkk		
IORLW	k	Inclusive OR literal with W	1	11 1000 kkkk kkkk	Z	
MOVLW	k	Move literal to W	1	11 00xx kkkk kkkk		
RETFIE	-	Return from interrupt	2	00 0000 0000 1001		
RETLW	k	Return with literal in W	2	11 01xx kkkk kkkk		
RETURN	-	Return from Subroutine	2	00 0000 0000 1000		
SLEEP	-	Go into standby mode	1	00 0000 0110 0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11 110x kkkk kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11 1010 kkkk kkkk	Z	

Note:

1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

3: If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

PROGRAM CODING

The following are the PIC programming codes which are successfully debugged in the MPLAB simulator and loaded in the PIC 16F877 microcontroller chip.

```
;-----------------------------------
; Program for 3 phase to 3 phase cycloconverter
;-----------------------------------
list p=16f877
include <p16f877.inc>
;-----------------------------------
status equ 03h                ;variable declaration
porta equ 05h
portb equ 06h
portc equ 07h
portd equ 08h
trisa equ 85h
trisb equ 86h
trisc equ 87h
trisd equ 88h
rp0 equ 5
rp1 equ 6
count equ 25h
c equ 26h
;-----------------------------------------------
bsf status,rp0                ;initialization
bcf status,rp1
clrf trisa
```

```
clrf trisc
clrf trisd
movlw b'00001111'
bcf status,rp0
movlw 35
movwf c
;----------------------------------------
org 40
mainloop
;----------------------------------------
movlw 1                         ;firing angle control
movwf count
movlw 0
btfsc portb,3
addlw 20
btfsc portb,4
addlw 20
btfsc portb,5
addlw 20
btfsc portb,6
addlw 20
addwf count,1
;----------------------------------------
```

```
Skip0
        btfsc portb,0      ;when V_RN starts positive cycle
        goto skip0
        bcf portc,5
        bcf portc,3
        call fangle
        bsf portc,6        ;to trigger T10
skip1
        btfss portb,2      ;when V_BN starts negative cycle
        goto skip1
        bcf portd,6
        call fangle
        bsf portc,0        ;to trigger T0 and T12
        bsf portd,4
skip2
        btfsc portb,1      ;when V_YN starts positive cycle
        goto skip2
        bcf portc,6
        call fangle
        bsf portc,7        ;to trigger T11 and T17
        bsf porta,1
skip3
        btfss portb,0      ;when V_RN starts negative cycle
        goto skip3
        bcf portc,0
        bcf portd,4
```

```
        call fangle
        bsf portc,1         ;to trigger T1
skip4
        btfsc portb,2       ;when V_BN starts positive cycle
        goto skip4
        bcf portc,7
        bcf porta,1
        call fangle
        bsf portd,7         ;to trigger T15
skip5
        btfss portb,1       ;when V_YN starts negative cycle
        goto skip5
        bcf portc,1
        call fangle
        bsf portc,2         ;to trigger T2 and T8
        bsf portc,4
skip6
        btfsc portb,0       ;when V_RN starts positive cycle
        goto skip6
        bcf portd,7
        call fangle
        bsf portd,0         ;to trigger T4 and T16
        bsf porta,0
skip7
        btfss portb,2       ;when V_BN starts negative cycle
        goto skip7
        bcf portc,2
```

```
        bcf portc,4
        call fangle
        bsf portd,2        ;to trigger T6
skip8
        btfsc portb,1      ;when VYN starts positive cycle
        goto skip8
        bcf portd,0
        bcf porta,0
        call fangle
        bsf portd,1        ;to trigger T5
skip9
        btfss portb,0      ;when VRN starts negative cycle
        goto skip9
        bcf portd,2
        call fangle
        bsf portd,3        ;to trigger T7 and T13
        bsf portd,5
skip10
        btfsc portb,2      ;when VBN starts positive cycle
        goto skip10
        bcf portd,1
        call fangle
        bsf portc,3        ;to trigger T3 and T9
        bsf portc,5
skip11
        btfss portb,1      ;when VYN starts negative cycle
        goto skip11
```

```
        bcf portd,3
        bcf portd,5
        call fangle
        bsf portd,6         ;to trigger T14
goto mainloop
;-----------------------------------------
;         DELAY SUB-ROUTINE
;-----------------------------------------
fangle
decfsz c,1
goto fangle
movlw 35
movwf c
decfsz count,1
goto fangle
return
;-----------------------------------------
end
```

CONCLUSION

CONCLUSION

Three phase cyclconverter circuit has been designed, fabricated and successfully implemented using PIC microcontroller. This module gives a three phase AC output of variable frequency. In this project, we have an exclusive study of embedded system. Since the size and cost of this system is low, there is future scope for this project in industries. This scheme can be easily extended for the implementation of three phase AC motor drives.

BIBILIOGRAPHY

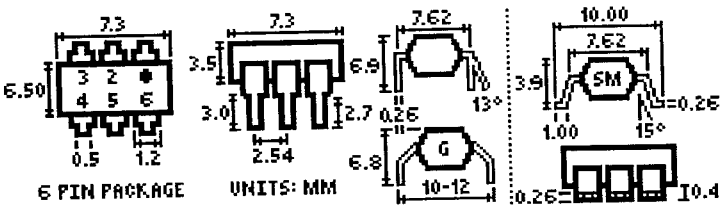
BIBILIOGRAPHY

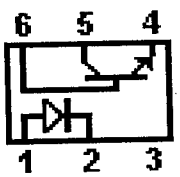
- B. K. Bose, Power Electronics and Ac Drives, Prentice-Hall, New Jersey, 1986
- B. R. Pelly, Thyristor Phase-Controlled Converters and Cycloconverters, Wiley, New York, 1971
- Muhammad H. Rashid, Power electronics circuits, devices and applications, Prentice-Hall, June 2001
- D. Roy Choudhury, Shail Jain, New Age International (P) Ltd, 1999
- www.Microchip.com

APPENDIX

MCT2E, MCT2
OPTICALLY COUPLED ISOLATORS

Circuit





Features

2500 or 1500 V Isolation.
High DC Current Transfer Ratio.
Low Cost Dual-In-Line Package.

Description

The MCT2E, MCT2 are optically coupled isolators consisting of a Gallium Arsenide infrared emitting diode and an NPN silicon phototransistor mounted in a standard 6-pin dual-in-line package. Surface Mount Option Available.
All electrical parameters are 100% tested by manufacturing. Specifications are guaranteed to a cumulative 0.65% AQL.

Absolute Maximum Ratings (Ta=25°C)

Storage Temperature:	-55°C to +150°C
Operating Temperature:	-55°C to +100°C
Lead Soldering:	260°C for 10s, 1.6mm from case
Input-to-Output Isolation Voltage:	±1500V (MCT2)
	±2500V (MCT2E)

Input Diode

Forward DC Current:	60mA
Reverse DC Voltage:	3V
Peak Forward Current:	3A (t p=10μs)
Power Dissipation:	100mW
Derate Linearly:	1.33mW/°C above 25°C

Output Transistor

Collector-Emitter Voltage:	30V
Emitter-Collector Voltage:	7V
Collector-Base Voltage:	70V
Power Dissipation:	150mW
Derate Linearly:	2.00mW/°C above 25°C

Package

Total Power Dissipation:	250mW
Derate Linearly:	3.3mW/°C above 25°C

Electro-optical Characteristics (Ta=25°C)

INPUT	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_F	Forward Current	I_F=20mA		1.2	1.5	V
I_R	Reverse Current	V_R=3V			10	μA
V_R	Reverse Breakdown Voltage	I_R=10μA	3			V
OUTPUT						
BV_{CEO}	Collector-Emitter Voltage	I_C=1mA	30			V
BV_{ECO}	Emitter-Collector Voltage	I_E=100μA	7			V
BV_{CBO}	Collector-Base Voltage	I_C=100μA	70			V
I_{CEO}	Collector-Emitter Dark Current	V_{CE}=10V, I_B=0			50	nA
I_{CBO}	Collector-Base Dark Current	V_{CB}=10V, I_E=0			20	nA
C_{CE}	Collector-Emitter Capacitance	V_{CE}=0		10		pF
H_{FE}		V_{CE}=5.0V, I_C=100μA	100	150		

COUPLED	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_C/I_F	DC Current Transfer Ratio	I_F=10mA, V_{CE}=10V, I_B=0	20			%
R_{IO}	Input-to-Output Isolation Resistance	V_{IO}=500V, (note 1)	1E11			ohm
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	I_F=10mA, I_C=2.5mA			0.4	V
C_{IO}	Capacitance Input to Output	f=1MHz, (note 1)		0.6		pF
T_R	Output Rise Time	V_{CC}=10V, I_C=2mA		2		µs
T_F	Output Fall Time	R_L=100ohm		2		µs
	Input-Output Isolation Voltage	(Note 1)				
	MCT2E		2500			V
	MCT2		1500			V

Notes

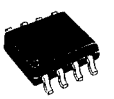
1. Measured with input leads shorted together and output leads shorted together

UA741

GENERAL PURPOSE SINGLE OPERATIONAL AMPLIFIER

- LARGE INPUT VOLTAGE RANGE
- NO LATCH-UP
- HIGH GAIN
- SHORT-CIRCUIT PROTECTION
- NO FREQUENCY COMPENSATION
- REQUIRED
- SAME PIN CONFIGURATION AS THE UA709

N
DIP8
(Plastic Package)



D
SO8
(Plastic Micropackage)

DESCRIPTION

The UA741 is a high performance monolithic operational amplifier constructed on a single silicon chip. It is intented for a wide range of analog applications.

- Summing amplifier
- Voltage follower
- Integrator
- Active filter
- Function generator

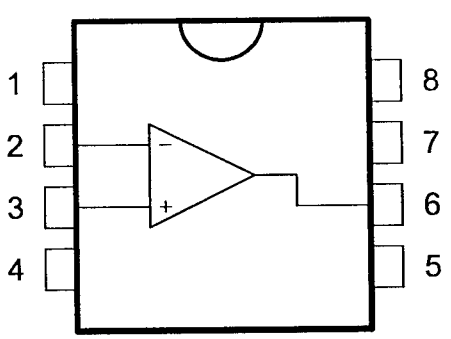
The high gain and wide range of operating voltages provide superior performances in integrator, summing amplifier and general feedback applications. The internal compensation network (6dB/ octave) insures stability in closed loop circuits.

ORDER CODE

Part Number	Temperature Range	Package	
		N	D
UA741C	0°C, +70°C	•	•
UA741I	-40°C, +105°C	•	•
UA741M	-55°C, +125°C	•	•
Example : UA741CN			

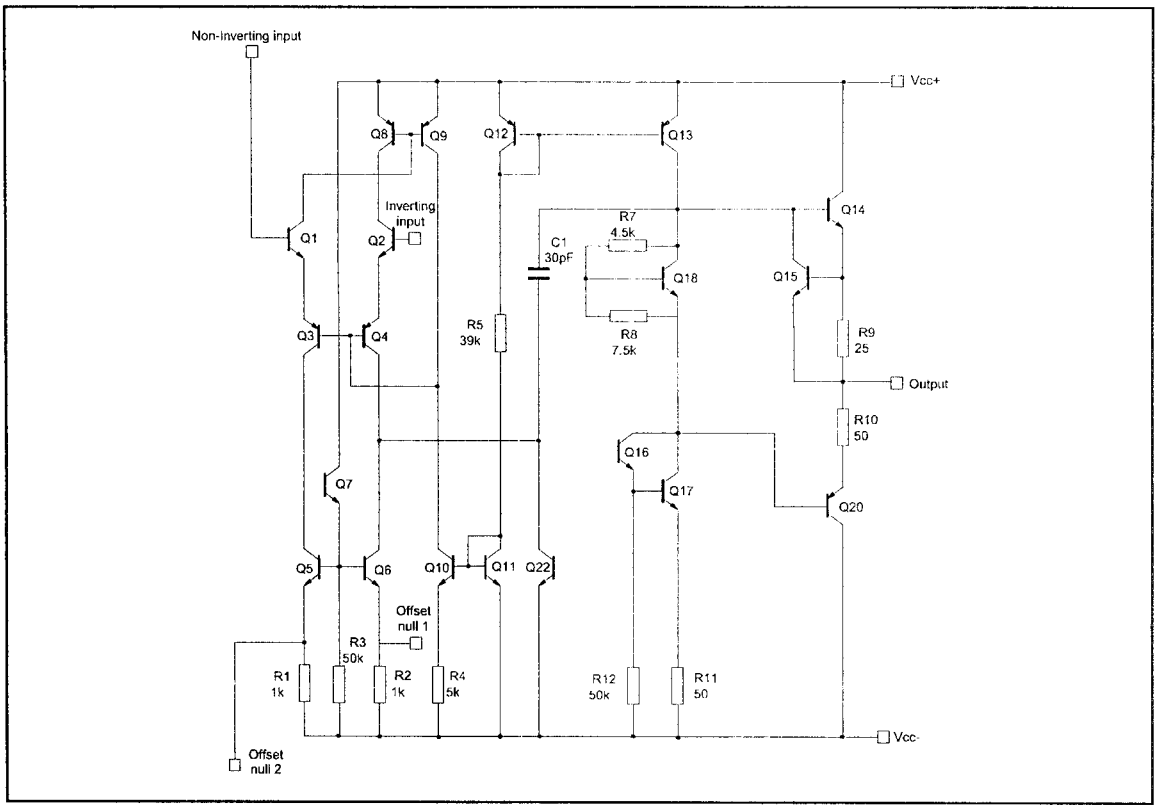
N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)

PIN CONNECTIONS (top view)



1 - Offset null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	UA741M	UA741I	UA741C	Unit
V_{CC}	Supply voltage	±22			V
V_{id}	Differential Input Voltage	±30			V
V_i	Input Voltage	±15			V
P_{tot}	Power Dissipation [1]	500			mW
	Output Short-circuit Duration	Infinite			
T_{oper}	Operating Free-air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150			°C

1. Power dissipation must be considered to ensure maximum junction temperature (Tj) is not exceeded.

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage ($R_s \leq 10k\Omega$) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$		1	5 6	mV
I_{io}	Input Offset Current T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$		2	30 70	nA
I_{ib}	Input Bias Current T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$		10	100 200	nA
A_{vd}	Large Signal Voltage Gain (V_o = ±10V, R_L = 2kΩ) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	50 25	200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_s \leq 10k\Omega$) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	77 77	90		dB
I_{CC}	Supply Current, no load T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$		1.7	2.8 3.3	mA
V_{icm}	Input Common Mode Voltage Range T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	±12 ±12			V
CMR	Common Mode Rejection Ratio ($R_S \leq 10k\Omega$) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	70 70	90		dB
I_{OS}	Output short Circuit Current	10	25	40	mA
$\pm V_{opp}$	Output Voltage Swing T_{amb} = +25°C R_L = 10kΩ R_L = 2kΩ $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 10kΩ R_L = 2kΩ	12 10 12 10	14 13		V
SR	Slew Rate V_i = ±10V, R_L = 2kΩ, C_L = 100pF, unity Gain	0.25	0.5		V/µs
t_r	Rise Time V_i = ±20mV, R_L = 2kΩ, C_L = 100pF, unity Gain		0.3		µs
K_{ov}	Overshoot V_i = 20mV, R_L = 2kΩ, C_L = 100pF, unity Gain		5		%
R_i	Input Resistance	0.3	2		MΩ
GBP	Gain Bandwith Product V_i = 10mV, R_L = 2kΩ, C_L = 100pF, f =100kHz	0.7	1		MHz
THD	Total Harmonic Distortion f = 1kHz, A_v = 20dB, R_L = 2kΩ, V_o = $2V_{pp}$, C_L = 100pF, T_{amb} = +25°C		0.06		%
e_n	Equivalent Input Noise Voltage f = 1kHz, R_s = 100Ω		23		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase Margin		50		Degrees

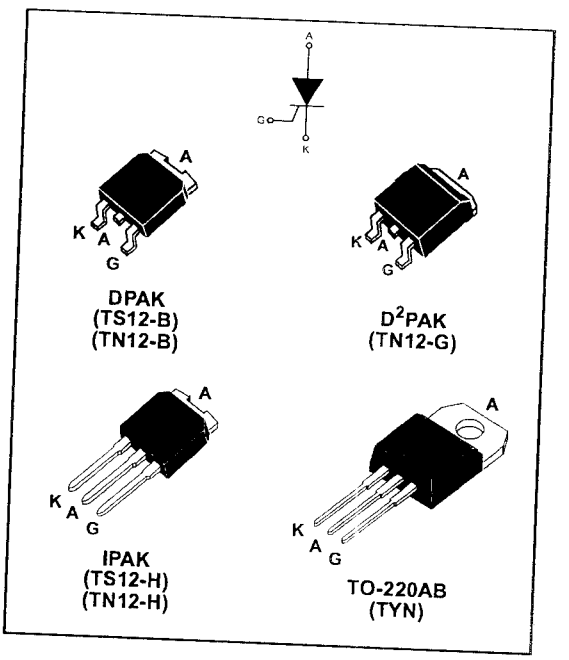
TN12, TS12 and TYNx12 Series

SENSITIVE & STANDARD

12A SCRs

MAIN FEATURES:

Symbol	Value	Unit
$I_{T(RMS)}$	12	A
V_{DRM}/V_{RRM}	600 to 1000	V
I_{GT}	0.2 to 15	mA



DESCRIPTION

Available either in sensitive (TS12) or standard (TYN, TN12...) gate triggering levels, the 12A SCR series is suitable to fit all modes of control found in applications such as overvoltage crowbar protection, motor control circuits in power tools and kitchen aids, in-rush current limiting circuits, capacitive discharge ignition, voltage regulation circuits...

Available in though-hole or surface-mount packages, they provide an optimized performance in a limited space area.

ABSOLUTE RATINGS (limiting values)

Symbol	Parameter			Value		Unit
$I_{T(RMS)}$	RMS on-state current (180° conduction angle)		Tc = 105°C	12		A
$I_{T(AV)}$	Average on-state current (180° conduction angle)		Tc = 105°C	8		A
				DPAK / IPAK	D²PAK / TO-220AB	
I_{TSM}	Non repetitive surge peak on-state current	tp = 8.3 ms	Tj = 25°C	115	146	A
		tp = 10 ms		110	140	
I^2t	I^2t Value for fusing	tp = 10 ms	Tj = 25°C	60	98	A²s
dI/dt	Critical rate of rise of on-state current I_G = 2 x I_{GT} , tr ≤ 100 ns	F = 60 Hz	Tj = 125°C	50		A/µs
I_{GM}	Peak gate current	tp = 20 µs	Tj = 125°C	4		A
$P_{G(AV)}$	Average gate power dissipation		Tj = 125°C	1		W
T_{stg} T_j	Storage junction temperature range Operating junction temperature range			- 40 to + 150 - 40 to + 125		°C
V_{RGM}	Maximum peak reverse gate voltage (for TN12 & TYN)			5		V

ELECTRICAL CHARACTERISTICS (Tj = 25°C, unless otherwise specified)

■ SENSITIVE

Symbol	Test Conditions			TS1220	Unit
I_{GT}	V_D = 12 V R_L = 140 Ω		MAX.	200	µA
V_{GT}			MAX.	0.8	V
V_{GD}	$V_D = V_{DRM}$ R_L = 3.3 kΩ R_{GK} = 1 kΩ	Tj = 125°C	MIN.	0.1	V
V_{RG}	I_{RG} = 10 µA		MIN.	8	V
I_H	I_T = 50 mA R_{GK} = 1 kΩ		MAX.	5	mA
I_L	I_G = 1 mA R_{GK} = 1 kΩ		MAX.	6	mA
dV/dt	V_D = 67 % V_{DRM} R_{GK} = 220 Ω	Tj = 125°C	MIN.	5	V/µs
V_{TM}	I_{TM} = 24 A tp = 380 µs	Tj = 25°C	MAX.	1.6	V
V_{t0}	Threshold voltage	Tj = 125°C	MAX.	0.85	V
R_d	Dynamic resistance	Tj = 125°C	MAX.	30	mΩ
I_{DRM} I_{RRM}	$V_{DRM} = V_{RRM}$ R_{GK} = 220 Ω	Tj = 25°C	MAX.	5	µA
		Tj = 125°C		2	mA

■ STANDARD

Symbol	Test Conditions			TN1215		TYN		Unit
				B/H	G	x12T	x12	
I_{GT}	V_D = 12 V R_L = 33 Ω		MIN.	2		0.5	2	mA
V_{GT}			MAX.	15		5	15	
V_{GD}	$V_D = V_{DRM}$ R_L = 3.3 kΩ	Tj = 125°C	MAX.	1.3				V
I_H	I_T = 500 mA Gate open		MIN.	0.2				V
I_L	I_G = 1.2 I_{GT}		MAX.	40	30	15	30	mA
dV/dt	V_D = 67 % V_{DRM} Gate open	Tj = 125°C	MAX.	80	60	30	60	mA
V_{TM}	I_{TM} = 24 A tp = 380 µs	Tj = 25°C	MIN.	200		40	200	V/µs
V_{t0}	Threshold voltage	Tj = 125°C	MAX.	1.6				V
R_d	Dynamic resistance	Tj = 125°C	MAX.	0.85				V
I_{DRM} I_{RRM}	$V_{DRM} = V_{RRM}$	Tj = 125°C	MAX.	30				mΩ
		Tj = 25°C		5				µA
		Tj = 125°C		2				mA

THERMAL RESISTANCES

Symbol	Parameter			Value	Unit
$R_{th(j-c)}$	Junction to case (DC)			1.3	°C/W
$R_{th(j-a)}$	Junction to ambient		TO-220AB	60	°C/W
			IPAK	100	
		S = 1 cm²	D²PAK	45	
		S = 0.5 cm²	DPAK	70	

S = Copper surface under tab

Fig. 3-2: Relative variation of thermal impedance junction to ambient versus pulse duration (recommended pad layout, FR4 PC board).

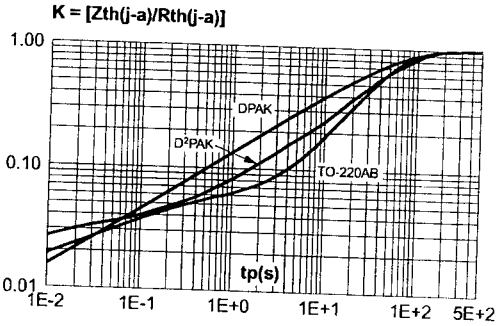


Fig. 4-1: Relative variation of gate trigger current, holding current and latching versus junction temperature for TS12 series.

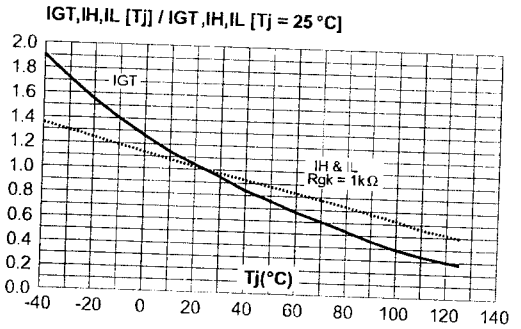


Fig. 4-2: Relative variation of gate trigger current, holding current and latching current versus junction temperature for TN12 & TYN series.

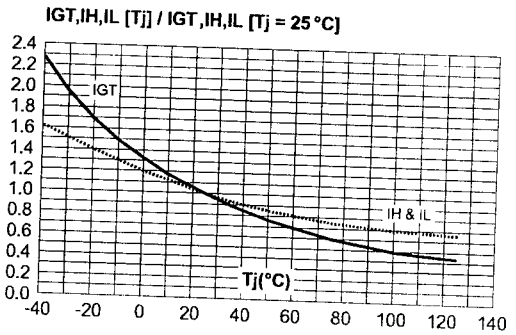


Fig. 5: Relative variation of holding current versus gate-cathode resistance (typical values) for TS12 series.

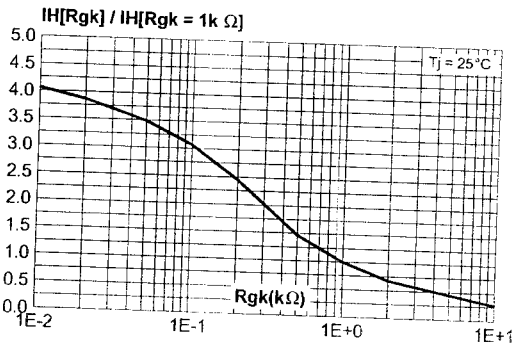


Fig. 6: Relative variation of dV/dt immunity versus gate-cathode resistance (typical values) for TS12 series.

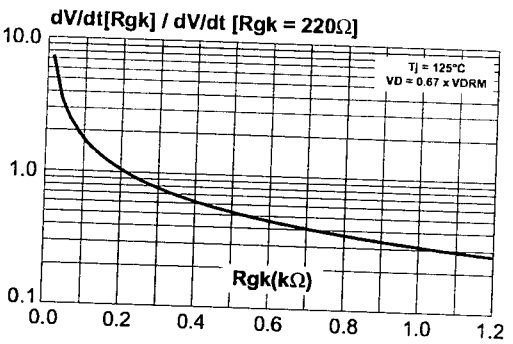


Fig. 7: Relative variation of dV/dt immunity versus gate-cathode capacitance (typical values) for TS12 series.