Register Number:……..

KUMARAGURU
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B.E DEGREE EXAMINATIONS: DEC 2022

(Regulation 2018)

Third Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U18ECI3203: Digital System Design

COURSE OUTCOMES

CO1: Apply Boolean algebra, Karnaugh map and Tabulation method to design combinational logic circuits (K3)
CO2: Design and verify sequential logic circuits using flipflops (K4).
CO3: Apply state machine models to design sequential logic circuits (K4).
CO4: Explain different logic families based on performance (K2).
CO5: Design combinational circuits using programmable logic devices (K3).

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-
PART A (10 x 2 = 20 Marks)
(Answer not more than 40 words)

1.	Convert $(101101)_2$ into decimal digit.		CO1	[K_2]
2.	Recall the limitations of Karnaugh map.		CO1	[K_1]
3.	List the design procedure for combinational circuits.		CO1	[K_1]
4.	Draw 1 x 4 demultiplexer logic diagram.		CO1	[K_2]
5.	Define race around condition.		CO2	[K_1]
6.	Find the number of flip flops needed to implement mod 15 counter.		CO2	[K_3]
7.	The propagation delay t_{pd} for each flip-flop is 50 ns. Determine the maximum operating frequency for MOD - 32 ripple counter.		CO3	[K_3]
8.	Define critical race.		CO3	[K_1]
9.	Outline the advantages and disadvantages of TTL.		CO4	[K_1]
10.	List the types of programmable logic devices.		CO5	[K_1]

Answer any FIVE Questions:-
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11.	a)	(i)Simplify Y = (A + B) (A + C') (B' + C')	8	CO1	[K_3]
		(ii)Prove ABC + ABC' + AB'C + A'BC = AB + AC + BC			

	b)	Reduce the expression F = m(1,6,12,13,14) + d(2,4) is SOP and POS forms.	8	CO1	[K_3]
12.	a)	Design a 4-bit magnitude comparator with three outputs : A>B, A=B, A<B	8	CO1	[K_3]
	b)	(i) Implement F(A, B, C, D) = Σ (1, 3, 4, 11, 12, 13, 14, 15) using multiplexer (ii) Implementation of a Full Adder with a Decoder: S(x, y, z) = ∑(1, 2, 4, 7) C(x, y, z) = ∑(3, 5, 6, 7)	8	CO1	[K_3]
13.	a)	Explain Parallel IN Serial OUT shift registers with neat diagram.	5	CO2	[K_3]
	b)	Design a counter that can count the sequence 000,001,011,100,101,111	10	CO2	[K_4]
14.	a)	Develop a circuit that has no static hazards and implement the hazard free circuit using NAND gates F(a,b,c,d)=Σ(0,2,6,7,8,10,12)	8	CO3	[K_3]
	b)	Draw a logic diagram of product of sum expression (x1+x2')(x2+x3).Show that there is a static 0 hazard when x1 and x3 are 0 and x2 goes from 0 to 1.Find a way to remove the hazards by adding one more OR gate.	8	CO3	[K_3]
15.	a)	Explain the working of TTL with Totem pole output.	12	CO4	[K_2]
	b)	Compare ECL,TTL and CMOS families.	4	CO4	[K_2]
16.		Construct the combinational logic circuit using PLA and PAL for the following Boolean functions, F1(A, B,C)=Σ m(0, 1,3,4) and F2(A, B, C)=Σ m (1, 2, 3,4,5).	16	CO5	[K_3]

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Please indicate knowledge level (K_1toK_6) and Course Outcome level (CO1 to CO5) against each question for each subdivision.