Register Number:……..

KUMARAGURU
college of technology
character is life

B.E DEGREE EXAMINATIONS: NOV/DEC 2022

(Regulation 2018)

Third Semester

INFORMATION SCIENCE AND ENGINEERING

U18IST3002: Computer Architecture

COURSE OUTCOMES

CO1: Identify the different addressing modes used in a processor.
CO2: Apply the knowledge of arithmetic operations in the design of a fast adder.
CO3: Classify the control units present in a processor.
CO4: Analyze the various performance enhancement techniques of Cache memories.
CO5: Point out how the pipeline processor improves performance of a computer.

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-
PART A (10 x 2 = 20 Marks)
(Answer not more than 40 words)

1.	Define Clock Rate.	CO1	[K_1]
2.	List the four commonly used Condition Code flags in Condition Code Register.	CO1	[K_2]
3.	Show the structure of a 4 bit carry-lookahead adder.	CO2	[K_1]
4.	Recall and write the Add/subtract rule for floating point numbers.	CO2	[K_1]
5.	Give the block diagram of a complete processor.	CO3	[K_1]
6.	List few situations where μPC is not incremented.	CO3	[K_1]
7.	Differentiate Write through and Write back method.	CO4	[K_2]
8.	Outline Hit and Miss rate.	CO4	[K_2]
9.	Show the 4-stage pipeline of an instruction execution.	CO5	[K_2]
10.	Tell the purpose of Vectored Interrupts.	CO5	[K_1]

Answer any FIVE Questions:-
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11.	a)	Illustrate how the processor and memory inter-operates to execute an instruction.	8	CO1	[K_2]
	b)	Identify the different ways in which the location of an operand can be specified in an instruction.	8	CO1	[K_3]

12.	a)	Apply Booth's algorithm to multiply the numbers: 23 and -9 with the help of the flowchart.	8	CO2	[K_3]
	b)	Demonstrate how Floating-point operations are implemented, with the help of a diagram.	8	CO2	[K_3]
13.	a)	Develop the control sequence for execution of a complete instruction including Branch instructions.	8	CO3	[K_3]
	b)	There are two approaches used by the control unit for generating the control signals in proper sequence - Interpret this statement and explain any one approach in detail.	8	CO3	[K_3]
14.	a)	Analyze the various mapping functions available for mapping memory blocks to cache memory.	8	CO4	[K_4]
	b)	Examine the address translation process for translating virtual address to physical address.	8	CO4	[K_4]
15.	a)	Examine the effect of branch instructions in pipeline and explain the techniques to mitigate the effect.	8	CO5	[K_4]
	b)	Identify the purpose of DMA with suitable diagram. Discuss its advantages and disadvantages.	8	CO5	[K_4]
16.	a)	Discuss about the Superscalar architecture with its pros and cons.	8	CO5	[K_4]
	b)	Discover the methods used by the processor for handling simultaneous interrupt requests.	8	CO5	[K_4]

****