KUMARAGURU
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B.E DEGREE EXAMINATIONS: DEC 2022

(Regulation 2018)

Seventh Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U18ECE0041**:** VLSI Testing and Testability

COURSE OUTCOMES

CO1: Discuss various fault models and fault simulation techniques
CO2: Examine faults in combinational logic circuits
CO3: Examine faults in sequential logic circuits
CO4: Compare various methods for delay tests
CO5: Explain different testability methods
CO6: Outline fault diagnosis approaches

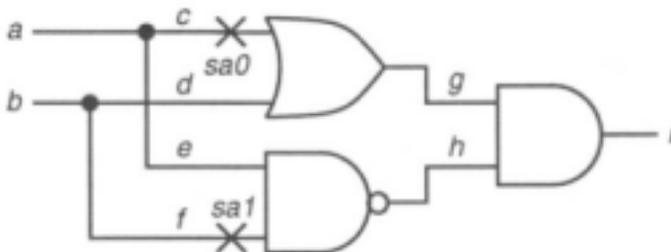**Time: Three Hours**   **Maximum Marks: 100**

Answer all the Questions:-
PART A (10 x 2 = 20 Marks)
(Answer not more than 40 words)

1. Show that the two faults c s-a-0 and f s-a-1 are equivalent in the circuit.   CO1   [K2]

2. Recall Permanent fault, intermittent fault, and transient fault.   CO1   [K3]

3. Can a gate on the D- frontier have both D and $\overline{D}$ among its input values?   CO2   [K2]

4. "Random Test generation for sequential circuits is more complicated than combinational   CO3   [K2]
   circuits." Justify this statement.

5. Define Testable fault and a false path with respect to delay test.   CO4   [K2]

6. Outline the relation between number of paths and the path delay fault in a combinational circuit. CO4   [K2]

7. Define controllability and observability.   CO5   [K2]

8. The given circuit depicts a complex circuit using Scan cell design. Identify the operation   CO5   [K2]
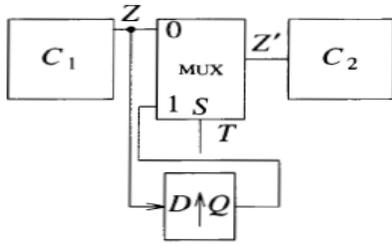   carried out by the circuit.

9.	Justify the need for fault diagnosis.			CO6	[K₂]
10.	Define plausible faults.			CO6	[K₂]

Answer any FIVE Questions:-
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11.	a)	Define Logic Simulation. Explain in detail any one type of logic simulation.	8	CO1	[K₂]
	b)	Explain in detail about serial and parallel fault simulation techniques	8	CO1	[K₂]
12.	a)	Outline the basic steps involved in implementing PODEM (Path Oriented Decision Making) algorithm.	6	CO2	[K₂]
	b)	Determine a suitable test vector to detect the s-a-0 at α using D-algorithm.	10	CO2	[K₃]
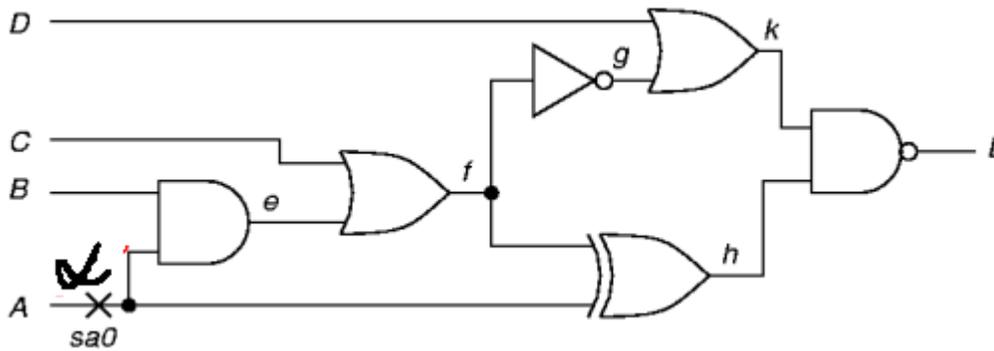
13.		Explain how iterative array models are used for test generation for SSFs(single stuck at Faults) in sequential circuits with an example.	16	CO3	[K₃]
14.	a)	Generate a test for H STR (Slow To Rise) fault,	6	CO4	[K₃]
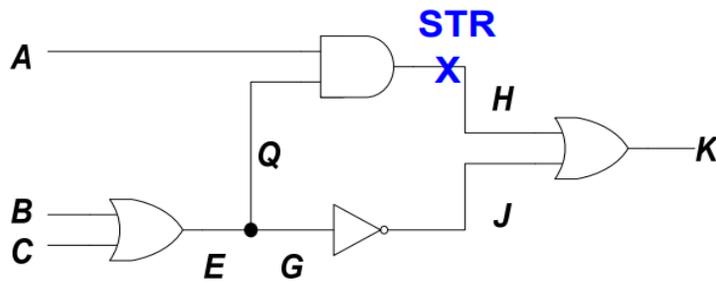
b) Explain the following path delay test methodologies with suitable diagrams.   10   CO4 [K$_2$]

    i)   Enhanced scan test

    ii)   normal scan sequential test

    iii)   Variable- clock Non-scan sequential test

15. Describe how DFT(Design for Testability) is achieved using Boundary scan   16   CO5 [K$_3$] standards to carry out the board level and chip level tests. Support your answer with neat block diagrams.

16. Explain the creation of fault dictionary used in the fault diagnosis with an example   16   CO6 [K$_2$]

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