KUMARAGURU
college of technology
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Register Number:……..

M.E DEGREE EXAMINATIONS: DEC 2022

(Regulation 2018)

First Semester

EMBEDDED SYSTEMS TECHNOLOGIES

P18EST1001: Advanced Digital System Design

COURSE OUTCOMES

After successful completion of this course, the students should be able to:

CO1: Apply the Design procedure of Clocked synchronous and asynchronous sequential circuits for developing simple digital system

CO2: Analyze the Clocked synchronous sequential circuits and asynchronous sequential circuits in digital system

CO3: Understand the basic and advanced concepts in testing of digital circuits

CO4: Apply the techniques to design synchronous sequential circuit using programmable devices

CO5: Familiarize basics and programming of VHDL for digital circuit design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Find the correct sequence for analysis of synchronous sequential circuit: CO1 [K_2]

   1. State diagram
   2. State table
   3. Equations for the outputs and the flip-flop inputs.
   4. Circuit diagram

   a) 4-2-3-1 b) 2-1-3-4

   c) 1-2-3-4 d) 4-3-2-1

2. Reduced state table with 7 states require _____ flip flops to design state machine. CO1 [K_2]

   a) 7 b) 8

   c) 3 d) 4

3. Hazard is due to CO2 [K_2]

   a) Unequal delay b) Transitions in the circuit

   c) AND gate d) NOR gate

4. Matching type item with multiple choice code CO3 [K_2]

List I	List II
A. Asynchronous Sequential Machine	i. input and state
B. Synchronous sequential circuit	ii. input
C. Mealy circuit	iii. Fundamental mode operation
D. Moore circuit	iv. Flip Flop required

a) A-i; B-ii; C-iii; D-iv
b) A-iii; B-iv; C-i; D-ii
c) A-iv; B-ii; C-iii; D-i
d) A-iii; B-ii; C-i; D-iv

5. _____ is not fault type. CO3 [K_2]

a) s-a-0
b) s-a-1
c) bridging
d) Weak wire

6. BIST stands for CO3 [K_2]

a) Built In Self Test
b) Built In Stuck at Test
c) Bridge In Self Test
d) Bridge In Stuck at Test

7. Assertion (A): FPGA is programmable device. CO4 [K_2]
Reason (R): VHDL can be used to program the FPGA.

a) Both A and R are Individually true and R is correct explanation of A
b) Both A and R are Individually true and R is not correct explanation of A
c) A is true but R is false
d) A is false but R is true

8. Programmable AND & Programmable OR used in _____. CO4 [K_2]

a) CPLD
b) FPGA
c) PLA
d) PAL

9. Find the correct statement: CO5 [K_2]

1. VHDL is Hardware Description language
2. <= is signal assignment operator
3. Process is sequential statement
4. VHDL is non-IEEE standard language

a) 1 and 2 only
b) 1 and 3 only
c) 1, 2 and 4 only
d) 3 and 4 only

10. In VHDL, _____is used in process statement. CO5 [K_3]

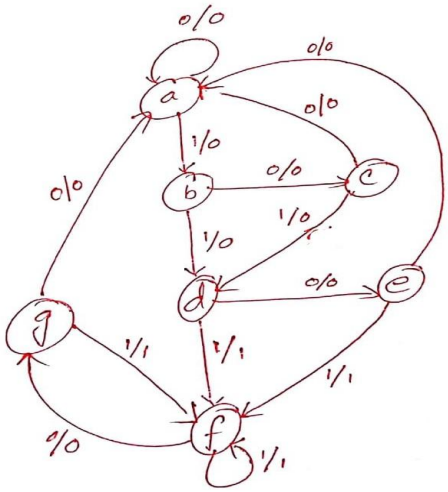
a) entity
b) architecture
c) Sensitivity list
d) Event list

PART B (10 x 2 = 20 Marks)

11.	Draw a sample of state diagram.	CO1	[K_2]
12.	Justify the need for state table reduction.	CO1	[K_4]
13.	Write the importance of fundamental mode in Asynchronous sequential circuit.	CO2	[K_1]
14.	Differentiate static and dynamic hazard.	CO2	[K_2]
15.	Justify how Yield of IC fabrication is related with testing.	CO3	[K_4]
16.	Write the features of BIST in latest ICs.	CO3	[K_2]
17.	What is meant by GAL?	CO4	[K_4]
18.	Implement XOR gate using LUT method.	CO4	[K_3]
19.	Write VHDL program for half adder using data flow modelling.	CO5	[K_3]
20.	Why concurrent statements are called so?	CO5	[K_2]

PART C (6 x 5 = 30 Marks)

21.	Draw the reduced state diagram for the following state diagram using equivalent state method.	CO1	[K_5]

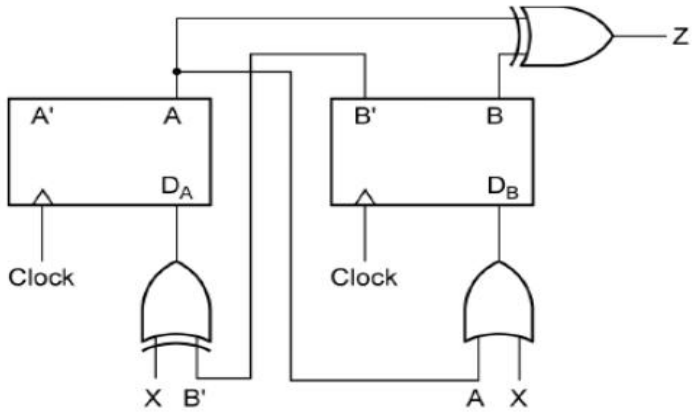


22.	Illustrate non-critical race condition with suitable example.	CO2	[K_3]
23.	Discuss the working of BIST with suitable clock diagram.	CO3	[K_2]
24.	Design and implement the following Boolean relation using PLA with neat diagram.	CO4	[K_5]
25.	Design and implement full subtractor in VHDL.	CO5	[K_5]

26. Describe any four concurrent statements of VHDL with suitable example for each. CO5 [K_2]

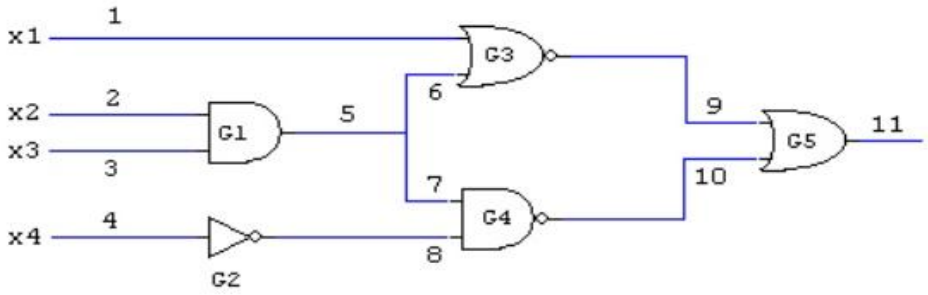
Answer any FOUR Questions
PART D (4 x 10 = 40 Marks)

27. Analyze the following synchronous sequential circuit with state table and state diagram. CO1 [K_4]



28. Design state machine for book vending machine for the following specifications. Cost of the book is Rs.15. Machine can accept either Rs.20 or Rs.5 currency notes. Machine dispenses one book and change Rs.5 when Rs. 20 is inserted; and dispenses book alone when three Rs.5 currency notes are inserted. CO2 [K_6]

29. Determine the test vector for the faults 2:sa0; 10:sa1; 11:sa0 in the given combinational circuit using path sensitization method. CO3 [K_5]



30. Describe the functional block diagram for CLB used in Xilinx 3000 FPGA device with neat sketch. CO4 [K_2]

31. Design and implement 8 bit UP counter in VHDL using any one type of modelling. CO5 [K_5]

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