Register Number:……..

KUMARAGURU
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B.E DEGREE EXAMINATIONS: APRIL / MAY 2023

(Regulation 2018)

Sixth Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U18ECI6203: VLSI and HDL Programming

COURSE OUTCOMES

CO1: Implement and verify combinational and sequential circuits using Verilog HDL.
CO2: Explain working and electrical properties of MOSFET.
CO3: Discuss the CMOS fabrication Technologies.
CO4: Apply CMOS logics in complex digital circuits.
CO5: Discuss various implementation strategies.

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-
PART A (10 x 2 = 20 Marks)
(Answer not more than 40 words)

1.	Design a half adder in structural modeling using Verilog HDL	CO1	[K_2]
2.	Illustrate the edge sensitive sequential UDPs.	CO1	[K_2]
3.	Show the equation for describing the channel length modulation effect in NMOS transistor	CO2	[K_2]
4.	Find the operating region of MOSFET biased with Vgs=1.5 V , Vds=1 V,Vds(sat)=0.6V, Vt=0.4V.	CO2	[K_2]
5.	What is Latch up? How to prevent Latch Up?	CO3	[K_1]
6.	Outline the stick diagram and layout for CMOS inverter	CO3	[K_2]
7.	Construct an XOR Gate using Pass transistor logic	CO4	[K_2]
8.	Determine the propagation delay of n-bit Linear carry select adder.	CO4	[K_2]
9.	List out the advantages of FPGA	CO5	[K_2]
10.	Define SoC	CO5	[K_1]

Answer any FIVE Questions:-
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11.	a)	Build a JK flip flop and SR Flip flop circuit using an always statement with necessary logic diagram using Behavioral modeling in Verilog HDL	8	CO1	[K_3]
	b)	Develop 4-bit Ripple Carry Adder using structural modeling of Verilog code	8	CO1	[K_3]

12.	a)	Illustrate the working of NMOS Enhancement Transistor in detail.	8	CO2	[K_3]
	b)	Summarize the various modes of MOSFET transistor operation with necessary diagrams.	8	CO2	[K_3]
13.		Explain the steps involved in the fabrication of CMOS transistor using N-well process with necessary diagram..	16	CO3	[K_2]
14.	a)	Construct the two input EX-OR / EX-NOR using Differential Cascode Voltage Switch Logic with neat diagram.	10	CO4	[K_3]
	b)	Build AND/NAND gates using Dual-Rail Domino Logic.	6	CO4	[K_3]
15.		Summarise the Components of SoC and Demonstrate the Design flow of SoC in details.	16	CO5	[K_L]
16.	a)	Explain the working of a Carry - Save adder. Mention the advantages of the same composed to other types of adders.	10	CO4	[K_3]
	b)	Derive the expression for pull-up to pull-down ratio of a CMOS inverter driven by another CMOS inverter.	6	CO2	[K_2]

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