



B.E. DEGREE EXAMINATIONS: APRIL / MAY 2023

(Regulation 2018)

Sixth Semester

ELECTRICAL AND ELECTRONICS ENGINEERING

U18EEE0005: VLSI Design

COURSE OUTCOMES

After successful completion of this course, the students will be able to:

- CO1:** Recollect and study the fundamentals of electronics devices and circuits.
CO2: Understand the principle and working of MOS and CMOS device.
CO3: Apply the fundamentals of digital circuits and CMOS technology to develop different design techniques.
CO4: Design various digital modules and systems using different CMOS design techniques.
CO5: Analyse the different CMOS digital modules for performance parameters such as gate size and power.
CO6: Understand the concepts of programmable devices for custom design.

Time: Three Hours

Maximum Marks: 100

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

(Answer not more than 40 words)

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|--|-----------------------|
| 1. Draw the construction diagram of NMOS transistor. | CO1 [K2] |
| 2. Draw the stick diagram for CMOS inverter. | CO2 [K2] |
| 3. Implement 2 input NOR gate using pseudo NMOS logic. | CO3 [K3] |
| 4. Justify the need for low power design. | CO3 [K2] |
| 5. Draw the block diagram for multiplexer based latch. | CO4 [K2] |
| 6. Draw the circuit diagram for 1T DRAM cell. | CO4 [K ₂] |
| 7. Why ripple carry adder is slower? | CO5 [K2] |
| 8. What is barrel shifter? | CO5 [K ₂] |
| 9. Differentiate semicustom and full custom design. | CO6 [K2] |
| 10. List out the major elements of FPGA. | CO6 [K2] |

Answer any FIVE Questions:-

PART B (5 x 4 = 20 Marks)

(Answer not more than 80 words)

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| 11. Illustrate the body effect of MOS transistors with suitable circuit diagram. | CO1 [K ₂] |
| 12. Derive the basic current equation for the MOS transistor. | CO2 [K ₃] |

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|-----|---|-----|-------------------|
| 13. | Illustrate the working of clocked CMOS logic with suitable circuit diagram. | CO3 | [K ₃] |
| 14. | Design suitable pipelined architecture to implement the following function and explain the pipeline concept with time computation table.
$\log(a + b)$ | CO4 | [K ₅] |
| 15. | Derive the necessary equations for 4 bit carry look ahead adder. | CO5 | [K ₃] |
| 16. | Write note on Gate array logic with necessary sketch. | CO6 | [K ₂] |

**Answer any FIVE Questions:-
PART C (5 x 12 = 60 Marks)
(Answer not more than 300 words)**

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|-----|--|----|-----|-------------------|
| 17. | Describe the working of NMOS transistor using biasing circuit with Drain characteristics and Transfer characteristic curves. | 12 | CO1 | [K ₂] |
| 18. | Explain the working of CMOS inverter using its characteristic curve with various regions. | 12 | CO2 | [K ₂] |
| 19. | Design and implement the following Boolean equation using pseudo CMOS logic with circuit diagram. | | CO3 | [K ₃] |
| | 1) $F' = (A.B) + (C + D + E)$ | 6 | | |
| | 2) $R = (L + M.N).(O.P.Q)$ | 6 | | |
| 20. | a) Illustrate the working of 4x4 NAND ROM circuit using MOS devices with suitable example binary values. | 6 | CO4 | [K ₃] |
| | b) Explain the working of 6T RAM cell with suitable circuit diagram. | 6 | CO4 | [K ₂] |
| 21. | Design and draw the block diagram for 4x4 array multiplier using CMOS logic. | 12 | CO5 | [K ₃] |
| 22. | Describe the working of any one type of Configurable Logic Block(CLB) in FPGA with neat sketch. | 12 | CO6 | [K ₂] |
