



B.E/B.TECH DEGREE EXAMINATIONS: APRIL / MAY 2023

(Regulation 2018)

Fourth Semester

ELECTRICAL AND ELECTRONICS ENGINEERING

U18EEI4203: Digital Electronics

COURSE OUTCOMES

- CO1:** Understand the operation of basic logic gates and logic families.
CO2: Analyze, Design and Implement various combinational logic circuits.
CO3: Design counters and simple synchronous sequential logic circuits using Flip Flops.
CO4: Classify different semiconductor memories and identify suitable PLD for the applications.
CO5: Design, Simulate and Implement simple digital circuits using suitable software tools and hardware components.

Time: Three Hours

Maximum Marks: 100

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

(Answer not more than 40 words)

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|---|-----|-------------------|
| 1. Realize AND gate and OR gate using NAND gate. | CO1 | [K ₃] |
| 2. Convert $Y=A+BC'+AB+A'BC$ into canonical form. | CO1 | [K ₃] |
| 3. Illustrate the design procedure for Combinational Circuits. | CO2 | [K ₂] |
| 4. Develop a 2 to 4 line decoder with enable input to 1x 4 Demultiplexer. | CO2 | [K ₄] |
| 5. Construct D flip flop to T flip flop. | CO3 | [K ₃] |
| 6. Compare the logic of synchronous counter and ripple counter. | CO3 | [K ₂] |
| 7. What is Hazard? Give its types. | CO4 | [K ₁] |
| 8. Write the Difference between Mealy and Moore model Sequential circuit. | CO4 | [K ₂] |
| 9. List the applications of ROM. | CO5 | [K ₂] |
| 10. How the memories are classified? | CO5 | [K ₂] |

Answer any FIVE Questions:-

PART B (5 x 16 = 80 Marks)

(Answer not more than 400 words)

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|--|----|-----|-------------------|
| 11. a) Simplify the following expression using Quine McCluskey Method
$F(w, x, y, z) = \Sigma (0,2,4,5,6,7,8,10,13,15)$ | 10 | CO1 | [K ₃] |
| b) Simplify the function using Karnaugh map
$F(w, x, y, z) = \Sigma (2,3,10,11,12,13,14,15)$ | 6 | CO1 | [K ₃] |

12.	a)	Build the Carry look ahead adder.	10	CO2	[K ₃]
	b)	Implement $F(A,B,C,D)=\Sigma m(0,2,3,6,8,10,11,12,13,14)$ using 8x1 multiplexer.	6	CO2	[K ₃]
13.		Using T Flip-flop design binary counter which counts in the sequence 000, 001, 010, 011, 100, 101, 110, 111, 000.	16	CO3	[K ₃]
14.	a)	Explain about Master Slave JK Flip flop.	8	CO3	[K ₂]
	b)	Describe about 4 bit Ring Counter using D Flip flop.	8	CO3	[K ₂]
15.		Construct the transition table, state table and state diagram for the mealy model sequential circuit.	16	CO4	[K ₃]
16.		Discuss in detail about Field Programmable Gate Arrays (FPGAs).	16	CO5	[K ₂]
