



B.E. DEGREE EXAMINATIONS: APRIL / MAY 2023

(Regulation 2018)

Fourth Semester

ELECTRICAL AND ELECTRONICS ENGINEERING

U18EEI4203: Digital Electronics

COURSE OUTCOMES

CO1: Understand the operation of basic logic gates and logic families

CO2: Analyze, Design and Implement various combinational logic circuits

CO3: Design counters and simple synchronous sequential logic circuits using Flip Flops

CO4: Classify different semiconductor memories and identify suitable PLD for the applications

Time: Three Hours

Maximum Marks: 100

Answer all the Questions: -

PART A (10 x 2 = 20 Marks)

(Answer not more than 40 words)

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|---|-----|-------------------|
| 1. Convert the given expression into canonical SOP Form: $Y=AB+A'C+BC'$ | CO1 | [K ₂] |
| 2. Convert the decimal number 475.25 into binary equivalent. | CO1 | [K ₂] |
| 3. What is a demultiplexer and how does it differ from a decoder? | CO2 | [K ₂] |
| 4. Compare combinational and sequential circuits. | CO2 | [K ₂] |
| 5. A asynchronous counter has 14 stable states 0000 through 1101. If the input frequency is 50kHz what would be the output frequency? | CO3 | [K ₂] |
| 6. Write the characteristic equation of SR flipflop. | CO3 | [K ₂] |
| 7. Compare Moore and Mealy model. | CO3 | [K ₂] |
| 8. What do you mean by hazards in sequential circuits? | CO3 | [K ₂] |
| 9. Classify the semiconductor memories. | CO4 | [K ₂] |
| 10. Define noise margin. | CO4 | [K ₂] |

Answer any FIVE Questions: -
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11. a) Simplify the following Boolean function by using a Quine-McClusky Method. 10 CO1 [K₂]
 $F(A, B, C, D) = \sum m(0, 1, 5, 7, 8, 9, 10, 11, 14, 15)$.
- b) Simplify the following expressions using Boolean laws. 6 CO1 [K₂]
- (i) $y = \overline{\overline{A\overline{B}} + ABC + A(B + \overline{A\overline{B}})}$
- (ii) $y = AB + (A + B)(\overline{A} + B)$
12. a) Implement the following Boolean function using 8:1 multiplexer: 10 CO2 [K₃]
 $F(A, B, C, D) = \sum m(1, 3, 4, 6, 8, 12, 13, 14, 15)$
- b) Design full adder using logic gates. 6 CO2 [K₂]
13. a) Design a MOD-10 synchronous counter using JK flip flop. 10 CO3 [K₃]
- b) Draw and explain the 3-bit serial in serial out shift register. 6 CO3 [K₂]
14. a) Design a sequential circuit to detect the following sequence using D flipflop's. 10 CO3 [K₃]
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graph LR
 A((A)) -- "0/0" --> A
 A -- "1/0" --> B((B))
 B -- "1/0" --> C((C))
 C -- "0/1" --> A
 C -- "1/0" --> C
 C -- "0/0" --> A

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- b) Define the following (i) State assignment (ii) State table (iii) state Diagram 6 CO3 [K<sub>2</sub>]
15. a) Implement the following two Boolean functions with a PLA: 10 CO4 [K<sub>2</sub>]  
 $F1(A, B, C) = \sum m(4, 5, 7)$  and  $F2(A, B, C) = \sum m(1, 3, 5, 7)$
- b) Explain the working of a 2 input Totem pole NAND gate 6 CO4 [K<sub>2</sub>]
16. a) Simplify the following Boolean expression using Karnaugh map. Draw the logic diagram for the simplified expression. 10 CO2 [K<sub>3</sub>]  
 $F(A, B, C, D) = \sum m(1, 7, 9, 12, 13, 14, 15) + \sum d(5, 11)$
- b) Realize D flip flop using JK flip flop. 6 CO3 [K<sub>2</sub>]

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