Register Number:……..

KUMARAGURU
college of technology
character is life

B.E DEGREE EXAMINATIONS: APRIL / MAY 2023

(Regulation 2017)

Fifth Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U17ECI5202**:** VLSI and HDL Programming

COURSE OUTCOMES

CO1: Discuss the CMOS fabrication Technologies.
CO2: Explain working and electrical properties of MOSFET.
CO3: Apply CMOS logics in complex digital circuits(K3)
CO4: Implement and verify combinational and sequential circuits using Verilog HDL.
CO5: Discuss various implementation strategies.

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-
PART A (10 x 2 = 20 Marks)
(Answer not more than 40 words)

1.	Define latch up	CO1	[K_1]
2.	Make use of CMOS design rules and give the stick diagram of CMOS inverter with necessary monochrome coding or color coding	CO1	[K_3]
3.	Compare enhancement and depletion mode MOSFETs	CO2	[K_2]
4.	Recall the output current equation of an enhancement mode NMOS for all three regions of operation.	CO2	[K_1]
5.	Applying the pass transistors, Model a AND gate.	CO3	[K_3]
6.	Applying transmission gates, Model a 2X1 Multiplexer.	CO3	[K_3]
7.	List any 4 types of operators used in verilog HDL with an example each.	CO4	[K_1]
8.	Compare and contrast Tasks and Functions	CO4	[K_2]
9.	List any two advantages of carry select adder	CO5	[K_1]
10.	Recall the applications of SoC	CO5	[K_1]

Answer any FIVE Questions:-
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11.	a)	Determine the drain current for N type MOSFET in various regions of operation with necessary equations.	10	CO2	[K_2]
	b)	Discuss about body effect and channel length modulation in MOSFETs.	6	CO2	[K_2]

12.	a)	Elaborate the steps involved in the fabrication of NMOS with a neat sketch of all the steps.	12	CO1	[K_2]
	b)	Applying the design rules, construct a NAND gate with its stick diagram.	4	CO1	[K_3]
13.	a)	Applying CMOS logic styles mentioned below, implement the NAND logic. i) Dynamic logic ii) Domino logic iii) Static CMOS logic iv) Pass transistors	10	CO3	[K_3]
	b)	Describe NORA logic design style with an example.	6	CO3	[K_2]
14.	a)	Design an ALU that performs 8 different functions of your choice using Verilog HDL.	10	CO4	[K_3]
	b)	Categorize the various modeling abstractions in Verilog HDL with its features.	6	CO4	[K_2]
15.	a)	Outline the design flow of SoC with a neat flow chart.	8	CO5	[K_2]
	b)	Illustrate the method to accumulate partial products in array form, in a 4x4 array multiplier with a neat sketch.	8	CO5	[K_3]
16.		Deduce the output voltage of CMOS inverter for all the operating regions with necessary equations and transfer curves.	16	CO2	[K_3]

****