



M.E. DEGREE EXAMINATIONS: APRIL / MAY 2023

(Regulation 2018)

Second Semester

EMBEDDED SYSTEMS TECHNOLOGIES

P18ESE2002: CMOS VLSI Design

COURSE OUTCOMES

- CO1:** Understand the fundamental concepts of VLSI design process and CMOS fabrication process.
- CO2:** Study the electrical properties of MOS devices and characteristics of CMOS logic.
- CO3:** Interpret the CMOS design rules and circuit characteristics.
- CO4:** Design simple digital modules using CMOS logic.
- CO5:** Apply verilog HDL on design of simple digital circuits

Time: Three Hours

Maximum Marks: 100

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. VLSI technology uses _____ to form integrated circuit. CO1 [K₂]
a) transistors b) switches
c) diodes d) buffers
2. Oxidation of silicon wafer leads to CO1 [K₂]
a) contact b) Silicon di oxide
c) Silicon oxide d) Poly silicon
3. In CMOS logic circuit the n-MOS transistor acts as: CO2 [K₂]
a) Load b) Pull up network
c) Pull down network d) Not used in CMOS circuits

4. CO2 [K₂]

Match the following	
List I	List II
A. Velocity	i. V_{ds}/L
B. I_{ds}	ii. L / v
C. Transit time	iii. Q_c / τ
D. E_{ds}	iv. μ / E_{ds}

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|--|-----|-------------------|
| 18. Implement 2X1 MUX using pass transistors. | CO4 | [K ₃] |
| 19. What are bit wise operators in Verilog HDL? | CO5 | [K ₂] |
| 20. “Always” and “initial” statements differ in executing the statements. How? | CO5 | [K ₂] |

PART C (6 x 5 = 30 Marks)

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|---|-----|-------------------|
| 21. Discuss the oxidation and diffusion process in brief. | CO1 | [K ₂] |
| 22. Derive current equation for MOS device. | CO2 | [K ₂] |
| 23. Draw CMOS circuit for half adder with sum and carry output. | CO4 | [K ₃] |
| 24. Write short notes on Precharge-Evaluate logic. | CO4 | [K ₂] |
| 25. Write note on CMOS design rules. | CO3 | [K ₂] |
| 26. Write a Verilog coding for 2X4 decoder using behavioral modeling. | CO5 | [K ₃] |

Answer any FOUR Questions

PART D (4 x 10 = 40 Marks)

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|---|-----|-----------------------|
| 27. Derive the CMOS inverter DC characteristics and obtain the relationship for output voltage at different region in the transfer characteristics. | CO2 | [K ₂] |
| 28. Discuss the twin-tub procedure for fabrication of CMOS device. | CO1 | [K ₂] |
| 29. i) Describe the latch up issue with necessary diagram. | 6 | CO3 [K ₂] |
| ii) Write short note on area capacitance. | 4 | |
| 30. Design and implement 8x1 MUX using Verilog HDL. | CO5 | [K ₂] |
| 31. Implement the following Boolean equation using CMOS and Psuedo NMOS logic. $F=[A+(B.C)]+[(D.E)+(G+H)]$ | CO4 | [K ₃] |
