



M.E. DEGREE EXAMINATIONS: APRIL / MAY 2023

(Regulation 2018)

Second Semester

EMBEDDED SYSTEMS TECHNOLOGIES

P18EST2003: VHDL

COURSE OUTCOMES

CO1: Acquire the Knowledge in VHDL constructs.

CO2: Acquire the knowledge of programming structure of simple and complex design.

CO3: Write program using signal components and configuration

CO4: Familiarize sub programming, packages and files of VHDL.

CO5: Write and implement programs using HDL tools

Time: Three Hours

Maximum Marks: 100

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Identify the correct VLSI design flow: CO1 [K₂]
1.synthesis 2. Simulation 3. Idea to Boolean expression 4. Design entry through HDL
a) 1-2-3-4 b) 4-3-2-1
c) 3-4-2-1 d) 2-3-4-1

2. The expansion of VHDL is CO1 [K₁]
a) Virtual Hardware Description Logic b) Very high speed integrated circuit
Hardware Description Logic
c) Very high speed integrated circuit d) Very high speed integrated circuit
Hardware Description Language Hardware Design Language

3. Process are declared in VHDL is CO2 [K₂]
a) Only in sequential statements b) Only in concurrent statements
c) Both sequential and concurrent d) Only in library
statements

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|-----|-------------------------------|-----|--------------------------------------|
| 10. | The expansion of FPGA | CO5 | [K ₁] |
| a) | Field Programmable Grid Array | b) | Fixed Programmable Gate Array |
| c) | Field Programmable Gate Array | d) | Field Programmable Gate Architecture |

PART B (10 x 2 = 20 Marks)

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|-----|---|-----|-------------------|
| 11. | List the features of VHDL. | CO1 | [K ₂] |
| 12. | Differentiate between VHDL and Verilog HDL | CO1 | [K ₂] |
| 13. | Write VHDL code for D-type flipflop. | CO2 | [K ₃] |
| 14. | Write VHDL code for 4bit counter | CO2 | [K ₃] |
| 15. | List the different libraries in VHDL. | CO3 | [K ₂] |
| 16. | Write syntax for generate statement in VHDL | CO3 | [K ₂] |
| 17. | Specify the uses of USE and LIBRARY clauses. | CO4 | [K ₂] |
| 18. | Define simulation, also mention different EDA tools | CO4 | [K ₂] |
| 19. | Write Verilog code for xor gate. | CO5 | [K ₂] |
| 20. | What is FPGA? Also list its features. | CO5 | [K ₂] |

PART C (6 x 5 = 30 Marks)

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|-----|---|-----|-------------------|
| 21. | Explain the VLSI design flow with neat diagram. | CO1 | [K ₂] |
| 22. | Design 4x1 MUX, also write its VHDL code using Case statement. | CO2 | [K ₃] |
| 23. | Design a JK flipflop, also write its VHDL code. | CO3 | [K ₃] |
| 24. | Illustrate the structural modelling in VHDL with relevant examples. | CO3 | [K ₂] |
| 25. | Explain the features of packages in VHDL with examples. | CO4 | [K ₂] |
| 26. | Design a Full adder, also write its Verilog HDL code. | CO5 | [K ₃] |

Answer any FOUR Questions

PART D (4 x 10 = 40 Marks)

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|-----|--|-----|-------------------|
| 27. | Explain various levels of descriptions in VHDL with relevant examples. | CO1 | [K ₂] |
| 28. | Design and implement 4x4 binary array multiplier through VHDL. | CO2 | [K ₃] |
| 29. | Design a 4bit ALU, also write its VHDL code. | CO3 | [K ₃] |
| 30. | Explain Spartan FPGA architecture with neat diagram. | CO5 | [K ₂] |
| 31. | Define procedure and function. Discuss the various types of function overloading with suitable examples. | CO4 | [K ₂] |
