



B.E/B.TECH DEGREE EXAMINATIONS: APRIL /MAY 2024

(Regulation 2018)

Seventh Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U18ECE0045: Low power VLSI

COURSE OUTCOMES

- CO1:** Discuss the sources of power dissipation in CMOS logic design.
CO2: Illustrate low power design and optimization techniques.
CO3: Estimate power at different levels.
CO4: Examine leakage reduction techniques.
CO5: Analyze the effects of voltage scaling.
CO6: Discuss effect of capacitance on power reduction.

Time: Three Hours

Maximum Marks: 100

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

(Answer not more than 40 words)

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|---|-----|-------------------|
| 1. Infer about the needs for VLSI Design. | CO1 | [K ₂] |
| 2. Explain about power optimization in VLSI circuits. | CO2 | [K ₂] |
| 3. Define power optimization in Behavioral synthesis. | CO2 | [K ₂] |
| 4. Describe about event driven gate level power simulation. | CO3 | [K ₂] |
| 5. Illustrate the importance of power estimation. | CO3 | [K ₂] |
| 6. Outline the structure of MTCMOS NAND gate. | CO4 | [K ₂] |
| 7. Discuss on power gating granularity with neat diagram. | CO4 | [K ₂] |
| 8. Build the impact of supply voltage scaling in the performance of the VLSI circuit. | CO5 | [K ₃] |
| 9. Model the variable voltage generator in DVFS. | CO5 | [K ₃] |
| 10. Outline various capacitance minimization methods. | CO6 | [K ₂] |

Answer any FIVE Questions:-

PART B (5 x 16 = 80 Marks)

(Answer not more than 400 words)

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|---|----|-----|-------------------|
| 11. a) Explain about the basic principles of Low Power VLSI design. | 16 | CO1 | [K ₂] |
| 12. a) Describe the three layout optimization approaches for reducing physical capacitance. | 8 | CO2 | [K ₂] |

	b)	Interpret the banked organization of SRAM to achieve reduced power.	8	CO2	[K ₂]
13.	a)	Outline the propagation of statistical quantities in the probabilistic power analysis	8	CO3	[K ₂]
	b)	Infer about the Monte Carlo simulation Procedure.	8	CO3	[K ₂]
14.	a)	Discuss on different switching fabric with neat sketch.	8	CO4	[K ₂]
	b)	Summarize on VTCMOS approach of minimizing leakage power.	8	CO4	[K ₂]
15.	a)	Organize the architecture level voltage scaling that improves the performance of low power circuits.	8	CO5	[K ₃]
	b)	Build about the Dynamic voltage and frequency scaling approach in CMOS Circuits.	8	CO5	[K ₃]
16.	a)	Infer about the importance of caching in VLIW processor with its architecture, and compare with Superscalar processor.	10	CO6	[K ₂]
	b)	Describe the technology behind Transmeta Crusoe processor.	6	CO6	[K ₂]
