



B.E/B.TECH DEGREE EXAMINATIONS: APRIL/ MAY 2024

(Regulation 2018)

Seventh Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U18ECE0043: System on Chip

COURSE OUTCOMES

- CO1:** Discuss system architectures and components.
CO2: Outline system level design methodology.
CO3: Compare hardware software co design strategies.
CO4: Illustrate SOC design approach.
CO5: Discuss SOC design implementation tools.
CO6: Summarize SOC testing techniques.

Time: Three Hours

Maximum Marks: 100

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

(Answer not more than 40 words)

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|--|-----|-------------------|
| 1. List the types of IP cores. | CO1 | [K ₂] |
| 2. Why is the cache memory required? | CO1 | [K ₂] |
| 3. What are the components of a System? | CO2 | [K ₂] |
| 4. Identify the use of APB protocol. | CO2 | [K ₂] |
| 5. List the advantages of superscalar architecture? | CO3 | [K ₂] |
| 6. Identify the significance of hardware software trade-off? | CO3 | [K ₂] |
| 7. What is the need for RTOS in SoC? | CO4 | [K ₂] |
| 8. List the topologies of NoC. | CO4 | [K ₂] |
| 9. What are the steps followed in SoC design flow? | CO5 | [K ₂] |
| 10. What is the need for testing wrappers? | CO5 | [K ₂] |

Answer any FIVE Questions:-

PART B (5 x 16 = 80 Marks)

(Answer not more than 400 words)

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|---|---|-----|-------------------|
| 11. a) Distinguish semi-custom and full custom design flow. | 8 | CO1 | [K ₃] |
| b) Illustrate the Memory and Addressing of SoC. | 8 | CO1 | [K ₂] |

12.	a)	Compare and contrast CISC and RISC machine.	8	CO2	[K ₂]
	b)	Explain the architecture of VLIW processor.	8	CO2	[K ₂]
13.	a)	Explain the architecture of AMBA.	8	CO3	[K ₂]
	b)	Identify the features of dataflow models in Hardware / Software co-design.	8	CO3	[K ₂]
14.		Make use of a block diagram, explain the architecture of Micro blaze processor.	16	CO4	[K ₃]
15.	a)	Explain the function of RTOS and different types of RTOS.	8	CO5	[K ₂]
	b)	What are the tools used in the Implementation of SoC? Explain.	8	CO5	[K ₂]
16.		Illustrate the P1500 Wrapper standardization for testing SoC and explain.	16	CO6	[K ₂]
