



B.E DEGREE EXAMINATIONS: APRIL /MAY 2024

(Regulation 2018)

Sixth Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U18ECI6203: VLSI and HDL Programming

COURSE OUTCOMES

- CO1:** Implement and verify combinational and sequential circuits using Verilog HDL.
CO2: Explain working and electrical properties of MOSFET.
CO3: Discuss the CMOS fabrication Technologies.
CO4: Apply CMOS logics in complex digital circuits.
CO5: Discuss various implementation strategies.

Time: Three Hours

Maximum Marks: 100

Answer all the Questions

PART A (10 x 2 = 20 Marks)

(Answer not more than 40 words)

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|---|-----|-------------------|
| 1. Develop a Verilog code for a two input CMOS NAND gate using switch level modeling. | CO1 | [K ₃] |
| 2. Differentiate Tasks and Functions. | CO1 | [K ₃] |
| 3. Outline the structure of NMOS transistor. | CO2 | [K ₂] |
| 4. What is Body effect? | CO2 | [K ₂] |
| 5. Identify the importance of Photolithography. | CO3 | [K ₂] |
| 6. Outline the stick diagram of CMOS inverter. | CO3 | [K ₂] |
| 7. List the advantages of TSPC logic. | CO4 | [K ₂] |
| 8. Construct 2X1 MUX using Transmission gate. | CO4 | [K ₃] |
| 9. Illustrate the applications of SoC. | CO5 | [K ₃] |
| 10. Identify the building blocks of FPGA. | CO5 | [K ₂] |

Answer any FIVE Questions
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

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|-----|----|--|----|-----|-------------------|
| 11. | a) | Illustrate the different looping statements available in Verilog with suitable examples. | 8 | CO1 | [K ₃] |
| | b) | Develop a Verilog code for a Negative edge triggered JK flip-flop using case statement with logic diagram and truth table. | 8 | CO1 | [K ₃] |
| 12. | | Explain the operation of CMOS inverter and obtain the output voltage expressions and also outline the DC characteristics. | 16 | CO2 | [K ₂] |
| 13. | | Examine the steps involved in the fabrication of CMOS transistor using N- well process with neat sketch. | 16 | CO3 | [K ₂] |
| 14. | a) | Construct a 4 bit Carry Lookahead adder circuit and explain the operation of the same. | 8 | CO4 | [K ₃] |
| | b) | Model a two input AND/NAND gate using DCVS logic. | 8 | CO4 | [K ₃] |
| 15. | a) | Explain the structure of Configurable Logic Block of Xilinx 4000 FPGA architecture. | 8 | CO5 | [K ₂] |
| | b) | Illustrate SoC design flow with a neat flow chart. | 8 | CO5 | [K ₂] |
| 16. | a) | Summarize the operation and characteristics of depletion mode N channel MOSFET in detail. | 8 | CO2 | [K ₂] |
| | b) | Determine the Pull-up to Pull-down ratio for an NMOS Inverter driven by another inverter. | 8 | CO2 | [K ₃] |
