Register Number:……..

KUMARAGURU
college of technology
character is life

B.E/B.TECH DEGREE EXAMINATIONS: APRIL /MAY 2024

(Regulation 2018)

Fourth Semester

ELECTRICAL AND ELECTRONICS ENGINEERING

U18EEI4203: Digital Electronics

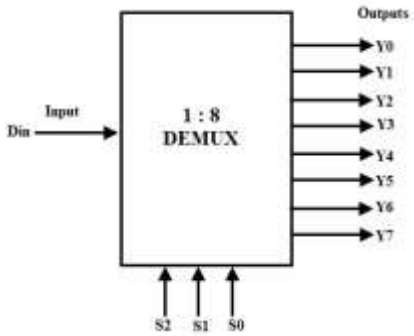
COURSE OUTCOMES

CO1: Understand the operation of basic logic gates and logic families.
CO2: Analyze, Design and Implement various combinational logic circuits.
CO3: Design counters and simple synchronous sequential logic circuits using Flip Flops.
CO4: Classify different semiconductor memories and identify suitable PLD for the applications.
CO5: Design, Simulate and Implement simple digital circuits using suitable software tools and hardware components.

Time: Three Hours **Maximum Marks: 100**

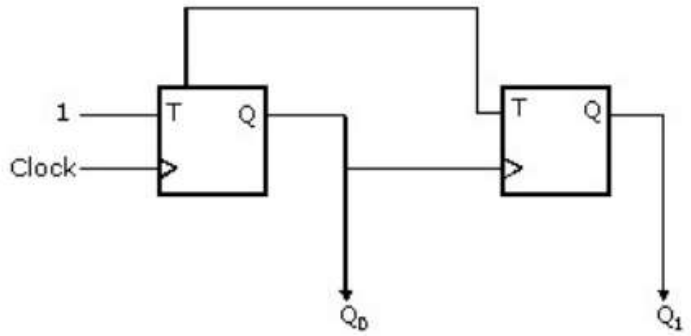
Answer all the Questions:-
PART A (10 x 2 = 20 Marks)
(Answer not more than 40 words)

1.	Write the Binary Equivalent of 18_d.	CO1	[K_2]
2.	Which Gate Produce output Logic 1 when the inputs were different and the same results in Logic 0 for same input combinations? Justify with its truth table.	CO1	[K_2]
3.	Plot the k-map for the output function F = ∑ A,B,C(1,3,6,7) and Simplify it.	CO2	[K_3]
4.	Evaluate the output Y values when Din = 1, s0=s1=s2=1	CO2	[K_4]



5.	Whether Flip-flop or latch is level sensitive? Sketch Master Slave Flip flop.	CO3	[K_2]
6.	Write the excitation table of JK Flip flop.	CO3	[K_2]
7.	Differentiate Moore and Mealy Model.	CO5	[K_2]

8. In the sequential circuit shown below, if the initial value of the output Q1Q0 is 00, what is the next values of Q1Q0 after a clock Period? CO5 [K_3]

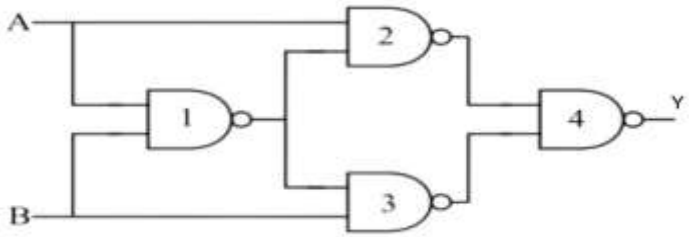


9. Compare PROM, PLA, PAL. CO4 [K_2]

10. Which logic CMOS or TTL logic is mostly preferred? Justify your answer. CO4 [K_2]

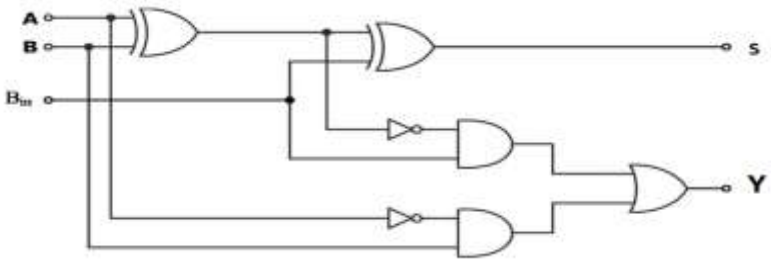
Answer any FIVE Questions:-
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11. a) Evaluate the function Y and comment on the behavior of the Circuit. 8 CO1 [K_4]

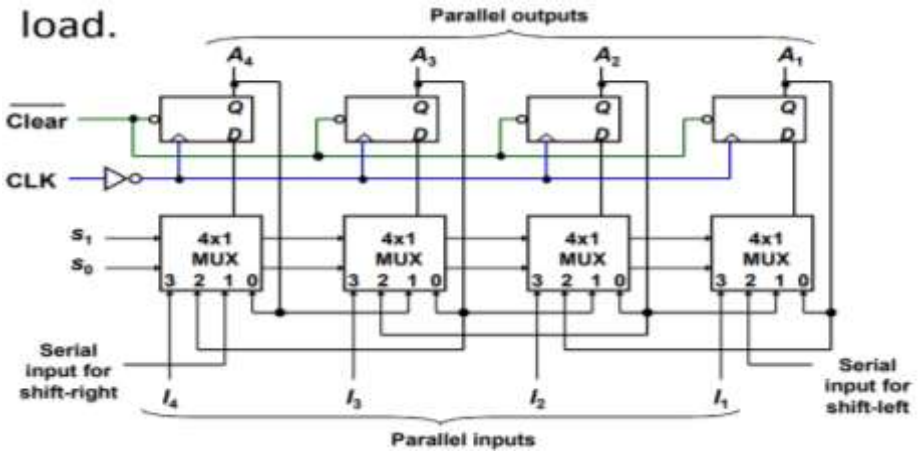


b) Simplify the following expression using K-map and sketch its simplified combinational circuit. Simplify $P = \Pi\ (0, 1, 2, 3, 8, 9, 10, 13)$. 8 CO1 [$K_3$]

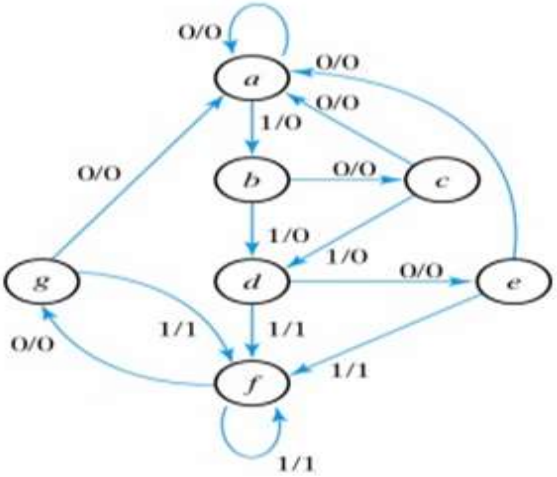
12. a) Evaluate the function S and function Y and comment on the behavior of the Circuit. 6 CO2 [K_4]



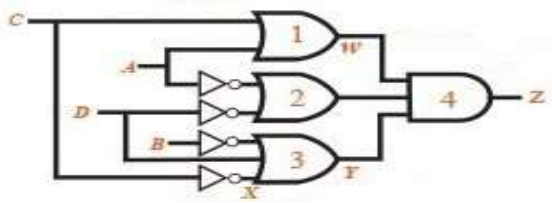
	b)	Design a 2 bit Comparator Circuit.	10	CO2	[K3]
13.	a)	Design a synchronous counter using D flip flops that goes through states 0, 1, 2, 4, 0. The unused states must always go to zero on the next clock pulse.	12	CO3	[K3]
	b)	Evaluate the value of S1 and S0 in following Universal shift register for Shift Right, shift left and Parallel loading.	4	CO3	[K4]



14.	a)	Sketch the reduced state diagram after State reduction in the following diagram.	8	CO5	[K3]



	b)	Design the Hazard free circuit for the following Circuits.	8	CO5	[K3]

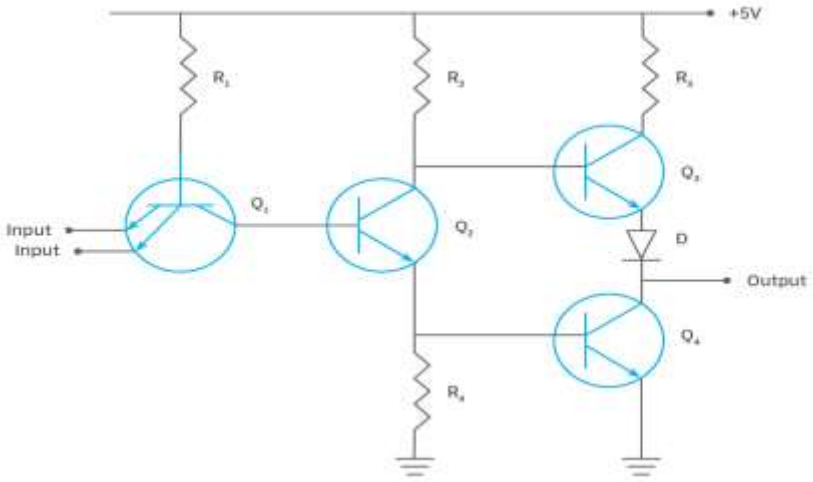


15. a) Implement the following Boolean functions using PLA. 8 CO4 [K3]

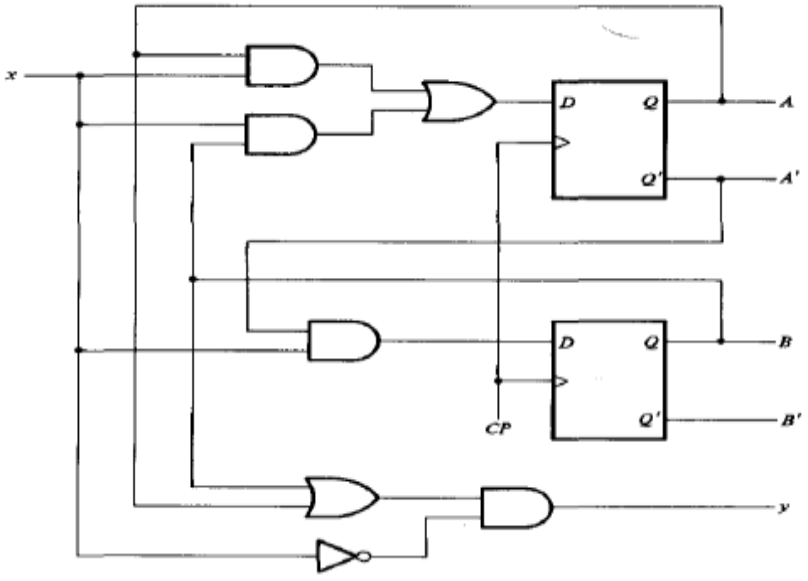
i. A(X,Y,Z)=∑m(5,6,7)

ii. B(X,Y,Z)=∑m(3,5,6,7)

b) Recognize the TTL Logic Gate from following diagram and explain its operation. 8 CO4 [K3]



16. a) Derive the State table for the following sequential circuit. 10 CO5 [K4]



b) Implement the function with MUX F(A, B, C, D) = Σ(1, 3, 4, 11, 12, 13, 14, 15). 6 CO2 [K3]

****