KUMARAGURU college of technology
character is life

Register Number:……..…

M.E. DEGREE EXAMINATIONS: NOV/DEC 2023

(Regulation 2018)

First Semester

EMBEDDED SYSTEMS TECHNOLOGIES

P18EST1001**:** Advanced Digital System Design

COURSE OUTCOMES

CO1: Apply the Design procedure of Clocked synchronous and asynchronous sequential circuits for developing simple digital system

CO2: Analyze the Clocked synchronous sequential circuits and asynchronous sequential circuits in digital system

CO3: Understand the basic and advanced concepts in testing of digital circuits

CO4: Apply the techniques to design synchronous sequential circuit using programmable devices

CO5: Familiarize basics and programming of VHDL for digital circuit design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Assertion (A):The behaviour of a clocked sequential circuit determined from its input. CO1 [K_3]
   Reason (R): The output of clocked sequential circuit determined from its flip-flop state.
   a) Both A and R are True. R is the correct explanation of A
   b) Both A and R are True. R is not correct explanation of A
   c) Both A and R are False. R is the correct explanation of A
   d) Both A and R are False. R is not correct explanation of A

2. Assertion (A): Iterative circuit consists of number of identical cells. CO1 [K_3]
   Reason (R): Cells are interconnected in regular manner.
   a) Both A and R are True. R is not correct explanation of A
   b) Both A and R are False. R is the correct explanation of A
   c) Both A and R are False. R is not correct explanation of A
   d) Both A and R are True. R is the correct explanation of A

3. Assertion (A): Logic equations are necessary for Asynchronous sequential circuit design. CO2 [K_4]
   Reason (R): Logic equations for Asynchronous sequential circuit design obtained by

reducing the Flow table

a) Both A and R are True. R is not correct explanation of A

b) Both A and R are False. R is the correct explanation of A

c) Both A and R are True. R is the correct explanation of A

d) Both A and R are False. R is not correct explanation of A

4. Matching type item with multiple choice code COL [K_L]

List I	List II
A. Moore circuit	i. Asynchonous sequential circuit
B. State feedback in combinational logic	ii. Model representation of synchronous sequential circuit
C. State box	iii. Race condition
D. Change in response to change in input variable	iv. ASM chart

	A	B	C	D
a)	(i)	(ii)	(iii)	(iv)
b)	(ii)	(i)	(iv)	(iii)
c)	(ii)	(iv)	(i)	(iii)
d)	(ii)	(iii)	(i)	(iv)

5. Assertion (A): Fault detection means the discovery of something wrong in a digital system or circuit CO3 [K_2]

Reason (R): Fault diagnosis includes both fault detection and fault location

a) Both A and R are True. R is the correct explanation of A

b) Both A and R are True. R is not correct explanation of A

c) Both A and R are False. R is the correct explanation of A

d) Both A and R are False. R is not correct explanation of A

6. CPLD has _____ level of programmability. CO3 [K_2]

a) Four level

b) Two level

c) Three level

d) One level

7. Asynchronous reset in FPGA is used for_____ CO4 [K_3]

a) Routing congestion

b) Reduce logic

c) Reset state machines

d) All the above

8. Assertion (A):CPLD consists of bunch of PLD blocks. CO4 [K_3]

Reason (R):CPLD arrangement of many SPLD-like blocks.

a) Both A and R are True. R is not correct

b) Both A and R are False. R is the correct

explanation of A

c) Both A and R are True. R is the correct explanation of A

d) Both A and R are False. R is not correct explanation of A

9. VHDL modeling is carried out using — CO5 [K_2]

a) Dataflow
b) Behavioural
c) Strutural
d) All the above

10. Relational operators in VHDL returns — CO5 [K_2]

a) Boolean type
b) Integer type
c) Character type
d) String type

PART B (10 x 2 = 20 Marks)

11.	Where iterative circuits are used?	CO1	[K_3]
12.	What do you mean by synchronous sequential circuit?	CO1	[K_3]
13.	List the design steps in asynchronous sequential logic circuit.	CO2	[K_4]
14.	Compare synchronous sequential and asynchronous sequential circuits.	CO2	[K_4]
15.	What do you mean by fault location?	CO3	[K_2]
16.	Calculate the total number of input combinations necessary to test a sequential circuit with ‘n’ inputs and ‘m’ flip-flops.	CO3	[K_2]
17.	List the type of PLDs.	CO4	[K_2]
18.	What is FPGA?	CO4	[K_3]
19.	Enumerate the types of objects used in VHDL.	CO5	[K_2]
20.	Mention the usage of entity element in VHDL.	CO5	[K_2]

PART C (10 x 5 = 50 Marks)

21.	List the three elements of ASM chart and draw the same with illustration.	CO1	[K_3]
22.	Draw the Moore model and Mealy model of clocked synchronous sequential circuit and explain its basic operation.	CO1	[K_3]
23.	Differentiate static and dynamic hazards in Asynchronous Sequential Circuit.	CO2	[K_4]
24.	Define Mixed Operating Mode in Asynchronous circuits. Draw a typical mixed mode flip-flop.	CO2	[K_4]
25.	Brief about Stuck-At-Fault model with an example.	CO3	[K_2]
26.	Illustrate Boolean difference method with example to find test vectors.	CO3	[K_2]
27.	Draw and explain the architecture of PLDs architecture.	CO4	[K_3]
28.	Explain the function of Generic Array Logic with neat block diagram.	CO4	[K_3]

29.	Write a VHDL code for 4 bit parallel subtractor using structural modeling.	CO5	[K_2]
30.	Write a VHDL code for 4 bit serial adder.	CO5	[K_2]

Answer any TWO Questions

PART D (2 x 10 = 20 Marks)

31.	Describe the iterative circuit design with an example comparator circuit design.	CO1	[K_3]
32.	Explain the functions of input – output black in XGMX 2000 FPGA using table architecture	CO4	[K_2]
33.	Write a VHDL program to build a 4-bit binary counter. Verify the output waveform of the program (the digital circuit) with the counter's truth table.	CO5	[K_2]

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