Register Number:……..

KUMARAGURU
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B.E/B.TECH DEGREE EXAMINATIONS: NOV/DEC 2023

(Regulation 2018)

Seventh Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U18ECE0041**:** VLSI Testing and Testability

COURSE OUTCOMES

CO1: Discuss various fault models and fault simulation techniques.

CO2: Examine faults in combinational logic circuits.

CO3: Examine faults in sequential logic circuits.

CO4: Compare various methods for delay tests.

CO5: Explain difference testability methods.

CO6: Outline fault diagnosis approaches.

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-
PART A (10 x 2 = 20 Marks)
(Answer not more than 40 words)

1.	What is meant by fault dominance?	CO1	[K_1]
2.	Mention the two basic steps in Test Generation used in path sensitization method.	CO1	[K_1]
3.	How back tracing is done in combinational logic circuits?	CO2	[K_1]
4.	Define Random Test Generation, with a suitable example.	CO3	[K_1]
5.	What is meant by Pseudo exhaustive test?	CO4	[K_1]
6.	Give the expressions to compare the controllability and observability values for a T flip flop with a synchronous clear input.	CO4	[K_2]
7.	Infer about BIST with necessary diagram?	CO5	[K_2]
8.	List out the JTAG testing features.	CO5	[K_1]
9.	What are the components in fault diagnosis?	CO6	[K_1]
10.	Explain about dynamic diagnosis.	CO6	[K_2]

Answer any FIVE Questions:-
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11.	a)	Summarize on various fault models with suitable illustrations.	8	CO1	[K_2]
	b)	Discuss about various fault simulation techniques.	8	CO1	[K_2]

12.	a)	With a suitable example explain fault detection using Boolean difference.	8	CO2	[K_2]
	b)	Explain PODEM Algorithm with suitable examples.	8	CO2	[K_2]
13.		Describe various DFT approaches used for testing digital circuits.	16	CO3	[K_2]
14.	a)	Outline about the BIST architecture with necessary diagram.	10	CO4	[K_2]
	b)	Explain about Boundary Scan techniques.	6	CO4	[K_2]
15.	a)	Define controllability and observability. Explain any four Ad hoc techniques.	10	CO5	[K_2]
	b)	Elaborate on full scan LSSD with necessary diagrams.	6	CO5	[K_2]
16.		Explain about the methods adopted for fault diagnosis in combinational circuits.	16	CO6	[K_2]

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