Register Number:……..

KUMARAGURU
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B.E/B.TECH DEGREE EXAMINATIONS: NOV/DEC 2023

(Regulation 2018)

Seventh Semester

ELECTRONICS AND COMMUNCIATION ENGINEERING

U18ECE0043**:** System on Chip

COURSE OUTCOMES

CO1: Discuss system architectures and components.

CO2: Outline system level design methodology.

CO3: Compare hardware software co design strategies.

CO4: Illustrate SOC design approach.

CO5: Discuss SOC design implementation tools.

CO6: Summarize SOC testing techniques.

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-
PART A (10 x 2 = 20 Marks)
(Answer not more than 40 words)

1.	Recall tradeoff with respect to SoC.	CO1	[K_2]
2.	List any two differences between semi-custom and full custom design flow.	CO1	[K_1]
3.	List the components of a System.	CO2	[K_1]
4.	What is the bus size of an APB?	CO2	[K_1]
5.	Recall the significance of VLIW architecture.	CO3	[K_2]
6.	Define Interconnection.	CO3	[K_1]
7.	What do you mean by reconfiguration in communication architecture.	CO4	[K_2]
8.	List any four topologies used in NoC.	CO4	[K_1]
9.	What is the standard of JTAG?	CO5	[K_1]
10.	Recall the name of the fault model when VDD is connected at the output of the gate	CO5	[K_1]

Answer any FIVE Questions:-
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11.	a)	Summarize the five different design considerations in SoC.	8	CO1	[K_2]
	b)	Explain Memory and Addressing design and issues with respect to SoC.	8	CO1	[K_2]

12.	a)	List the similarities and differences between CISC and RISC machine.	8	CO2	[K_1]
	b)	Illustrate the importance of Instruction level parallelism with a example.	8	CO2	[K_2]
13.	a)	Summarize the driving factors of hardware and Software co-design.	8	CO3	[K_2]
	b)	Interpret the dataflow models in Hardware / Software co-design.	8	CO3	[K_2]
14.	a)	Elaborate on the architecture of Microblaze with a neat diagram.	8	CO4	[K_2]
	b)	Explain the Network on Chip (NoC) architecture with a neat diagram.	8	CO4	[K_2]
15.	a)	Outline concept of Task in RTOS with neat diagram.	8	CO5	[K_2]
	b)	Summarize the tools used in Design Implementation of SoC? Explain.	8	CO5	[K_2]
16.	a)	Elaborate on the P1500 Wrapper standardization for testing SoC.	8	CO6	[K_2]
	b)	Clarify the the types of testing used in VLSI design and explain each of them.	8	CO6	[K_2]

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