Register Number:……..

KUMARAGURU
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B.E/B.TECH DEGREE EXAMINATIONS: NOV/DEC 2023

(Regulation 2018)

Seventh Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U18ECE0045: Low Power VLSI

COURSE OUTCOMES

CO1: Discuss the sources of power dissipation in CMOS logic design.

CO2: Illustrate low power design and optimization techniques.

CO3: Estimate power at different levels.

CO4: Examine leakage reduction techniques.

CO5: Analyze the effects of voltage scaling.

CO6: Discuss the effect of capacitance on power reduction.

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-
PART A (10 x 2 = 20 Marks)
(Answer not more than 40 words)

1.	Illustrate the hierarchy of limits of power.	CO1	[K_2]
2.	Recall the basic principles of circuit level limits.	CO1	[K_1]
3.	What is power optimization in VLSI?	CO2	[K_1]
4.	Identify the importance of power estimation.	CO3	[K_1]
5.	Summerize on event driven gate level power simulation.	CO3	[K_2]
6.	What is meant by transistor stacking?	CO4	[K_2]
7.	Outline the structure of MTCMOS NAND gate.	CO4	[K_2]
8.	Categorize the different voltage scaling approaches.	CO5	[K_2]
9.	Outline the AND gate using adiabatic logic.	CO5	[K_2]
10.	List the various capacitance minimization methods.	CO6	[K_1]

Answer any FIVE Questions:-
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11.	a)	Build the expression for the short component of power in CMOS circuits.	10	CO1	[K_3]
	b)	Explain how diode leakage current arises in CMOS.	6	CO1	[K_2]

12.		Explain the architecture optimization with suitable example.	16	CO2	[K_2]
13.	a)	Examine the propagation of statistical quantities in the probabilistic power analysis.	8	CO3	[K_3]
	b)	Illustrate the propagation of static probability in logic circuits.	8	CO3	[K_2]
14.		Explain power gating granularity and power gating topologies with neat diagram.	16	CO4	[K_2]
15.	a)	Interpret the Dynamic voltage and frequency scaling approach.	8	CO5	[K_2]
	b)	Explain how the loop unrolling algorithm and pipelining can be used for achieving low power in the first order IIR filter.	8	CO5	[K_2]
16.	a)	Outline the structure of Transmeta's Crusoe (VLIW) processor and explain the operation of the same.	8	CO6	[K_2]
	b)	Develop a Parallel-Pipelined 16-bit adder and elaborate the same.	8	CO6	[K_3]

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