Register Number:……..

KUMARAGURU
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B.E/B.TECH DEGREE EXAMINATIONS: NOV/DEC 2023

(Regulation 2018)

Sixth Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U18ECI6203T**:** VLSI and HDL Programming

COURSE OUTCOMES

CO1: Implement and verify combinational and sequential circuits using Verilog HDL.
CO2: Explain working and electrical properties of MOSFET.
CO3: Discuss the CMOS fabrication Technologies.
CO4: Apply CMOS logics in complex digital circuits.
CO5: Discuss various implementation strategies.

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions: -
PART A (10 x 2 = 20 Marks)
(Answer not more than 40 words)

1.	In the order of least to highest level of abstraction, list the various modeling types used in Verilog HDL	CO1	[K1]
2.	Distinguish Continuous assignment statement from Procedural assignment statement.	CO1	[K2]
3.	Justify the statement and state whether it's true or false with necessary justification - A pass transistor can drive more than one transistor without any degradation.	CO4	[K2]
4.	Define the effect of velocity saturation in short channel transistors	CO2	[K1]
5.	Name any two specific applications of FPGA.	CO5	[K1]
6.	Using pass transistors, model an AND logic.	CO4	[K3]
7.	List any four ideal characteristics of CMOS Inverter.	CO2	[K1]
8.	Which method of CMOS Fabrication completely neglects latch up effects? How?	CO3	[K2]
9.	Rephrase the significance of demarcation line in stick diagrams.	CO3	[K2]
10.	Recall any two advantages of SoC.	CO5	[K1]

Answer any FIVE Questions:-
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11.	a)	Explain the steps involved in the fabrication of CMOS using N well methodology with necessary diagrams.	8	CO3	[K2]
	b)	Make use of CMOS Design rules and model a NOR gate using static CMOS	8	CO3	[K3]

Logic with its stick diagram and layout.

12.	a)	Deduce the drain current equation for an enhancement mode N-type MOSFET with necessary V-I plots.	8	CO2	[K_2]
	b)	Explain the working of a CMOS Inverter specifying the five regions of operation with S curve.	8	CO2	[K_2]
13.	a)	Design an 8x3 Encoder using behavioral modeling, in Verilog HDL	8	CO1	[K_3]
	b)	Construct a Verilog code to implement a arithmetic logic unit that performs eight different functions.	8	CO1	[K_3]
14.	a)	Outline the principle and working of Field Programmable Gate Array with its subcomponents in detail.	8	CO5	[K_2]
	b)	Explain the SoC design flow with a neat diagram.	8	CO5	[K_2]
15.	a)	Adapt the Boolean expression F = AB+CD using the following logic design styles i) Domino logic ii) Static CMOS Logic iii) Pseudo NMOS logic	8	CO4	[K_3]
	b)	Interpret and appraise the logic design style that helps in overcoming errors due to race conditions.		CO4	[K_2]
16.	a)	Elaborate every step of VLSI Design flow with a neat diagram.	10	CO1	[K_2]
	b)	Compare Enhancement and Depletion mode MOSFETs.	6	CO2	[K_2]

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