Register Number:……………..

KUMARAGURU
college of technology
character is life

B.E/B.TECH DEGREE EXAMINATIONS: NOV/DEC 2023

(Regulation 2018)

Fifth Semester

ELECTRICAL AND ELECTRONICS ENGINEERING

U18EEE0005:VLSI Design

COURSE OUTCOMES

CO1: Recollect and study the fundamentals of electronics devices and circuits.

CO2: Understand the principle and working of MOS and CMOS device.

CO3: Apply the fundamentals of digital circuits and CMOS technology to develop different design techniques.

CO4: Design various digital modules and systems using different CMOS design techniques.

CO5: Analyse the different CMOS digital modules for performance parameters such as gate size and power.

CO6: Understand the concepts of programmable devices for custom design.

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

(Answer not more than 40 words)

1.	Differentiate NMOS and PMOS transistors.	CO1	[K2]
2.	Write the current equation in saturation mode of MOS characteristics.	CO2	[K2]
3.	Write the working of transmission gate with its circuit diagram.	CO3	[K2]
4.	Justify why NMOS is preferred for Pull Down network.	CO3	[K4]
5.	Draw the circuit diagram for positive edge triggered register element.	CO4	[K3]
6.	How many address lines required for 2KB memory?	CO4	[K3]
7.	List out few high speed adders	CO5	[K2]
8.	Write the advantages of barrel shifter.	CO5	[K2]
9.	What is FPGA?	CO6	[K2]
10.	List the advantages of semi-custom design.	CO6	[K2]

Answer any FIVE Questions:-

PART B (5 x 16 = 80 Marks)

(Answer not more than 400 words)

11.	a)	Derive the current equation for MOS device.	8	CO1	[K3]
	b)	What are the types of scaling models and scaling factors? Derive scaling factors for 1.Gate area 2. Gate capacitance 3. Gate delay	8	CO2	[K3]

12.	a)	Illustrate how NOR based 4x4 bit ROM can be designed to store following data. 1100; 1110; 0010; 0000;	10	CO4	[K_5]
	b)	Explain the working of accumulator with suitable clock diagram.	6	CO4	[K_2]
13.	a)	Describe the types of power dissipation in MOS circuits.	8	CO3	[K_2]
	b)	Design CMOS and Pseudo NMOS circuit to implement following Boolean function. i) F'=[(A+B).(C.D)] .(E+G)	8	CO3	[K_5]
14.	a)	Design and implement CMOS based 4 bit adder using full adder circuit.	16	CO4	[K_5]
15.	a)	Explain the working of 4 bit barrel shifter with circuit diagram.	8	CO4	[K_3]
	b)	Implement the following Boolean equation using RAM based LUT method. Z=(A'.B) + (C.D)	8	CO6	[K_5]
16.	a)	Explain the Gate Array based semi custom design with its types.	8	CO6	[K_2]
	b)	Illustrate typical Configurable Logic Block with its working and suitable diagram	8	CO6	[K_2]

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