Register Number:……..

KUMARAGURU
college of technology
character is life

B.E/B.TECH DEGREE EXAMINATIONS: NOV/DEC 2023

(Regulation 2018)

Third Semester

INFORMATION TECHNOLOGY

U18ITT3001: Computer Architecture

COURSE OUTCOMES

CO1: Explain micro level operations of computer using the concepts of hardware and software coordination.

CO2: Compare different types of memories and their performances.

CO3: Apply the knowledge of binary arithmetic operations to understand the design of hardware components.

CO4: Enumerate various control methodologies using programming and their effect on the hardware components.

CO5: Describe the performance enhancement techniques for data handling and I/O handling.

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

(Answer not more than 40 words)

1.	State the need for indirect addressing mode. Give an example.	CO1	[K_2]
2.	List the functions of control unit.	CO1	[K_1]
3.	Predict the reasons why the performance of a pipelined processor suffers.	CO2	[K_1]
4.	Define data hazard. Give an example for data hazard.	CO2	[K_2]
5.	Identify the overflow/underflow conditions for floating point addition and subtraction?	CO3	[K_2]
6.	Subtract $(11011)_2 - (10011)_2$ using 2's complement arithmetic operation.	CO3	[K_2]
7.	Differentiate between fine-grained multi-threading and coarse grained multi- threading.	CO4	[K_2]
8.	Evaluate how many total bits are required for a direct mapped cache with 16KB of data and 4-wordblocks, assuming a 32bit address?	CO4	[K_2]
9.	Define hit rate and miss rate.	CO5	[K_2]
10.	Compare UMA and NUMA multiprocessors.	CO5	[K_2]

.

Answer any FIVE Questions:-
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11.	a)	Explain in detail the functional units of a computer system with neat diagram.	16	CO1	[K_2]
12.	a)	Draw a simple MIPS data path with the control unit and explain the execution of ALU instructions.	16	CO2	[K_3]
13.	a)	Divide (12)10 by (3)10 using the restoring and non restoring division algorithm with step by step intermediate results.	16	CO3	[K_3]
14.	a)	Illustrate the methods used to improving cache performance and correlate the various mapping functions that can be applied on cache memories.	16	CO4	[K_3]
15.	a)	Explain with diagrammatic illustration Flynn's classification.	16	CO5	[K_2]
16.	a)	Assume a two address format specified as source, destination. Describe the following sequence of instructions and connect the addressing modes used and the operation done in every instruction. 1. Add R4,R3 2. Add R1, (1001) 3. Add R3, (R1 + R2) 4. Add R4, #3 5. Add R1, (R2)+	16	CO1	[K_3]

****